

1 PRODUCT OVERVIEW

OVERVIEW

The KS57C5204/C5208/C5304/C5308/C5312 single-chip CMOS microcontroller has been designed for high-performance using SAM 47 (Samsung Arrangeable Microcontrollers). SAM 47, Samsung's newest 4-bit CPU core is notable for its low energy consumption and low operating voltage.

You can select from three ROM sizes: 4K, 8K, or 12K bytes.

Except for the difference in ROM size, the features and functions of the KS57C5204 and the KS57C5208 are identical and the KS57C5304, KS57C5308, and the KS57C5312 are identical.

With its DTMF generator, watchdog timer function, and versatile 8-bit timer/counters, the KS57C5204/C5208 /C5304/C5308/C5312 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 35 pins of the available 42-pin SDIP or 44-pin QFP package for the KS57C5204/C5208, and up to 23 pins of the available 30-pin SDIP or 32-pin SOP package for the KS57C5304/C5308/C5312 can be assign to I/O. Six vectored interrupts for KS57C5204/C5208 and four vectored interrupts for KS57C5304/C5308/C5312 provide fast response to internal and external events. In addition, the KS57C5204/C5208/C5304/C5308/C5312's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C5204/C5208 microcontroller is also available in OTP (One Time Programmable) version, KS57P5208. The KS57C5304/C5308/C5312 microcontroller is also available in OTP (One Time Programmable) version, KS57P5308/P5312. The KS57P5208/P5308/P5312 microcontroller has an on-chip 8K-byte (P5208/P5308) or 12K-byte (P5312) one-time-programmable EPROM instead of masked ROM. The KS57P5208 is comparable to KS57C5204/C5208, both in function and in pin configuration. Also, the KS57P5308/P5312 is comparable to the KS57C5304/C5308/C5312, both in function and in pin configuration.

FEATURES

Memory

- 768 × 4-bit RAM
- 4,096 × 8-bit ROM (KS57C5204/C5304)
- 8,192 × 8-bit ROM (KS57C5208/C5308)
- 12,288 × 8-bit ROM (KS57C5312)

I/O Pins

- Input only: 4 pins (KS57C5204/C5208)
1 pins (KS57C5304/C5308/C5312)
- I/O: 35 pins (KS57C5204/C5208)
23 pins (KS57C5304/C5308/C5312)
- N-channel open-drain I/O: 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

DTMF Generator

- 16 dual-tone frequencies for tone dialing

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

Two 8-Bit Timer/Counters

- Programmable 8-bit timer
- External event counter function
- Arbitrary clock frequency output

Watch Timer

- Real-time and time interval generation
- Four frequency outputs to the BUZ pin

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary

format

Interrupts

- 3 external interrupt vectors (KS57C5204/C5208)
1 external interrupt vectors
(KS57C5304/C5308/C5312)
- 3 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal, or ceramic for main system clock
- Main system clock frequency: 0.4–6.0 MHz
(typical)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, and 15.3 μs at 4.19 MHz
- 1.12, 2.23, 17.88 μs at 3.58 MHz
- 0.67, 1.33, 10.7 μs at 6.0 MHz

Operating Temperature

- –40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Types

- 42 SDIP, 44 QFP (KS57C5204/C5208)
- 30 SDIP, 32 SOP (KS57C5304/C5308/C5312)

BLOCK DIAGRAM

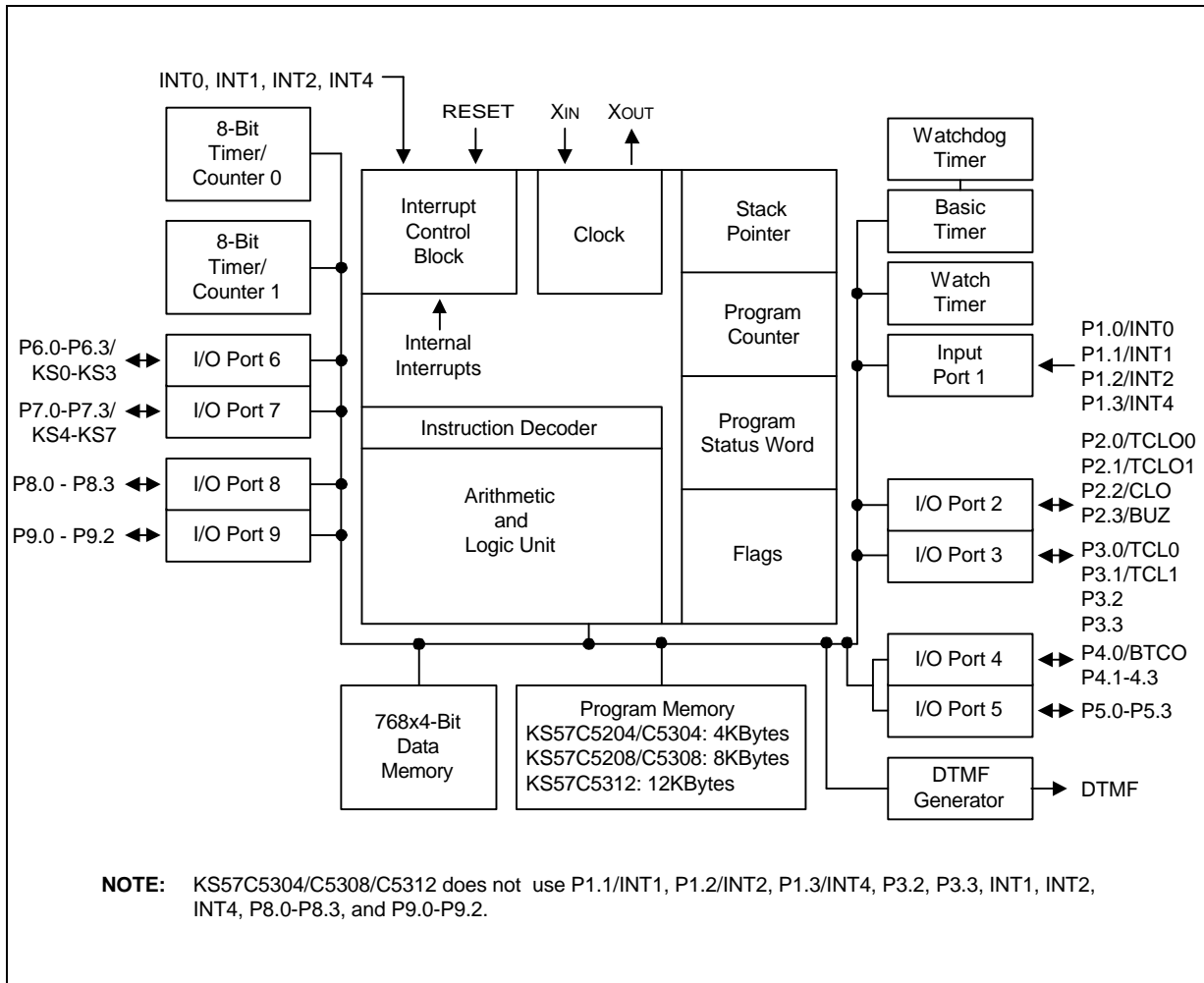


Figure 1-1. KS57C5204/C5208/C5304/C5308/C5312 Simplified Block Diagram

PIN ASSIGNMENTS

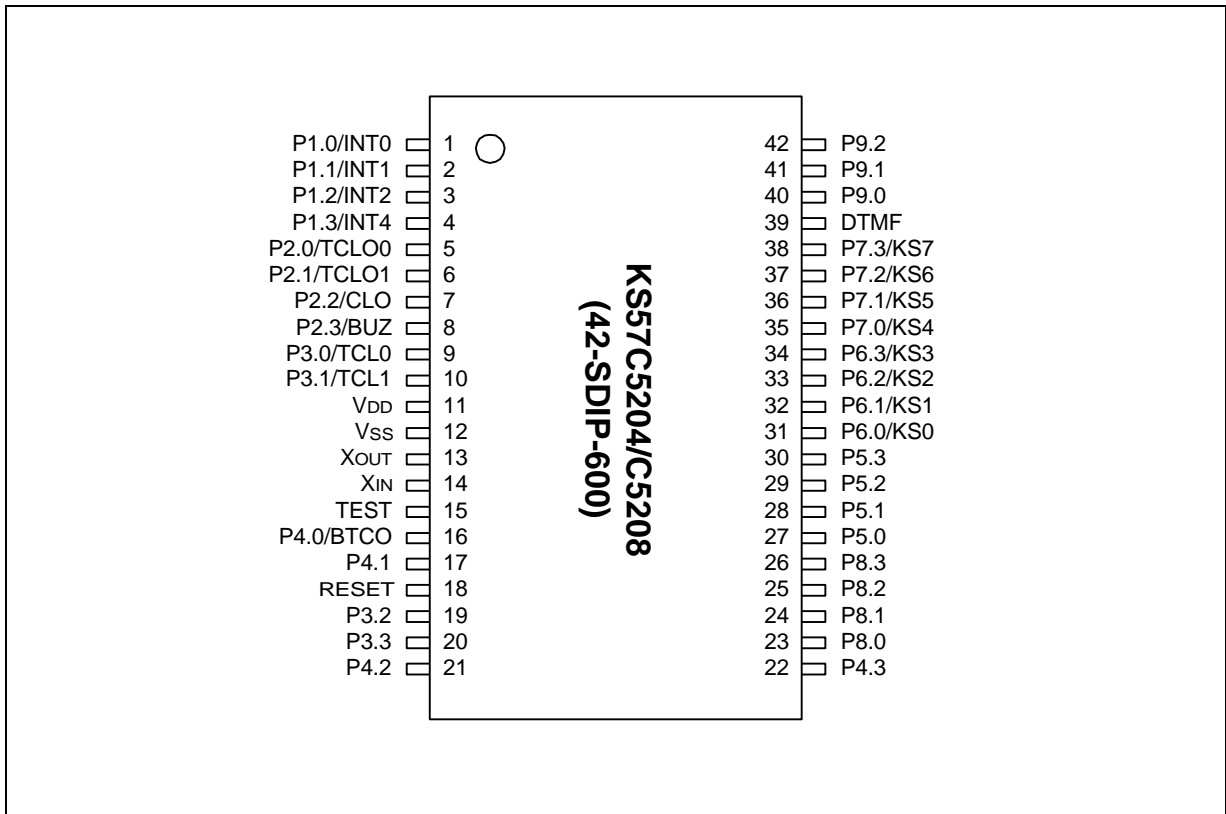


Figure 1-2. KS57C5204/C5208 Pin Assignment Diagram (42-SDIP)

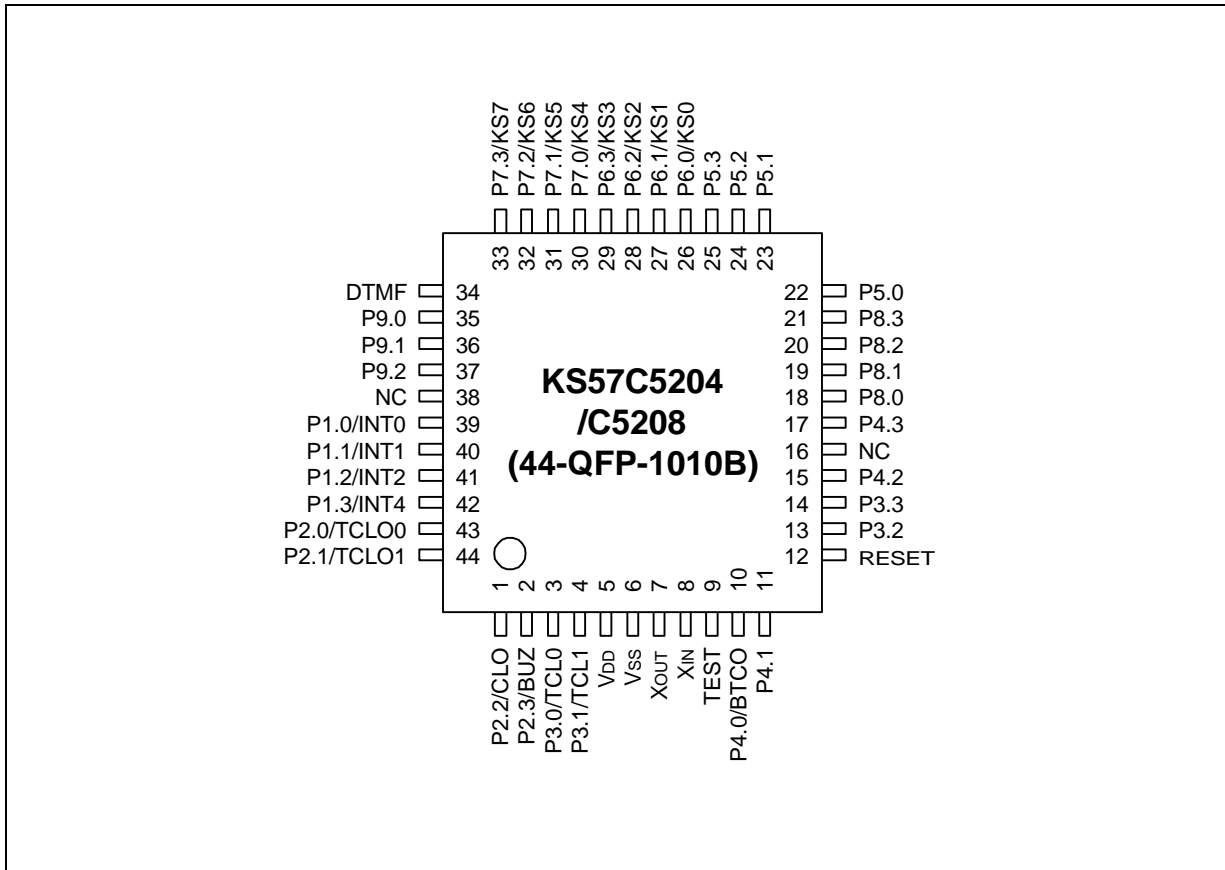


Figure 1-3. KS57C5204/C5208 Pin Assignment Diagram (44-QFP)

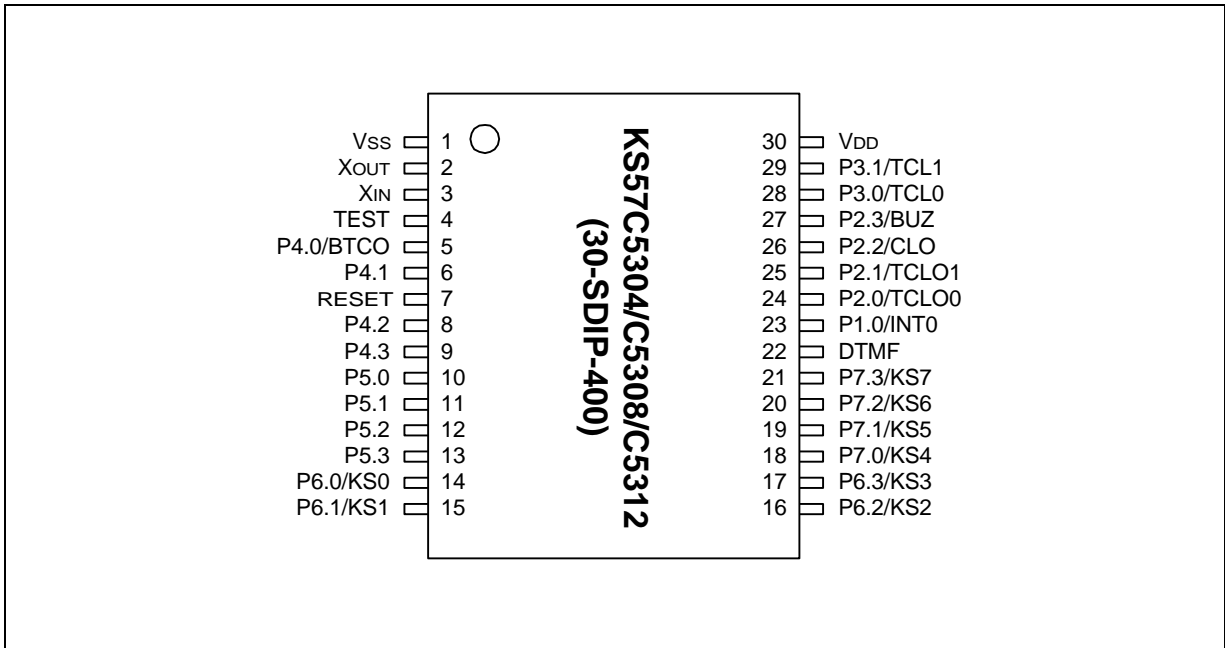


Figure 1-4. KS57C5304/C5308/C5312 Pin Assignment Diagram (30-SDIP)

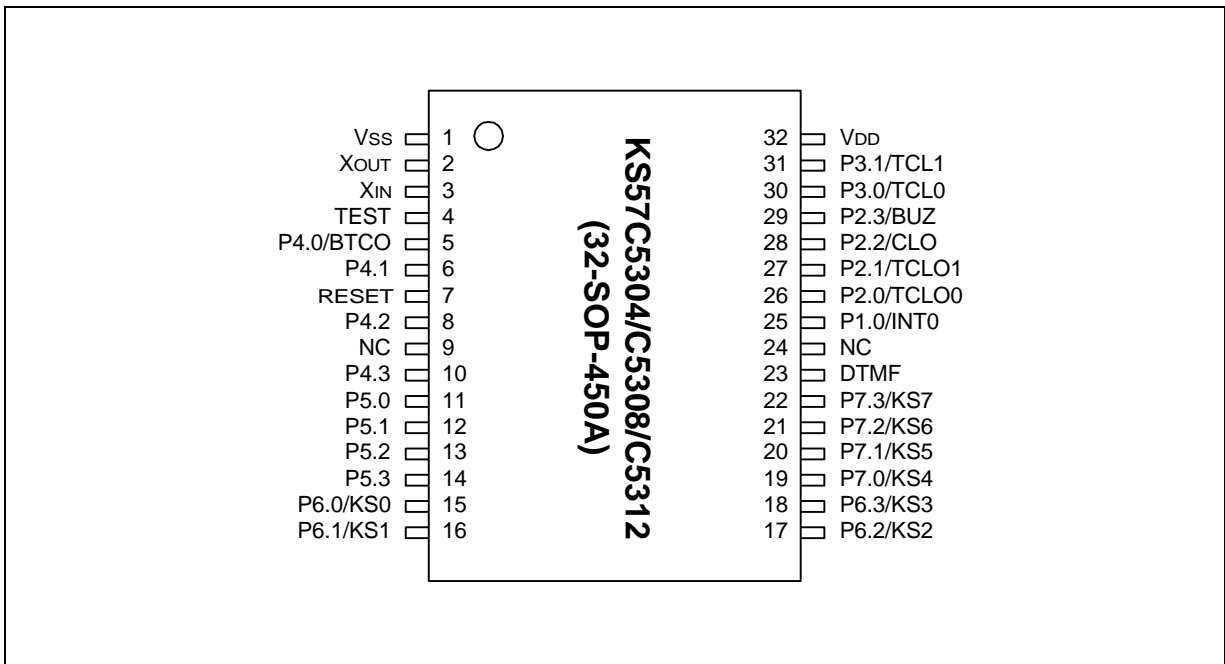


Figure 1-5. KS57C5304/C5308/C5312 Pin Assignment Diagram (32-SOP)

PIN DESCRIPTIONS

Table 1-1. KS57C5204/C5208 Pin Descriptions

Pin Name	Pin Type	Reset Value	Description	Pin Number	Share Pin	Circuit Type
P1.0 P1.1 P1.2 P1.3	I	I	4-bit input port. 1-bit and 4-bit read and test is possible. Each pull-up resistors are assignable by software.	1 (39) 2 (40) 3 (41) 4 (42)	INT0 INT1 INT2 INT4	A-4
P2.0 P2.1 P2.2 P2.3	I/O	I	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output.	5 (43) 6 (44) 7 (1) 8 (2)	TCLO0 TCLO1 CLO BUZ	D-2
P3.0 P3.1 P3.2 P3.3			4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 2 and 3 can be paired to enable 8-bit data transfer.	9 (3) 10 (4) 19 (13) 20 (14)	TCL0 TCL1	
P4.0 P4.1 P4.2 P4.3 P5.0-P5.3	I/O	I	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. N-channel open-drain or push-pull output can be selected by software (1-bit unit) Ports 4 and 5 can be paired to support 8-bit data transfer.	16 (10) 17 (11) 21 (15) 22 (17) 27-30 (22-25)	BTCO	E-2
P6.0-P6.3 P7.0-P7.3			4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	31-34 (26-29) 35-38 (30-33)	KS0-KS3 KS4-KS7	
P8.0-P8.3 P9.0-P9.2	I/O	I	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 8 and 9 can be paired to enable 8-bit data transfer.	23-26 (18-21) 40-42 (35-37)	–	D-2

Table 1-1. KS57C5204/C5208 Pin Descriptions (Continued)

Pin Name	Pin Type	Reset Value	Description	Pin Number	Share Pin	Circuit Type
DTMF	O	–	DTMF output.	39 (34)	–	G-6
BTCO	I/O	I	Basic timer clock output	16 (10)	P4.0	E-2
INT0 INT1	I	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	1 (39) 2 (40)	P1.0 P1.1	A-4
INT2	I	I	Quasi-interrupt with detection of rising edges	3 (41)	P1.2	A-4
INT4	I	I	External interrupt with detection of rising and falling edges.	4 (42)	P1.3	A-4
TCL00	I/O	I	Timer/counter 0 clock output	5 (43)	P2.0	D-2
TCL01	I/O	I	Timer/counter 1 clock output	6 (44)	P2.1	D-2
CLO	I/O	I	Clock output	7 (1)	P2.2	D-2
BUZ	I/O	I	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 4.19 MHz for buzzer sound	8 (2)	P2.3	D-2
TCL0	I/O	I	External clock input for timer/counter 0	9 (3)	P3.0	D-4
TCL1	I/O	I	External clock input for timer/counter 1	10 (4)	P3.1	D-4
KS0-KS3 KS4-KS7	I/O	I	Quasi-interrupt inputs with falling edge detection	31-34 (26-29) 35-38 (30-33)	P6.0-P6.3 P7.0-P7.3	D-4
V _{DD}	–	–	Power supply	11 (5)	–	–
V _{SS}	–	–	Ground	12 (6)	–	–
RESET	–	–	RESET signal	18 (12)	–	B
X _{IN} X _{OUT}	–	–	Crystal, or ceramic oscillator signal for main system clock. (For external clock input, use X _{IN} and input X _{IN} 's reverse phase to X _{OUT})	14 (8) 13 (7)	–	–
TEST	–	–	Chip test input pin, Hold GND when the device is operating.	15 (9)	–	–
NC	–	–	No connection	(16, 38)	–	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1-2. KS57C5304/C5308/C5312 Pin Descriptions

Pin Name	Pin Type	Description	Pin Number	Share Pin	Circuit Type
P1.0	I	1-bit input port. 1-bit and 4-bit read and test is possible. Each bit pull-up resistors are assignable.	23 (25)	INT0	A-4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 2 and 3 can be paired to enable 8-bit data transfer.	24 (26) 25 (27) 26 (28) 27 (29)	TCLO0 TCLO1 CLO BUZ	D-2
P3.0 P3.1			28 (30) 29 (31)	TCL0 TCL1	D-4
P4.0 P4.1 P4.2 P4.3 P5.0-P5.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. The N-channel open-drain or push-pull output can be selected by software (1-bit unit). Ports 4 and 5 can be paired to enable 8-bit data transfer.	5 (5) 6 (6) 8 (8) 9 (10) 10-13 (11-14)	BTCL0	E-2
P6.0-P6.3 P7.0-P7.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	14-17 (15-18) 18-21 (19-22)	KS0-KS3 KS4-KS7	D-4

Table 1-2. KS57C5304/C5308/C5312 Pin Descriptions (Continued)

Pin Name	I/O Type	Description	Pin Number	Share Pin	Circuit Type
DTMF	O	DTMF output.	22 (23)	–	G-6
INT0	I	External interrupt input. The triggering edge for INT0 is selectable.	23 (25)	P1.0	A-3
TCLO0	I/O	Timer/counter 0 clock output	24 (26)	P2.0	D-2
TCLO1	I/O	Timer/counter 1 clock output	25 (27)	P2.1	D-2
CLO	I/O	Clock output	26 (28)	P2.2	D-2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 4.19 MHz for buzzer sound	27 (29)	P2.3	D-2
TCL0	I/O	External clock input for timer/counter 0	28 (30)	P3.0	D-4
TCL1	I/O	External clock input for timer/counter 1	29 (31)	P3.1	D-4
BTCO	I/O	Basic timer clock output	5 (5)	P4.0	E-2
V _{DD}	–	Power supply	30 (32)	–	–
V _{SS}	–	Ground	1 (1)	–	–
X _{IN} X _{OUT}	–	Crystal, or ceramic oscillator signal for main system clock. (For external clock input, use X _{IN} and input X _{IN} 's reverse phase to X _{OUT})	3 (3) 2 (2)	–	–
NC	–	No connection	(9, 24)	–	–
TEST	–	Chip test input pin, Hold GND when the device is operating.	4 (4)	–	–
RESET	–	RESET signal	7 (7)	–	B
KS0-KS3 KS4-KS7	I/O	Quasi-interrupt inputs with falling edge detection	14-17 (15-18) 18-21 (19-22)	P6.0-P6.3 P7.0-P7.3	D-4

NOTE: Parentheses indicate the pin number for 32-SOP package.

PIN CIRCUIT DIAGRAMS

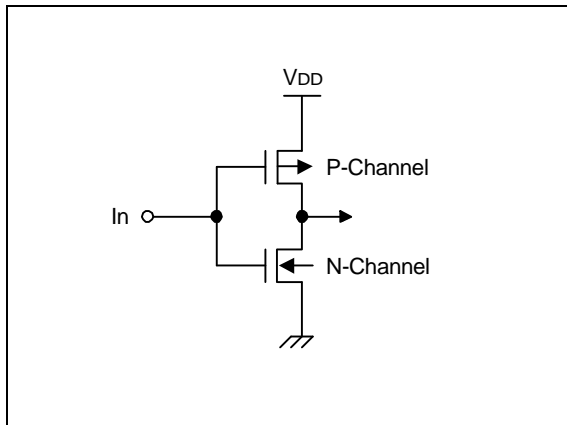


Figure 1-6. Pin Circuit Type A

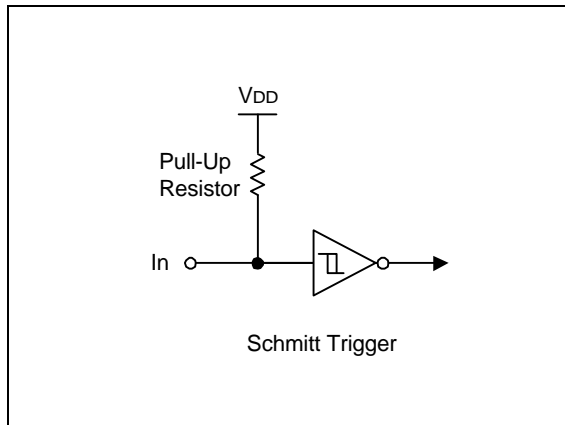


Figure 1-8. Pin Circuit Type B

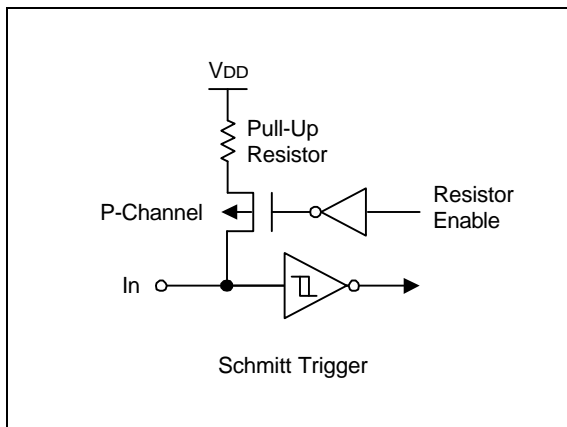


Figure 1-7. Pin Circuit Type A-4

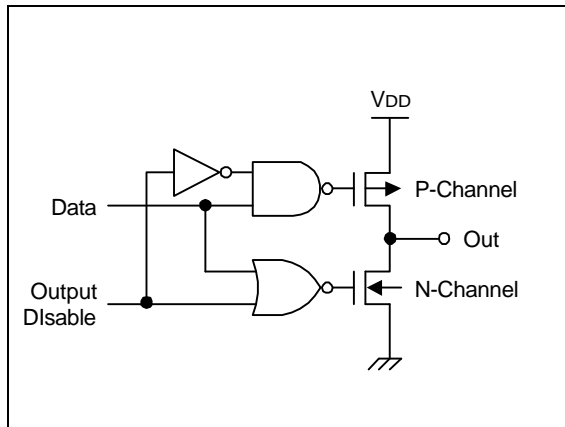


Figure 1-9. Pin Circuit Type C

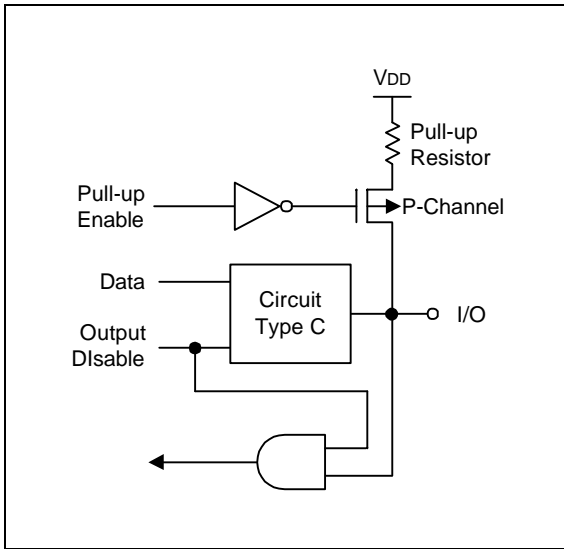


Figure 1-10. Pin Circuit Type D-2

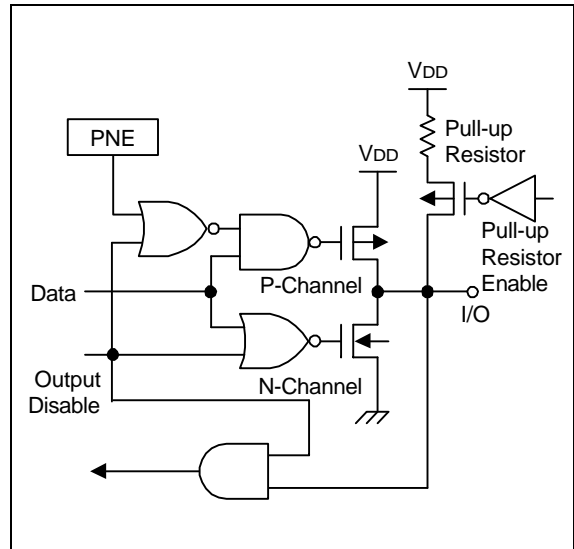


Figure 1-12. Pin Circuit Type E-2

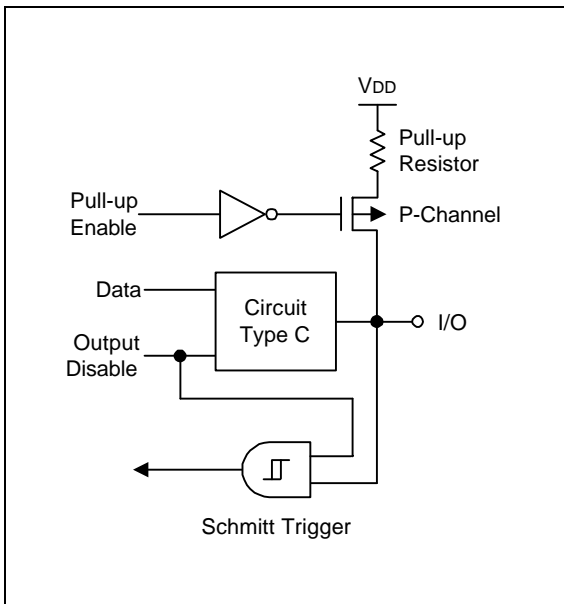


Figure 1-11. Pin Circuit Type D-4

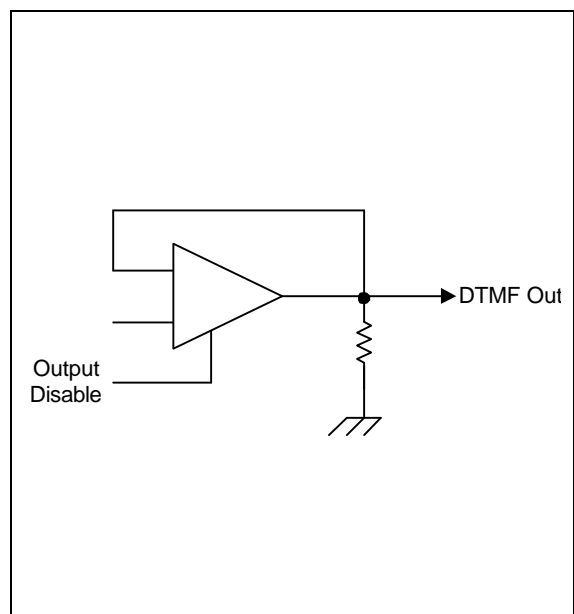


Figure 1-13. Pin Circuit Type G-6

13

ELECTRICAL DATA

OVERVIEW

In this section, information on KS57C5204/C5208/C5304/C5308/C5312 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

- Absolute maximum ratings
- D.C. electrical characteristics
- System clock oscillator characteristics
- I/O capacitance
- A.C. electrical characteristics
- Operating voltage range

Miscellaneous Timing Waveforms

- A.C timing measurement point
- Clock timing measurement at X_{IN} and X_{OUT}
- TCL timing
- Input timing for RESET
- Input timing for external interrupts

Stop Mode Characteristics and Timing Waveforms

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by RESET
- Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_O	–	– 0.3 to $V_{DD} + 0.3$	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value) + 15 (note)	mA
		All I/O ports active	+ 100 (Peak value) + 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	$^\circ\text{C}$
Storage Temperature	T_{stg}	–	– 65 to + 150	$^\circ\text{C}$

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 13-2. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for $V_{IH2} - V_{IH3}$	$0.7 V_{DD}$	–	V_{DD}	V
	V_{IH2}	Ports 1, 3, 6, 7, and RESET	$0.8 V_{DD}$		V_{DD}	
	V_{IH3}	X_{IN} and X_{OUT}	$V_{DD} - 0.1$		V_{DD}	
Input low voltage	V_{IL1}	All input pins except those specified below for $V_{IL2} - V_{IL3}$	–	–	$0.3 V_{DD}$	V
	V_{IL2}	Ports 1, 3, 6, 7, and RESET			$0.2 V_{DD}$	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	

Table 13-2. D.C. Electrical Characteristics (Continued)

 $(T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH}	$I_{OH} = -1\text{ mA}$ Ports except 1	$V_{DD} - 1.0$	–	–	V
Output low voltage	V_{OL1}	$V_{DD} = 4.5\text{ V}$ to 5.5 V $I_{OL} = 15\text{ mA}$, Ports 4 and 5 only $V_{DD} = 1.8$ to 5.5 V , $I_{OL} = 1.6\text{ mA}$	–	–	2	V
	V_{OL2}	$V_{DD} = 4.5\text{ V}$ to 5.5 V $I_{OL} = 4\text{ mA}$, all out ports except 4,5 $V_{DD} = 1.8$ to 5.5 V , $I_{OL} = 1.6\text{ mA}$	–	–	0.4	V
Input high leakage current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below	–	–	3	μA
	I_{LIH2}	$V_I = V_{DD}$ X_{IN} and X_{OUT}	–	–	20	μA
Input low leakage current	I_{LIL1}	$V_I = 0\text{ V}$ All input pins except below and RESET	–	–	–3	μA
	I_{LIL2}	$V_I = 0\text{ V}$ X_{IN} and X_{OUT} only	–	–	–20	μA
Output high leakage current	I_{LOH}	$V_O = V_{DD}$ All out pins	–	–	3	μA
Output low leakage current	I_{LOL}	$V_O = 0\text{ V}$ All out pins	–	–	–3	μA
Pull-up resistor	R_{L1}	$V_{DD} = 5\text{ V}$; $V_I = 0\text{ V}$ except RESET $V_{DD} = 3\text{ V}$	25	47	100	$\text{k}\Omega$
	R_{L2}	$V_{DD} = 5\text{ V}$; $V_I = 0\text{ V}$; RESET $V_{DD} = 3\text{ V}$	100	220	400	$\text{k}\Omega$
			200	450	800	$\text{k}\Omega$

Table 13-2. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

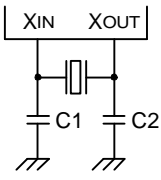
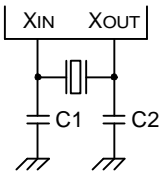
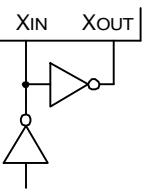
Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply current (1)	I _{DD1} (DTMF on)	Run mode; V _{DD} = 5 V ± 10% (2) 3.58 MHz crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	2.5 1.4	5.0 3.0	mA	
	I _{DD2} (DTMF off)	Run mode; V _{DD} = 5 V ± 10% crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	6.0 MHz	2.5	8.0	mA
				3.58 MHz	1.6	4.0	
				6.0 MHz 3.58 MHz	1.2 0.7	4.0 2.3	
	I _{DD3}	Idle mode; V _{DD} = 5 V ± 10% crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	6.0 MHz	0.7	2.5	mA
3.58 MHz				0.6	1.8		
6.0 MHz 3.58 MHz				0.3 0.2	1.5 1.0		
I _{DD4}	Stop mode; V _{DD} = 5 V ± 10% Stop mode; V _{DD} = 3 V ± 10%	–	0.01	0.01	3	μA	
			0.01	0.01	2		
Row tone level	V _{ROW}	V _{DD} = 2.0 V to 5.5 V RL = 12 kΩ, Temp = -30 °C to 60 °C	-16.0	-14.0	-11.0	dBV	
Ratio of column to row tone	dB _{CR}	V _{DD} = 2.0 V to 5.5 V RL = 12 kΩ, Temp = -30 °C to 60 °C	1	2	3	dB	
Distortion (Dual tone)	THD	V _{DD} = 2.0 V to 5.5 V 1MHz band; RL= 12 kΩ Temp = -30 °C to 60 °C	–	–	5	%	

NOTES:

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers.
2. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 13-3. Main System Clock Oscillator Characteristics

(T_A = -40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V _{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V _{DD} = 3 V	–	–	10	ms
External Clock		X _{IN} input frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		X _{IN} input high and low level width (t _{XH} , t _{XL})	–	83.3	–	1250	ns

NOTES:

- Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 13-4. Recommended Oscillator Constants

(T_A = -40 °C to +85 °C)

Manufacturer	Series Number ⁽¹⁾	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR 05M5	3.58 MHz-6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR 05MC5	3.58 MHz-6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR 05MC3	3.58 MHz-6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:

1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 13-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C _{IN}	f = 1 MHz; Unmeasured pins are returned to V _{SS}	–	–	15	pF
Output Capacitance	C _{OUT}		–	–	15	pF
I/O Capacitance	C _{IO}		–	–	15	pF

Table 13-6. A.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t _{CY}	V _{DD} = 2.7 V to 5.5 V	0.67	-	64	μs
		V _{DD} = 1.8 V to 5.5 V	1.33			
TCL0, TCL1 Input Frequency	f _{T10} , f _{T11}	V _{DD} = 2.7 V to 5.5 V	0	-	1.5	MHz
		V _{DD} = 1.8 V to 5.5V			1	MHz
TCL0, TCL1 Input High, Low Width	t _{TIH0} , t _{TIL0} t _{TIH1} , t _{TIL1}	V _{DD} = 2.7 V to 5.5 V	0.48	-	-	μs
		V _{DD} = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t _{INTH} , t _{INTL}	INT0, INT1, INT2, INT4, KS0-KS7	10	-	-	μs
RESET Input Low Width	t _{RSL}	Input	10	-	-	μs

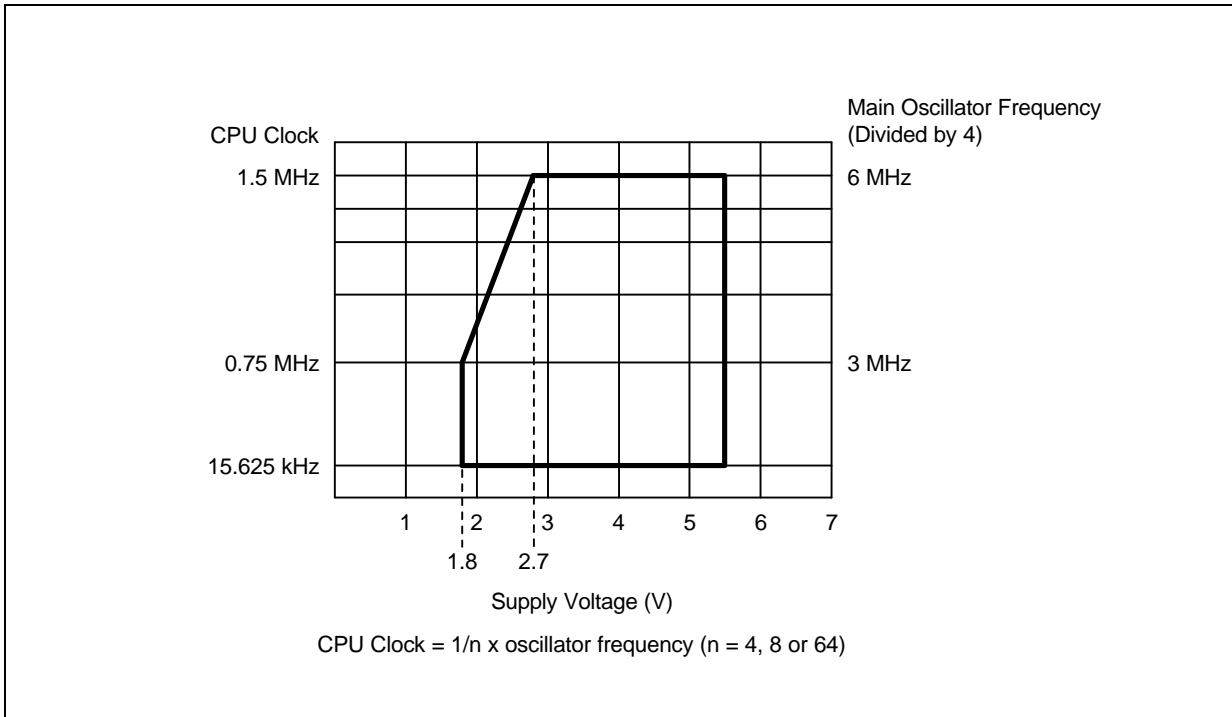


Figure 13-1. Standard Operating Voltage Range

Table 13-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = - 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDDR}	-	1.8	-	5.5	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.8 V	-	0.1	10	μA
Release signal set time	t _{SREL}	-	0	-	-	μs
Oscillator stabilization wait time (1)	t _{WAIT}	Released by RESET	-	2 ¹⁷ /f _X	-	ms
		Released by interrupt	-	(2)	-	

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

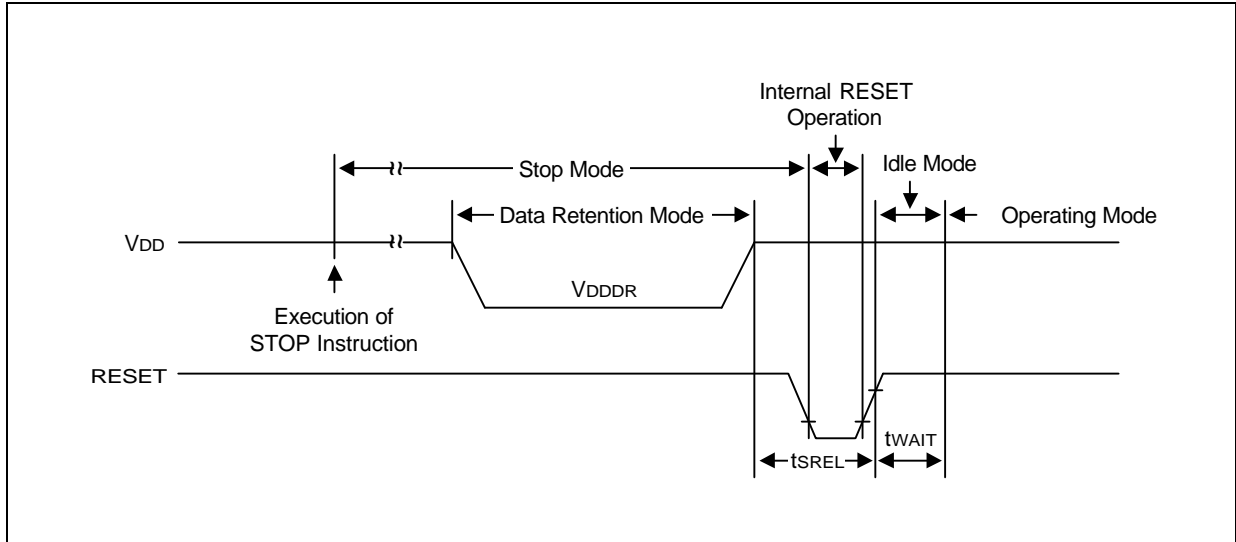


Figure 13-2. Stop Mode Release Timing When Initiated by RESET

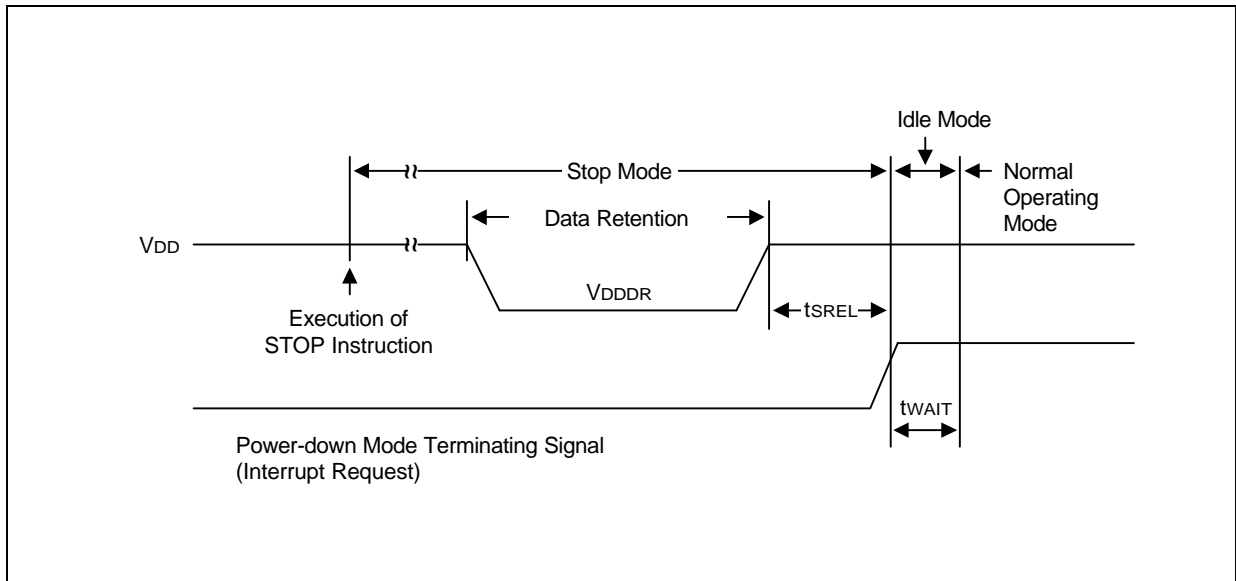


Figure 13-3. Stop Mode Release Timing When Initiated by Interrupt Request

Timing Waveforms (continued)

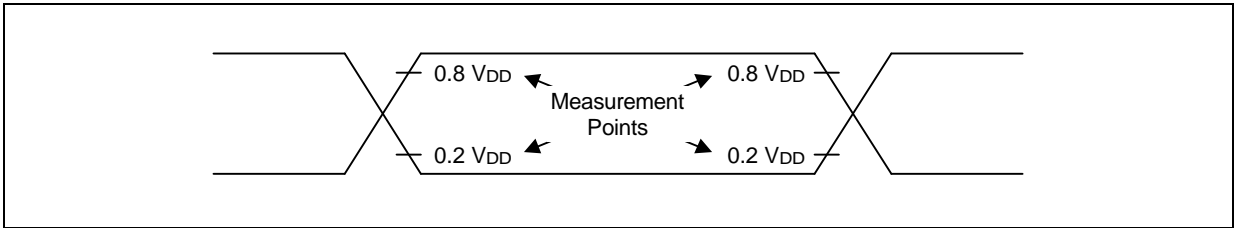


Figure 13-4. A.C. Timing Measurement Points (Except for X_{IN})

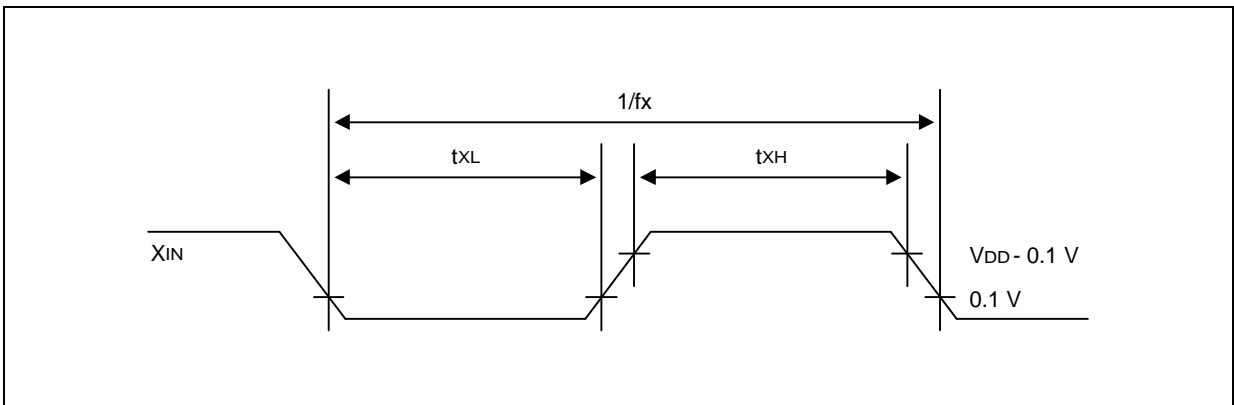


Figure 13-5. Clock Timing Measurement at X_{IN}

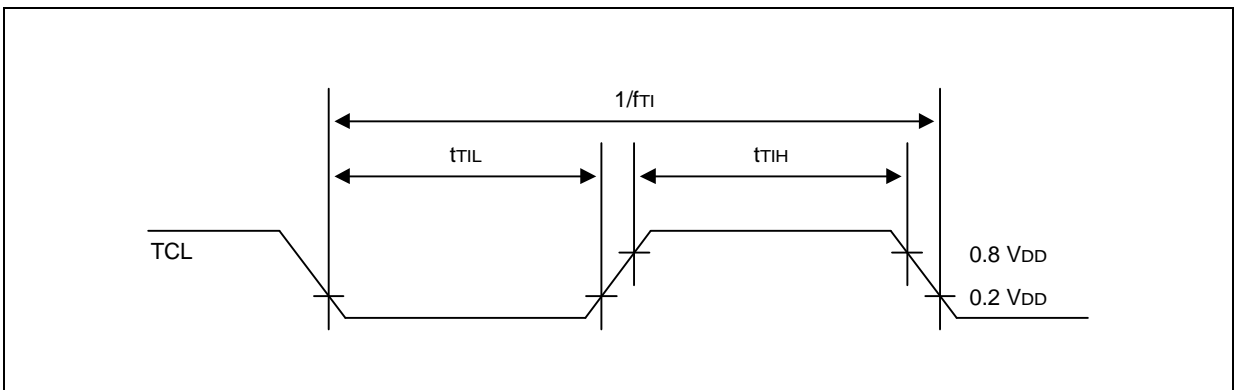


Figure 13-6. TCL Timing

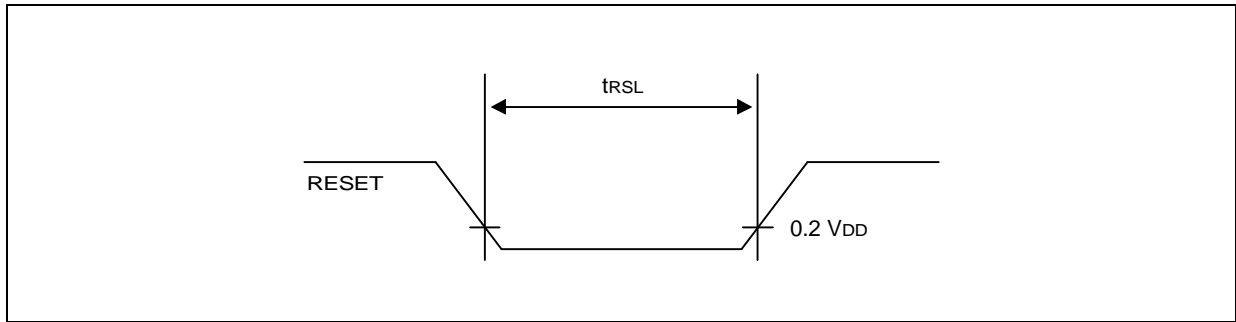


Figure 13-7. Input Timing for RESET Signal

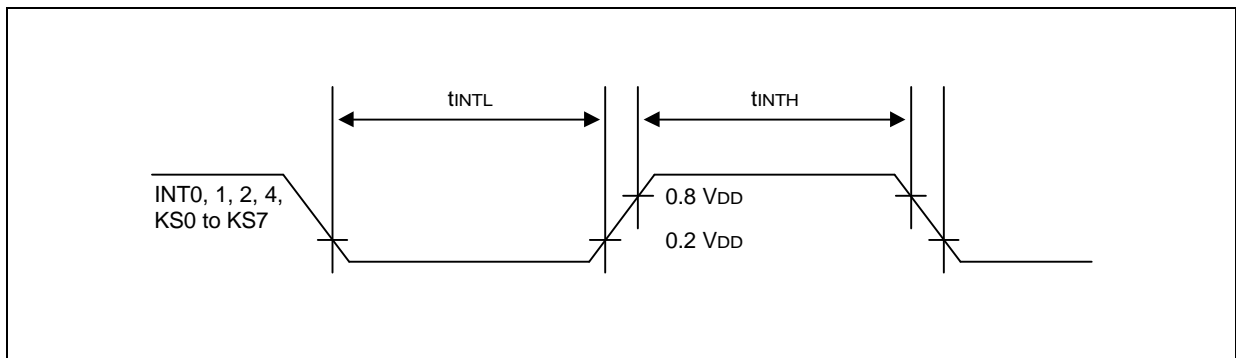


Figure 13-8. Input Timing for External Interrupts and Quasi-Interrupts

NOTES

14 MECHANICAL DATA

OVERVIEW

The KS57C5204/C5208 microcontroller are available in a 42-pin SDIP package (42-SDIP-600), and a 44-pin QFP package (44-QFP-1010B). The KS57C5304/C5308/C5312 microcontrollers are available in a 30-pin SDIP package (30-SDIP-400) and a 32-pin SOP package (32-SOP-450A).

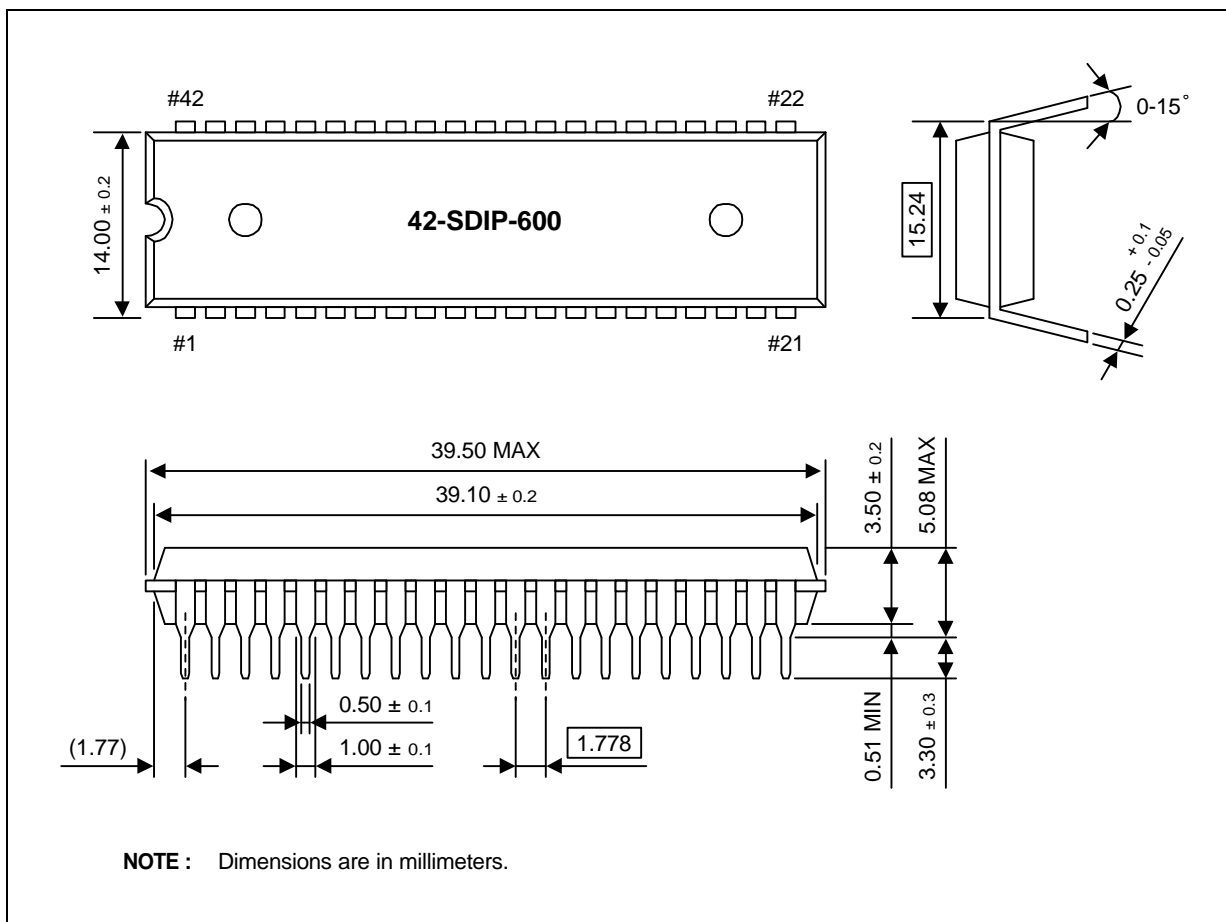


Figure 14-1. 42-SDIP-600 Package Dimensions

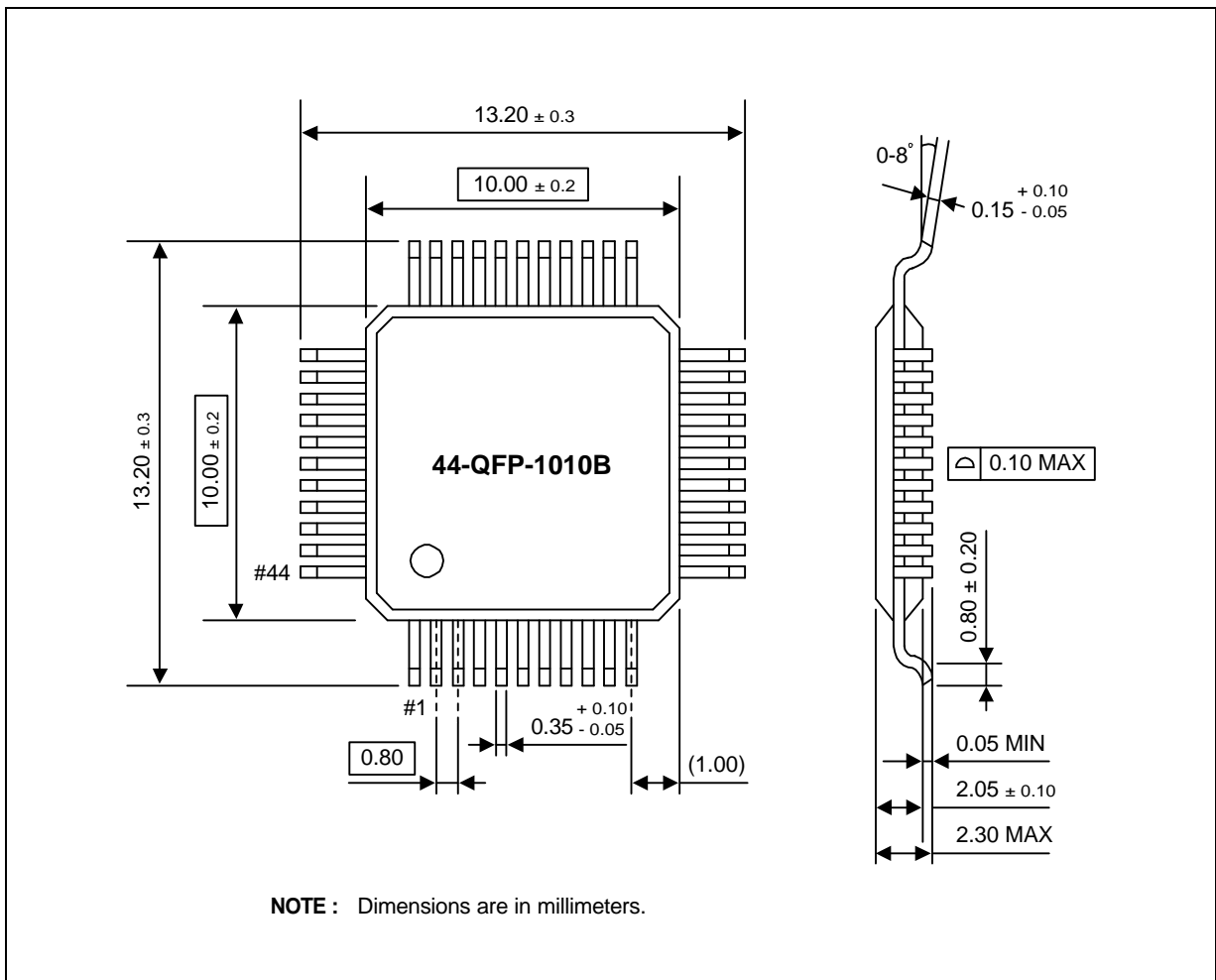


Figure 14-2. 44-QFP-1010B Package Dimensions

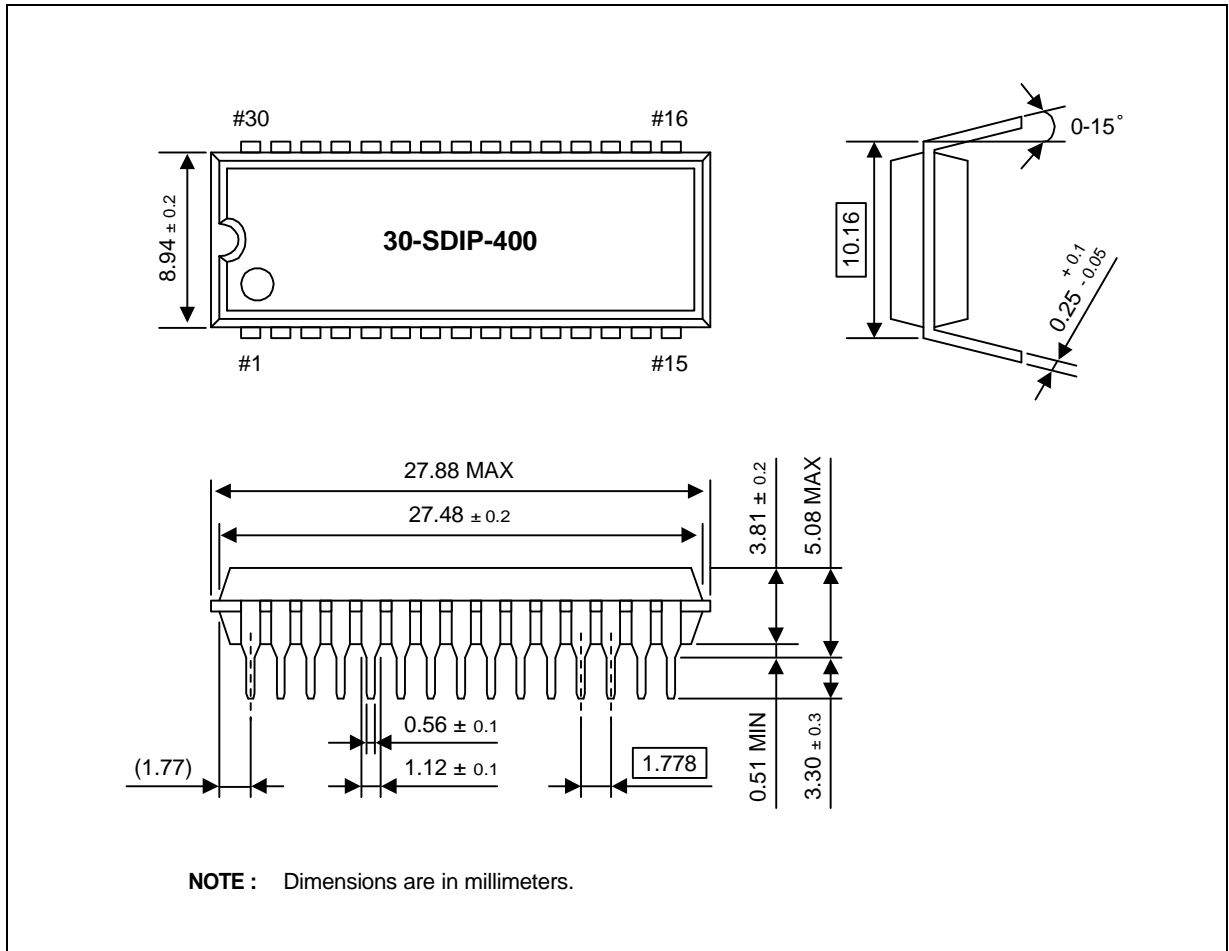


Figure 14-3. 30-SDIP-400 Package Dimensions

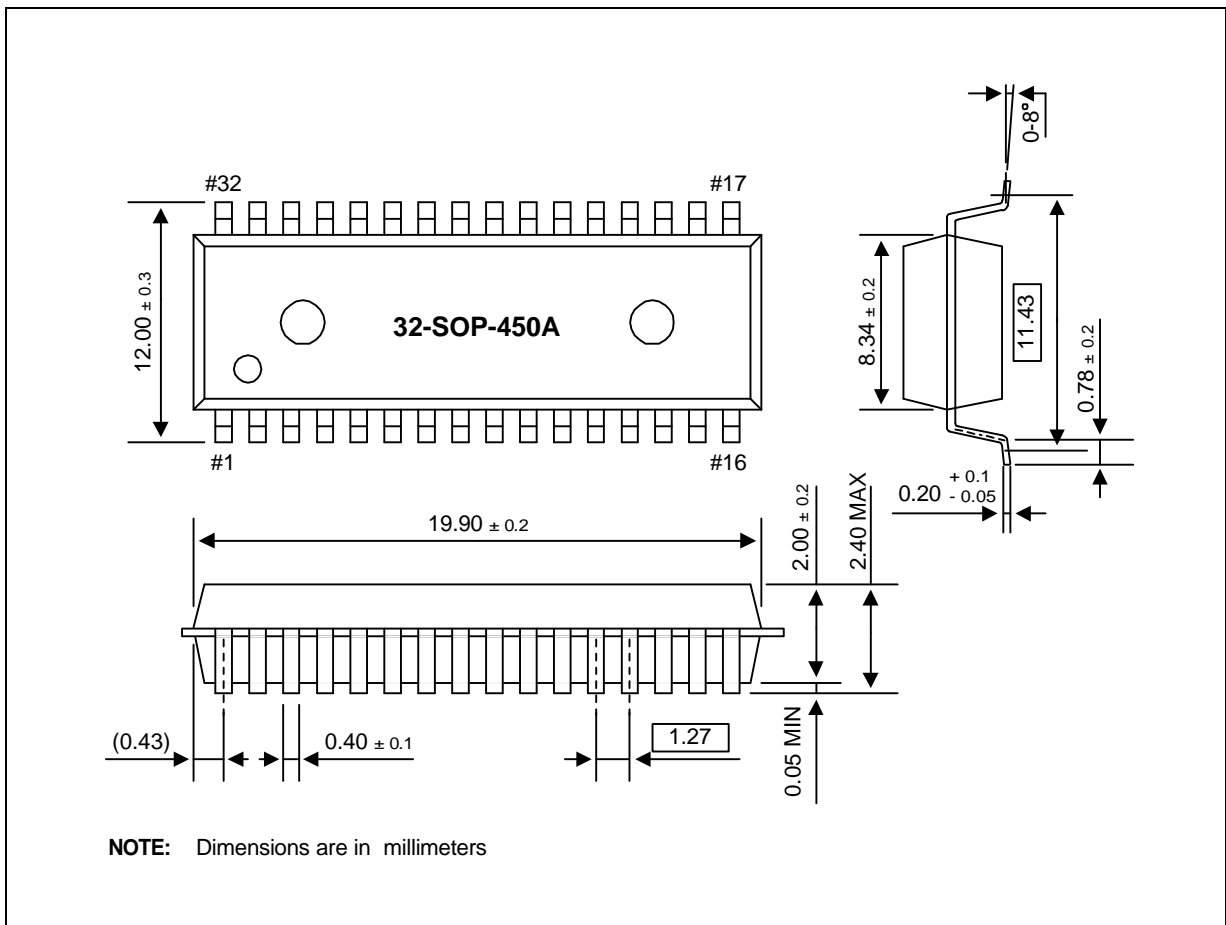


Figure 14-4. 32-SOP-450A Package Dimensions

15

KS57P5208/P5308/P5312 OTP

OVERVIEW

The KS57P5208/P5308/P5312 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C5204/C5208/C5304/C5308/C5312 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The KS57P5208/P5308/P5312 is fully compatible with the KS57C5208/C5308/C5312, both in function and in pin configuration. Because of its simple programming requirements, the KS57P5208/P5308/P5312 is ideal for use as an evaluation chip for the KS57C5208/C5308/C5312.

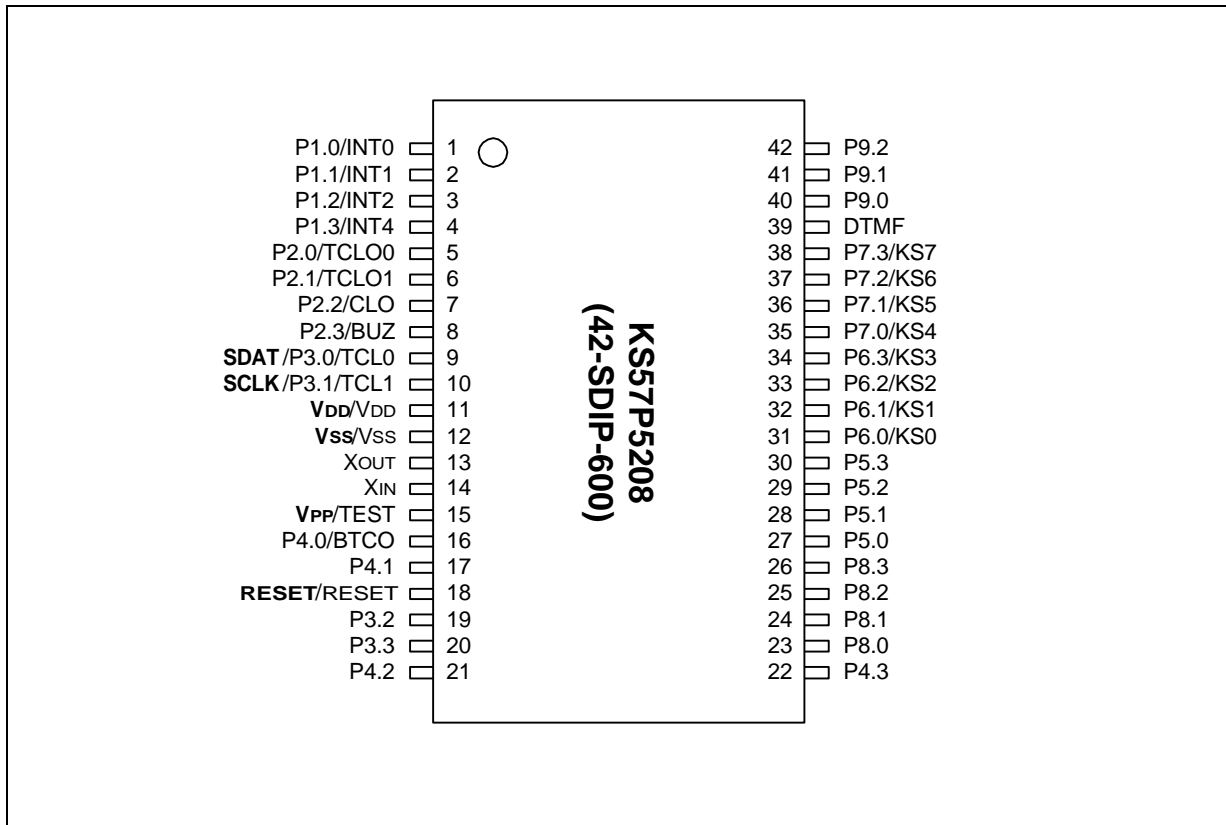


Figure 15-1. KS57P5208 Pin Assignment Diagram (42-SDIP)

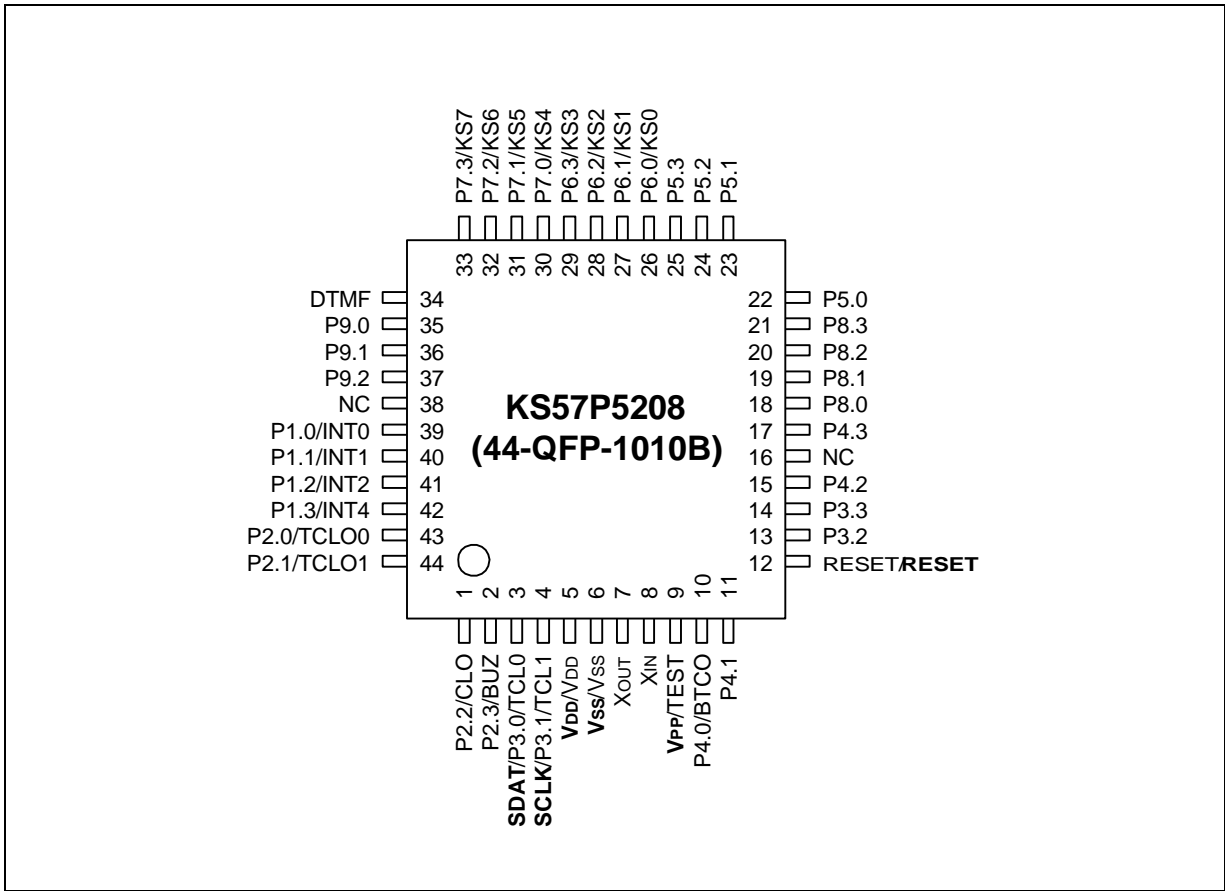


Figure 15-2. KS57P5208 Pin Assignment Diagram (44-QFP)

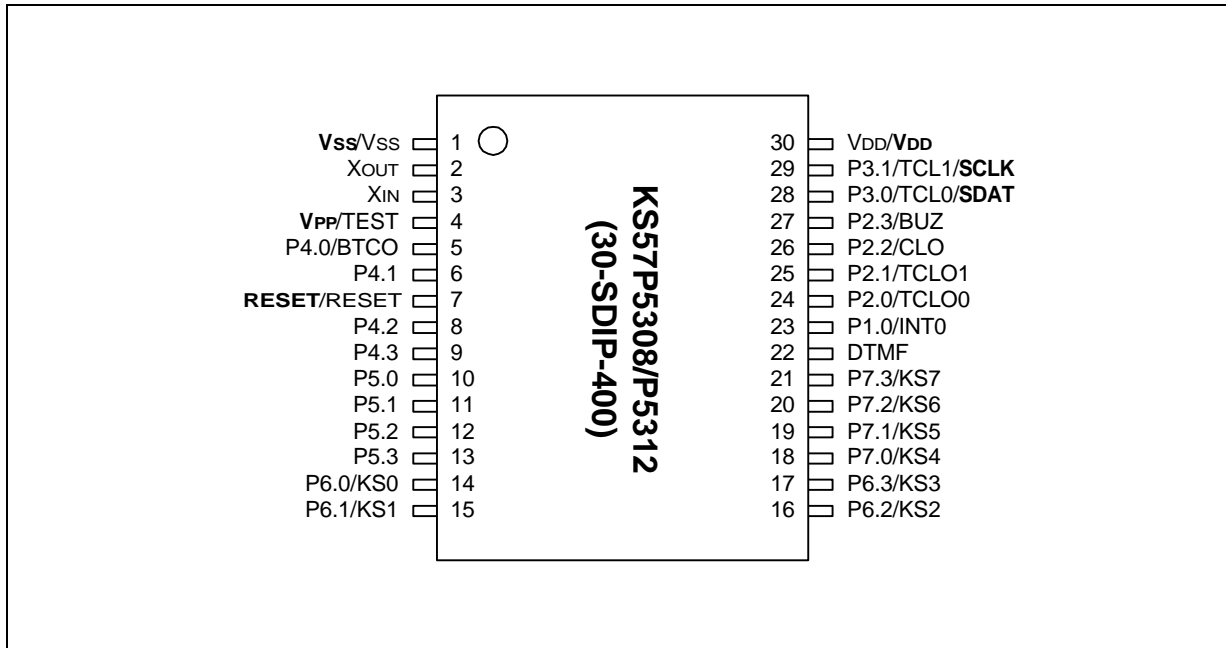


Figure 15-3. KS57P5308/P5312 Pin Assignment Diagram (30-SDIP)

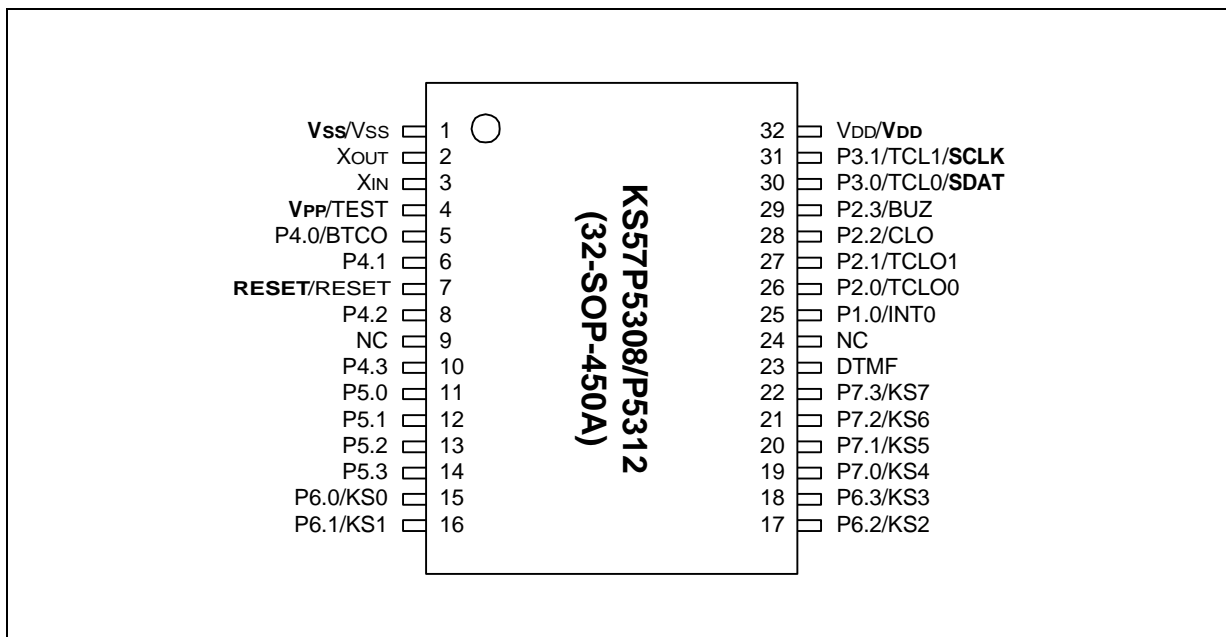


Figure 15-4. KS57P5308/P5312 Pin Assignment Diagram (32-SOP)

Table 15-1. KS57P5208 Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.0	SDAT	9 (3)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P3.1	SCLK	10 (4)	I/O	Serial clock pin. Input only pin.
TEST	V _{PP} (TEST)	15 (9)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) Hold GND when OPT is operating.
RESET	RESET	18 (12)	I	Chip initialization
V _{DD} / V _{SS}	V _{DD} / V _{SS}	11/12 (5/6)	I	Logic power supply pin. V _{DD} should be tied to +5 V during programming.

NOTE: Parentheses indicate pin numbers of 44 QFP package.

Table 15-2. KS57P5308/P5312 Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.0	SDAT	28 (30)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P3.1	SCLK	29 (31)	I/O	Serial clock pin. Input only pin.
TEST	V _{PP} (TEST)	4 (4)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) Hold GND when OPT is operating.
RESET	RESET	7 (7)	I	Chip initialization
V _{DD} / V _{SS}	V _{DD} / V _{SS}	30/1 (32/1)	I	Logic power supply pin. V _{DD} should be tied to +5 V during programming.

NOTE: Parentheses indicate pin numbers of 32 SDIP package.

Table 15-3. Comparison of KS57P5208 and KS57C5208 Features

Characteristic	KS57P5208	KS57C5208
Program Memory	8 K byte EPROM	8 K byte mask ROM
Operating Voltage (V_{DD})	1.8 V (3 MHz) to 5.5 V	1.8 V (3 MHz) to 5.5 V
OTP Programming Mode	$V_{DD} = 5 V$, $V_{PP}(\text{TEST}) = 12.5 V$	–
Pin Configuration	42 SDIP / 44 QFP	42 SDIP / 44 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

Table 15-4. Comparison of KS57P5308/P5312 and KS57C5308/C5312 Features

Characteristic	KS57P5308/P5312	KS57C5308/C5312
Program Memory	8 K byte EPROM / 12 K (P5312)	8 K byte mask ROM / 12 K (C5312)
Operating Voltage (V_{DD})	1.8 V (3 MHz) to 5.5 V	1.8 V (3 MHz) to 5.5 V
OTP Programming Mode	$V_{DD} = 5 V$, $V_{PP}(\text{TEST}) = 12.5 V$	–
Pin Configuration	30 SOP / 32 SOP	30 SOP / 32 SOP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the $V_{pp}(\text{TEST})$ pin of the KS57P5208/P5308/P5312, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-5. Operating Mode Selection Criteria

V_{DD}	$V_{pp}(\text{TEST})$	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5V	0	0000H	0	EPROM program
	12.5V	0	0000H	1	EPROM verify
	12.5V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

OTP ELECTRICAL DATA

Table 15-6. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to $V_{DD} + 0.3$	V
Output Voltage	V_O	–	– 0.3 to $V_{DD} + 0.3$	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value) + 15 (note)	mA
		All I/O ports active	+ 100 (Peak value) + 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	$^\circ\text{C}$
Storage Temperature	T_{stg}	–	– 65 to + 150	$^\circ\text{C}$

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 15-7. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for $V_{IH2} - V_{IH3}$	$0.7 V_{DD}$	–	V_{DD}	V
	V_{IH2}	Ports 1, 3, 6, 7, and RESET	$0.8 V_{DD}$		V_{DD}	
	V_{IH3}	X_{IN} and X_{OUT}	$V_{DD} - 0.1$		V_{DD}	
Input low voltage	V_{IL1}	All input pins except those specified below for $V_{IL2} - V_{IL3}$	–	–	$0.3 V_{DD}$	V
	V_{IL2}	Ports 1, 3, 6, 7, and RESET			$0.2 V_{DD}$	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	

Table 15-7. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V _{OH}	I _{OH} = -1 mA Ports except 1	V _{DD} - 1.0	-	-	V
Output low voltage	V _{OL1}	V _{DD} = 4.5 V to 5.5 V I _{OL} = 15 mA, Ports 4 and 5 only V _{DD} = 1.8 to 5.5 V, I _{OL} = 1.6mA	-	-	2	V
	V _{OL2}	V _{DD} = 4.5 V to 5.5 V I _{OL} = 4 mA, all out ports except 4,5 V _{DD} = 1.8 to 5.5 V, I _{OL} = 1.6mA	-	-	0.4	V
Input high leakage current	I _{LIH1}	V _I = V _{DD} All input pins except those specified below	-	-	3	μA
	I _{LIH2}	V _I = V _{DD} X _{IN} and X _{OUT}	-	-	20	μA
Input low leakage current	I _{LIL1}	V _I = 0 V All input pins except below and RESET	-	-	-3	μA
	I _{LIL2}	V _I = 0 V X _{IN} and X _{OUT} only	-	-	-20	μA
Output high leakage current	I _{LOH}	V _O = V _{DD} All out pins	-	-	3	μA
Output low leakage current	I _{LOL}	V _O = 0 V All out pins	-	-	-3	μA
Pull-up resistor	R _{L1}	V _{DD} = 5 V; V _I = 0 V except RESET V _{DD} = 3 V	25	47	100	kΩ
	R _{L2}	V _{DD} = 5 V; V _I = 0 V; RESET V _{DD} = 3 V	100	220	400	kΩ
			200	450	800	kΩ

Table 15-7. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

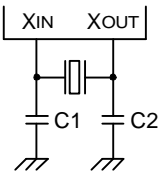
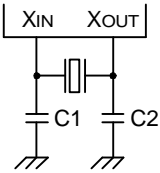
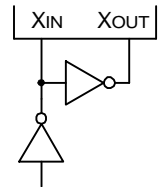
Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply current (1)	I _{DD1} (DTMF on)	Run mode; V _{DD} = 5 V ± 10% (2) 3.58 MHz crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	2.5 1.4	5.0 3.0	mA	
	I _{DD2} (DTMF off)	Run mode; V _{DD} = 5 V ± 10% crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	6.0 MHz	2.5	8.0	mA
				3.58 MHz	1.6	4.0	
				6.0 MHz	1.2	4.0	
I _{DD3}	Idle mode; V _{DD} = 5 V ± 10% crystal oscillator, C1 = C2 = 22 pF V _{DD} = 3 V ± 10%	–	6.0 MHz	0.7	2.5	mA	
			3.58 MHz	0.6	1.8		
			6.0 MHz	0.3	1.5		
			3.58 MHz	0.2	1.0		
I _{DD4}	Stop mode; V _{DD} = 5 V ± 10% Stop mode; V _{DD} = 3 V ± 10%	–	0.01	0.01	3	μA	
			0.01	0.01	2		
Row tone level	V _{ROW}	V _{DD} = 2.0 V to 5.5 V RL = 12 kΩ, Temp = -30 °C to 60 °C	-16.0	-14.0	-11.0	dBV	
Ratio of column to row tone	dB _{CR}	V _{DD} = 2.0 V to 5.5 V RL = 12 kΩ, Temp = -30 °C to 60 °C	1	2	3	dB	
Distortion (Dual tone)	THD	V _{DD} = 2.0 V to 5.5 V 1MHz band; RL= 12 kΩ Temp = -30 °C to 60 °C	–	–	5	%	

NOTES:

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers.
2. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 15-8. Main System Clock Oscillator Characteristics

(T_A = -40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V _{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V _{DD} = 3 V	–	–	10	ms
External Clock		X _{IN} input frequency (1)	V _{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V _{DD} = 1.8 V to 5.5 V	0.4	–	3	
		X _{IN} input high and low level width (t _{XH} , t _{XL})	–	83.3	–	1250	ns

NOTES:

- Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 15-9. Input/Output Capacitance $(T_A = 25\text{ }^\circ\text{C}, V_{DD} = 0\text{ V})$

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 15-10. A.C. Electrical Characteristics $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.67	–	64	μs
		$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	1.33	–		
TCL0, TCL1 Input Frequency	f_{TIO}, f_{TI1}	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0	–	1.5	MHz
		$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$			1	MHz
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.48	–	–	μs
		$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$				
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, KS0-KS7	10	–	–	μs
RESET Input Low Width	t_{RSL}	Input	10	–	–	μs

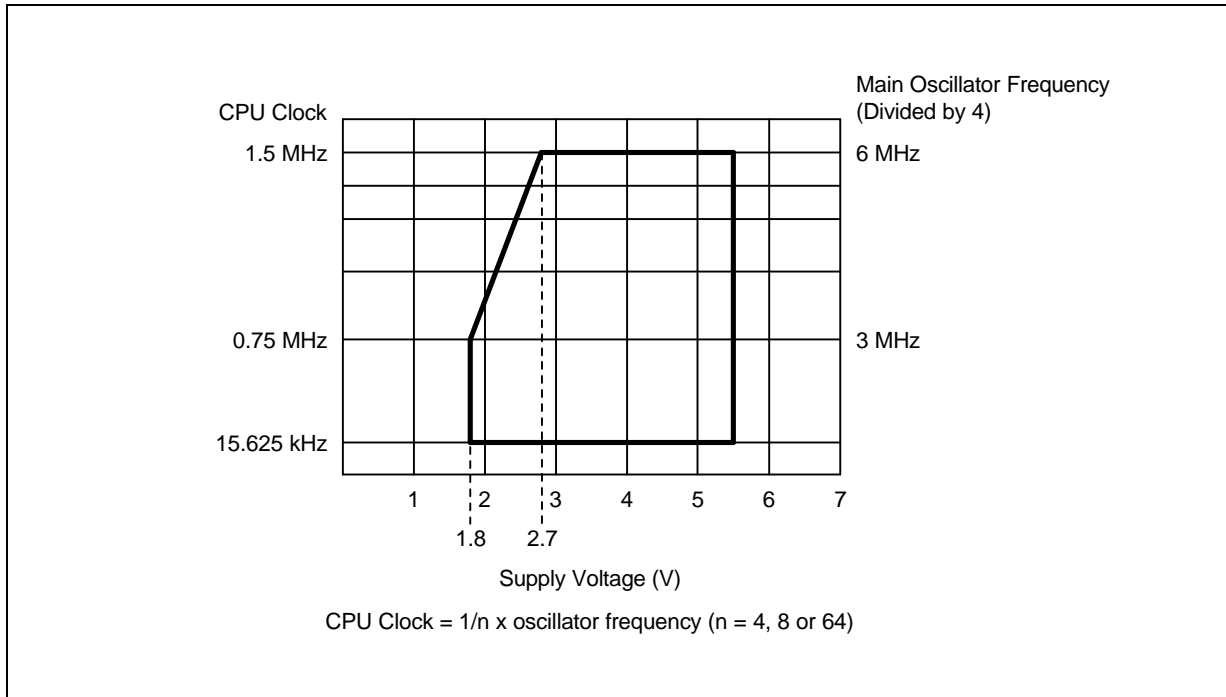


Figure 15-5. Standard Operating Voltage Range

Table 15-11. RAM Data Retention Supply Voltage in Stop Mode

(T_A = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDDR}	-	1.8	-	5.5	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.8 V	-	0.1	10	μA
Release signal set time	t _{SREL}	-	0	-	-	μs
Oscillator stabilization wait time (1)	t _{WAIT}	Released by RESET	-	2 ¹⁷ /f _X	-	ms
		Released by interrupt	-	(2)	-	ms

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

NOTES