

# 1

## PRODUCT OVERVIEW

### SAM8 PRODUCT FAMILY

Samsung's SAM8 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

### KS88C6108/C6116/P6116 MICROCONTROLLERS

The KS88C6108/C6116/P6116 single-chip 8-bit microcontroller is based on the powerful SAM8 CPU architecture. The internal register file is logically expanded to increase the on-chip register space. The KS88C6108/C6116/P6116 have 8/16 K bytes of on-chip program ROM.

Following Samsung's modular design approach, the following peripherals were integrated with the SAM8 core:

- Four programmable I/O ports (total 28 pins)
- One 8-bit basic timer for oscillation stabilization and watchdog functions
- One 8-bit general-purpose timer/counter with selectable clock sources
- One 8-bit counter with selectable clock sources, including Hsync or Csync input
- One 8-bit timer for interval mode
- PWM block with seven 8-bit PWM circuits
- Sync processor block (for Vsync and Hsync I/O, Csync input, and Clamp signal output)

- Multi master IIC-bus with DDC support.

The KS88C6108/C6116/P6116 are a versatile microcontroller that is ideal for use in multi-sync monitors or in general-purpose applications that require sophisticated timer/counter, PWM, sync signal processing, and multi-master IIC-bus support with DDC. It is available in a 42-pin SDIP or a 44-pin QFP package.



**Figure 1-1. KS88C6108/C6116/P6116 Microcontrollers**

## FEATURES

### CPU

- SAM8 CPU core

### Memory

- 8/16-Kbyte internal program memory (ROM)
- 272-byte general-purpose register area

### Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

### Instruction Execution Time

- 500 ns minimum (with 12 MHz CPU clock)

### Interrupts

- Nine interrupt sources
- Nine interrupt vectors
- Six interrupt levels
- Fast interrupt processing for a select level

### General I/O

- Four I/O ports (total 28 pins):

### 8-Bit Basic Timer

- Programmable timer for oscillation stabilization interval control or watchdog timer functions
- Three selectable internal clock frequencies

### Timer/Counters

- One 8-bit general-purpose timer/counter with programmable operating modes and the following clock source options:
  - Two selectable internal clock frequencies
- One 8-bit timer with interval operating mode
- One 8-bit counter with the following clock source options:

- Two selectable internal clock frequencies
- Hsync (or Csync) input from the sync processor block
- External clock source

### Pulse Width Modulator

- Seven 8-bit PWM modules:
  - 8-bit basic frame
  - Four push-pull and three n-channel, open-drain output channels
  - Selectable clock frequencies: 46.875 kHz at 12 MHz fosc.

### Sync Processor

- Detection of sync input signals (Vsync-I, Hsync-I, and Csync-I)
- Sync signal separation and output (Hsync-O, Vsync-O, and Clamp-O)
- Pseudo sync signal output
- Programmable clamp signal output

### DDC and Multi-Master IIC-Bus

- Serial peripheral interface
- Support for display data channel (DDC)

### Oscillator Frequency

- 6 MHz to 12 MHz external crystal oscillator
- Interval Max. 12MHz CPU clock

### Operating Temperature Range

- -40°C to +85°C

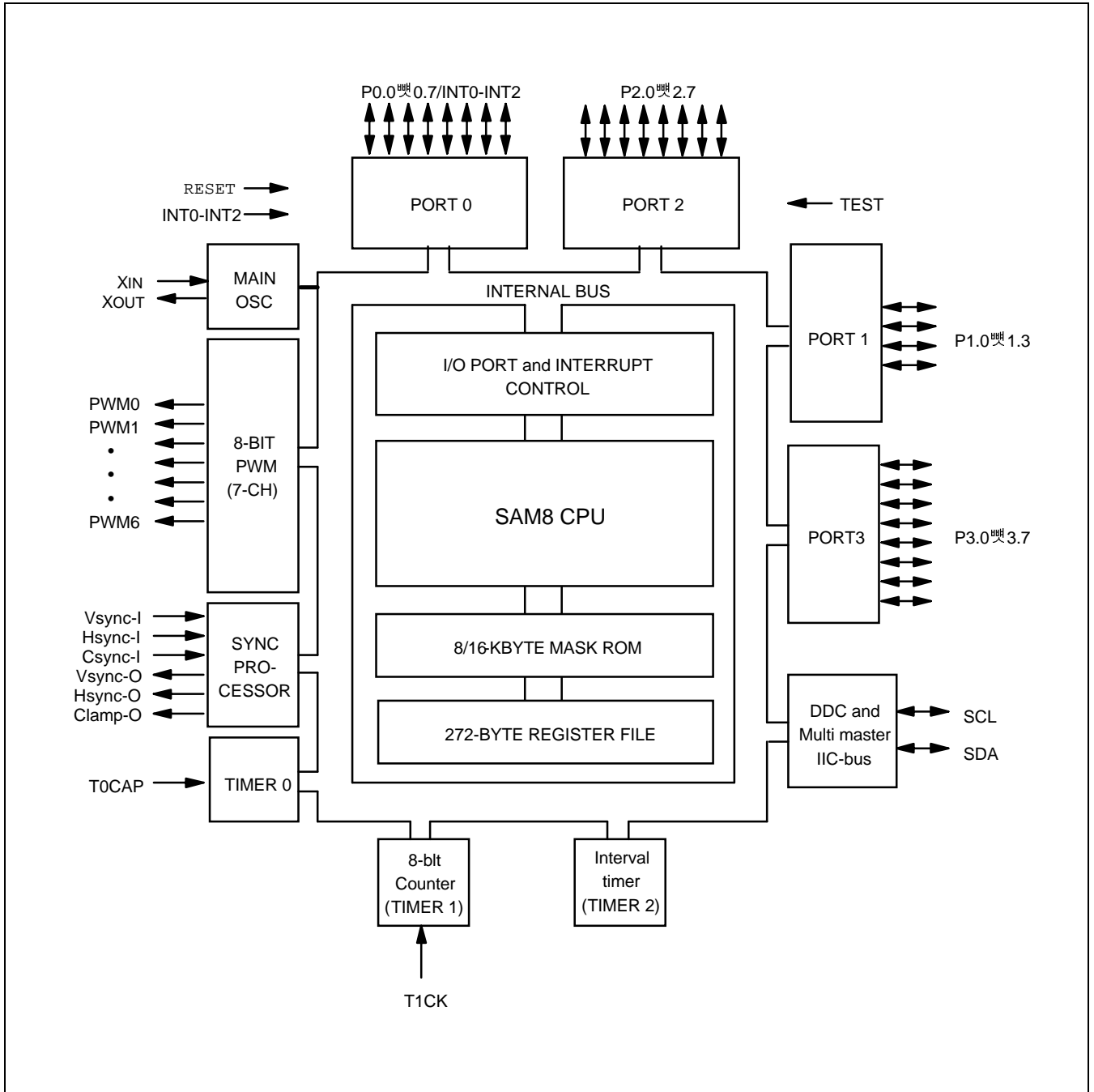
### Operating Voltage Range

- 4.5 V to 5.5 V

### Package Types

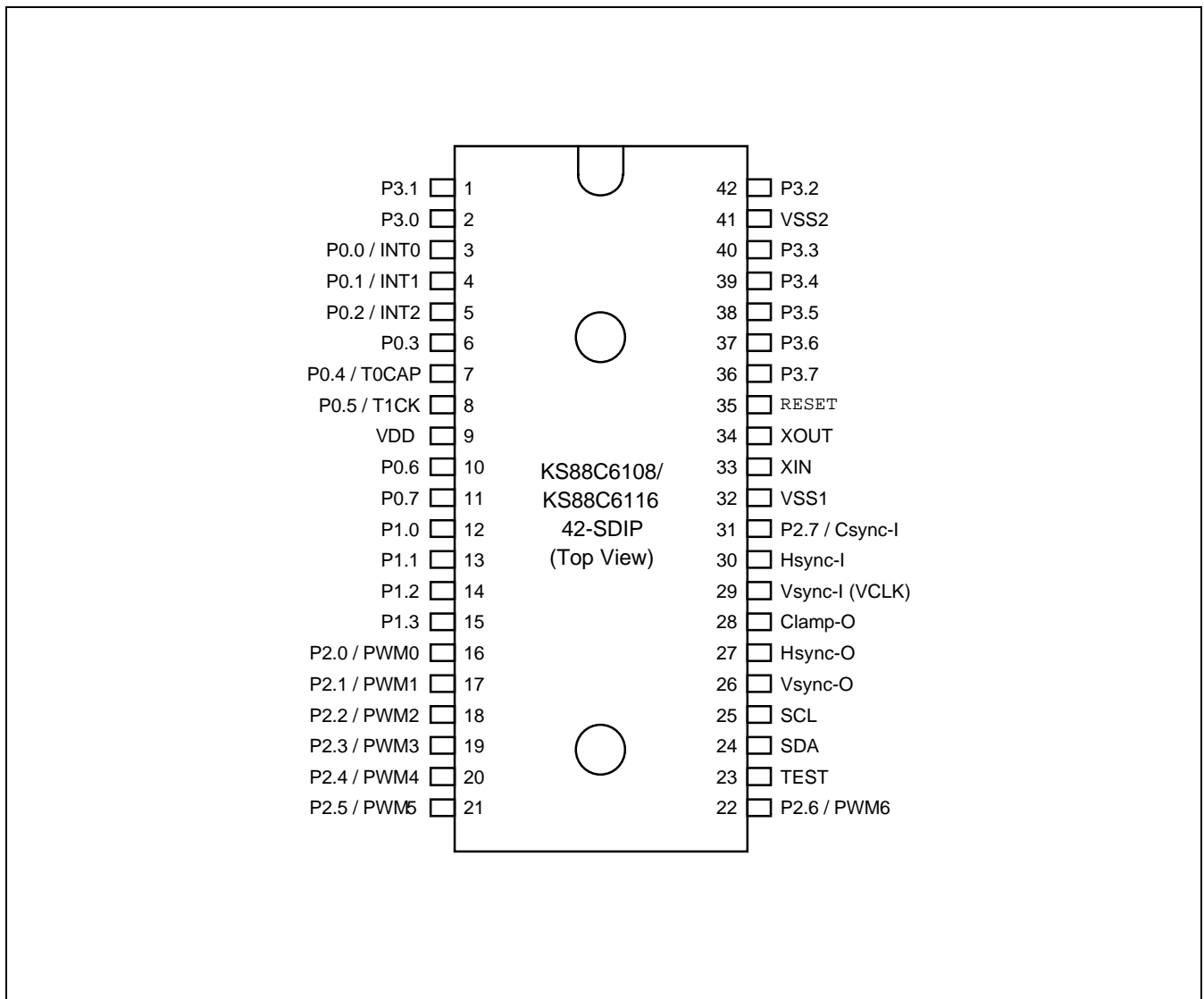
- 42-pin SDIP, 44-pin QFP

**BLOCK DIAGRAM**



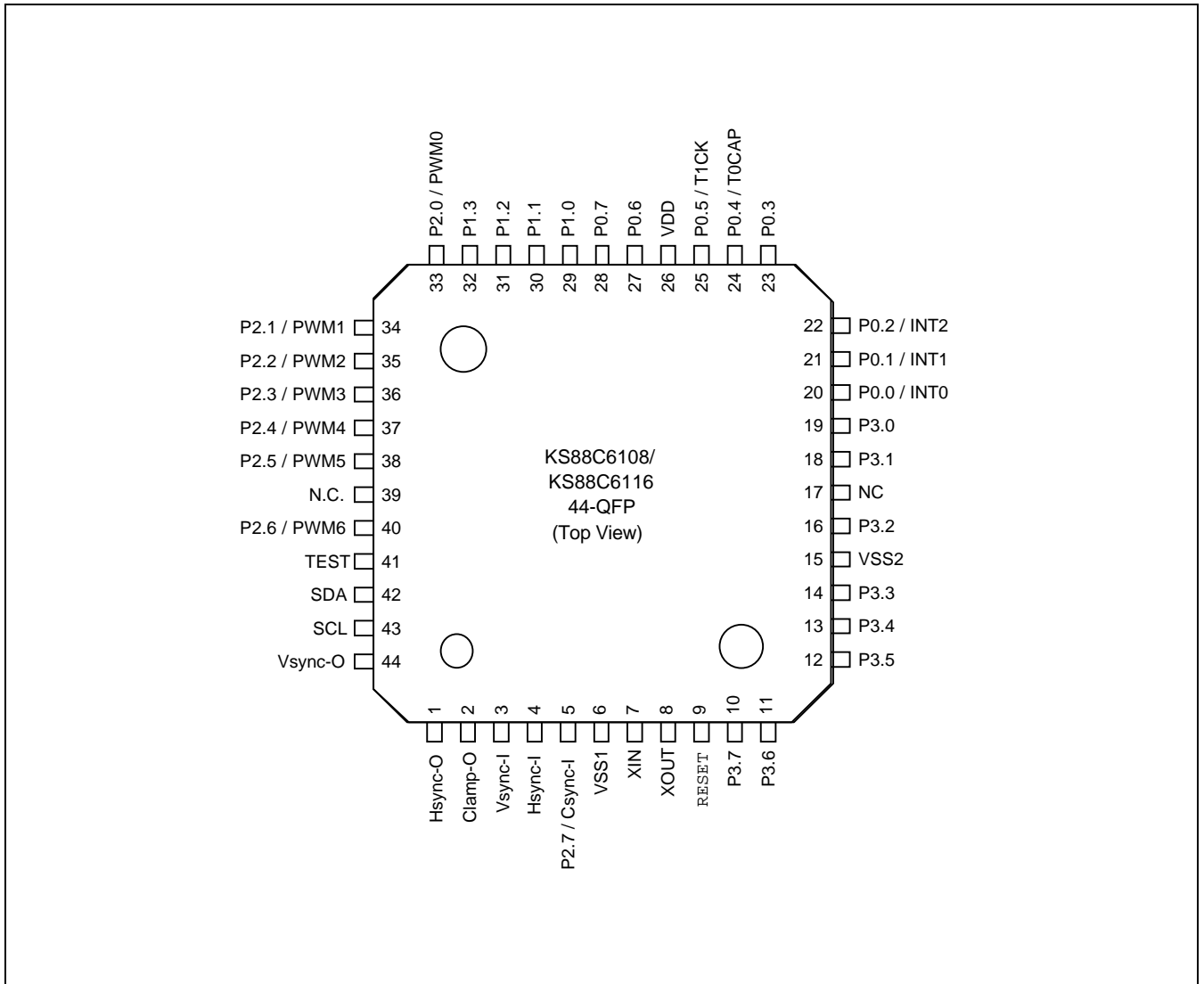
**Figure 1-2. Block Diagram**

**PIN ASSIGNMENTS**



**Figure 1-3. Pin Assignment Diagram (42-SDIP Package)**

**PIN ASSIGNMENTS (Cont.)**



**Figure 1-4. Pin Assignment Diagram (44-QFP Package)**

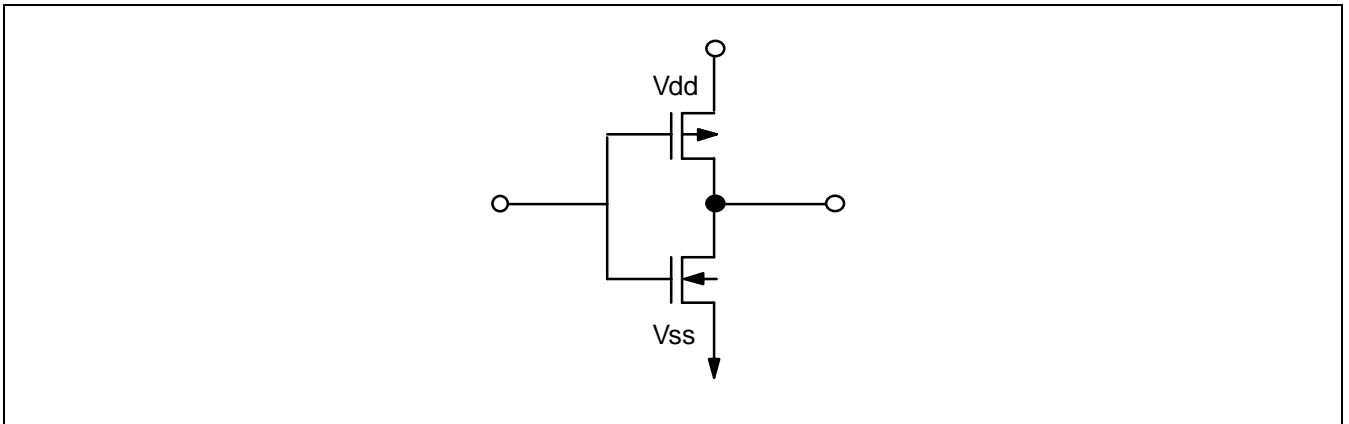
PIN DESCRIPTIONS

Table 1-1. KS88C6108/C6116/P6116 Pin Descriptions

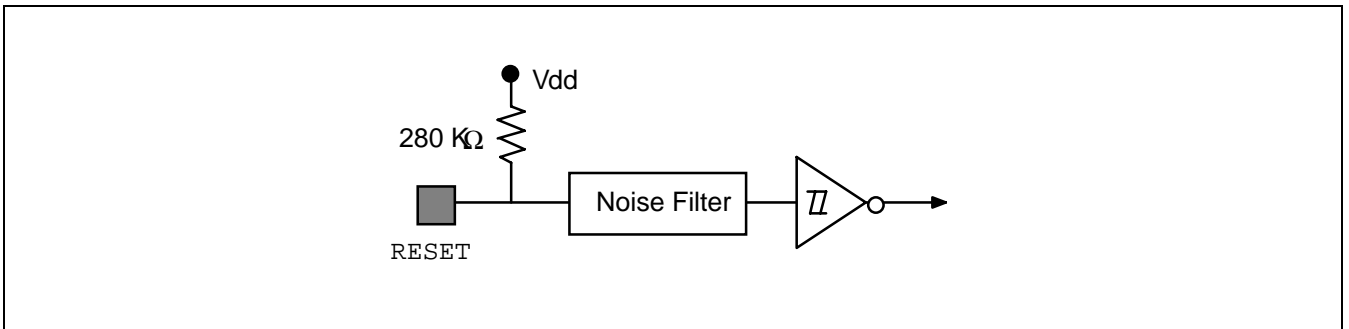
Pin Names	Pin Type	Pin Description	Circuit Type	SDIP Pin Numbers	Shared Functions
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	I/O	General-purpose, 8-bit I/O port. Share functions include three external interrupt inputs, I/O for timers 0 and 1. You can selectively configure port 0 pins to input or output mode.	D-1	3 4 5 6 7 8 10 11	INT0 INT1 INT2  T0CAP T1CK
P1.0–P1.3	I/O	General purpose, 8-bit I/O port. You can selectively configure port 1 pins to input or push-pull output mode.	D-1	12–15	–
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	General purpose, 8-bit I/O port. You can selectively configure port 2 pins to input or output mode. The port 2 pin circuit are designed to push-pull PWM output and Csync signal input.	D-1 D-1 D-1 D-1 E-1 E-1 E-1 D-1	16 17 18 19 20 21 22 31	PWM0 PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 Csync-I
P3.0–P3.7	I/O	General-purpose, 8-bit I/O port. You can selectively configure port 3 pins to input or output mode.	E	2, 1, 42, 40–36	–
Hsync-I Vsync-I Clamp-O Hsync-O Vsync-O SCL SDA	I I O O O I/O I/O	The pins are sync processor signal I/O and IIC-bus clock and data I/O	A A A A A G-3 G-3	30 29 28 27 26 25 24	–
VDD VSS1, VSS2	–	Power supply pins	–	9 32, 41	–
XIN, XOUT	–	System clock input and output pins	–	33, 34	–
RESET	I	System reset pin	B	35	–
TEST	I	Factory test pin input 0 V: normal operation 5 V: factory test mode	–	23	–

**NOTE:** See ‘Pin Circuit Diagrams’ on next two pages for detailed information on circuit types A, B, D-1, E, E-1, and G-3.

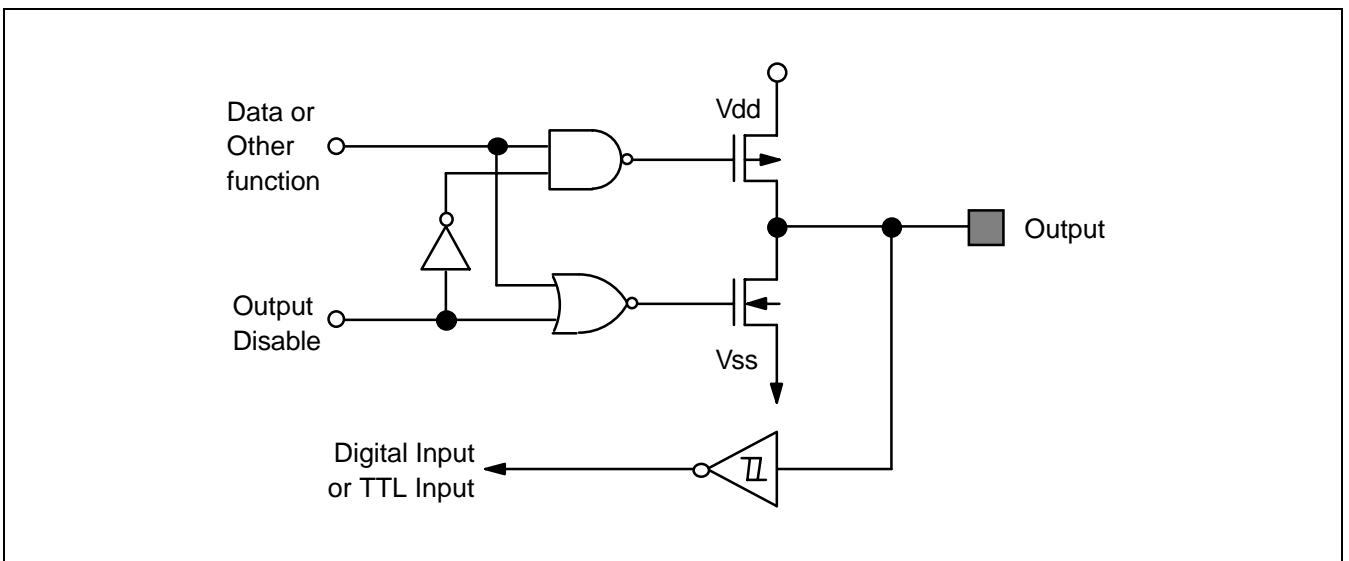
**PIN CIRCUITS**



**Figure 1-5. Pin Circuit Type A**



**Figure 1-6. Pin Circuit Type B (RESET)**



**Figure 1-7. Pin Circuit Type D-1**

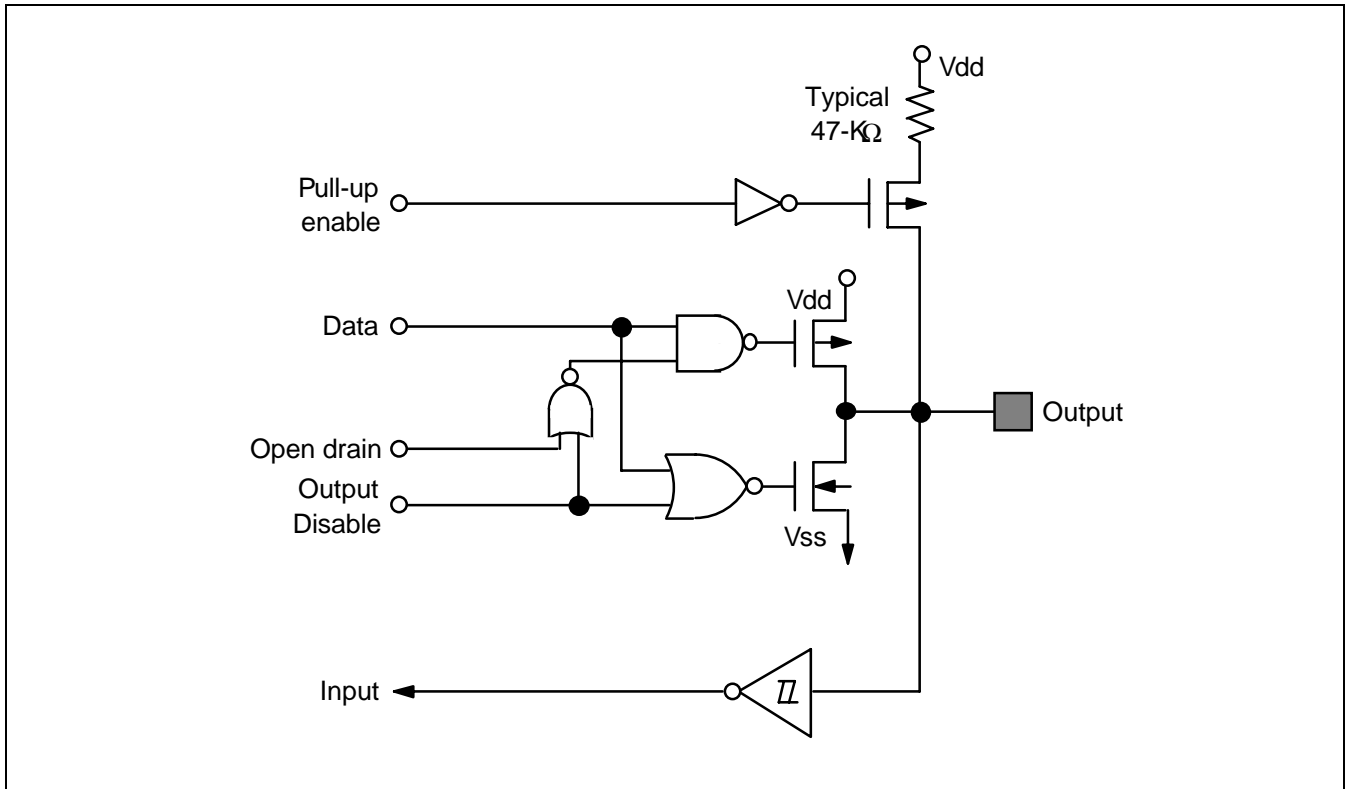


Figure 1-7. Pin Circuit Type E

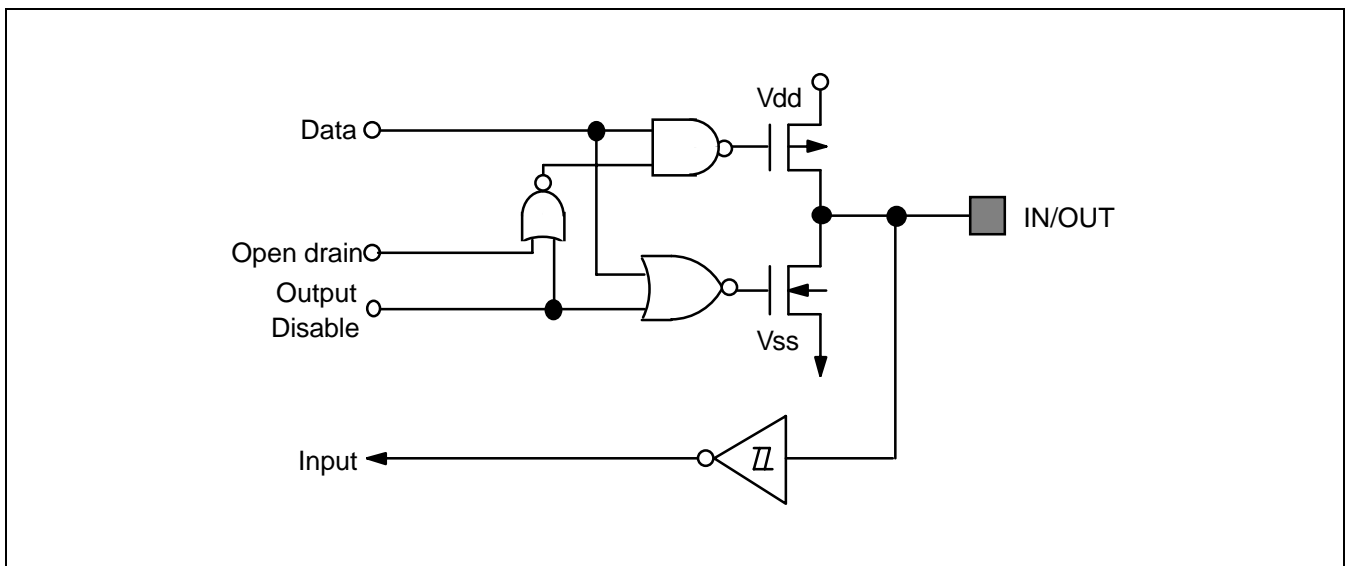


Figure 1-8. Pin Circuit Type E-1



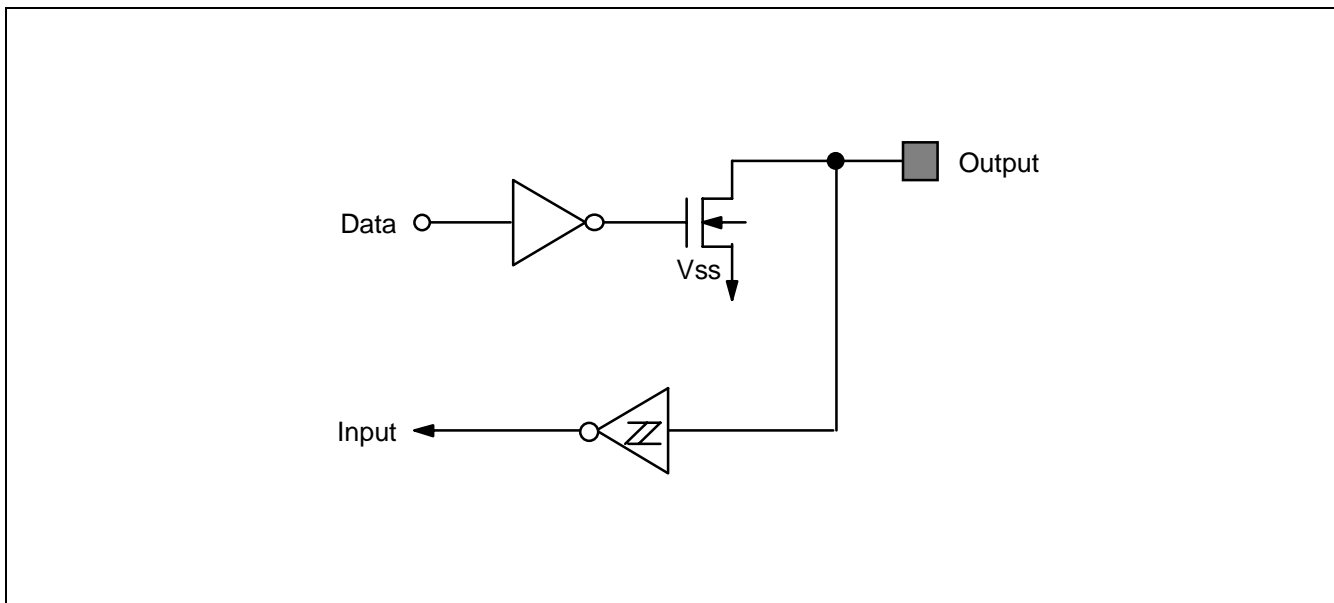


Figure 1-9. Pin Circuit Type G-3

NOTES

# 16

## ELECTRICAL DATA

### OVERVIEW

In this section, KS88C6108/C6116 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- I/O capacitance
- A.C. electrical characteristics
- Oscillation characteristics
- Oscillation stabilization time
- Schmitt trigger characteristics

Table 16-1. Absolute Maximum Ratings

(T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>	–	– 0.3 to + 7.0	V
Input voltage	V <sub>I1</sub>	Type C (n-channel, open-drain)	– 0.3 to + 10	V
	V <sub>I2</sub>	All port pins except V <sub>I1</sub>	– 0.3 to V <sub>DD</sub> + 0.3	
Output voltage	V <sub>O</sub>	All output pins	– 0.3 to V <sub>DD</sub> + 0.3	V
Output current High	I <sub>OH</sub>	One I/O pin active	– 10	mA
		All I/O pins active	– 60	
Output current Low	I <sub>OL1</sub>	One I/O pin active	+ 30	mA
	I <sub>OL2</sub>	Total pin current except port 3	+ 100	
	I <sub>OL3</sub>	Sync-processor I/O pins and IIC-bus clock and data pins	+ 150	
Operating temperature	T <sub>A</sub>	–	– 40 to + 85	°C
Storage temperature	T <sub>STG</sub>	–	– 65 to + 150	°C

Table 16-2. D.C. Electrical Characteristics

(T<sub>A</sub> = – 40°C to + 85°C, V<sub>DD</sub> = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High voltage	V <sub>IH1</sub>	All input pins except V <sub>IH2</sub> and V <sub>IH3</sub>	0.8 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	X <sub>IN</sub> , X <sub>OUT</sub>	V <sub>DD</sub> – 0.5		V <sub>DD</sub>	
	V <sub>IH3</sub>	TTL input (Hsyncl, Vsyncl and Csyncl)	2.0		V <sub>DD</sub>	
Input Low voltage	V <sub>IL1</sub>	All input pins except V <sub>IL2</sub> and V <sub>IL3</sub>	–	–	0.2 V <sub>DD</sub>	V
	V <sub>IL2</sub>	X <sub>IN</sub> , X <sub>OUT</sub>			0.4	
	V <sub>IL3</sub>	TTL input (Hsyncl, Vsyncl and Csyncl)			0.8	
Output High voltage	V <sub>OH1</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OH</sub> = – 8 mA Port 1 only	V <sub>DD</sub> – 1.0	–	–	V
	V <sub>OH2</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OH</sub> = – 2 mA Ports 0, 2, ClampO, H and VsyncO	V <sub>DD</sub> – 1.0			
	V <sub>OH3</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OH</sub> = – 6 mA, Port 3	V <sub>DD</sub> – 1.0			

Table 16-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low voltage	V <sub>OL1</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OL</sub> = 8 mA, port 1 only	-	-	0.4	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 2 mA Port 0, 2, ClampO, HsyncO and VsyncO			0.4	
	V <sub>OL3</sub>	I <sub>OL</sub> = 6 mA Port 3, SCL and SDA			0.4	
Input High leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> All input pins except X <sub>in</sub> , X <sub>out</sub>	-	-	3	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> X <sub>OUT</sub> only	-	-	20	
	I <sub>LIH3</sub>	V <sub>IN</sub> = V <sub>DD</sub> X <sub>IN</sub> only	2.5	6	20	
Input Low leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V All input pins except X <sub>in</sub> , X <sub>out</sub> and RESET	-	-	-3	μA
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V; X <sub>OUT</sub> only	-	-	-20	
	I <sub>LIL3</sub>	V <sub>IN</sub> = 0 V; X <sub>IN</sub> only	-2.5	-6	-20	
Output High leakage current	I <sub>LOHL</sub>	V <sub>OUT</sub> = V <sub>DD</sub> All output pins except port 1	-	-	3	μA
Output Low leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V	-	-	-3	μA
Pull-up resistor	R <sub>L1</sub>	V <sub>IN</sub> = 0 V; V <sub>DD</sub> = 4.5 V to 5.5 V Port 3	20	47	80	kΩ
	R <sub>L2</sub>	V <sub>IN</sub> = 0 V; V <sub>DD</sub> = 4.5 V to 5.5 V RESET only	150	280	480	
Supply current (NOTE)	I <sub>DD1</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V 12 MHz CPU clock	-	15	30	mA
	I <sub>DD2</sub>	Idle mode; V <sub>DD</sub> = 4.5 V to 5.5 V 12 MHz CPU clock		5	10	
	I <sub>DD3</sub>	Stop mode; V <sub>DD</sub> = 5.0 V		1	10	μA

**NOTE:** Supply current does not include drawn internal pull-up resistors and external loads of output.

Table 16-3. Data Retention Supply Voltage in Stop Mode

(T<sub>A</sub> = -40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDDR</sub>	Stop mode	2	–	6	V
Data retention supply current	I <sub>DDDR</sub>	Stop mode, V <sub>DDDR</sub> = 2.0 V	–	–	5	μA

**NOTES:**

1. During the oscillator stabilization wait time (t<sub>WAIT</sub>), all CPU operations must be stopped.
2. Supply current does not include drawn through internal pull-up resistors and external output current loads.

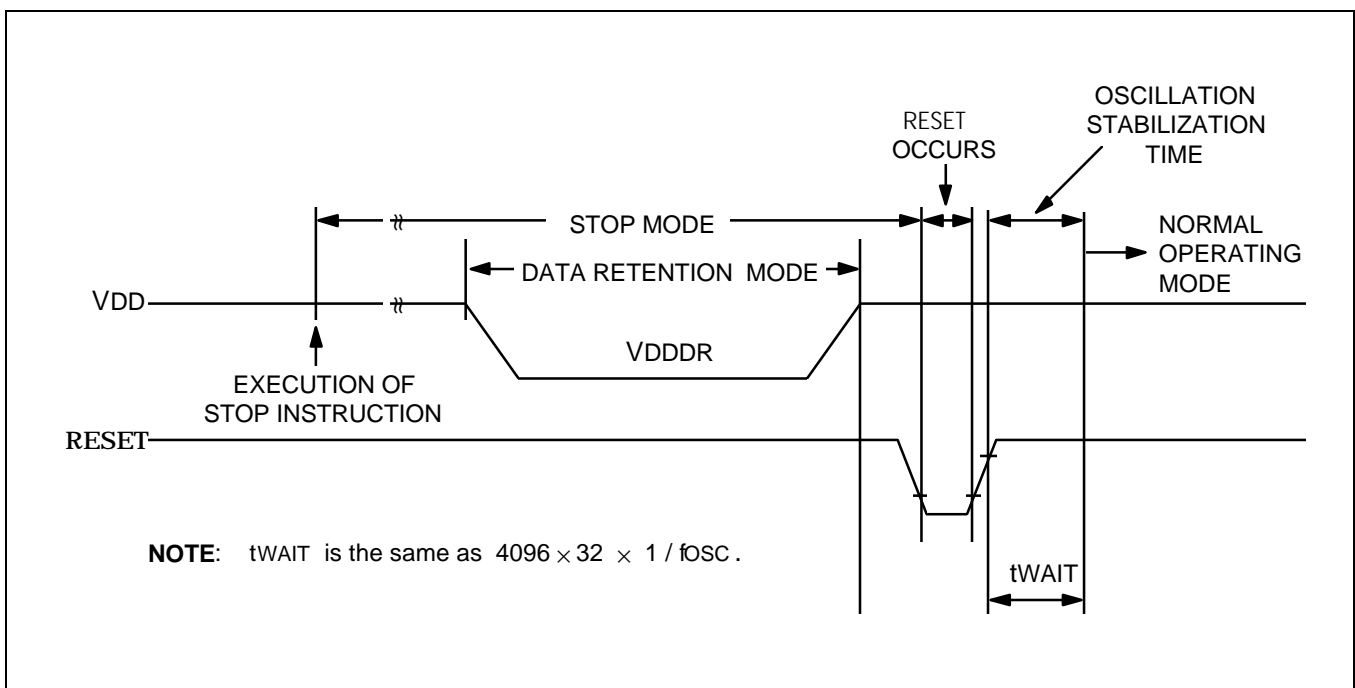


Figure 16-1. Stop Mode Release Timing When Initiated by a Reset

Table 16-4. Input/Output Capacitance

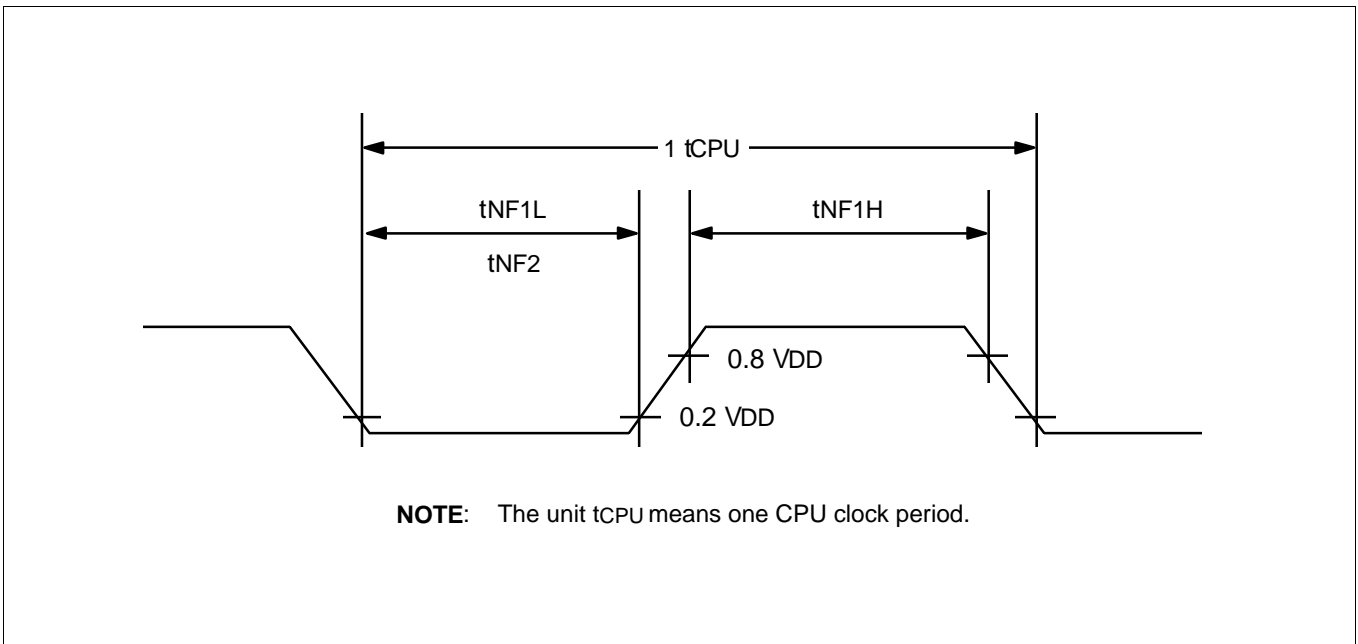
(T<sub>A</sub> = -40°C to + 85°C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz; unmeasured pins are connected to V <sub>SS</sub>	–	–	10	pF
Output capacitance	C <sub>OUT</sub>					
I/O capacitance	C <sub>IO</sub>					

**Table 16-5. A.C. Electrical Characteristics**

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Filter	$t_{NF1H}$ , $t_{NF1L}$	P0.2–P0.0, T0CAP and T1CK (RC delay)	300	–	–	ns
	$t_{NF2}$	RESET only (RC delay)	800	–	–	



**Figure 16-2. Input Timing Measurement Points for P0.0–P0.2, T0CAP and T1CK**

**Table 16-6. Oscillation Characteristics**

( $T_A = -40^\circ\text{C} + 85^\circ\text{C}$ )

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Main crystal or ceramic		$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	6	–	12	MHz
External clock (main)		$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	6	–	12	MHz

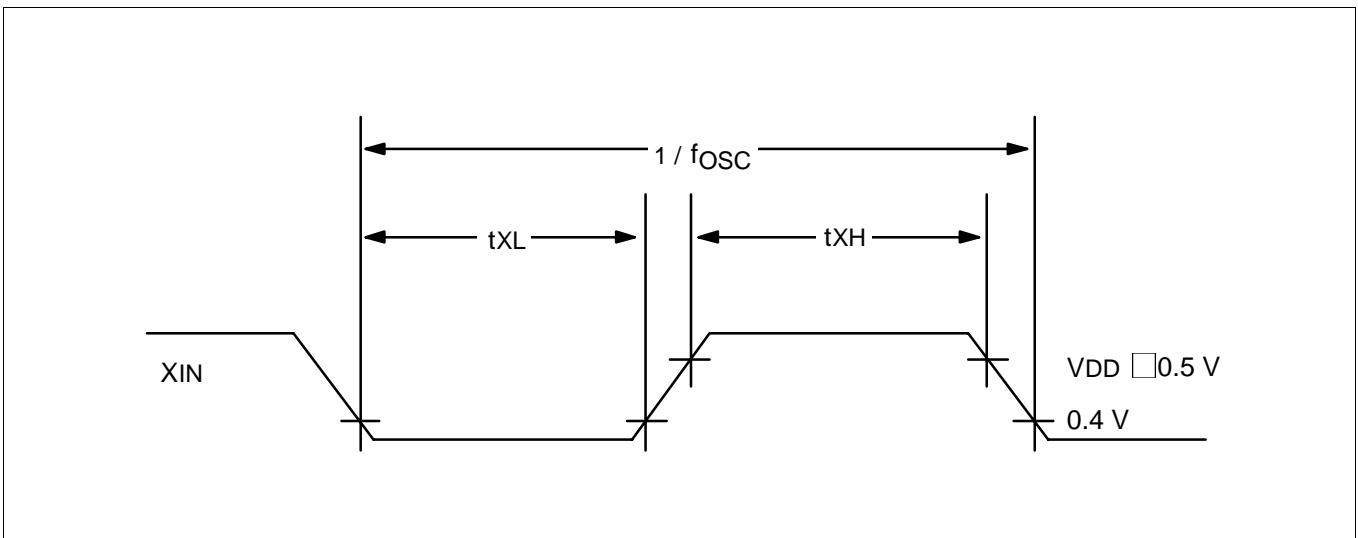
**NOTE:** The maximum oscillator frequency is 12 MHz. If you use an oscillator frequency higher than 12 MHz, you cannot select a non-divided CPU clock using CLKCON settings. That is, you must select one of the divide-by values.

**Table 16-7. Oscillation Stabilization Time**

( $T_A = -40^\circ\text{C} + 85^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V to } 5.5\text{ V}$ )

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	–	–	20	ms
Ceramic	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	–	–	10	
External clock	$X_{IN}$ input High and Low level width ( $t_{XH}$ , $t_{XL}$ )	25	–	500	ns

**NOTE:** Oscillation stabilization time is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released.



**Figure 16-3. Clock Timing Measurement Points for  $X_{IN}$**



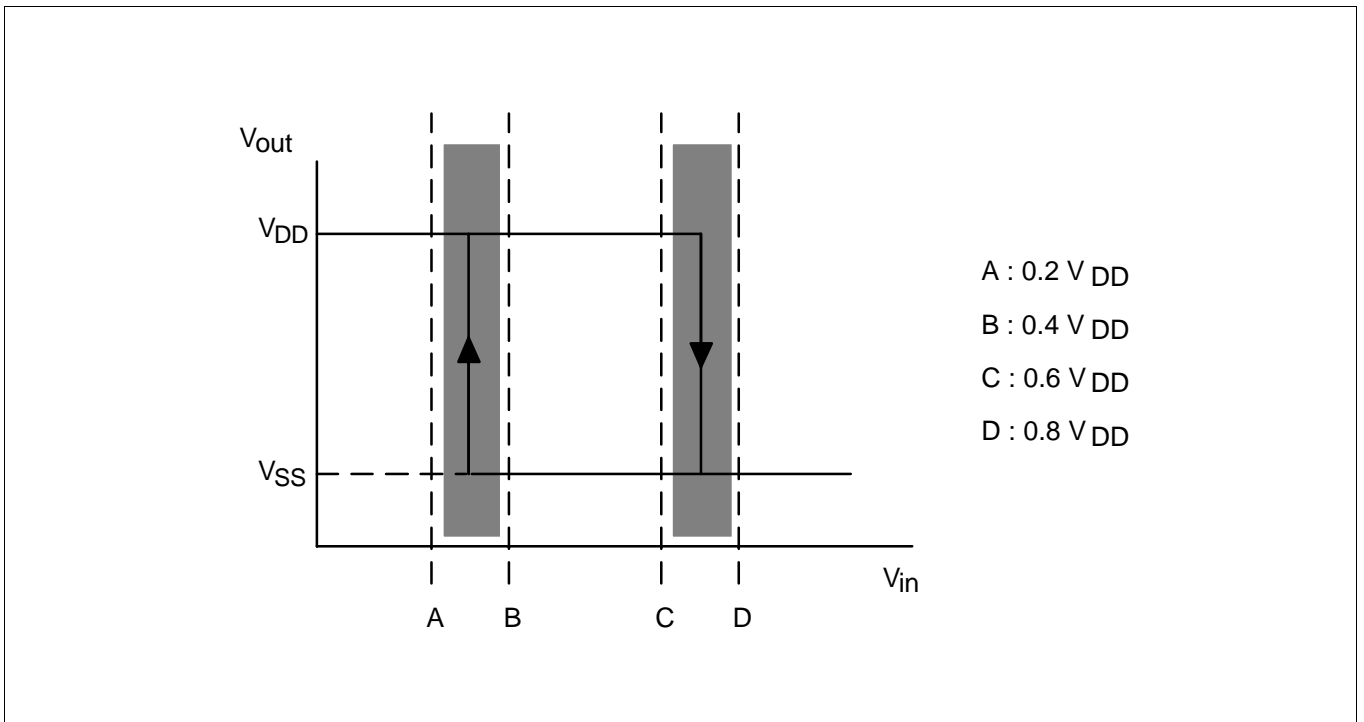


Figure 16-4. Schmitt Trigger Characteristics (Normal Port; except TTL Input)

NOTES

# 17 MECHANICAL DATA

## OVERVIEW

The KS88C6116 microcontroller is available in a 42-pin SDIP package (Samsung part number 42-SDIP-600) and a 44-QFP package (Samsung part number 44-QFP-1010B).

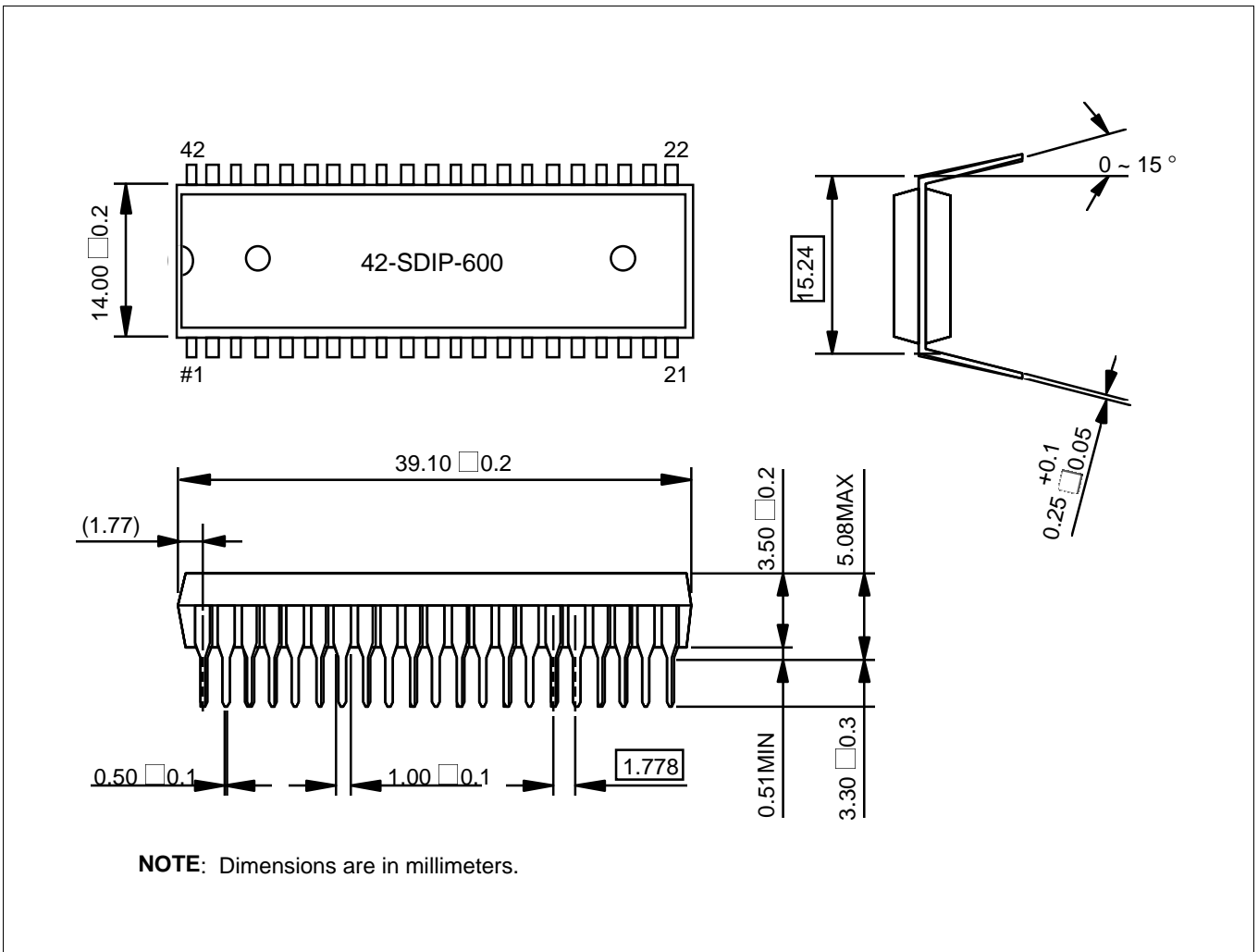
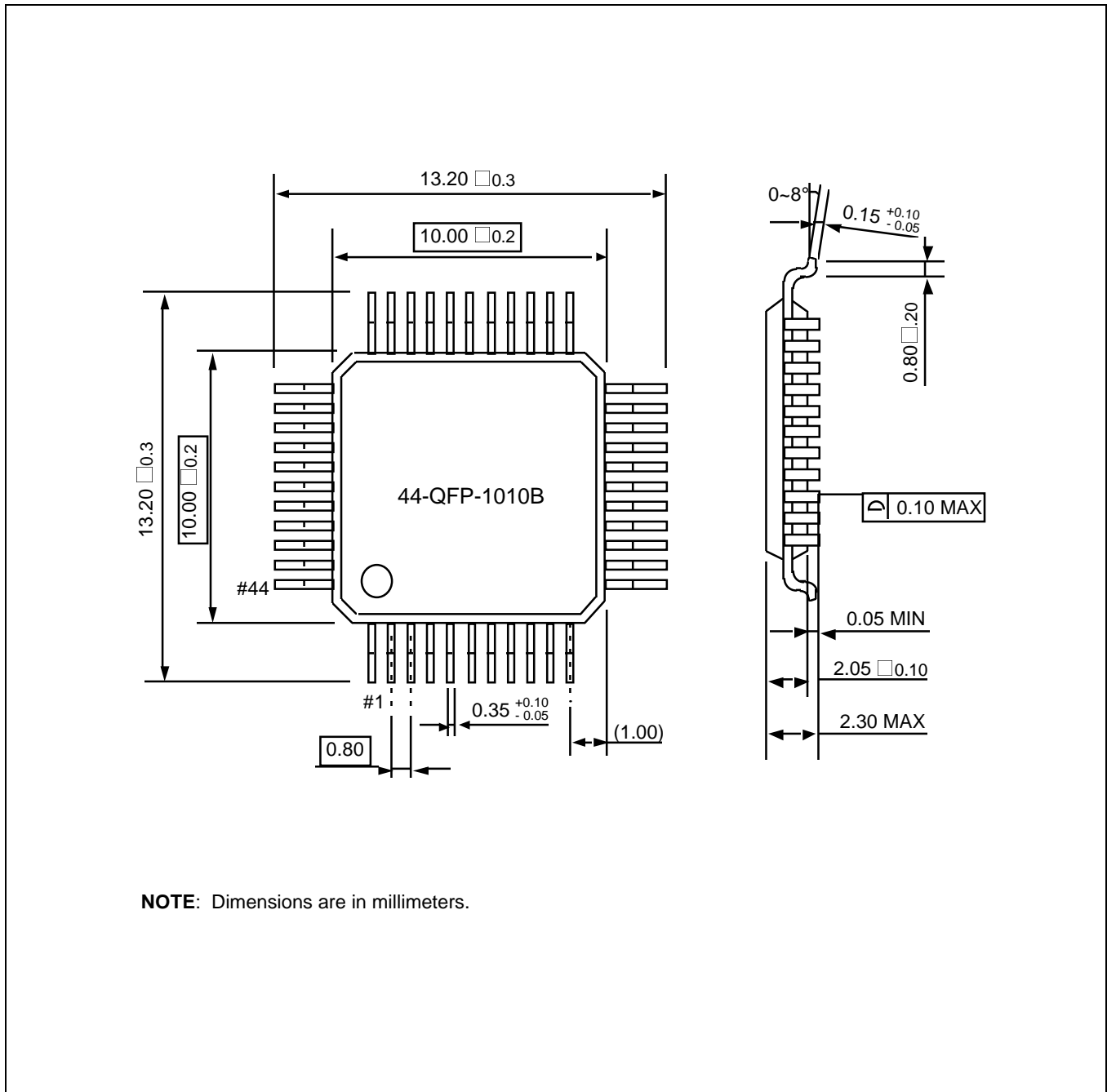


Figure 17-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)



NOTE: Dimensions are in millimeters.

Figure 17-2. 44-Pin QFP Package Mechanical Data (44-QFP-1010B)

# 18

## KS88P6116 OTP

### OVERVIEW

The KS88P6116 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS88C6108/C6116 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS88P6116 is fully compatible with the KS88C6108/C6116, both in function and in pin configuration. Because of its simple programming requirements, the KS88P6116 is ideal for use as an evaluation chip for the KS88C6108/C6116.

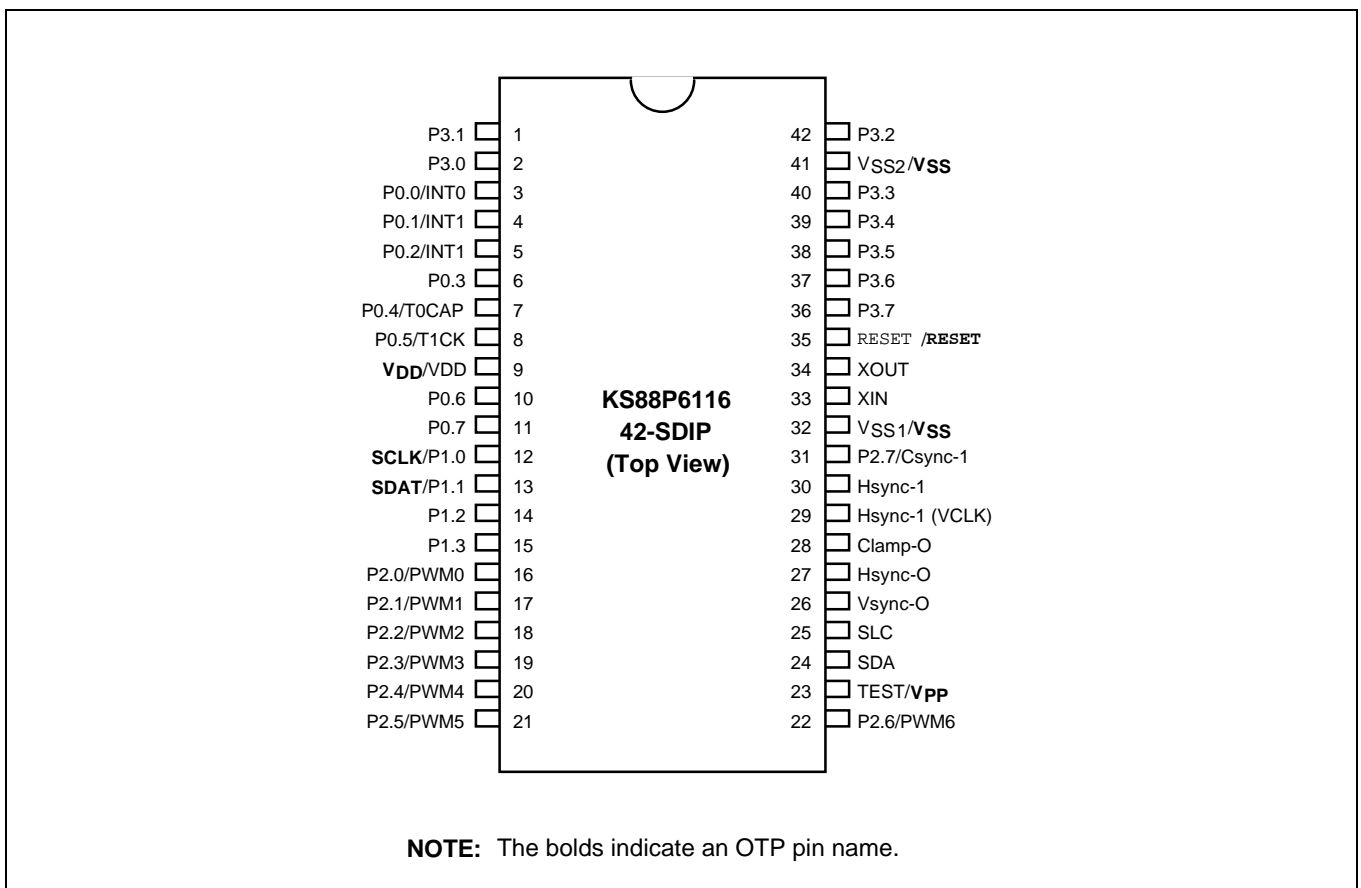


Figure 18-1. KS88P6116 Pin Assignments (42-SDIP Package)

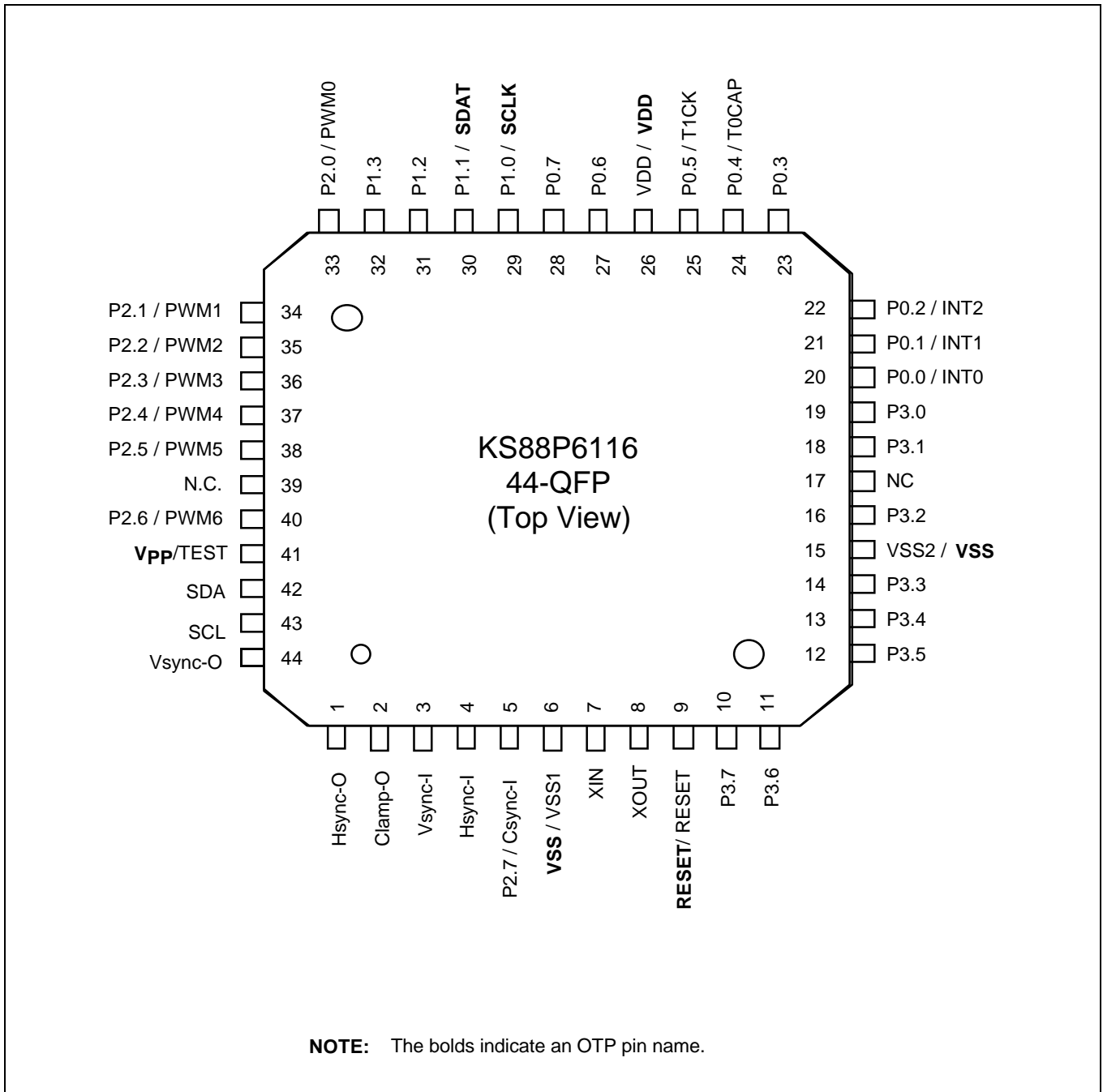


Figure 18-2. KS88P6116 Pin Assignments (44-QFP Package)

Table 18-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P1.1	SDAT	13 (*30)	I/O	Serial DATa Pin (Output when reading, Input when writing) Input & Push-pull Output Port can be assigned
P1.0	SCLK	12 (*29)	I	Serial CLock Pin (Input Only Pin)
TEST	V <sub>PP</sub> (TEST)	23 (*41)	I	EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5V is applied and when reading 5V is applied.(Option)
RESET	RESET	35 (*9)	I	Chip Initialization
V <sub>DD</sub> / V <sub>SS1</sub> / V <sub>SS2</sub>	V <sub>DD</sub> / V <sub>SS</sub> / V <sub>SS</sub>	9 / 32 / 41 (*26 / 6 / 15)	I	Logic Power Supply Pin. V <sub>DD</sub> should be tied to 5V during programming.

**NOTE:** \* means the 44-QFP OTP pin number.

Table 18-2. Comparison of KS88P6116 and KS88C6108/C6116 Features

Characteristic	KS88P6116	KS88C6108/C6116
Program Memory	16 K byte EPROM	16 K byte mask ROM
Operating Voltage (V <sub>DD</sub> )	4.5 V to 5.5 V	4.5 V to 5.5V
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST)=12.5V	
Pin Configuration	42SDIP, 44QFP	42SDIP, 44QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub>(TEST) pin of the KS88P6116, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 18-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>PP</sub> (TEST)	REG/MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

**NOTE:** "0" means Low level; "1" means High level.

## D.C. ELECTRICAL CHARACTERISTICS

Table 18-4. D.C. Electrical Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High leakage current	$I_{LIH1}$	$V_{IN} = V_{DD}$ ; All input pins except $X_{in}$ , $X_{out}$	–	–	3	$\mu\text{A}$
	$I_{LIH2}$	$V_{IN} = V_{DD}$ ; $X_{OUT}$ only			20	
	$I_{LIH3}$	$V_{IN} = V_{DD}$ ; $X_{IN}$ only	2.5	6	20	
Input Low leakage current	$I_{LIL1}$	$V_{IN} = 0\text{ V}$ ; All input pins except $X_{in}$ , $X_{out}$ and RESET	–	–	–3	$\mu\text{A}$
	$I_{LIL2}$	$V_{IN} = 0\text{ V}$ ; $X_{OUT}$ only	–	–	–20	
	$I_{LIL3}$	$V_{IN} = 0\text{ V}$ ; $X_{IN}$ only	–2.5	–6	–20	
Output High leakage current	$I_{LOH1}$	$V_{OUT} = V_{DD}$	–	–	3	$\mu\text{A}$
Output Low leakage current	$I_{LOL1}$	$V_{OUT} = 0\text{ V}$	–	–	–3	$\mu\text{A}$
Supply current	$I_{DD1}$	Normal operating mode; 12 MHz CPU clock	–	15	30	mA
	$I_{DD2}$	IDLE mode; 12 MHz CPU clock		5	10	
	$I_{DD3}$	Stop mode; $V_{DD} = 5.0\text{ V}$	–	1	10	$\mu\text{A}$
Data retention supply voltage	VDDDR	Stop mode	2	–	6	V
Data retention supply voltage	IDDDR	Stop mode; VDDDR = 2V	–	–	5	$\mu\text{A}$



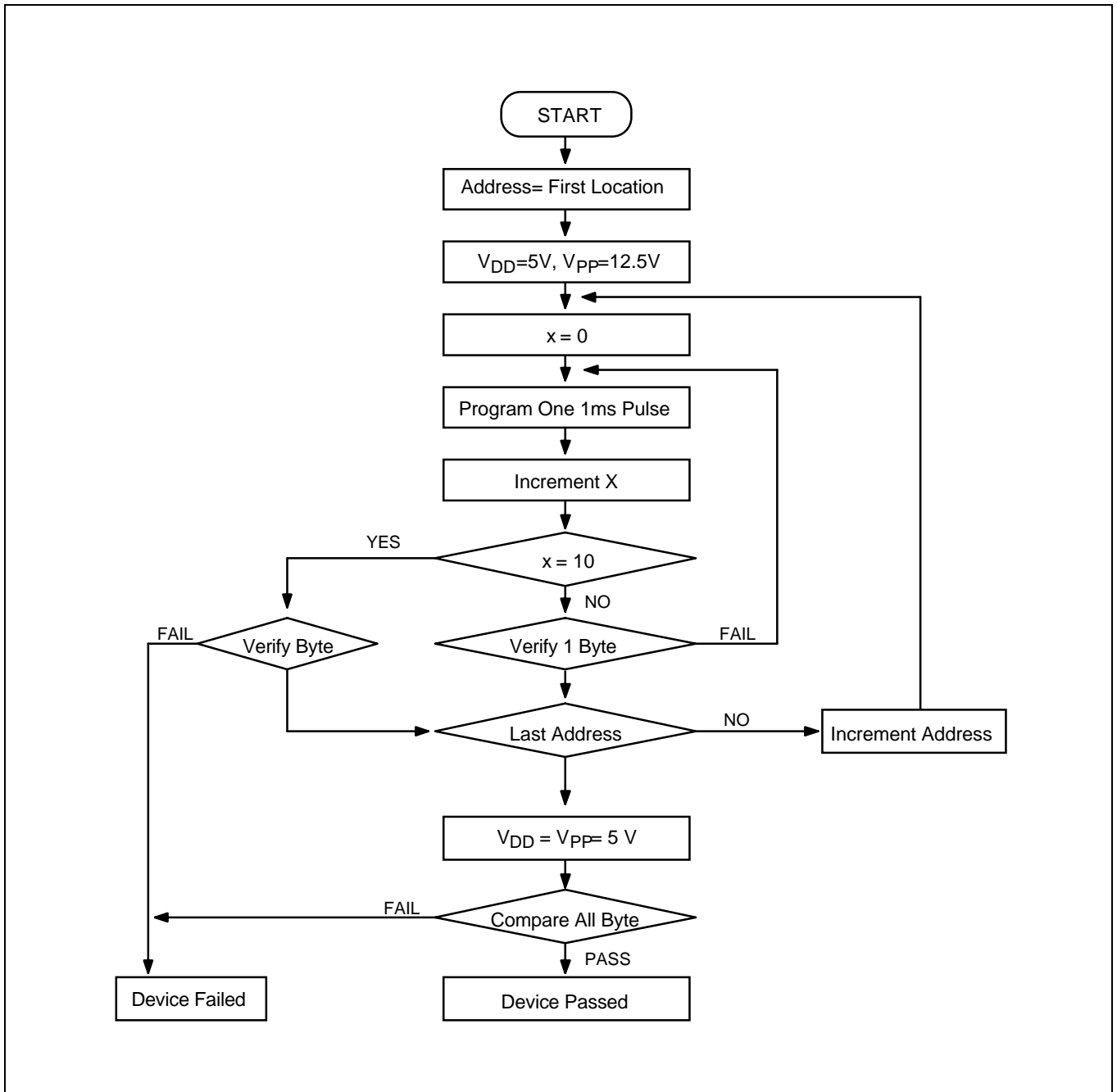


Figure 18-3. OTP Programming Algorithm

**NOTE**