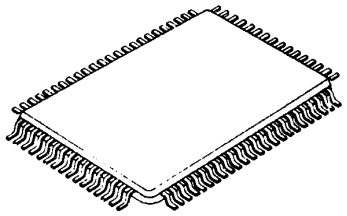
KS0118C GENLOCK ADC

INTRODUCTION

The KS0118C is a CMOS integrated circuit designed for the GEN LOCK and ND Conversion.
It is a Monolithic IC that enabled an analog NTSC composite video signal to digitize at a clock rate that is synchronized and locked to the incoming video horizontal line frequency.
It includes clamping function, 8-bit digitizing and creation of a line locked sampling clock.
It is possible to correspond to the video signal system of LDP by the use of KA9413, KA 9414-D ICS together, which is designed for the Digital Video Signal Processor.

80-QFP-1420C



ORDERING IN FORMATION

Device	Package	Operating Temperature
KS0118C	80-QFP-1420C	-20℃~+75℃

FEATURES

- NTSC Video Signal Input
- Line-locked Sync and Clock Generation
- Line to Line Jitter < 20 nsec
- Differential Gain 2% Differential Phase 2^{O}
- Programmable Sample Clock Frequency from 25 to 30 MHz
- Built-in 8 Bit CMOS Analog to Digital Converter
- Programmable Gain Control and Automatic DC Offset Control for Video Signal Input
- Programmable PLL Time Constants for Tracking Different Input Types
- Correctly Tracks Line Drop-outs
- Provides a Microprocessor 3 Wire Serial Interface
- Built-in Decimation Filter
  Single Power Supply: +5V

BLOCK DIAGRAM

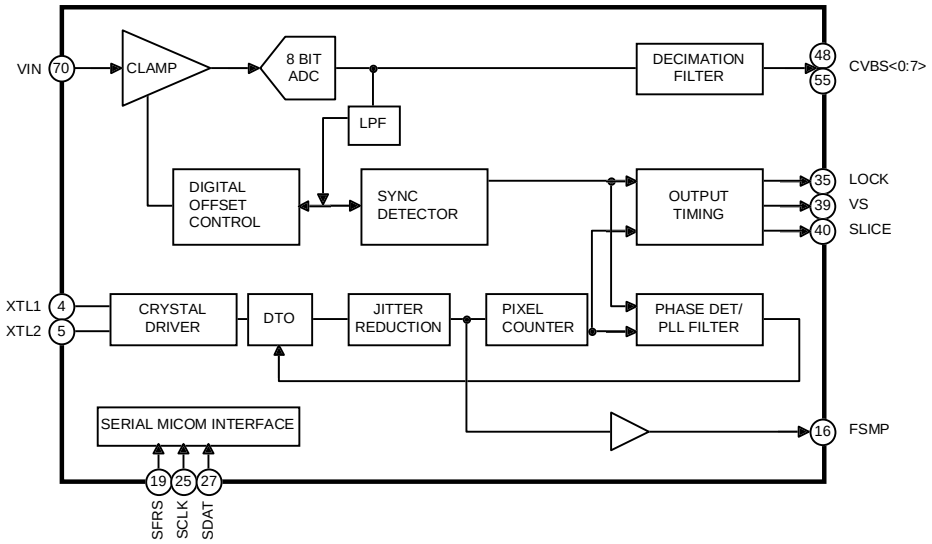


Fig. 1

PIN CONFIGURATION

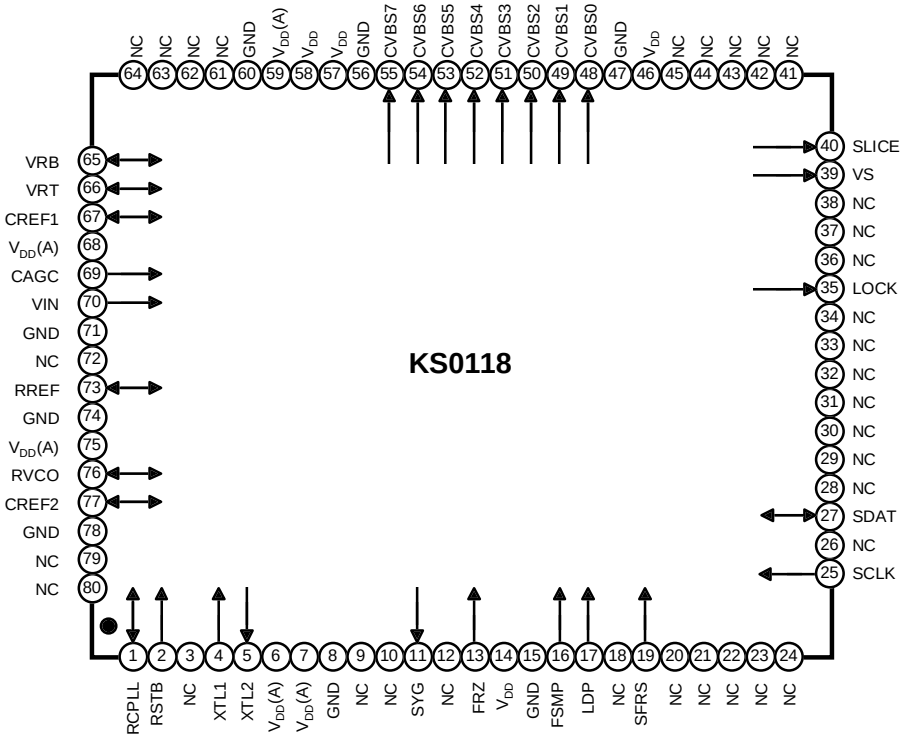


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	RCPLL	I/O	External Filter Pin for Analog PLL
2	RSTB	I	System Reset Signal Input (Active Low)
3	NC	-	No Connection
4	XTL1	I	Pin1 for External Crystal Oscillator
5	XTL2	O	Pin2 for External Crystal Oscillator
6	V_{DD}(A)	-	+ 5V Supply Voltage for Analog Domain
7	V_{DD}(A)	-	+ 5V Supply Voltage for Analog Domain
8	GND	-	Ground
9	NC	-	No Connection
10	NC	-	No Connection
11	SYG	O	Line Locked Horizontal Sync Signal
12	NC	-	No Connection
13	FRZ	I	Connect this Pin to + 5V for proper Operation
14	V_{DD}	-	+ 5V Supply Voltage for Digital Domain
15	GND	-	Ground
16	FSMP	O	Freq. & Phase compensated Sample Clock used for ADC
17	LDP	I	Connect this Pin to + 5V for proper Operation
18	NC	-	No Connection
19	SFRS	I	Frame Signal for Serial Data Interface
20	NC	-	No Connection
21	NC	-	No Connection
22	NC	-	No Connection
23	NC	-	No Connection
24	NC	-	No Connection
25	SCLK	I	Clock Signal Input for Serial Data Interface
26	NC	-	No Connection
27	SDAT	I/O	Serial Data in Serial Interface
28	NC	-	No Connection
29	NC	-	No Connection
30	NC	-	No Connection
31	NC	-	No Connection
32	NC	-	No Connection
33	NC	-	No Connection
34	NC	-	No Connection
35	LOCK	O	High when the GENLOCK is locked & in Tracking State
36	NC	-	No Connection
37	NC	-	No Connection
38	NC	-	No Connection
39	VS	O	Vertical Sync Signal Output
40	SLICE	O	Sync level. Low when CVBS < 32. This Signal is not Line locked

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
41	NC	-	No Connection
42	NC	-	No Connection
43	NC	-	No Connection
44	NC	-	No Connection
45	NC	-	No Connection
46	V_{DD}	-	+ 5V Supply Voltage for Digital Domain
47	GND	-	Ground
48	CVBS0	O	8 Bit Composite Video Baseband Signal
49	CVBS1	O	8 Bit Composite Video Baseband Signal
50	CVBS2	O	8 Bit Composite Video Baseband Signal
51	CVBS3	O	8 Bit Composite Video Baseband Signal
52	CVBS4	O	8 Bit Composite Video Baseband Signal
53	CVBS5	O	8 Bit Composite Video Baseband Signal
54	CVBS6	O	8 Bit Composite Video Baseband Signal
55	CVBS7	O	8 Bit Composite Video Baseband Signal
56	GND	-	Ground
57	V_{DD}	-	+ 5V Supply Voltage for Digital Domain
58	V_{DD}	-	+ 5V Supply Voltage for Digital Domain
59	V_{DD}(A)	-	+ 5V Supply Voltage for Digital Domain
60	GND	-	Ground
61	NC	-	No Connection
62	NC	-	No Connection
63	NC	-	No Connection
64	NC	-	No Connection
65	VRB	I/O	Bottom Voltage Reference for ADC
66	VRT	I/O	Top Voltage Reference for ADC
67	CREF1	I/O	Decoupling Pin for Reference Voltage
68	V_{DD}(A)	-	+5V Supply Voltage for Analog Domain
69	CAGC	I	Capacitor for Offset Control
70	VIN	I	Analog NTSC Video Signal Input (1Vpp)
71	GND	-	Ground
72	NC	-	No Connection
73	RREF	I/O	Current Setting Pin for Internal Analog Circuitry
74	GND	-	Ground
75	V_{DD}(A)	-	+ 5V Supply Voltage for Analog Domain
76	RVCO	I/O	Current Setting Pin for Analog VCO
77	CREF2	I/O	Decoupling Pin for Reference Voltage
78	GND	-	Ground
79	NC	-	No Connection
80	NC	-	No Connection

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 ~+7.0	V
Voltage on any Digital Pin	V_{PIN}	GND ~ V_{DD}	V
Operating Temperature	T_{OPR}	- 20 ~ + 75	℃
Storage Temperature	T_{STG}	-55 ~ +125	℃

ELECTRICAL CHARACTERISTICS

(Ta = 25℃, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Input High Voltage	V_{IH}	V_{DD} = 4.75V	4.0	-	-	V
Digital Input Low Voltage	V_{IL}	V_{DD} = 5.25V	-	-	1.0	V
Digital Output High Voltage	V_{OH}	V_{DD} = 4.75V	4.0	-	-	V
Digital Output Low Voltage	V_{OL}	V_{DD} = 5.25V	-	-	1.0	mA
Static Power Current	I_{CCS}	V_{DD} = 5.25V	34	74	94	mA
Dynamic Power Current	I_{CCD}	V_{DD} = 5.25V	140	-	200	mA
Serial uP I/O Set-up Time	t_{US}	XTL = 24.576MHz	-	-	10	ns
Serial uP I/O Hold Time	t_{UH}	XTL = 24.576MHz	-	-	10	ns
Differential Phase	DP	-	-	2.0	-	deg
Differential Gain	DG	-	-	2.0	-	%
Signal to Noise Ratio	SNR	-	35	-	-	dB
uP Maximum Data Rate	f_{MPU}	V_{DD} = 4.75V	5.0	-	-	MHz
Frequency Lock Range	FLT	XTL = 24.576MHz	28.60	-	28.66	MHz

TEST CIRCUIT

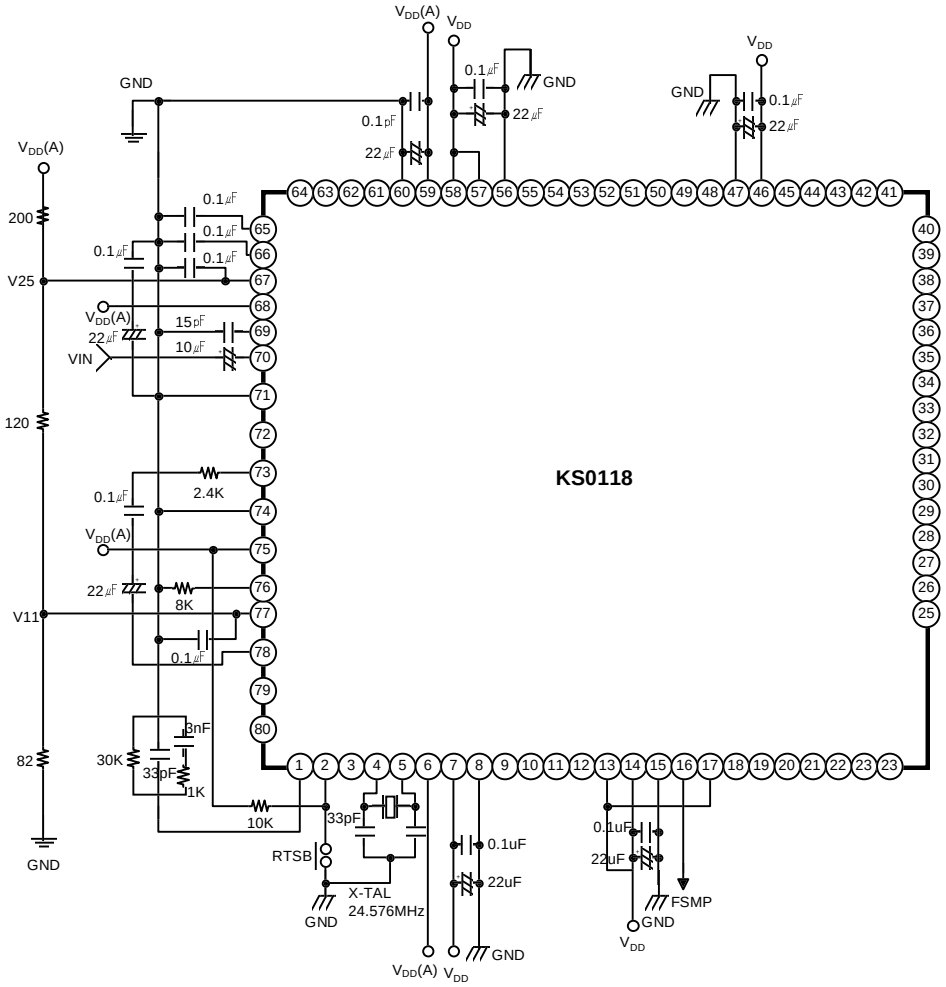


Fig. 3.

APPLICATION INFORMATION
FUNCTION DESCRIPTION

1. GENERAL DESCRIPTION
The KS0118C implements the funtions of an 8 Bit ADC, Analog Clamp, Analog PLL Clock Generator and Digital Timing Generation. Throuth the use of VLSl technology, the KS0118C combines analog circuits with digital signal processing to obtain locking characteristics not achievable by ordinary methods.
The KS0118C uses 1 external frequency reference to create many different programmable line lock sampling clocks.

2. ANALOG TO DIGITAL CONVERTER
The KS0118C uses a two step, 8 bit and auto zero ADC to digitize the analog video input.
The VRT and VRB pins are the top and bottom reference voltage for the ADC.
These references are generated internally but required 0.1μF decoupling capacitors to ground.

3. EXTERNAL FREQUENCY REFERENCE
The KS0118C requires an external stable frequency reference to generate the sampling clock. Although a wide range of frequency will work with the GENLOCK, it is recommended that 24.576MHz be used as the reference.
This can be derived from a standard crystal or an external clock.

4. ANALOG PHASE LOCK LOOP
The KS0118C has an internal PLL used for producing the sampling clock. This PLL requires an external loop filter at pin 1 (RCPLL) as shown in the application circuit.
The ground connections for this filter should be placed close to pin 78, while the inputs should be located close to pin 1.
The PLL also requires an external resistor to converter the voltage of the RCPLL node to a current for use by the internal VCO.
The voltage of the pin 76 (RVCO) will track RCPLL Although the absolute voltage of these pins depends on many factors, it will be between 0.75 and 4.50 voltalge.
The voltage will exhibit the standard characteristics of an analog PLL.

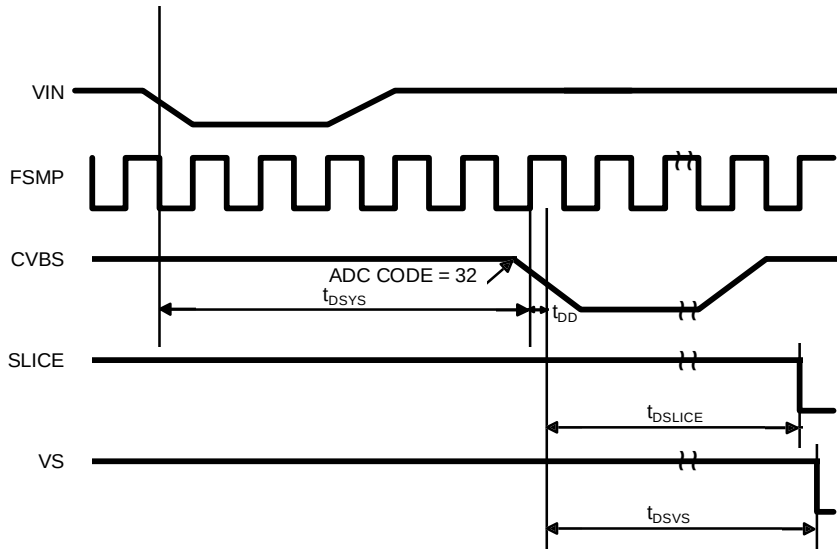


Fig. 4 Data Path Propagation Delay and Key Timing Signals

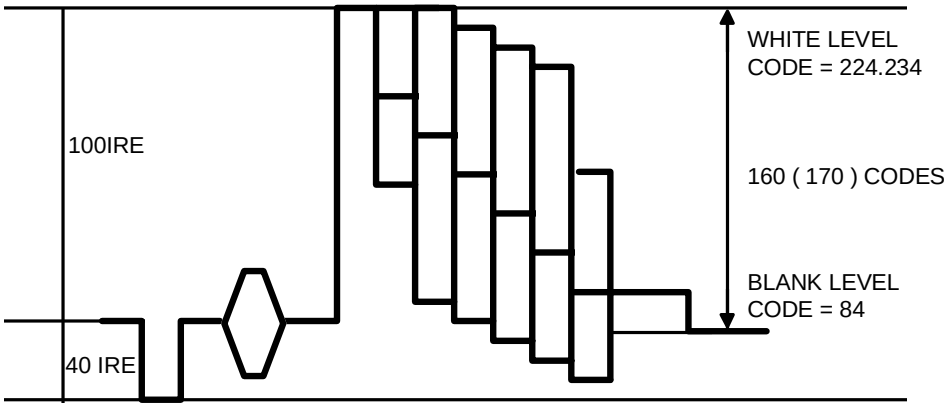


Fig. 5 Digitized Code Levels

APPLICATION CIRCUIT