

4M x 4Bit CMOS Quad $\overline{\text{CAS}}$ DRAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 4 bit Quad $\overline{\text{CAS}}$ with Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Refresh cycle (2K Ref. or 4K Ref.), access time (-5 or -6), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

This 4Mx4 Extended Data Out Quad $\overline{\text{CAS}}$ DRAM family is fabricated using Samsung's advanced CMOS process to realize high bandwidth, low power consumption and high reliability.

FEATURES

• Part Identification

- KM44C4005C/C-L (5V, 4K Ref.)
- KM44C4105C/C-L (5V, 2K Ref.)

• Active Power Dissipation

Unit : mW

| Speed | Refresh Cycle | |
|-------|---------------|-----|
| | 4K | 2K |
| -5 | 495 | 605 |
| -6 | 440 | 550 |

- Extended Data Out mode operation (Fast Page Mode with Extended Data Out)
- Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V \pm 10% power supply

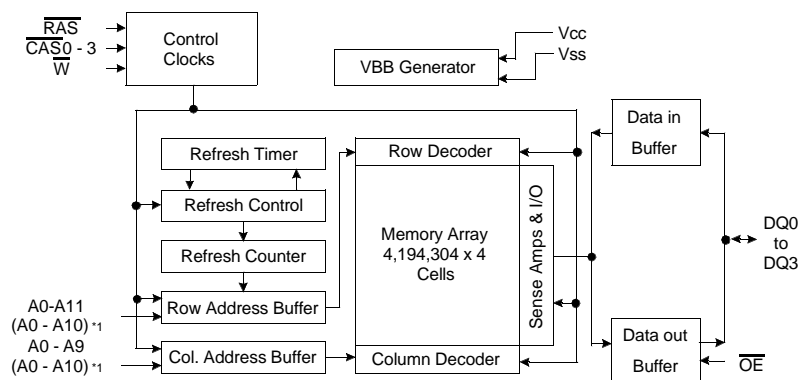
• Refresh Cycles

| Part NO. | Refresh cycle | Refresh period | |
|----------|---------------|----------------|-------|
| | | Normal | L-ver |
| C4005C | 4K | 64ms | 128ms |
| C4105C | 2K | 32ms | |

• Performance Range

| Speed | t _{TRC} | t _{CAC} | t _{RC} | t _{HPC} |
|-------|------------------|------------------|-----------------|------------------|
| -5 | 50ns | 13ns | 84ns | 20ns |
| -6 | 60ns | 15ns | 104ns | 25ns |

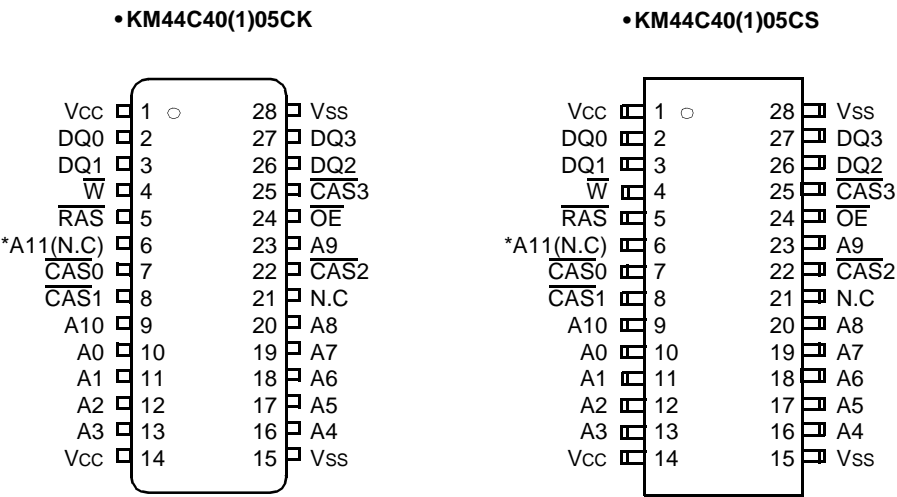
FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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PIN CONFIGURATION (Top Views)



*A11 is N.C for KM44C4105C(5V, 2K Ref. product)

K : 300mil 28 SOJ
 S : 300mil 28 TSOP II

| Pin Name | Pin Function |
|--|-----------------------------|
| A0 - A11 | Address Inputs (4K Product) |
| A0 - A10 | Address Inputs (2K Product) |
| DQ0 - 3 | Data In/Out |
| Vss | Ground |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{CAS0}}\sim\overline{\text{CAS3}}$ | Column Address Strobe |
| $\overline{\text{W}}$ | Read/Write Input |
| $\overline{\text{OE}}$ | Data Output Enable |
| Vcc | Power(+5.0V) |
| N.C | No Connection |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Units |
|---------------------------------------|------------------------------------|--------------|-------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1.0 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -1.0 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +150 | °C |
| Power Dissipation | P _D | 1 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Units |
|--------------------|-----------------|--------------------|-----|------------------------------------|-------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{CC} +1.0 ^{*1} | V |
| Input Low Voltage | V _{IL} | -1.0 ^{*2} | - | 0.8 | V |

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}

*2 : -2.0/20ns, Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Max | Units |
|--|-------------------|-----|-----|-------|
| Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt) | I _{I(L)} | -5 | 5 | uA |
| Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC}) | I _{O(L)} | -5 | 5 | uA |
| Output High Voltage Level(I _{OH} =-5mA) | V _{OH} | 2.4 | - | V |
| Output Low Voltage Level(I _{OL} =4.2mA) | V _{OL} | - | 0.4 | V |

DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol | Power | Speed | Max | | Units |
|------------------|-------------|------------|------------|------------|----------------|
| | | | KM44C4005C | KM44C4105C | |
| I _{CC1} | Don't care | -5 -6 | 90 80 | 110 100 | mA mA mA |
| I _{CC2} | Normal L | Don't care | 2 1 | 2 1 | mA mA |
| I _{CC3} | Don't care | -5 -6 | 90 80 | 110 100 | mA mA mA |
| I _{CC4} | Don't care | -5 -6 | 80 70 | 90 80 | mA mA mA |
| I _{CC5} | Normal L | Don't care | 1 250 | 1 250 | mA uA |
| I _{CC6} | Don't care | -5 -6 | 90 80 | 110 100 | mA mA mA |
| I _{CC7} | L | Don't care | 300 | 300 | uA |
| I _{CCS} | L | Don't care | 250 | 250 | uA |

I_{CC1}* : Operating Current (\overline{RAS} and \overline{CAS} cycling @trc=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address cycling @thpc=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} and \overline{CAS} cycling @trc=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, $\overline{CAS}=0.2V$,

DQ=Don't care, Trc=31.25us(4K/L-ver), 62.5us(2K/L-ver), TRAS=TRASmin~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}=\overline{CAS}=0.2V$, $\overline{W}=\overline{OE}=A0 \sim A11=V_{CC}-0.2V$ or $0.2V$,

DQ0 ~ DQ3= $V_{CC}-0.2V$, $0.2V$ or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6} address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, thpc.

KM44C4005C, KM44C4105C

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

| Parameter | Symbol | Min | Max | Units |
|---|--------|-----|-----|-------|
| Input capacitance [A0 ~ A11] | CIN1 | - | 5 | pF |
| Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CASx}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$] | CIN2 | - | 7 | pF |
| Output capacitance [DQ0 - DQ3] | CDQ | - | 7 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition : VCC=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V

| Parameter | Symbol | -5 | | -6 | | Units | Notes |
|---|--------|-----|-----|-----|-----|-------|----------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | trc | 84 | | 104 | | ns | |
| Read-modify-write cycle time | trwc | 106 | | 140 | | ns | |
| Access time from $\overline{\text{RAS}}$ | trac | | 50 | | 60 | ns | 3,4,10 |
| Access time from $\overline{\text{CAS}}$ | tcac | | 13 | | 15 | ns | 3,4,5,20 |
| Access time from column address | tAA | | 25 | | 30 | ns | 3,10 |
| $\overline{\text{CAS}}$ to output in Low-Z | tCLZ | 3 | | 3 | | ns | 3,20 |
| Output buffer turn-off delay from $\overline{\text{CAS}}$ | tCEZ | 3 | 13 | 3 | 15 | ns | 6,13 |
| $\overline{\text{OE}}$ to output in Low-Z | tOLZ | 3 | | 3 | | ns | 3 |
| Transition time (rise and fall) | tt | 2 | 50 | 2 | 50 | ns | 2 |
| $\overline{\text{RAS}}$ precharge time | trp | 30 | | 40 | | ns | |
| $\overline{\text{RAS}}$ pulse width | trAS | 50 | 10K | 60 | 10K | ns | |
| $\overline{\text{RAS}}$ hold time | trSH | 13 | | 15 | | ns | 16 |
| $\overline{\text{CAS}}$ hold time | tCSH | 38 | | 45 | | ns | 19 |
| $\overline{\text{CAS}}$ pulse width | tcAS | 8 | 10K | 10 | 10K | ns | 25 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | trCD | 20 | 37 | 20 | 45 | ns | 4,18 |
| $\overline{\text{RAS}}$ to column address delay time | trAD | 15 | 25 | 15 | 30 | ns | 10 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | trCP | 5 | | 5 | | ns | 17 |
| Row address set-up time | tASR | 0 | | 0 | | ns | |
| Row address hold time | trAH | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | ns | 18 |
| Column address hold time | tCAH | 8 | | 10 | | ns | 18 |
| Column address to $\overline{\text{RAS}}$ lead time | trAL | 25 | | 30 | | ns | |
| Read command set-up time | trCS | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{\text{CAS}}$ | trCH | 0 | | 0 | | ns | 8,17 |
| Read command hold time referenced to $\overline{\text{RAS}}$ | trRH | 0 | | 0 | | ns | 8 |
| Write command hold time | twCH | 10 | | 10 | | ns | 16 |
| Write command pulse width | twP | 10 | | 10 | | ns | |
| Write command to $\overline{\text{RAS}}$ lead time | trWL | 13 | | 15 | | ns | |
| Write command to $\overline{\text{CAS}}$ lead time | tcWL | 8 | | 10 | | ns | 19 |

AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -5 | | -6 | | Units | Notes |
|---|--------|-----|------|-----|------|-------|----------|
| | | Min | Max | Min | Max | | |
| Data set-up time | tDS | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 8 | | 10 | | ns | 9 |
| Refresh period (2K, Normal) | tREF | | 32 | | 32 | ms | |
| Refresh period (4K, Normal) | tREF | | 64 | | 64 | ms | |
| Refresh period (L-ver) | tREF | | 128 | | 128 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7,18 |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time | tCWD | 30 | | 34 | | ns | 7,16 |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time | tRWD | 67 | | 79 | | ns | 7 |
| Column address to $\overline{\text{W}}$ delay time | tAWD | 42 | | 49 | | ns | 7 |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time | tCPWD | 47 | | 54 | | ns | 7 |
| $\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | tCSR | 5 | | 5 | | ns | 18 |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | tCHR | 10 | | 10 | | ns | 17 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | tRPC | 5 | | 5 | | ns | 18 |
| Access time from $\overline{\text{CAS}}$ precharge | tCPA | | 28 | | 35 | ns | 3,17 |
| Hyper Page mode cycle time | tHPC | 20 | | 24 | | ns | 14,21 |
| Hyper Page read-modify-write cycle time | tHPRWC | 62 | | 71 | | ns | 14,21 |
| $\overline{\text{CAS}}$ precharge time (Hyper Page cycle) | tCP | 8 | | 10 | | ns | 22 |
| $\overline{\text{RAS}}$ pulse width (Hyper Page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge | tRHCP | 30 | | 35 | | ns | |
| $\overline{\text{OE}}$ access time | tOEA | | 13 | | 15 | ns | 23 |
| $\overline{\text{OE}}$ to data delay | tOED | 13 | | 15 | | ns | 24 |
| Output buffer turn off delay time from $\overline{\text{OE}}$ | tOEZ | 3 | 13 | 3 | 15 | ns | 6 |
| $\overline{\text{OE}}$ command hold time | tOEH | 13 | | 15 | | ns | |
| Write command set-up time (Test mode in) | tWTS | 10 | | 10 | | ns | 11 |
| Write command hold time (Test mode in) | tWTH | 10 | | 10 | | ns | 11 |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh) | tWRP | 10 | | 10 | | ns | |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh) | tWRH | 10 | | 10 | | ns | |
| Output data hold time | tDOH | 5 | | 5 | | ns | |
| Output buffer turn off delay from $\overline{\text{RAS}}$ | tREZ | 3 | 13 | 3 | 15 | ns | 6,13 |
| Output buffer turn off delay from $\overline{\text{W}}$ | tWEZ | 3 | 13 | 3 | 15 | ns | 6 |
| $\overline{\text{W}}$ to data delay | tWED | 15 | | 15 | | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time | tOCH | 5 | | 5 | | ns | |
| $\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$ | tCHO | 5 | | 5 | | ns | |
| $\overline{\text{OE}}$ precharge time | tOEP | 5 | | 5 | | ns | |
| $\overline{\text{W}}$ pulse width (Hyper Page Cycle) | twPE | 5 | | 5 | | ns | |
| $\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh) | trASS | 100 | | 100 | | us | 27,28,29 |
| $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh) | trPS | 90 | | 110 | | ns | 27,28,29 |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh) | tCHS | -50 | | -50 | | ns | 27,28,29 |
| Hold time $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high | tCLCH | 5 | | 5 | | ns | 15,26 |

TEST MODE CYCLE

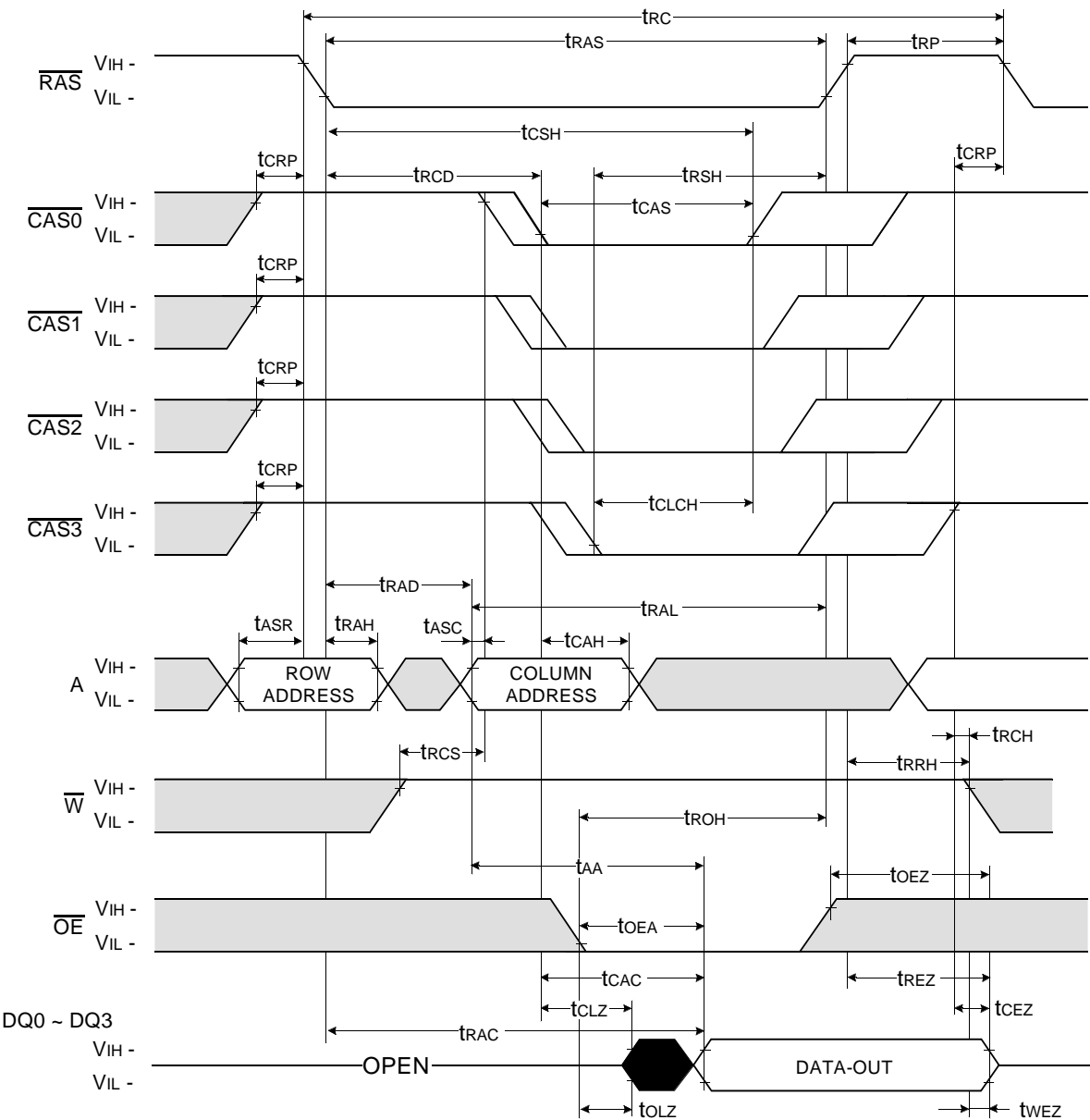
(Note 11)

| Parameter | Symbol | -5 | | -6 | | Units | Notes |
|---|--------------------|-----|------|-----|------|-------|-----------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | t _{RC} | 89 | | 109 | | ns | |
| Read-modify-write cycle time | t _{RWC} | 121 | | 145 | | ns | |
| Access time from $\overline{\text{RAS}}$ | t _{RAC} | | 55 | | 65 | ns | 3,4,10,12 |
| Access time from $\overline{\text{CAS}}$ | t _{CAC} | | 18 | | 20 | ns | 3,4,5,12 |
| Access time from column address | t _{AA} | | 30 | | 35 | ns | 3,10,12 |
| $\overline{\text{RAS}}$ pulse width | t _{RAS} | 55 | 10K | 65 | 10K | ns | |
| $\overline{\text{CAS}}$ pulse width | t _{CAS} | 13 | 10K | 15 | 10K | ns | |
| $\overline{\text{RAS}}$ hold time | t _{RSH} | 18 | | 20 | | ns | |
| $\overline{\text{CAS}}$ hold time | t _{CSH} | 43 | | 50 | | ns | |
| Column address to $\overline{\text{RAS}}$ lead time | t _{RAL} | 30 | | 35 | | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time | t _{CWD} | 35 | | 39 | | ns | 7 |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time | t _{RWD} | 72 | | 84 | | ns | 7 |
| Column address to $\overline{\text{W}}$ delay time | t _{AWD} | 47 | | 54 | | ns | 7 |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time | t _{CPWD} | 52 | | 59 | | ns | 7 |
| Hyper Page mode cycle time | t _{HPC} | 25 | | 30 | | ns | 14 |
| Hyper Page read-modify-write cycle time | t _{HPRWC} | 52 | | 61 | | ns | 14 |
| $\overline{\text{RAS}}$ pulse width (Hyper Page cycle) | t _{RASP} | 55 | 200K | 65 | 200K | ns | |
| Access time from $\overline{\text{CAS}}$ precharge | t _{CPA} | | 33 | | 40 | ns | 3 |
| $\overline{\text{OE}}$ access time | t _{OEa} | | 18 | | 20 | ns | |
| $\overline{\text{OE}}$ to data delay | t _{OEED} | 18 | | 20 | | ns | |
| $\overline{\text{OE}}$ command hold time | t _{OEh} | 18 | | 20 | | ns | |

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only.
If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes the $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. t_{RCH} and t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the first $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only.
If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the values of t_{RAC} , t_{AA} and t_{CAC} are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
13. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going.
If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
14. $t_{\text{ASC}} \geq 6\text{ns}$, Assume $t_{\text{T}} = 2.0\text{ns}$.
15. In order to hold the address latched by the first $\overline{\text{CAS}}$ going low, the parameter t_{CLCH} must be met.
16. The last $\overline{\text{CASx}}$ edge to go low.
17. The last $\overline{\text{CASx}}$ edge to go high.
18. The first $\overline{\text{CASx}}$ edge to go low.
19. The first $\overline{\text{CASx}}$ edge to go high.
20. Output parameter is referenced to corresponding $\overline{\text{CASx}}$ input.
21. The last rising $\overline{\text{CASx}}$ edge to next cycle's last rising $\overline{\text{CASx}}$ edge.
22. The last rising $\overline{\text{CASx}}$ edge to first falling $\overline{\text{CASx}}$ edge.
23. The first DQx controlled by the first $\overline{\text{CASx}}$ to go low.
24. The last DQx controlled by the last $\overline{\text{CASx}}$ to go high.
25. Each $\overline{\text{CASx}}$ must meet minimum pulse width.
26. The last falling $\overline{\text{CASx}}$ edge to the first rising $\overline{\text{CASx}}$ edge.
27. If $t_{\text{RAS}} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
28. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K)/2048(2K) cycles of burst refresh must be executed within 64ms/32ms before and after self refresh, in order to meet refresh specification.
29. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

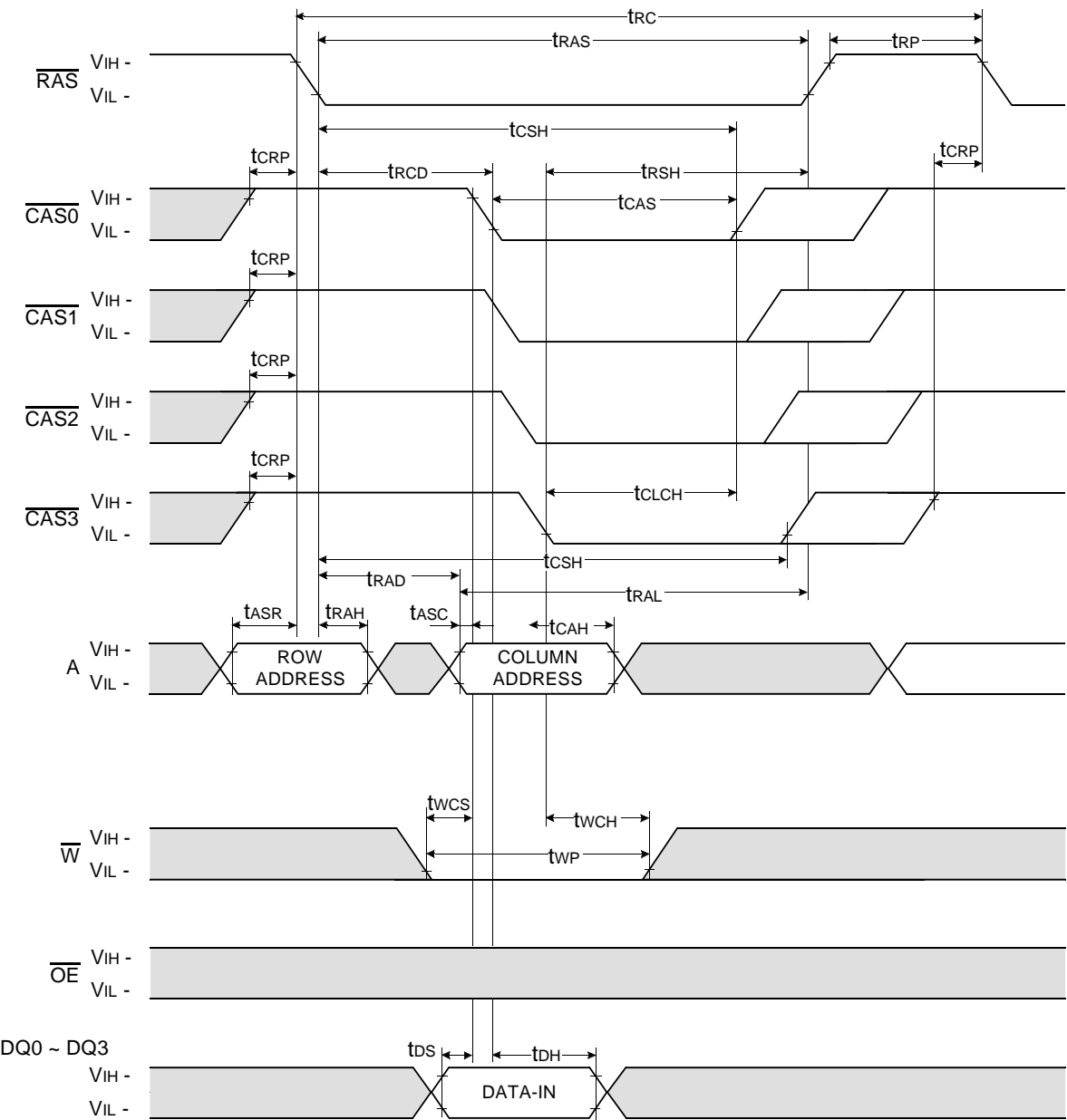
READ CYCLE



Don't care
Undefined

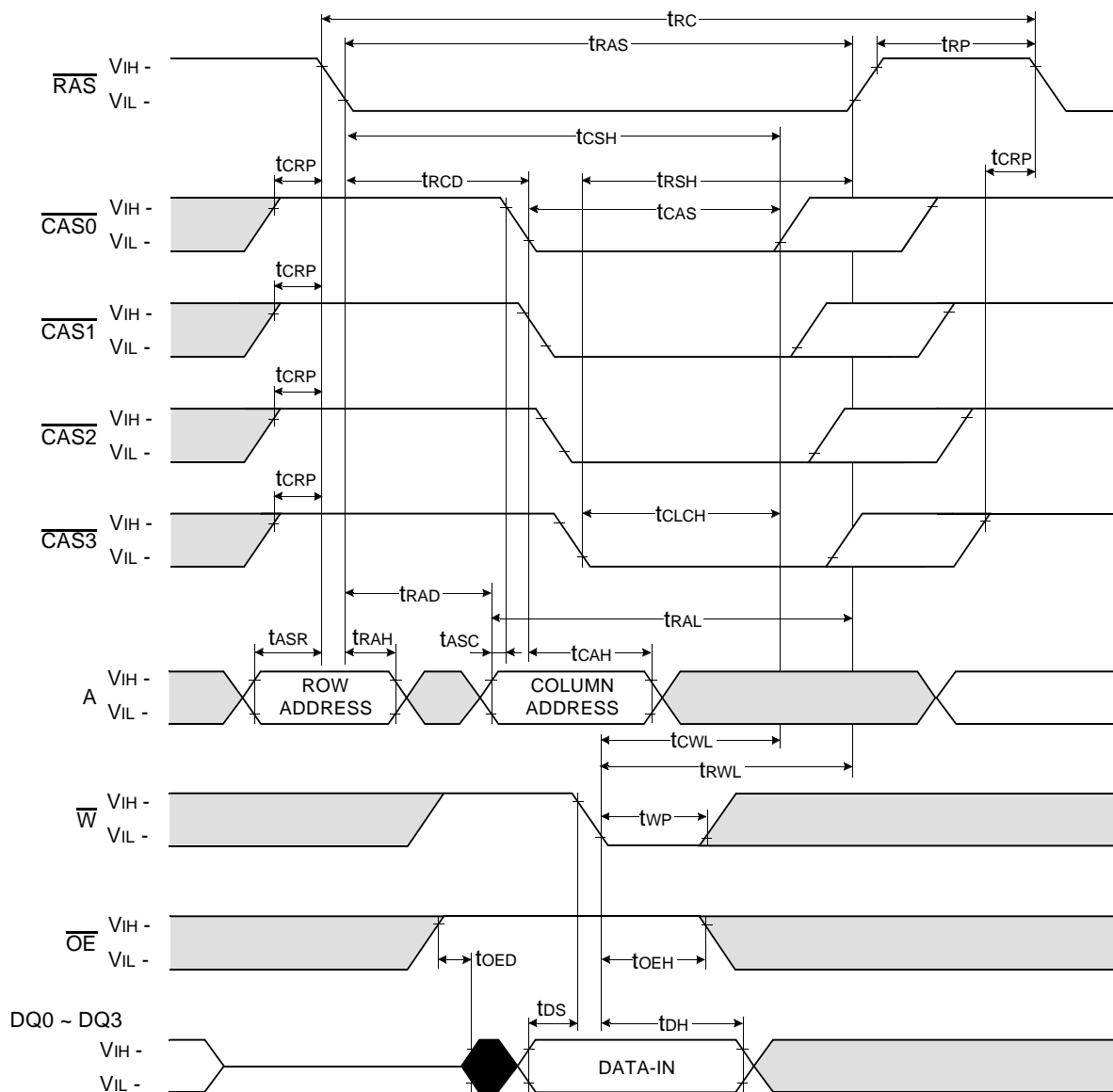
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

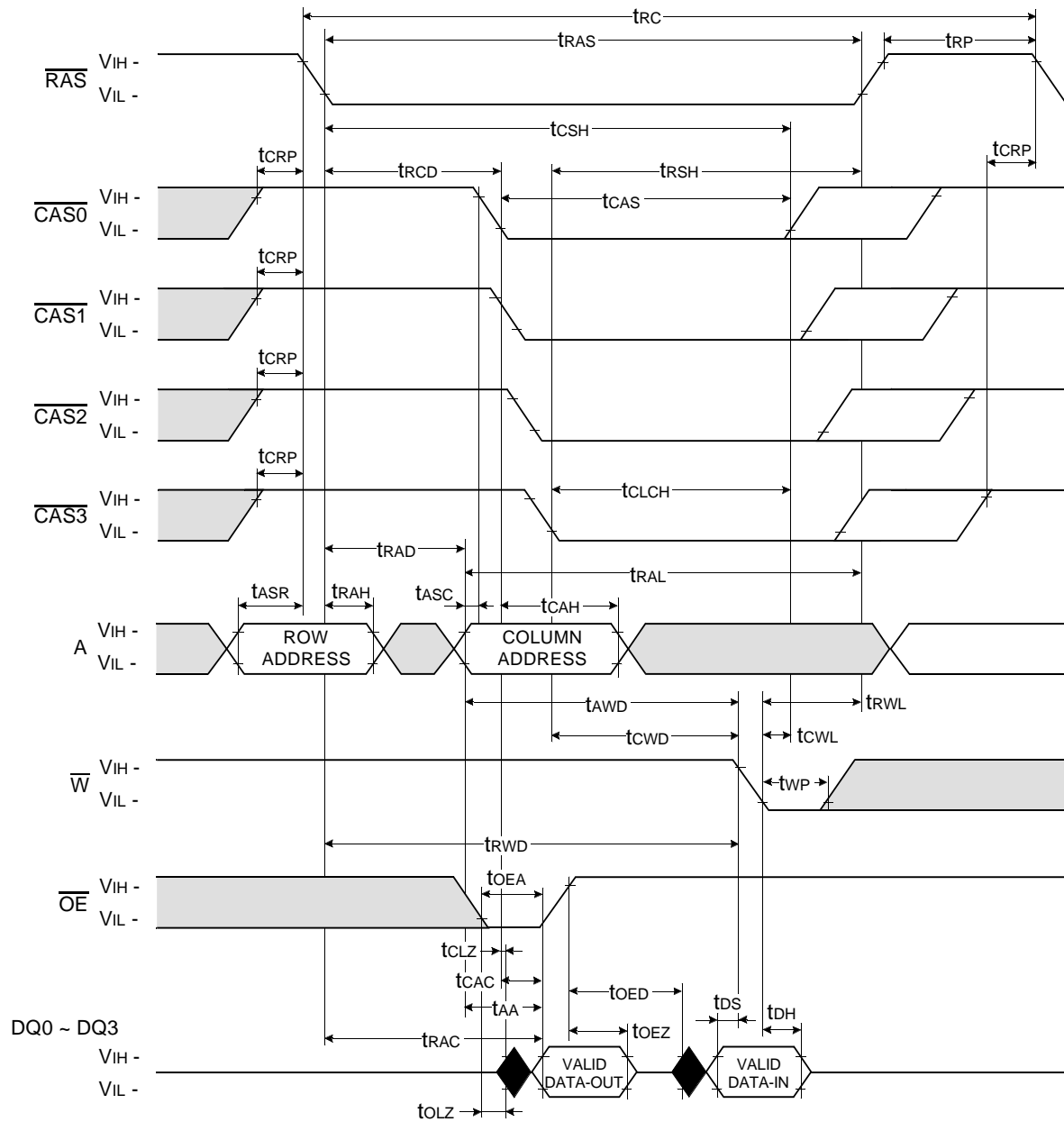


WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



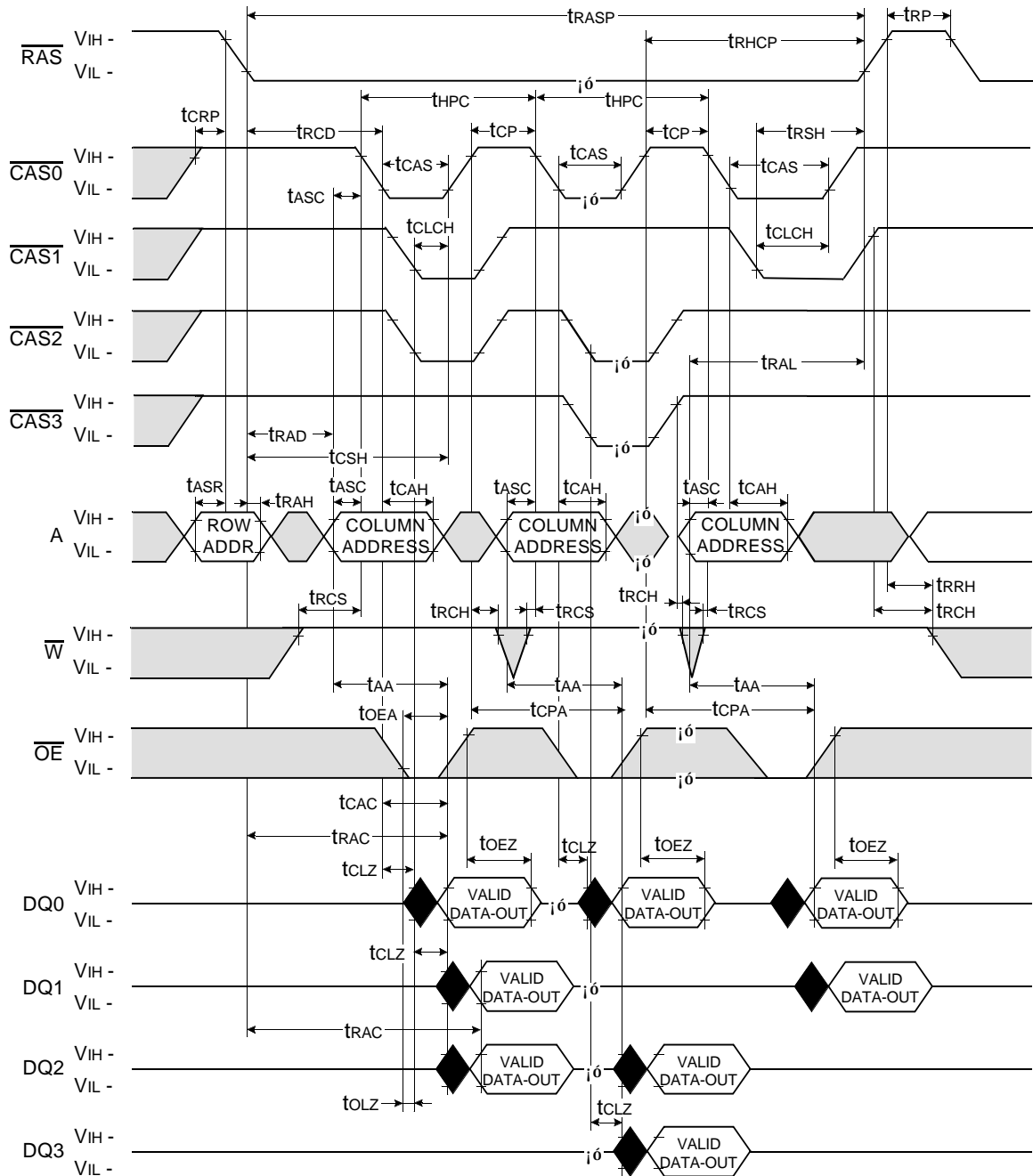
READ - MODIFY - WRITE CYCLE



Don't care

Undefined

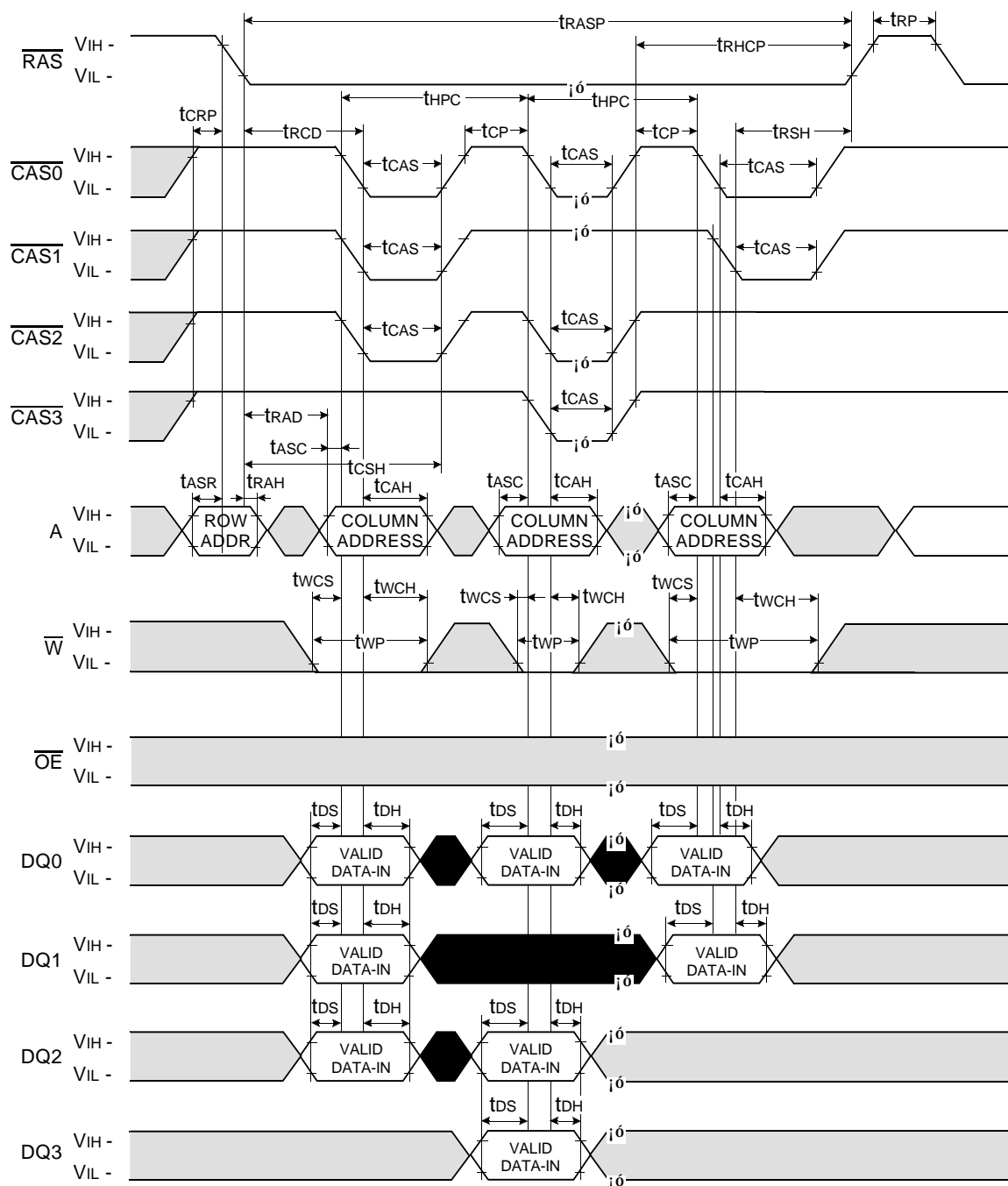
HYPER PAGE MODE READ CYCLE



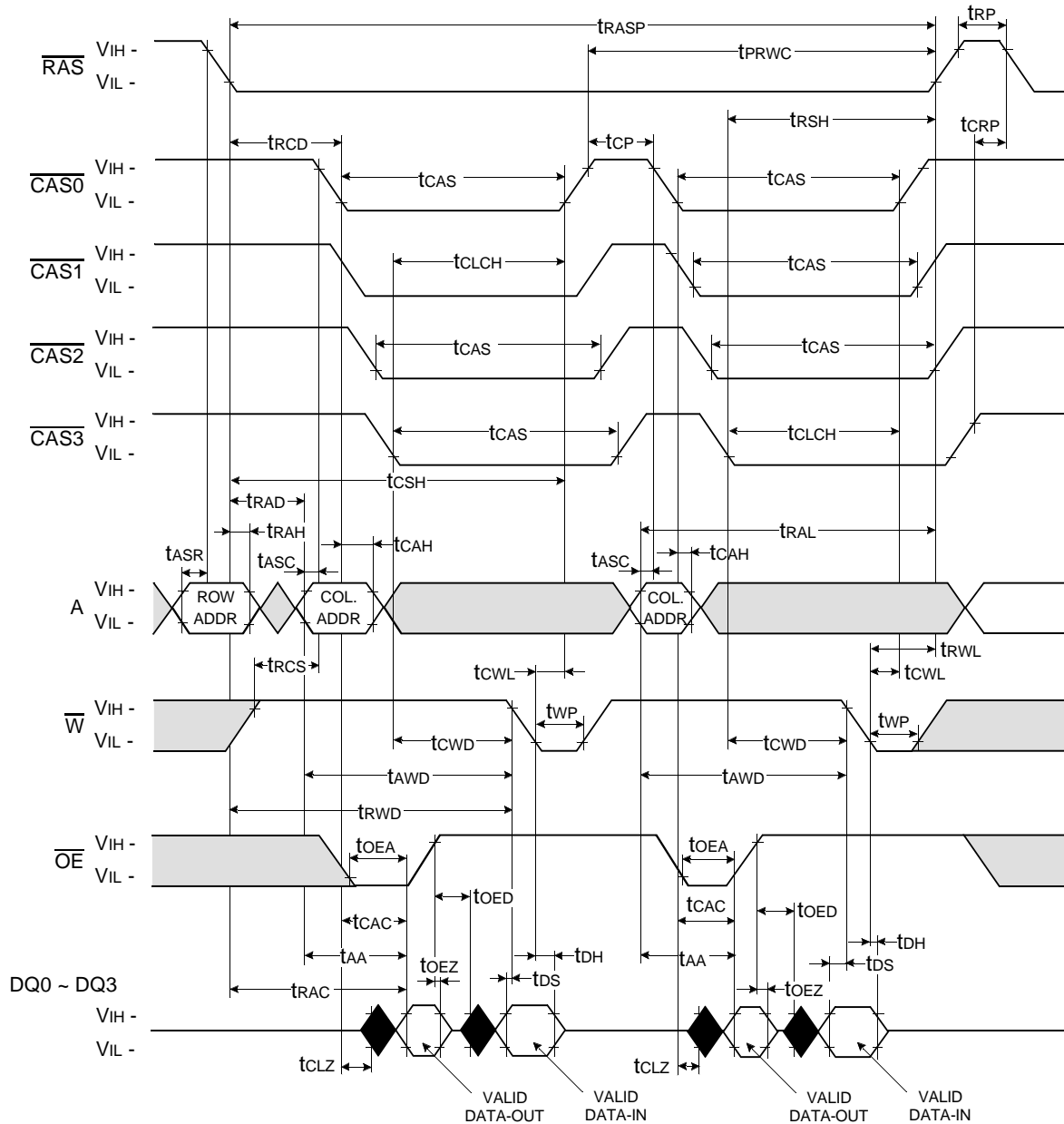
Don't care
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HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



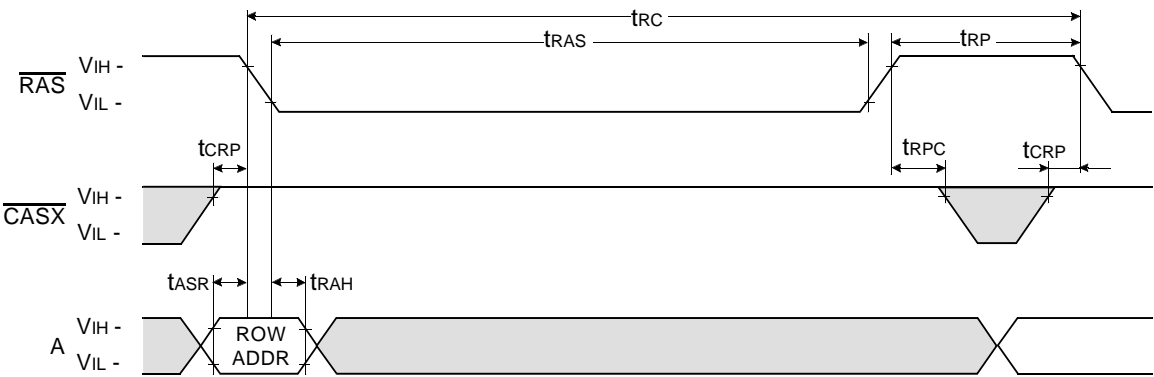
HYPER PAGE READ - MODIFY - WRITE CYCLE



$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

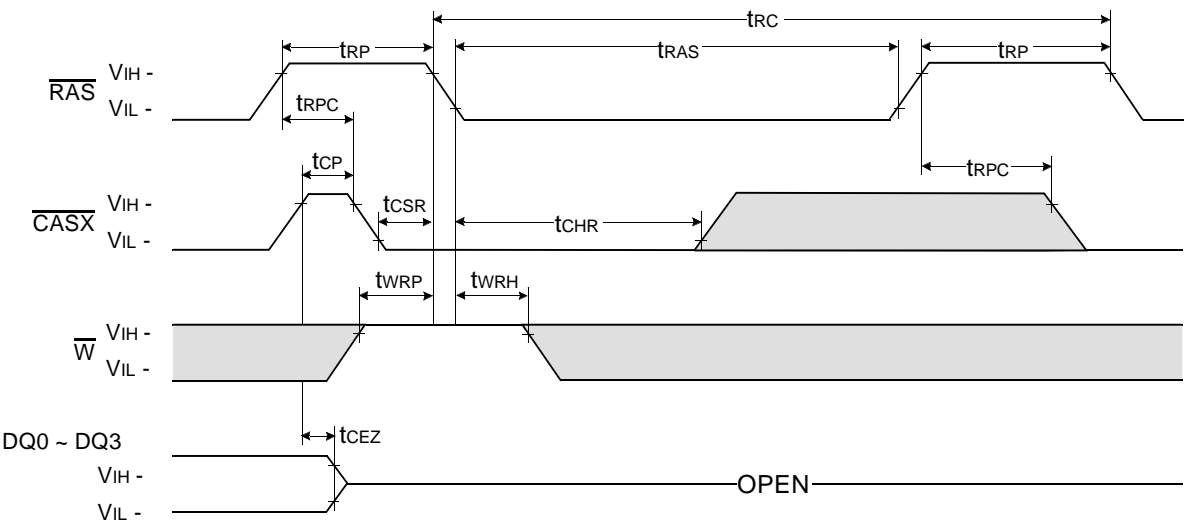
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



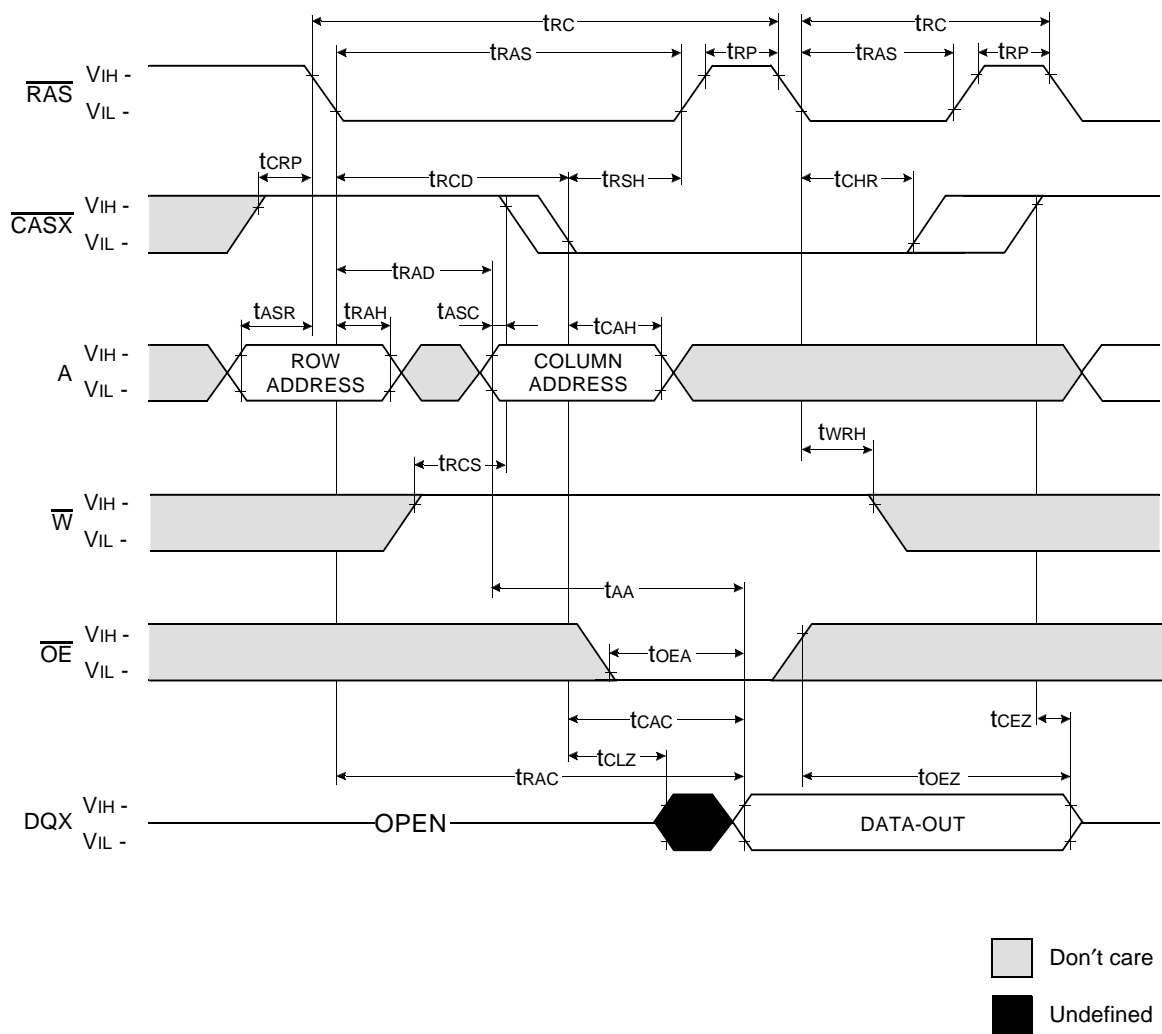
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



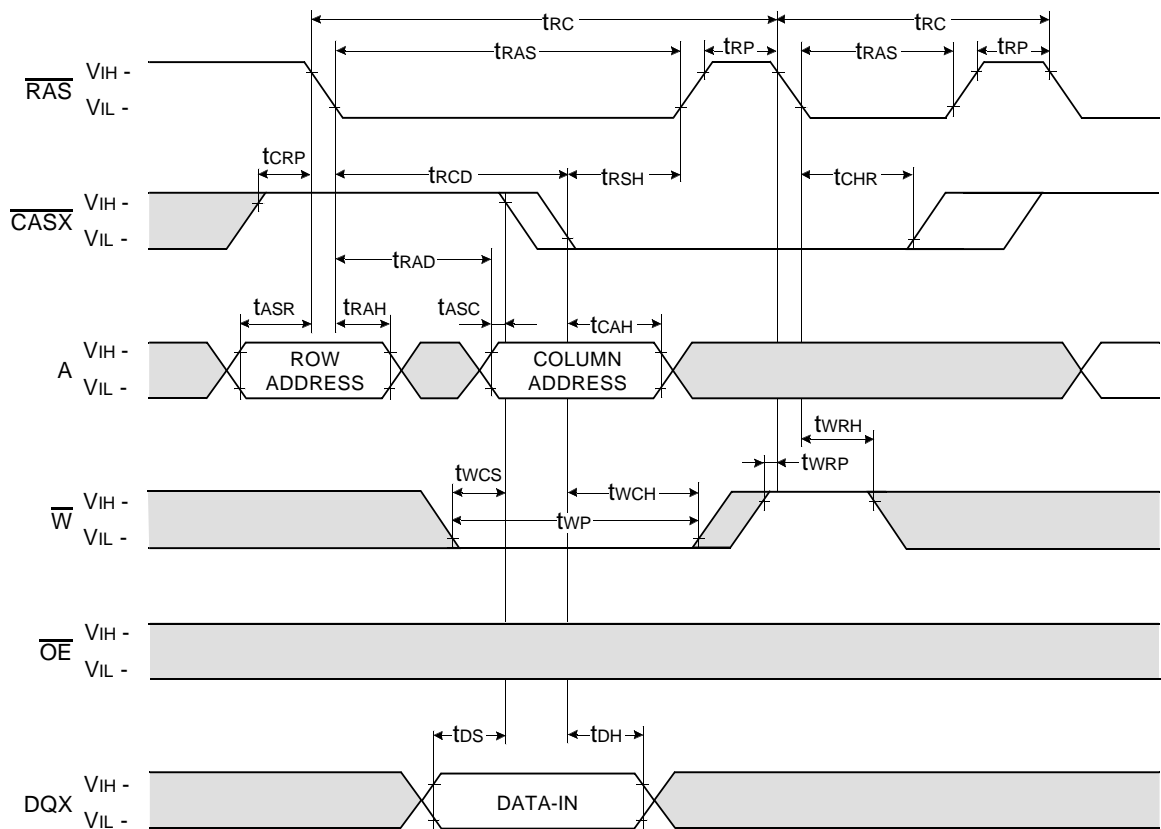
Don't care
 Undefined

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

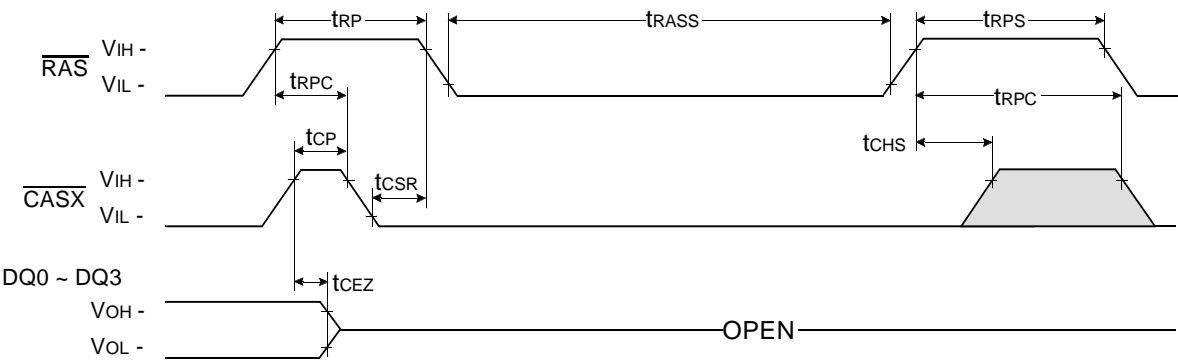
NOTE : DOUT = OPEN



Don't care
Undefined

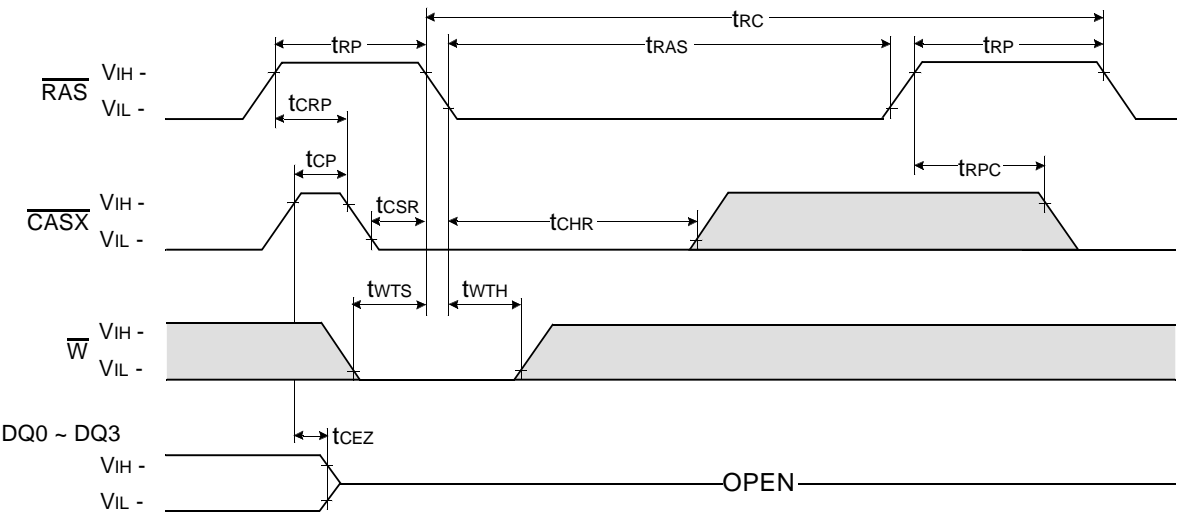
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : OE, A = Don't care, WE=Vcc-0.2V



TEST MODE IN CYCLE

NOTE : OE, A = Don't care



Don't care
Undefined

PACKAGE DIMENSION

