

524,288K WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

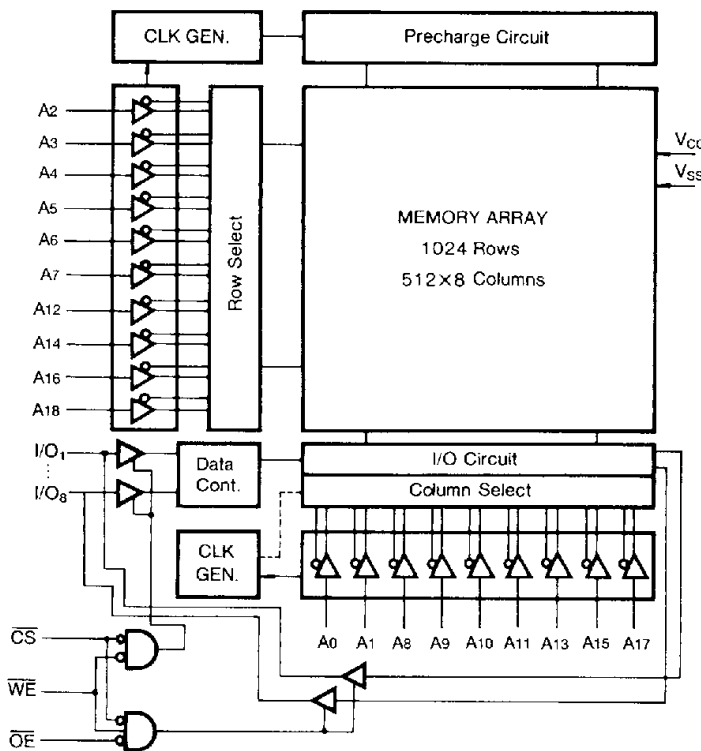
- Fast Access Time : 70,85,100ns(Max.)
- Low Power Dissipation  
Standby (CMOS) : 11mW(Typ.)  
1.1μW(Typ.) L-Version  
275μW(Typ.) LL-Version
- Operating : 137.5mW(Max.)
- Single 5V ± 10% power supply
- Wide temperature operatint: -40° C~85° C
- TTL Compatible inputs and outputs
- Three State Output
- Low Data Retention Voltage:2V(Min)
- Standard Pin Configuration  
KM684000LGI/LGI-L : 32-SOP-525  
KM684000LTI/LTI-L : 32-TSOP2-400F  
KM684000LRI/LRI-L : 32-TSOP2-400R

GENERAL DESCRIPTION

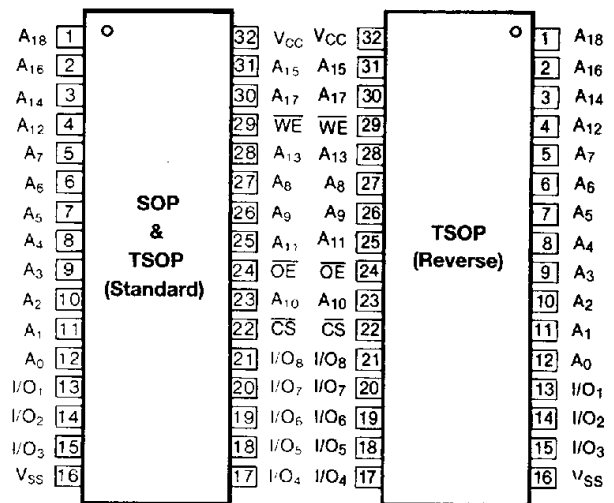
The KM684000LI/LI-L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524, 288 words by 8 bits.  
The device is fabricated using Samsung's advanced CMOS process.  
The KM684000LI/LI-L has an output enable input for precise control of the data outputs.  
It also has chip enable inputs for the minimum current power down mode  
The KM684000LI/LI-L has been designed for high speed and low power applications.  
It is particularly well suited for battery back-up nonvolatile memory application.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
WE	Write Enable input
CS	Chip Select Input
OE	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(+5V)
Vss	Ground



**ABSOLUTE MAXIMUM RATINGS\***

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>STG</sub>	-55 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING CONDITIONS** (T<sub>A</sub>=40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub>(min.)=-3.0V for < 50ns pulse

**DC AND OPERATING CHARACTERISTICS**

(T<sub>A</sub>=-40 to 85°C, V<sub>CC</sub>=5V ± 10%, unless otherwise specified)

Item	Symbol	Test Condition	Min	Max	Unit
Input Leakage Current	I <sub>I</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	+1	μA
Output Leakage Current	I <sub>O</sub>	$\overline{CS}$ =V <sub>IN</sub> or $\overline{WE}$ =V <sub>IL</sub> $\overline{OE}$ =V <sub>IH</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	+1	μA
Operating Power Supply Current	I <sub>CC</sub>	$\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , I <sub>IO</sub> =0mA		25	mA
Average Operating Current	I <sub>CC1</sub>	Cycle Time=1μs, 100% Duty $\overline{CS}$ ≤ 0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤ 0.2V, I <sub>IO</sub> =0mA		20	mA
	I <sub>CC2</sub>	Min Cycle, 100% Duty $\overline{CS}$ =V <sub>IL</sub> V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> I <sub>IO</sub> =0mA		70	mA
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub>		3	mA
	I <sub>SB1</sub>	$\overline{CS}$ ≥ V <sub>CC</sub> -0.2V	L	100	μA
V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2 or V <sub>IN</sub> ≤ 0.2V		L-L	50	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4		V



## CAPACITANCE (f=1MHz, TA=25°C)

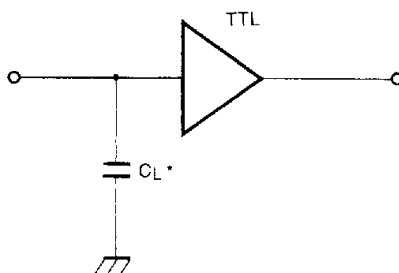
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	10	pF

\* Note : Capacitance is sampled and not 100% tested.

## TEST CONDITIONS (TA=-40 to 85°C, Vcc=5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C <sub>L</sub> =100pF+1TTL

## TEST CIRCUIT



\* Including Scope and Jig Capacitance

## READ CYCLE

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	70		85		100		ns
Address Access Time	t <sub>AA</sub>		70		85		100	ns
Chip Select to Output	t <sub>CO</sub>		70		85		100	ns
Output Enable to Valid Output	t <sub>OE</sub>		35		40		50	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	10		10		10		ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5		5		5		ns
Output Disable to High-Z Output	t <sub>HZ</sub>	0	25	0	30	0	30	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	25	0	30	0	30	ns
Output Hold from Address Change	t <sub>OH</sub>	10		10		10		ns

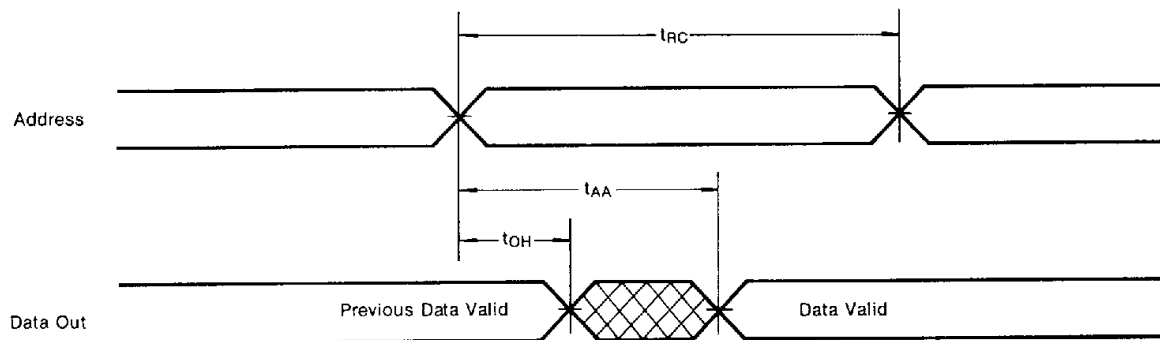
**WRITE CYCLE**

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	70		85		100		ns
Chip Select to End of Write	t <sub>CW</sub>	60		70		80		ns
Address Set-up Time	t <sub>AS</sub>	0		0		0		ns
Address Valid to End of Write	t <sub>AW</sub>	60		70		80		ns
Write Pulse Width	t <sub>WP</sub>	50		55		60		ns
Write Recovery Time	t <sub>WR</sub>	0		0		0		ns
Write to Output High-Z	t <sub>WHZ</sub>	0	30	0	30	0	30	ns
Data to Write Time Overlap	t <sub>DW</sub>	30		35		40		ns
Data Hold from Write Time	t <sub>DH</sub>	0		0		0		ns
End of Write to Output Low-Z	t <sub>OW</sub>	5		5		5		ns

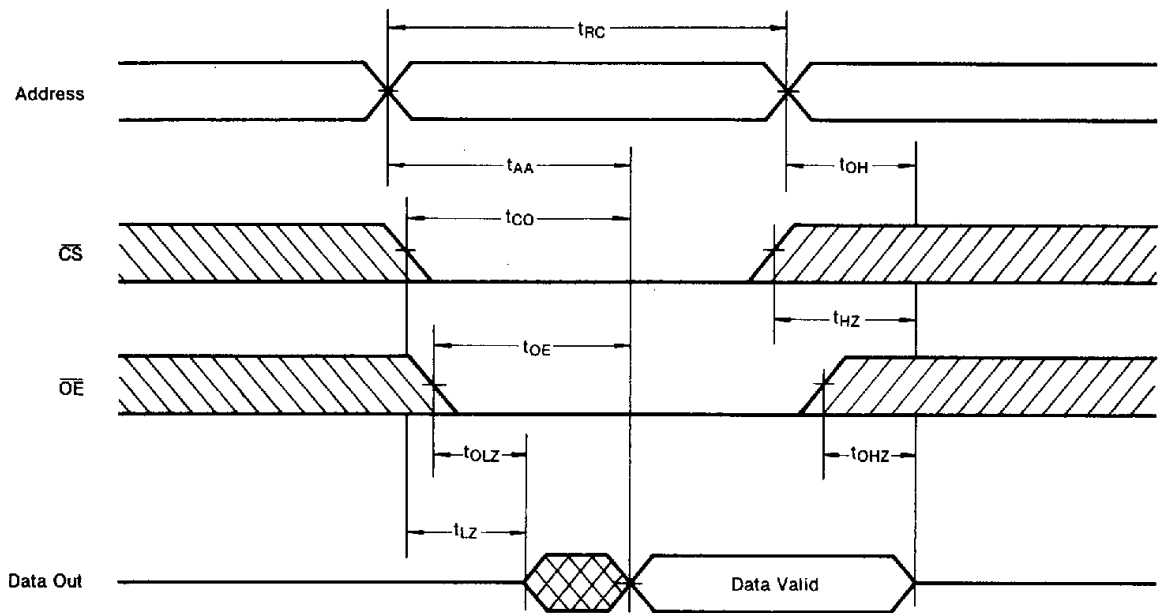
**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE (1)** (Address Controlled)

( $\overline{CS} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



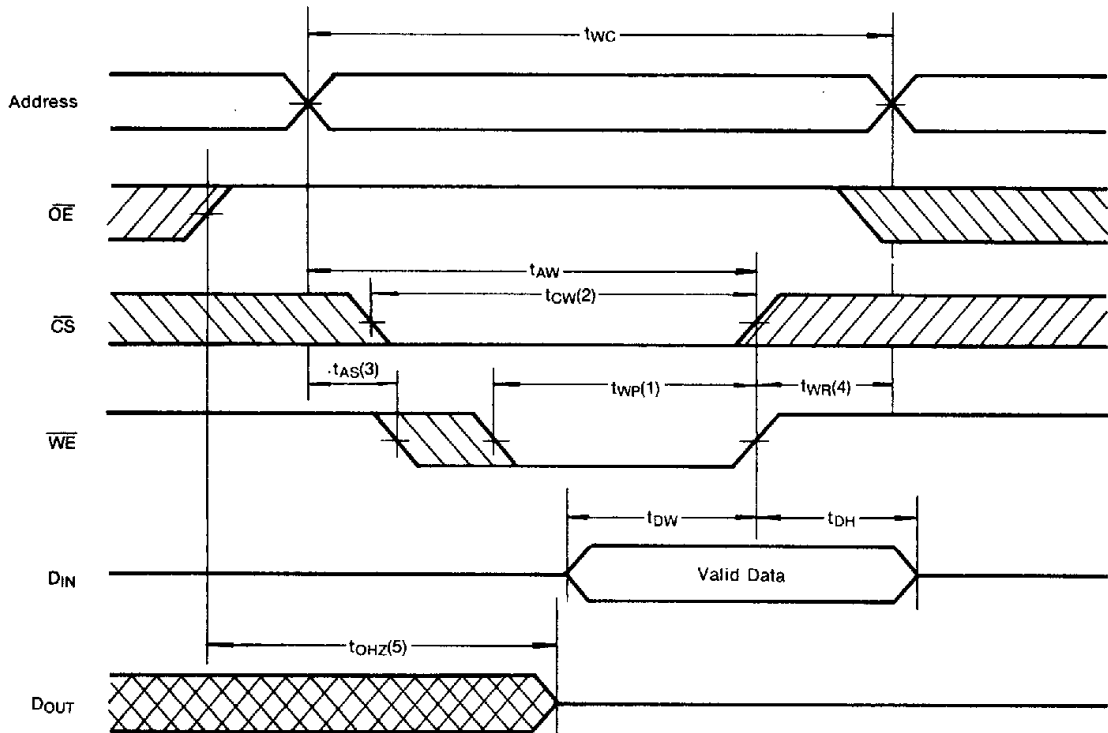
TIMING WAVEFORM OF READ CYCLE (2) ( $\overline{WE} = V_{IH}$ )



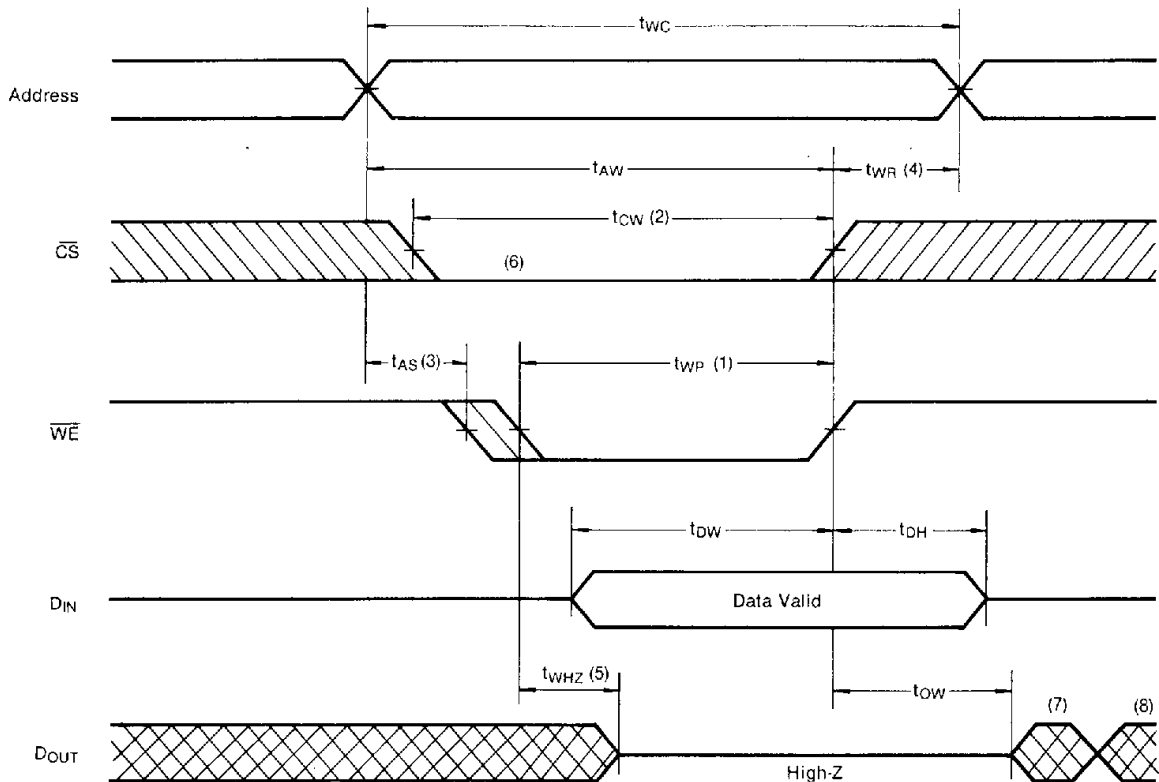
Notes (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
2. At any given temperature and voltage condition,  $t_{HZ}$  (max.) is less than  $t_{LZ}$  (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ( $\overline{OE} = \text{Clock}$ )



**TIMING WAVEFORM OF WRITE CYCLE (2) ( $\overline{OE}$  = Low Fixed)**



**Notes (WRITE CYCLE)**

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going low and  $\overline{WE}$  going low: A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$ , or  $\overline{WE}$  going high.
5. During this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain high impedance state.
7.  $D_{OUT}$  is the some phase of latest written data in this write cycle.
8.  $D_{OUT}$  is the read data of the new address.

**FUNCTIONAL DESCRIPTION**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	$V_{CC}$ Current
H	X*	X	Power Down	High-Z	$I_{SB}, I_{SB1}$
L	H	H	Output Disable	High-Z	$I_{CC}$
L	H	L	Read	$D_{OUT}$	$I_{CC}$
L	L	X	Write	$D_{IN}$	$I_{CC}$

\* Note: X means Don't Care.



**DATA RETENTION CHARACTERISTICS\*** (TA=40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for Data Retention	Vdr	$\overline{CS} \geq V_{cc} - 0.2V$	2.0		5.5	V
Data Retention Current	Idr	Vcc=3V			50*	$\mu A$
		$\overline{CS} \geq V_{cc} - 0.2V$			20**	$\mu A$
Data Retention Set-up Time	tSDR	See Data Retention	0			ns
Recovery Time	tRDR	Wave forms (below)	5			ns

\* 20 $\mu A$  (max) at 0°C~40°C

\*\* 5 $\mu A$  (max) at 0°C~40°C

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**DATA RETENTION WAVEFORM**

**L/L-L Power Version**

