

*1M x 16 Bit CMOS Dynamic RAM with Extended Data Out*

**FEATURES**

- Performance range:

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
KM416V1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- Extended Data Out Mode (Fast Page Mode with Extended Data Out)
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple  $+3.3\text{V} \pm 0.3\text{V}$  power supply
- Refresh Cycle
  - 4096 cycle/64ms (Normal)
  - 4096 cycle/128ms (L-version)
  - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

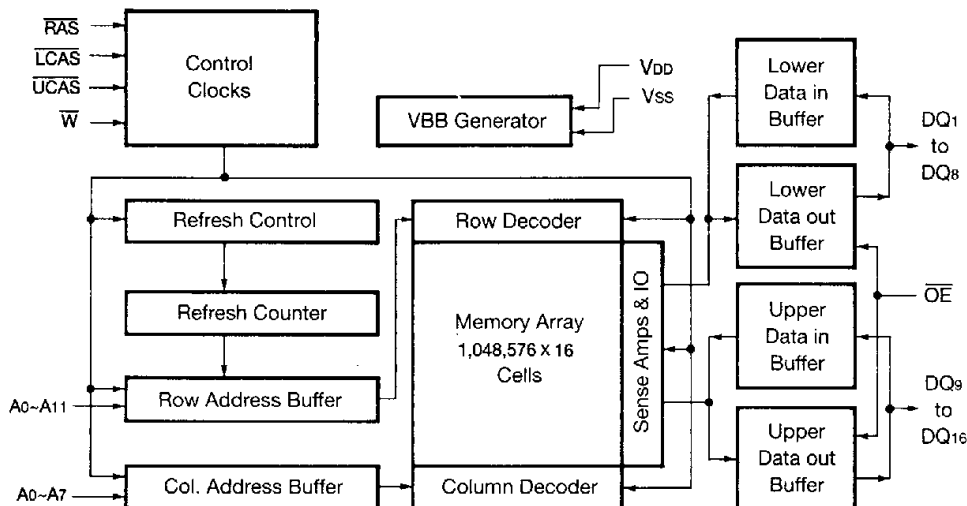
**GENERAL DESCRIPTION**

The Samsung KM416V1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

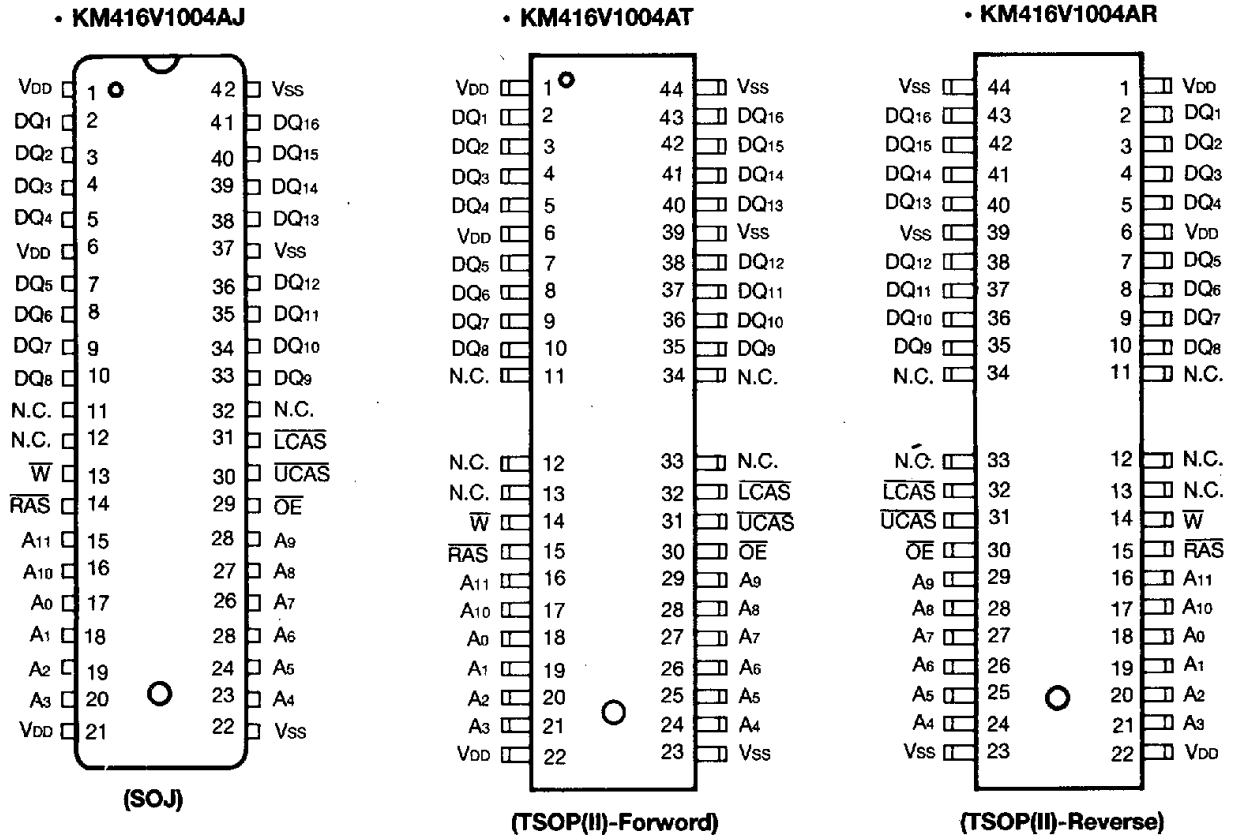
The KM416V1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability provides on-chip auto refresh as an alternative to  $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

**FUNCTIONAL BLOCK DIAGRAM**



## PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
Voltage on V <sub>DD</sub> Supply Relative to Vss	V <sub>DD</sub>	-0.5 to 4.6	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>DD</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.1	—	V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V

**DC AND OPERATING CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* ( $\overline{RAS}$ , $\overline{UCAS}$ or $\overline{LCAS}$ , Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I <sub>CC1</sub>	-	90 80 70	mA mA mA
Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$ )	KM416V1004A KM416V1004AL KM416V1004ALL	I <sub>CC2</sub>	-	2 1 1	mA mA mA
$\overline{RAS}$ -Only Refresh Current* ( $\overline{UCAS}=\overline{LCAS}=V_{IH}$ , $\overline{RAS}$ , Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I <sub>CC3</sub>	-	90 80 70	mA mA mA
EDO Mode Current* ( $\overline{RAS}=V_{IL}$ , $\overline{UCAS}$ or $\overline{LCAS}$ , Address Cycling @tPC=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I <sub>CC4</sub>	-	110 100 90	mA mA mA
Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{DD}-0.2V$ )	KM416V1004A KM416V1004AL KM416V1004ALL	I <sub>CC5</sub>	-	1 300 200	mA $\mu A$ $\mu A$
$\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current* ( $\overline{RAS}$ , $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I <sub>CC6</sub>	-	90 80 70	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V <sub>IH</sub> )=V <sub>DD</sub> -0.2V, Input Low Voltage(V <sub>IL</sub> )=0.2V $\overline{UCAS}$ , $\overline{LCAS}=0.2V$ DIN=Don't Care, trc=31.25 $\mu s$ (L-Version) trAS=trAS min~300ns	KM416V1004A-L	I <sub>CC7</sub>	-	450	$\mu A$

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**DC AND OPERATING CHARACTERISTICS** (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A11=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	I <sub>CCS</sub>	-	250	μA
Input Leakage Current (Any input 0 ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> +0.3V, all other pins not under test=0 V)	I <sub>I(L)</sub>	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> )	I <sub>O(L)</sub>	-10	10	μA
Output High Voltage Level (I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.4	-	V
Output Low Voltage Level (I <sub>OL</sub> =2mA)	V <sub>OL</sub>	-	0.4	V

\*NOTE: I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, Address can be changed maximum once while one Hyper page mode cycle time t<sub>HPC</sub>.

**CAPACITANCE** (T<sub>A</sub>=25°C, V<sub>DD</sub>=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~11)	C <sub>IN1</sub>	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	C <sub>IN2</sub>	-	7	pF
Output Capacitance (DQ1~DQ16)	C <sub>DQ</sub>	-	7	pF

**AC CHARACTERISTICS** (0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>DD</sub>=3.3V ± 0.3V, See notes 1,2)

(Test condition : V<sub>IH</sub>/V<sub>IL</sub>=2.1V/0.8V, V<sub>OH</sub>/V<sub>OL</sub>=2.0V/0.8V, Output Loading C<sub>L</sub>=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	110		130		150		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	155		185		205		ns	
Access time from $\overline{RAS}$	t <sub>RAC</sub>		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t <sub>CAC</sub>		17		20		20	ns	3,4,5
Access time from column address	t <sub>AA</sub>		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t <sub>CLZ</sub>	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t <sub>OLZ</sub>	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t <sub>CEZ</sub>	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t <sub>T</sub>	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t <sub>RP</sub>	40		50		60		ns	
$\overline{RAS}$ pulse width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t <sub>RSH</sub>	17		20		20		ns	
$\overline{CAS}$ hold time	t <sub>CSH</sub>	50		60		70		ns	
$\overline{CAS}$ pulse width	t <sub>CAS</sub>	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t <sub>RCD</sub>	20	45	20	50	20	60	ns	4



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	twCS	0		0		0		ns	8
Write command hold time	twCH	10		15		15		ns	
Write command hold time referenced to RAS	twCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	trWL	15		15		20		ns	
Write command to CAS lead time	tcWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to RAS	tdHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tcWD	40		50		50		ns	8,17
RAS to W delay time	trWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tcPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	20
RAS precharge to CAS hold time	trPC	5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tcPT	20		25		30		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	
OE access time	toEA		15		20		20	ns	
OE to data delay	toED	15		20		20		ns	
Output buffer turn off delay time from OE	toEZ	3	15	3	20	3	20	ns	7
OE command hold time	toEH	15		20		20		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
$\overline{\text{CAS}}$ precharge time (Hyper page mode)	tCP	10		10		10		ns	16
$\overline{\text{RAS}}$ pulse width (Hyper Page mode)	tRASP	60		70		80		ns	
$\overline{\text{RAS}}$ hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	15	3	20	3	20	ns	7
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		5		5		ns	
$\overline{\text{W}}$ pulse width	tWPE	5		5		5		ns	
$\overline{\text{W}}$ to data delay	tWED	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width (F-ver)	tRASS	100		100		100		$\mu\text{s}$	13
$\overline{\text{RAS}}$ precharge time (F-ver)	tRPS	110		130		150		ns	13
$\overline{\text{CAS}}$ hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416V1004A/A-L/A-F Truth Table

RAS	LCAS	UCAS	W	OE	DQ1-DQ8	DQ9-DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

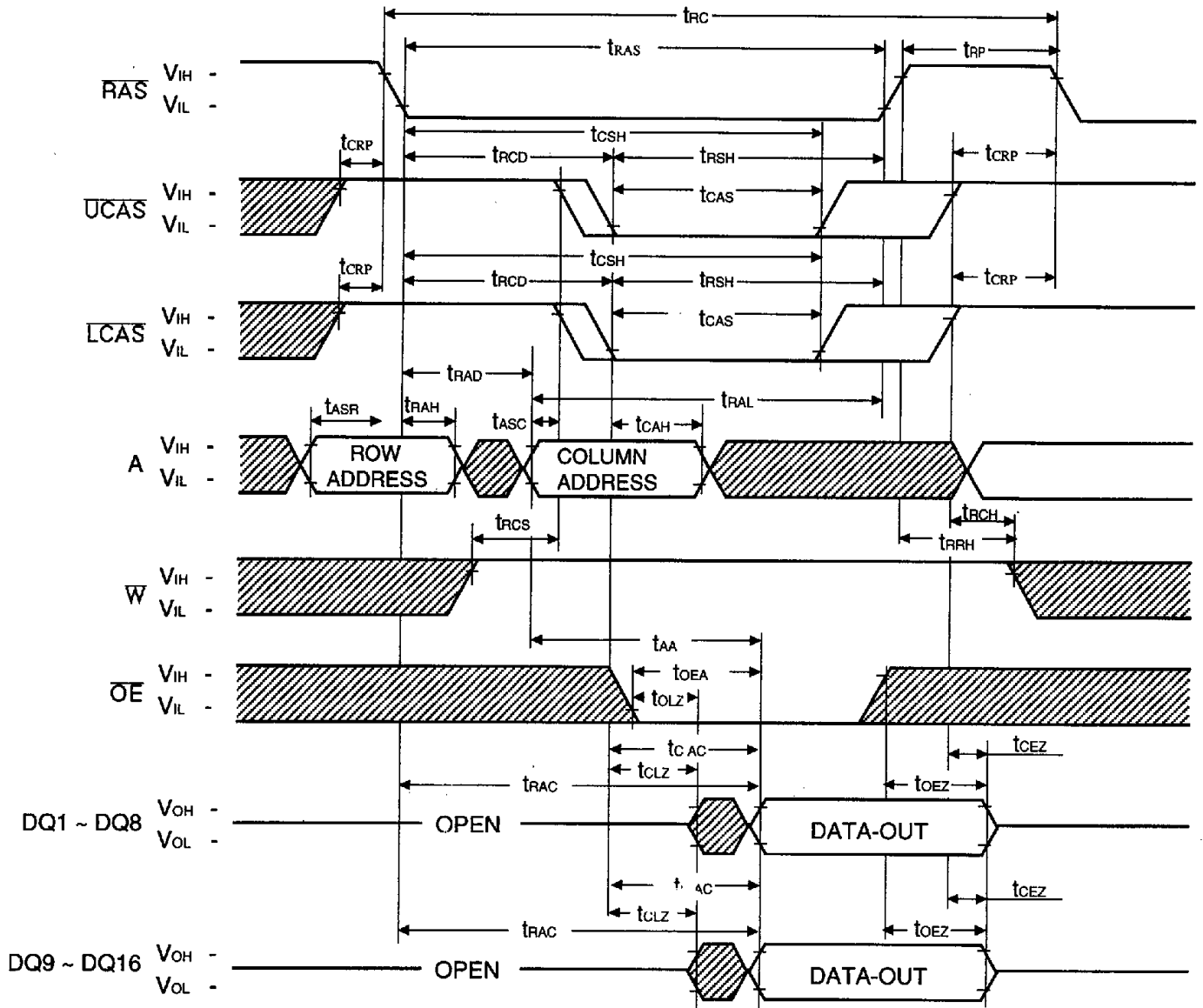


## NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
6.  $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  are referenced to  $t_{RAD}(\text{max})$ .
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min})$  the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{RWD} \geq t_{RWD}(\text{min})$  and  $t_{AWD} \geq t_{AWD}(\text{min})$ , then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles and to the  $\overline{\text{W}}$  leading edge in read-write cycles.
11. Operation within the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RAD}(\text{max})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled by  $t_{AA}$ .
12.  $t_{ASC} \geq t_{CP} \text{ min}$ , Assume  $t_{\tau} = 2.0\text{ns}$ .
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If  $\overline{\text{RAS}}$  goes to high before  $\overline{\text{CAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{CAS}}$  high going. If  $\overline{\text{CAS}}$  goes to high before  $\overline{\text{RAS}}$  high going, the open circuit condition of the output is achieved by  $\overline{\text{RAS}}$  high going.
15.  $t_{ASC}$ ,  $t_{CAH}$  are referenced to the earlier  $\overline{\text{CAS}}$  falling edge.
16.  $t_{CP}$  is specified from the last  $\overline{\text{CAS}}$  rising edge in the previous cycle to the first  $\overline{\text{CAS}}$  falling edge in the next cycle.
17.  $t_{CWD}$  is referenced to the later  $\overline{\text{CAS}}$  falling edge at word read-modify-write cycle.
18.  $t_{CWL}$  is specified from  $\overline{\text{W}}$  falling edge to the earlier  $\overline{\text{CAS}}$  rising edge.
19.  $t_{CSR}$  is referenced to earlier  $\overline{\text{CAS}}$  falling low before  $\overline{\text{RAS}}$  transition low.
20.  $t_{CHR}$  is referenced to the later  $\overline{\text{CAS}}$  rising high after  $\overline{\text{RAS}}$  transition low.
21.  $t_{DS}$ ,  $t_{DH}$  is independetly specified for lower byte  $D_{in(1-8)}$ , upper byte  $D_{in(9-16)}$

**TIMING DIAGRAM**  
**WORD READ CYCLE**

NOTE : D<sub>IN</sub> = OPEN

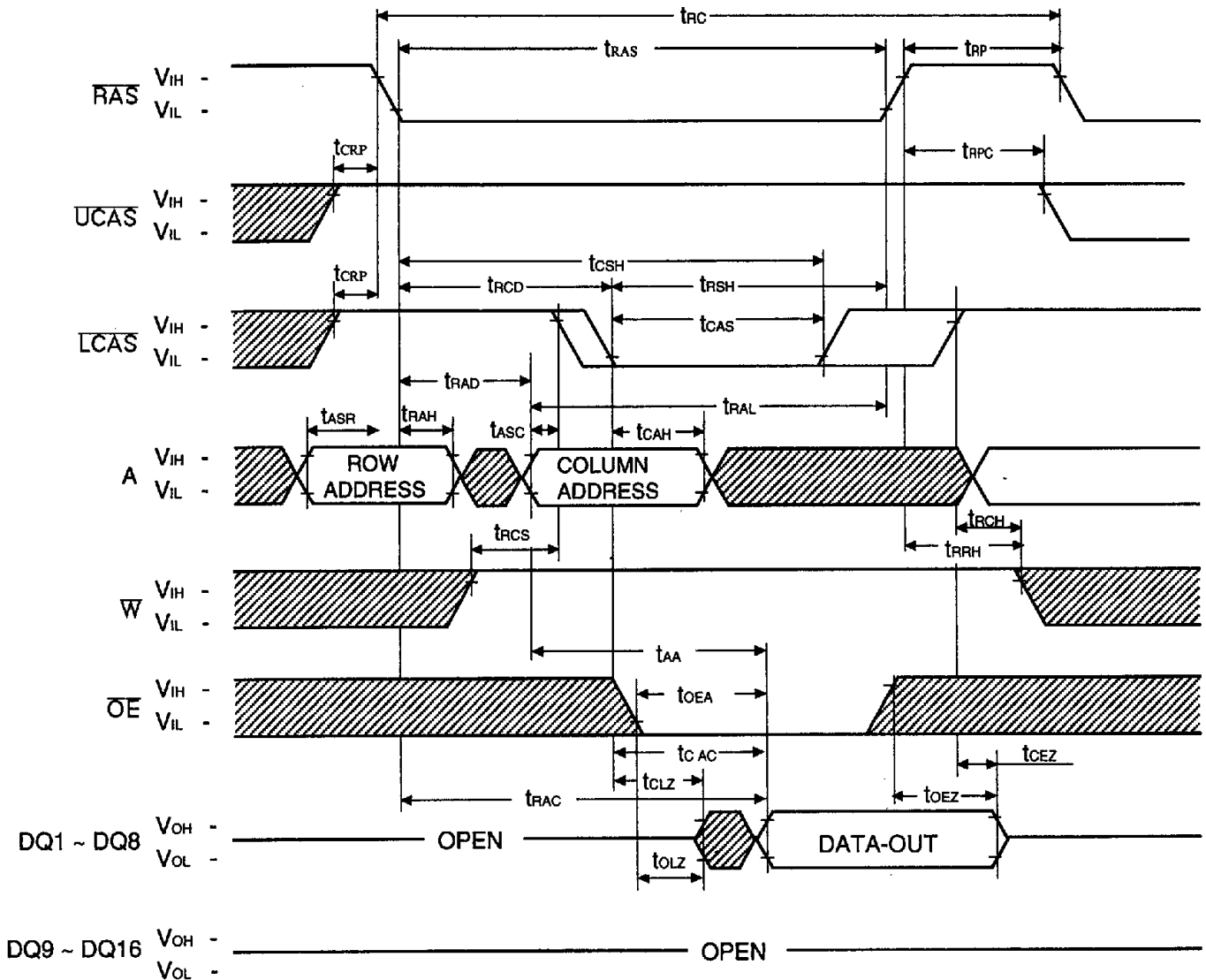


 Don't Care



**TIMING DIAGRAM**  
**LOWER BYTE READ CYCLE**

NOTE :  $D_{IN} = OPEN$

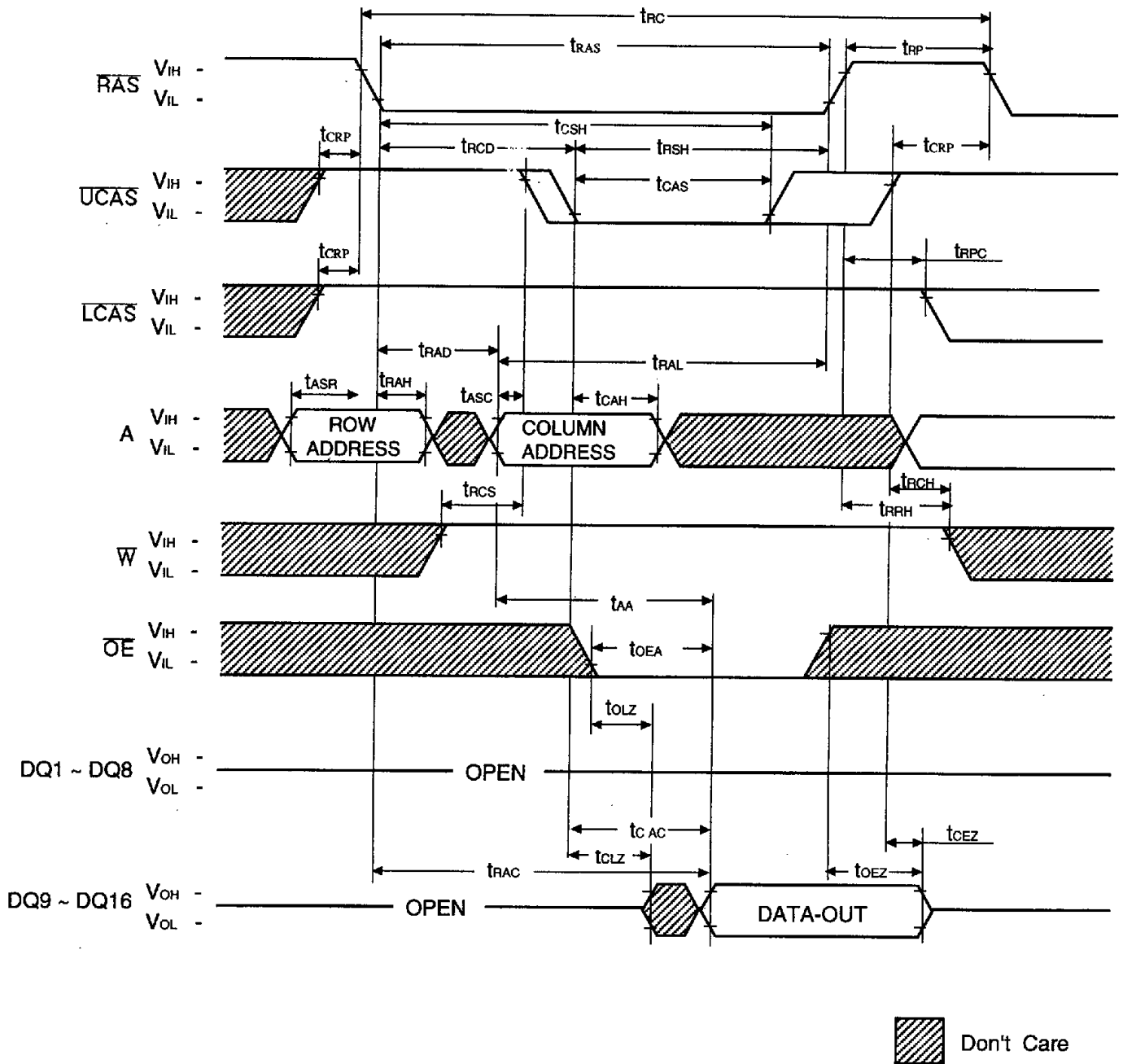


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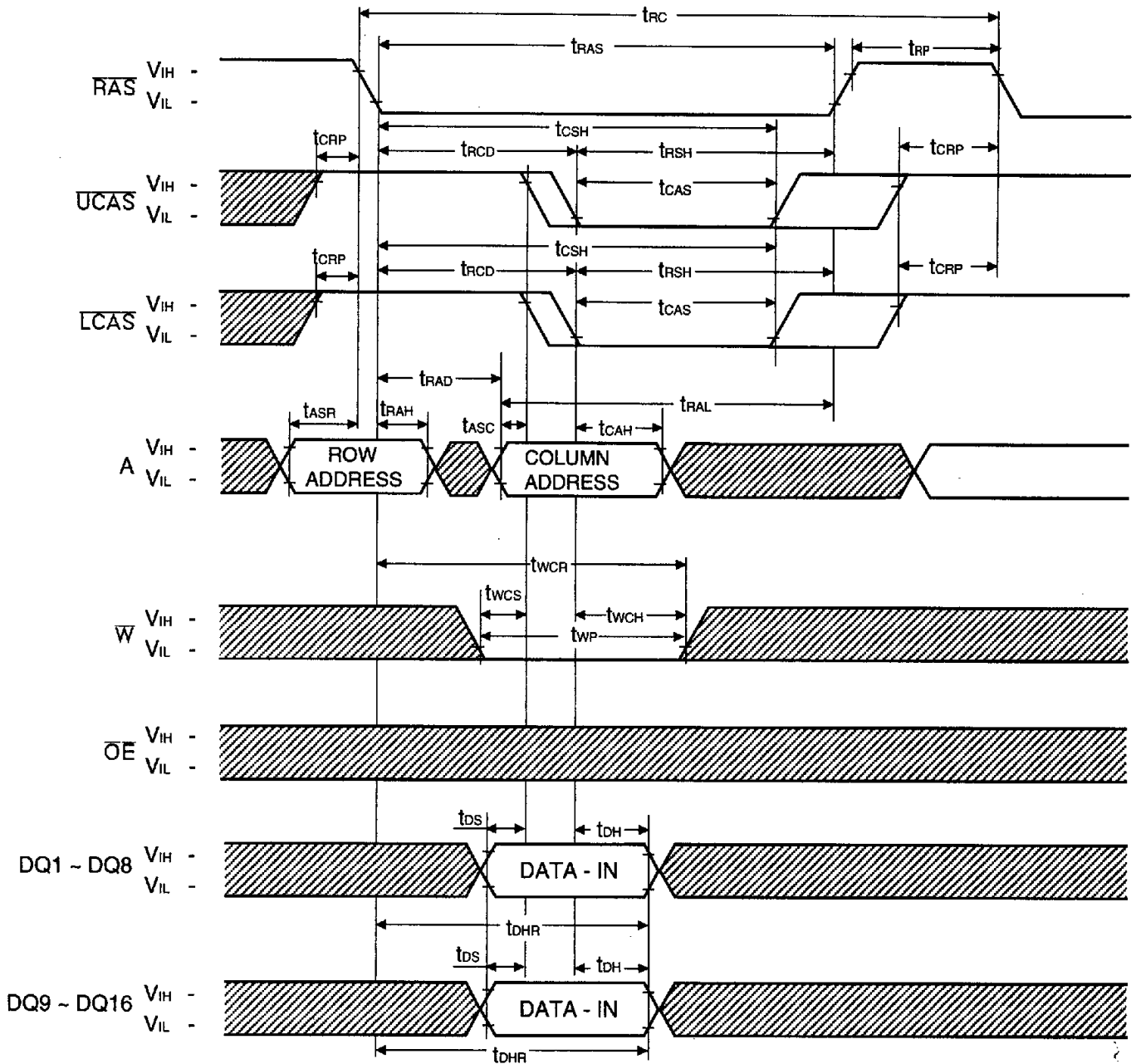
**TIMING DIAGRAM**  
**UPPER BYTE READ CYCLE**

NOTE : DIN = OPEN



**WORD WRITE CYCLE (EARLY WRITE)**

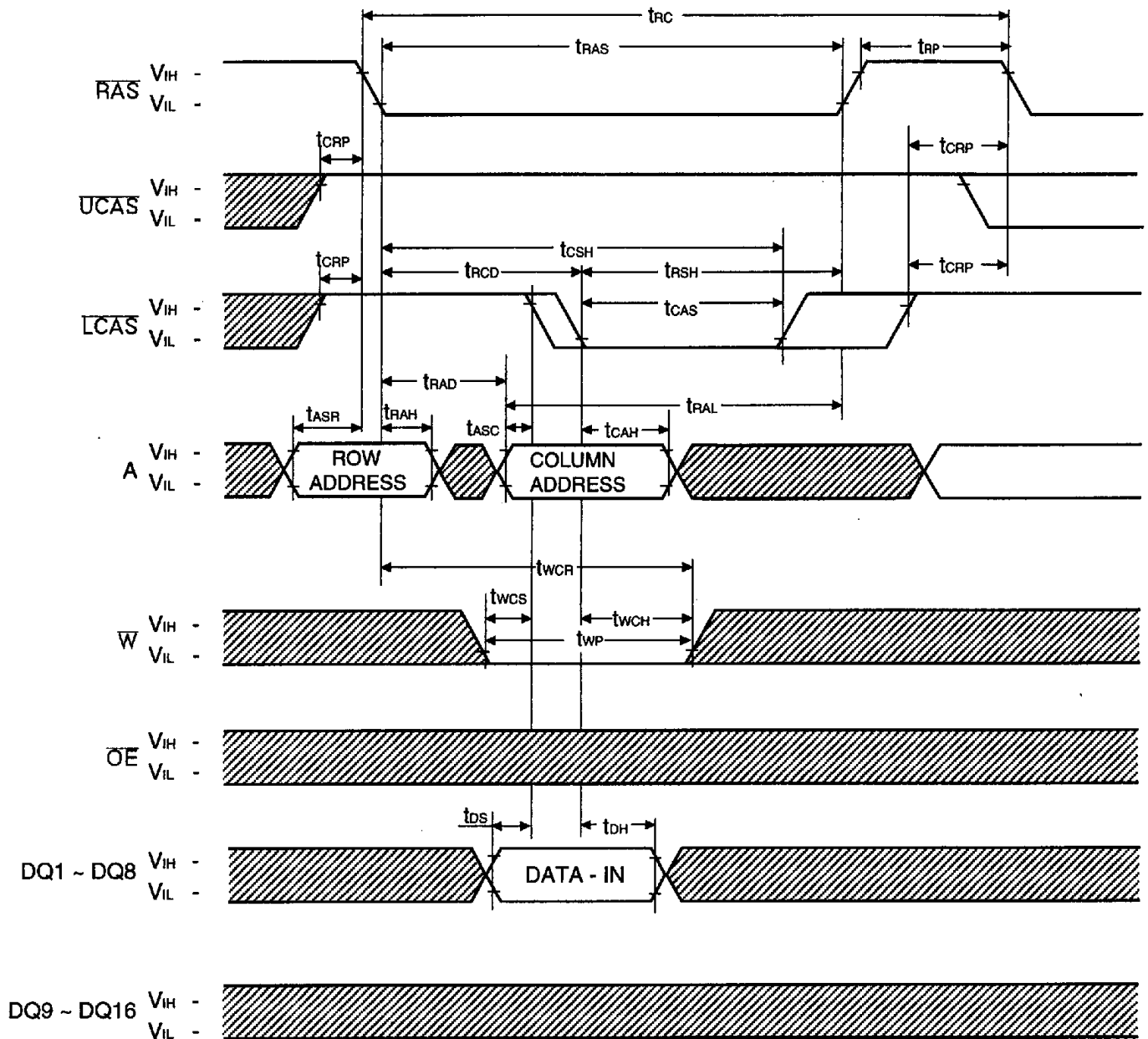
NOTE : D<sub>OUT</sub> = OPEN



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LOWER BYTE WRITE CYCLE (EARLY WRITE)

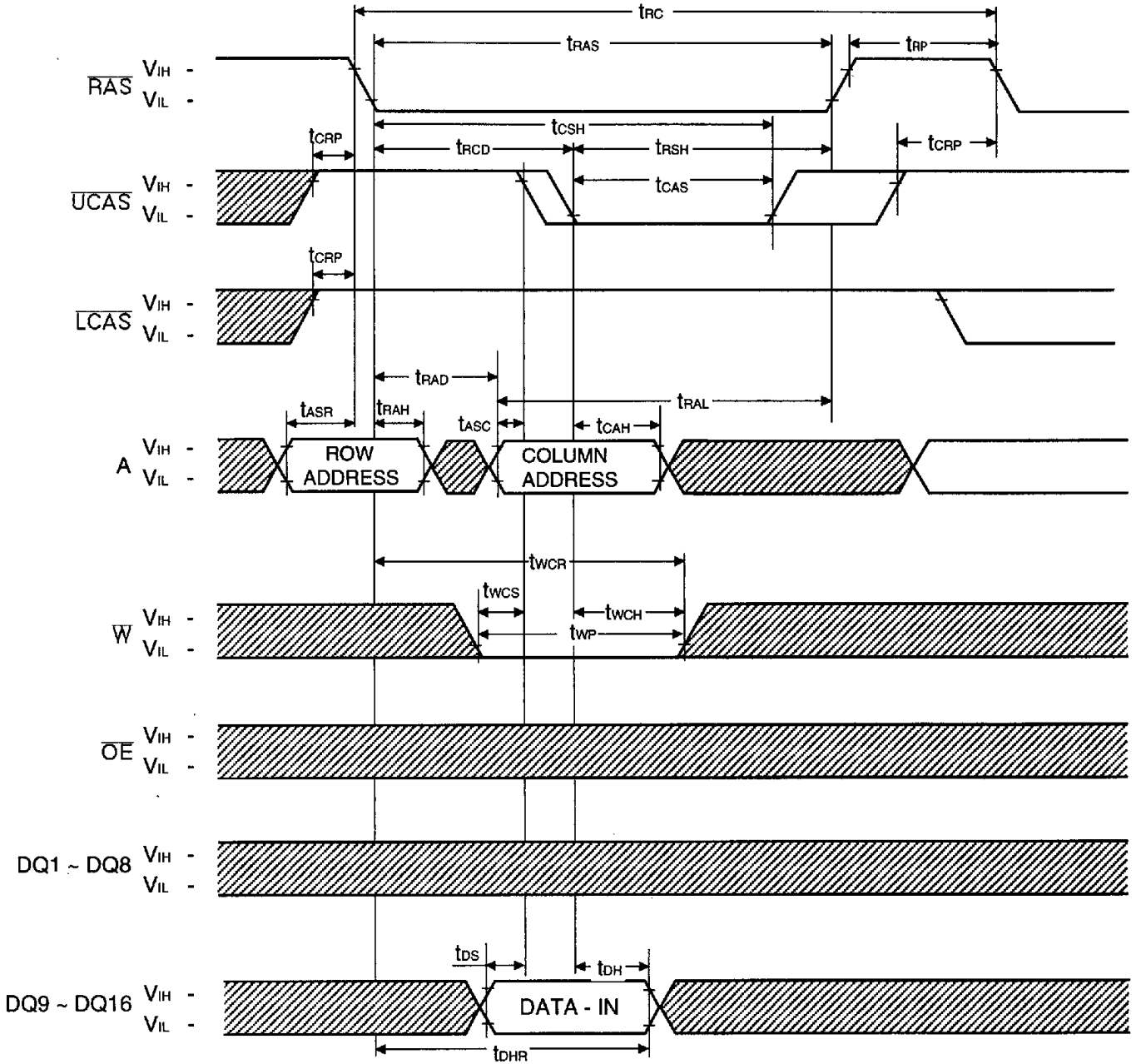
NOTE : DOUT = OPEN



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UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D<sub>OUT</sub> = OPEN

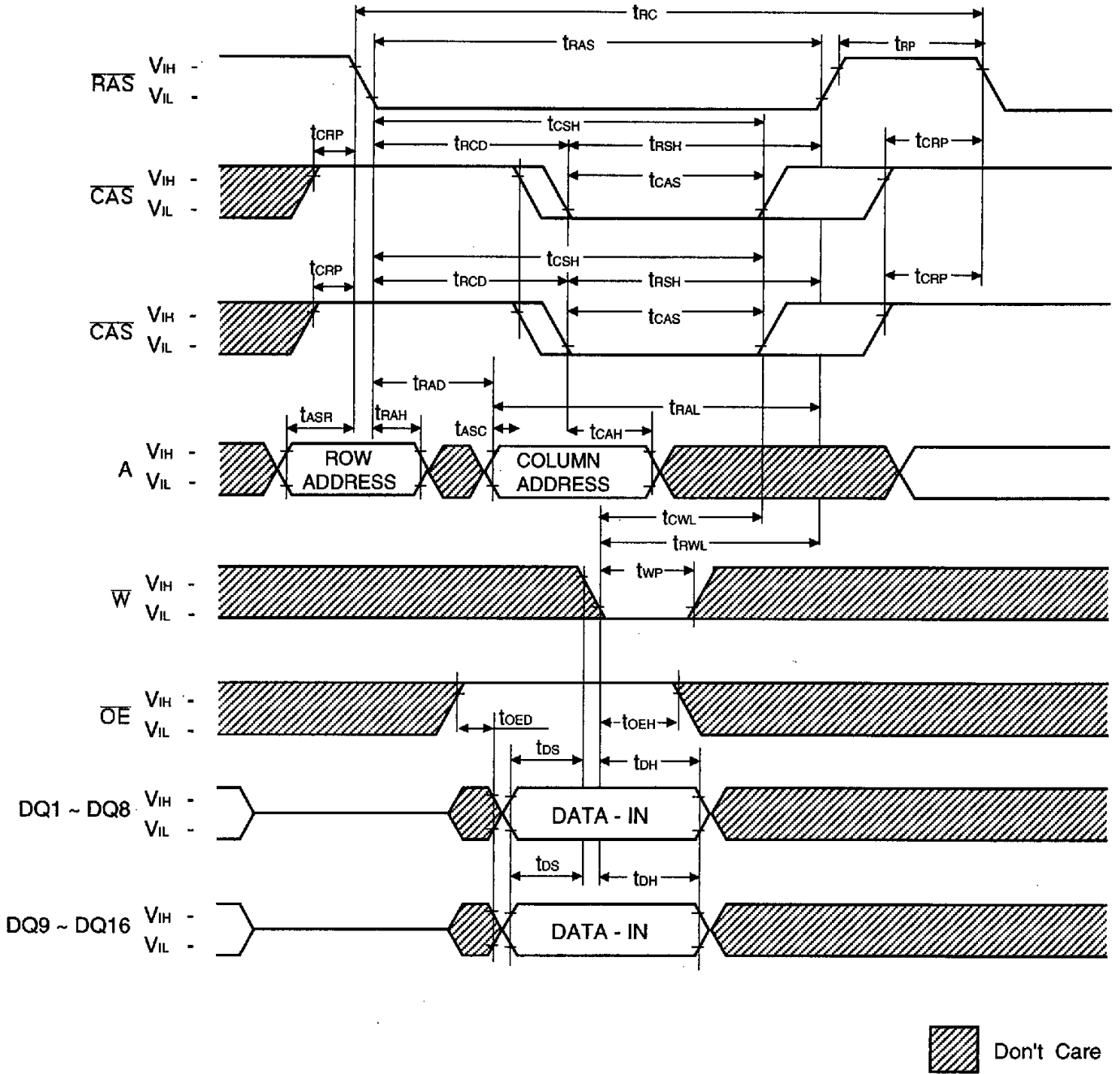


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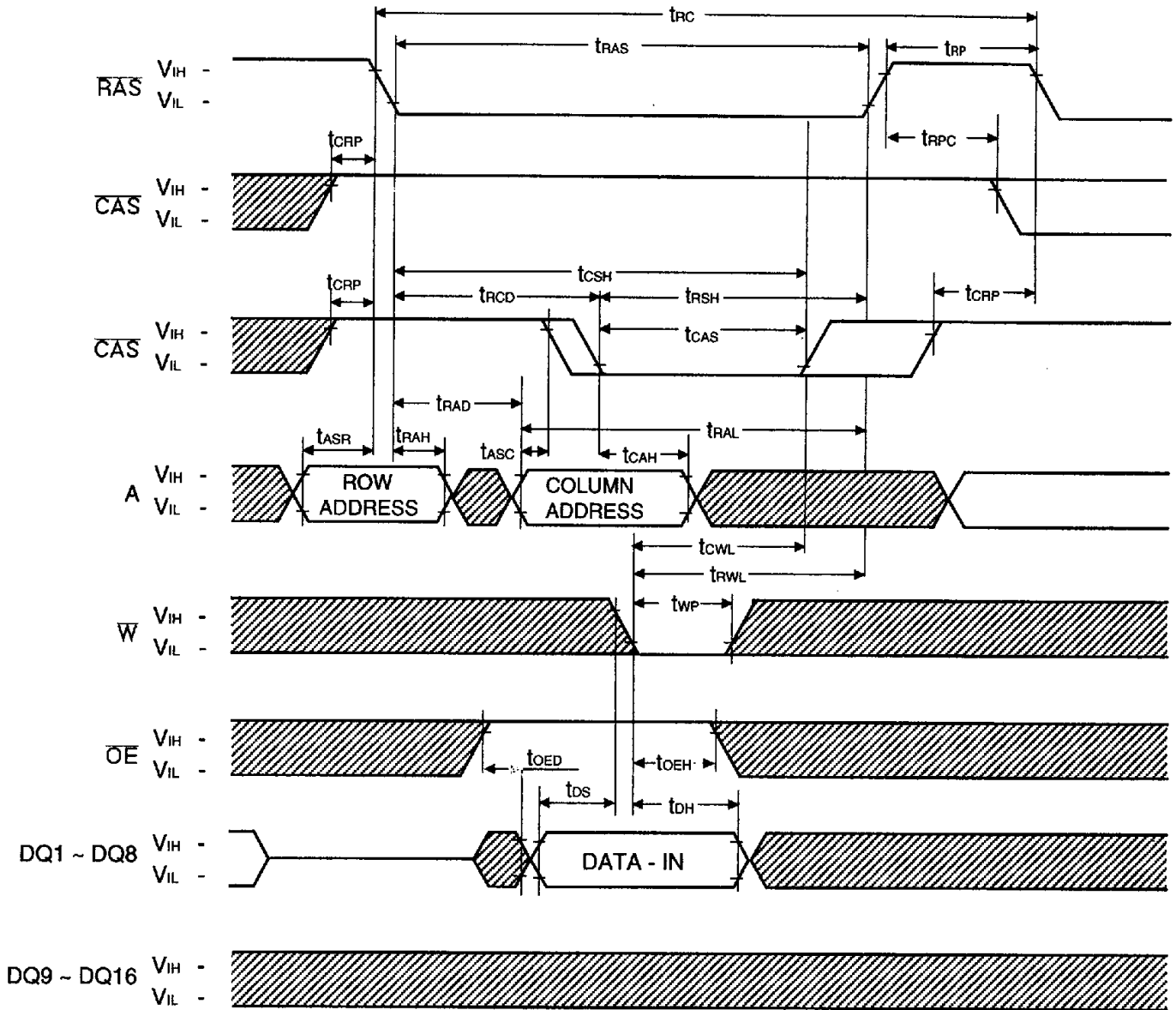
WORD WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)

NOTE : D<sub>OUT</sub> = OPEN



LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : Dout = OPEN

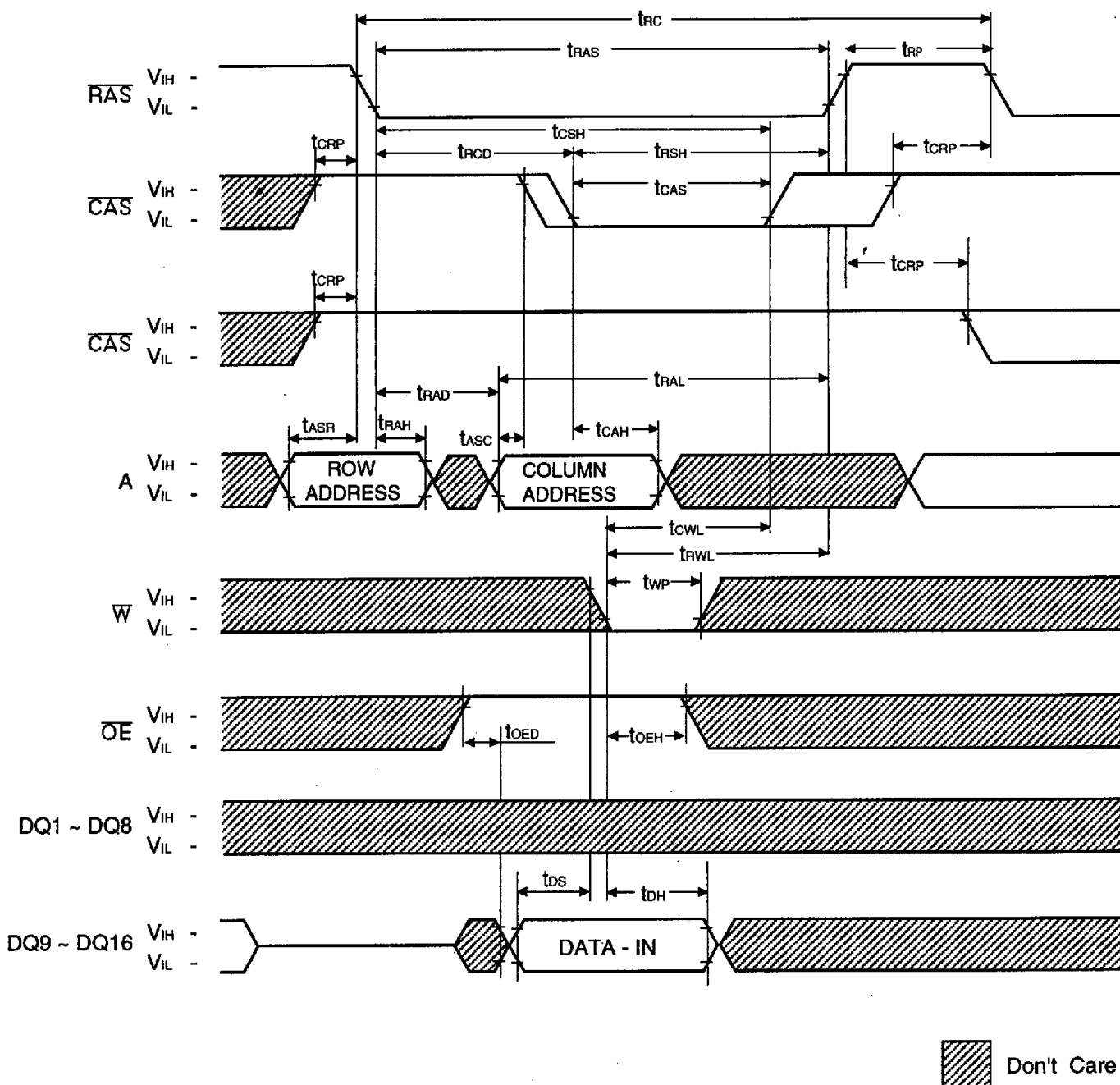


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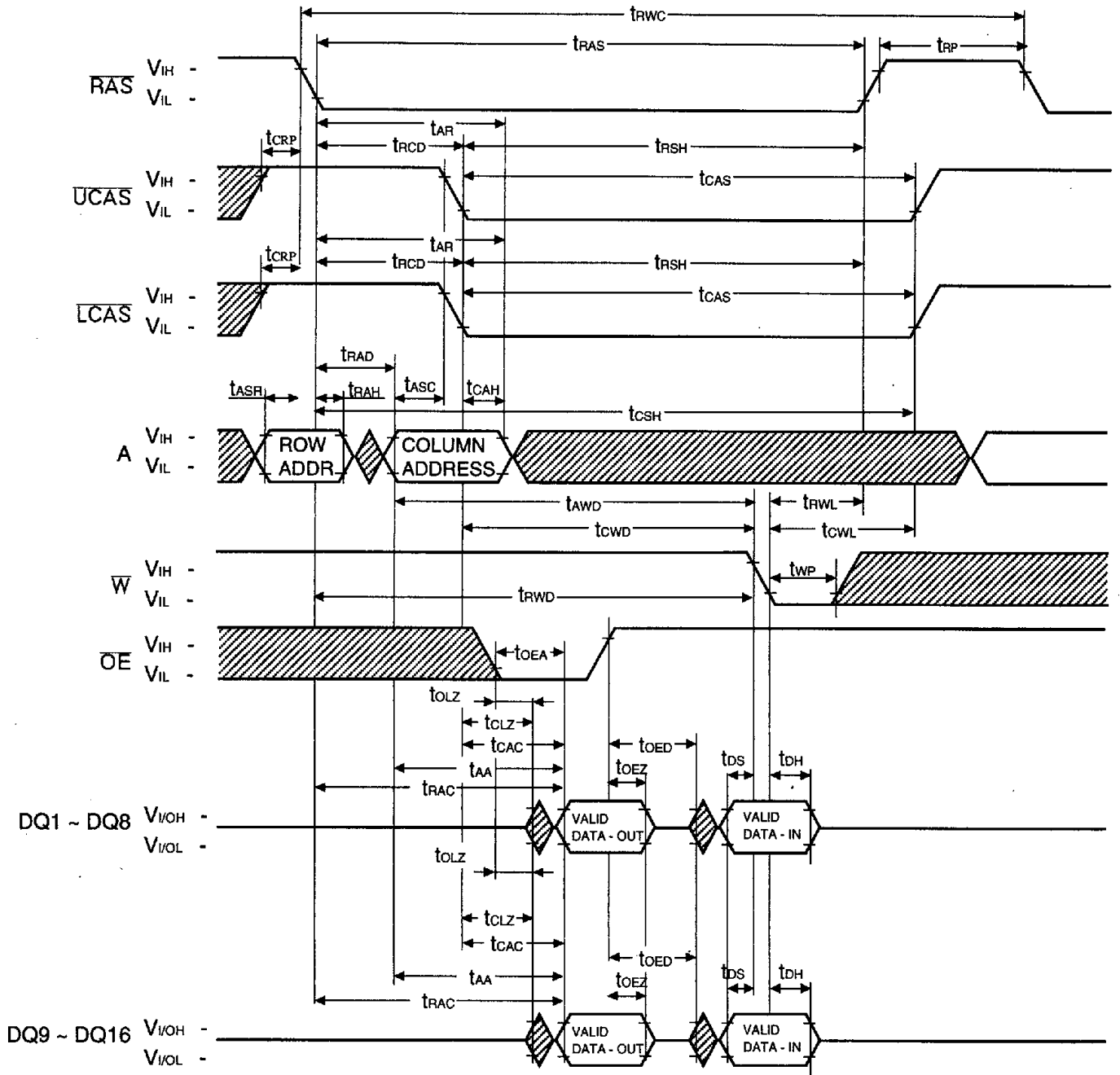
UPPER BYTE WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)

NOTE :  $D_{OUT}$  = OPEN





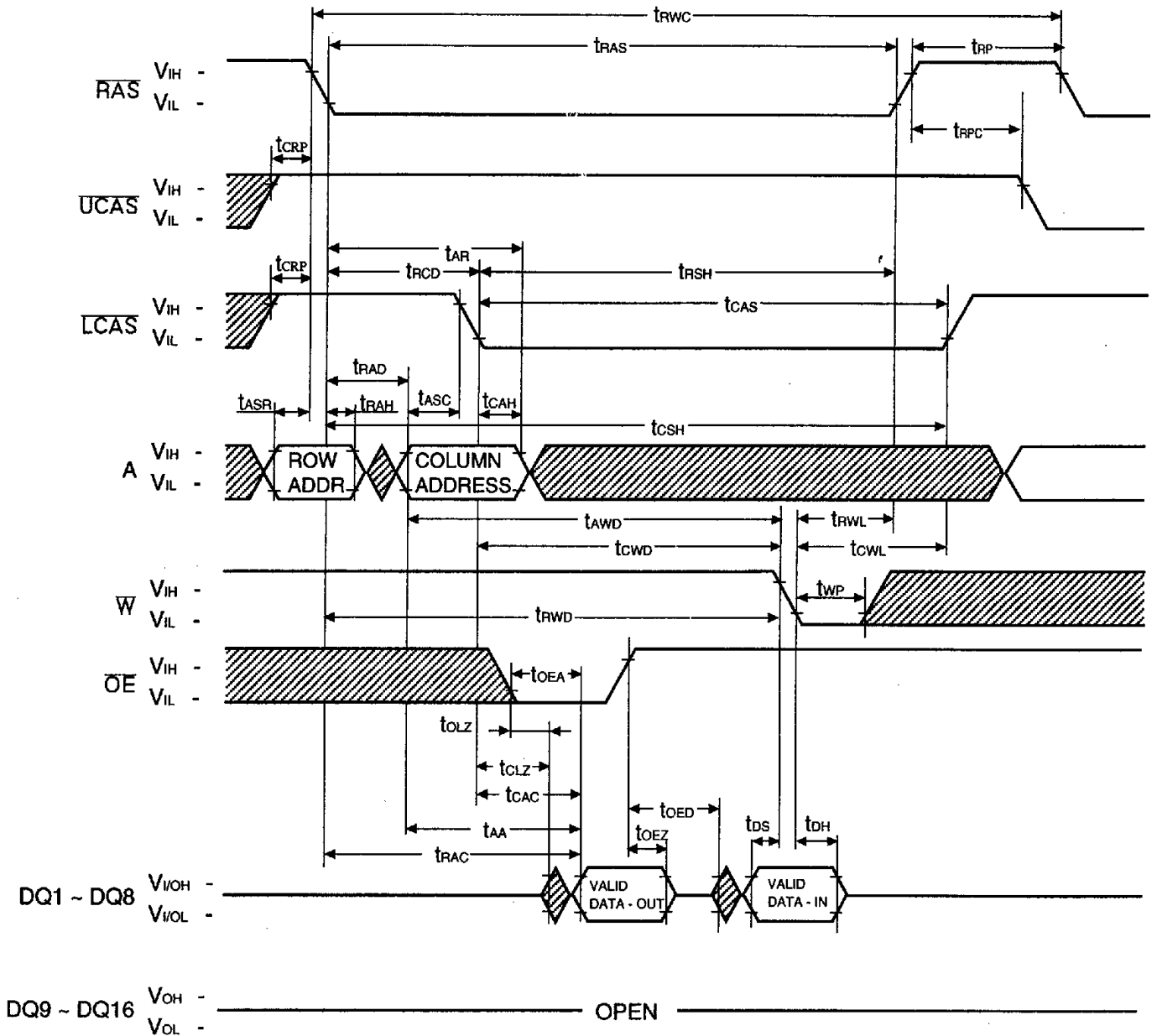
WORD READ - MODIFY - WRITE CYCLE



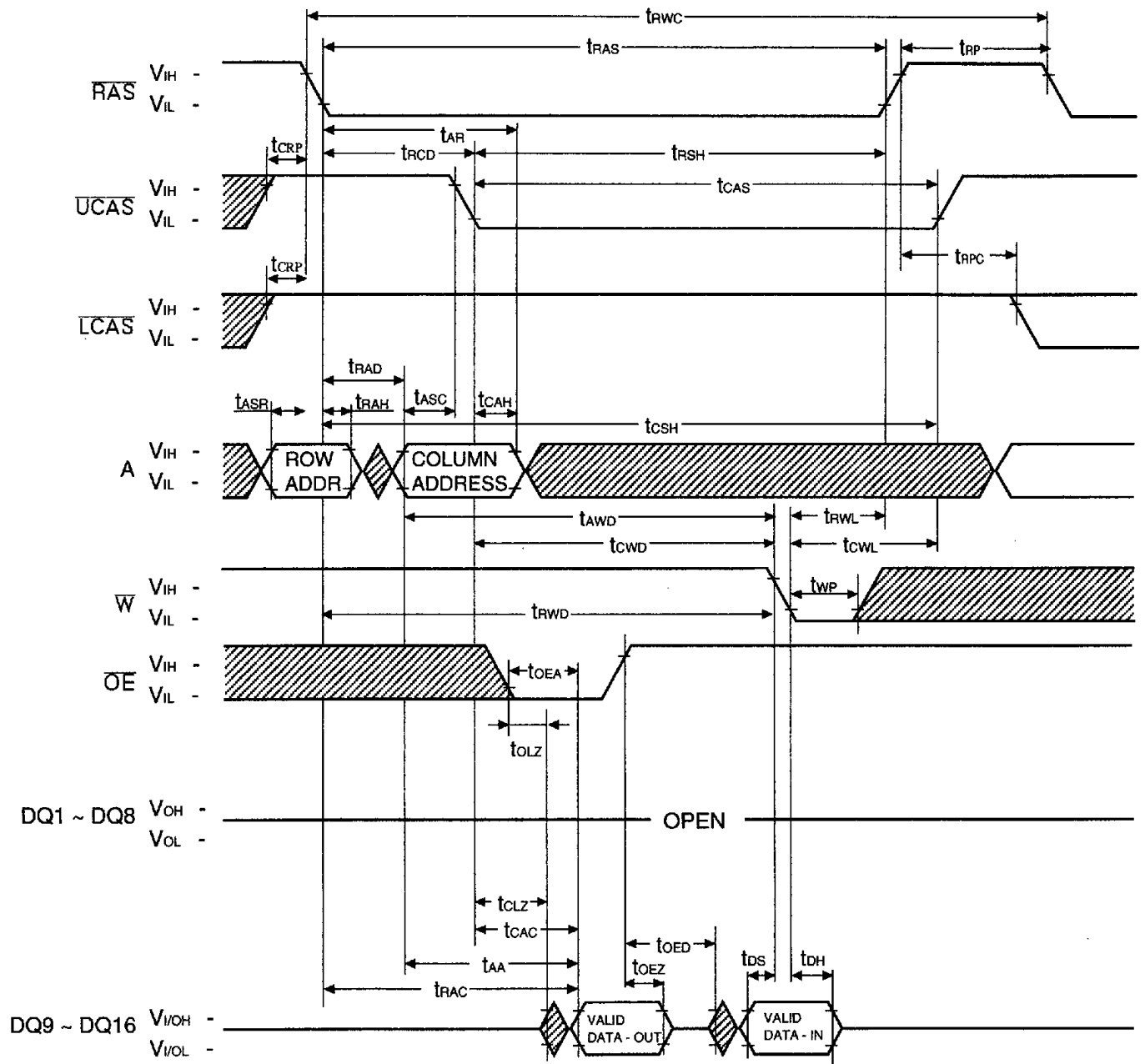
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LOWER-BYTE READ - MODIFY - WRITE CYCLE



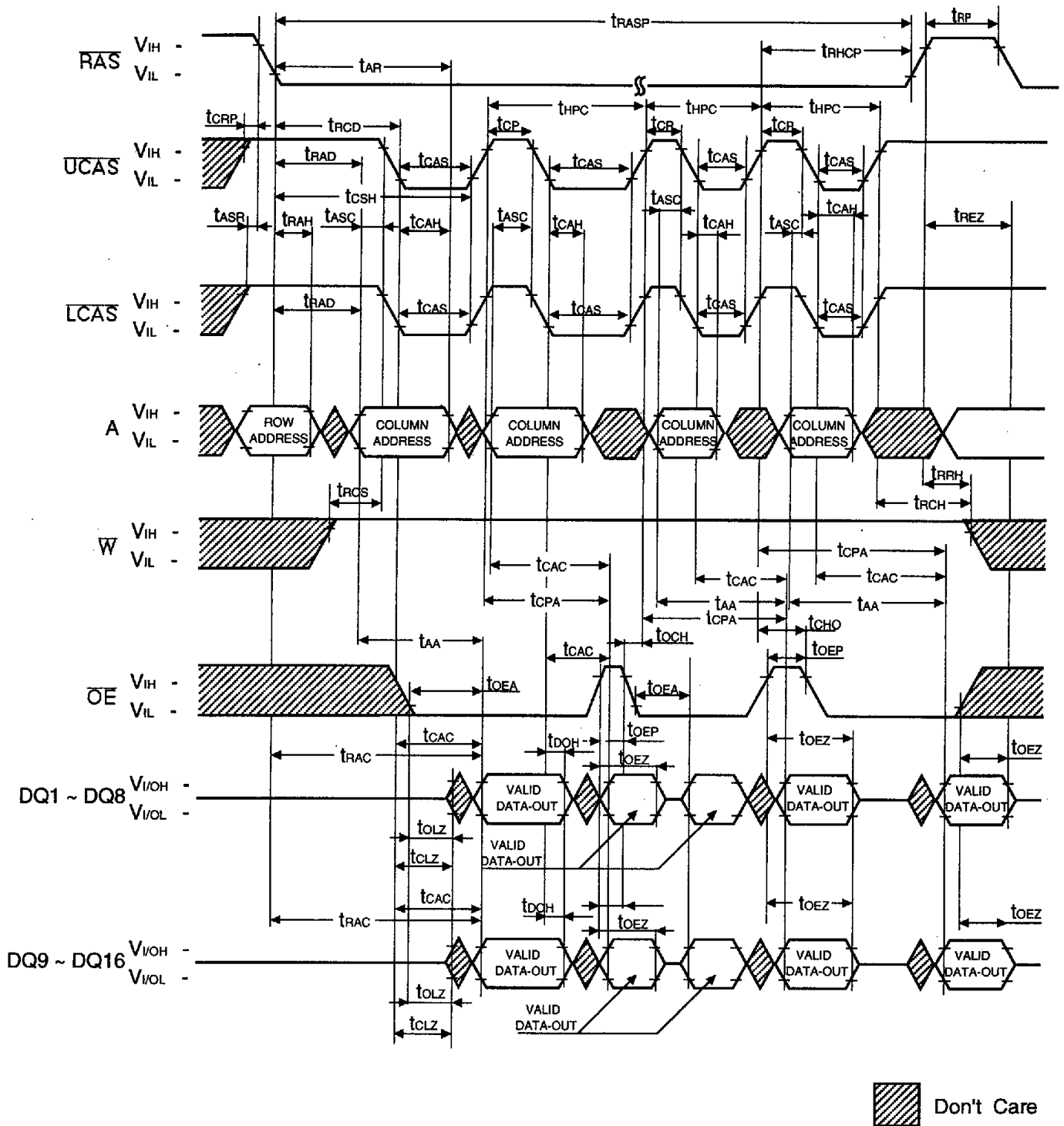
UPPER-BYTE READ - MODIFY - WRITE CYCLE



 Don't Care

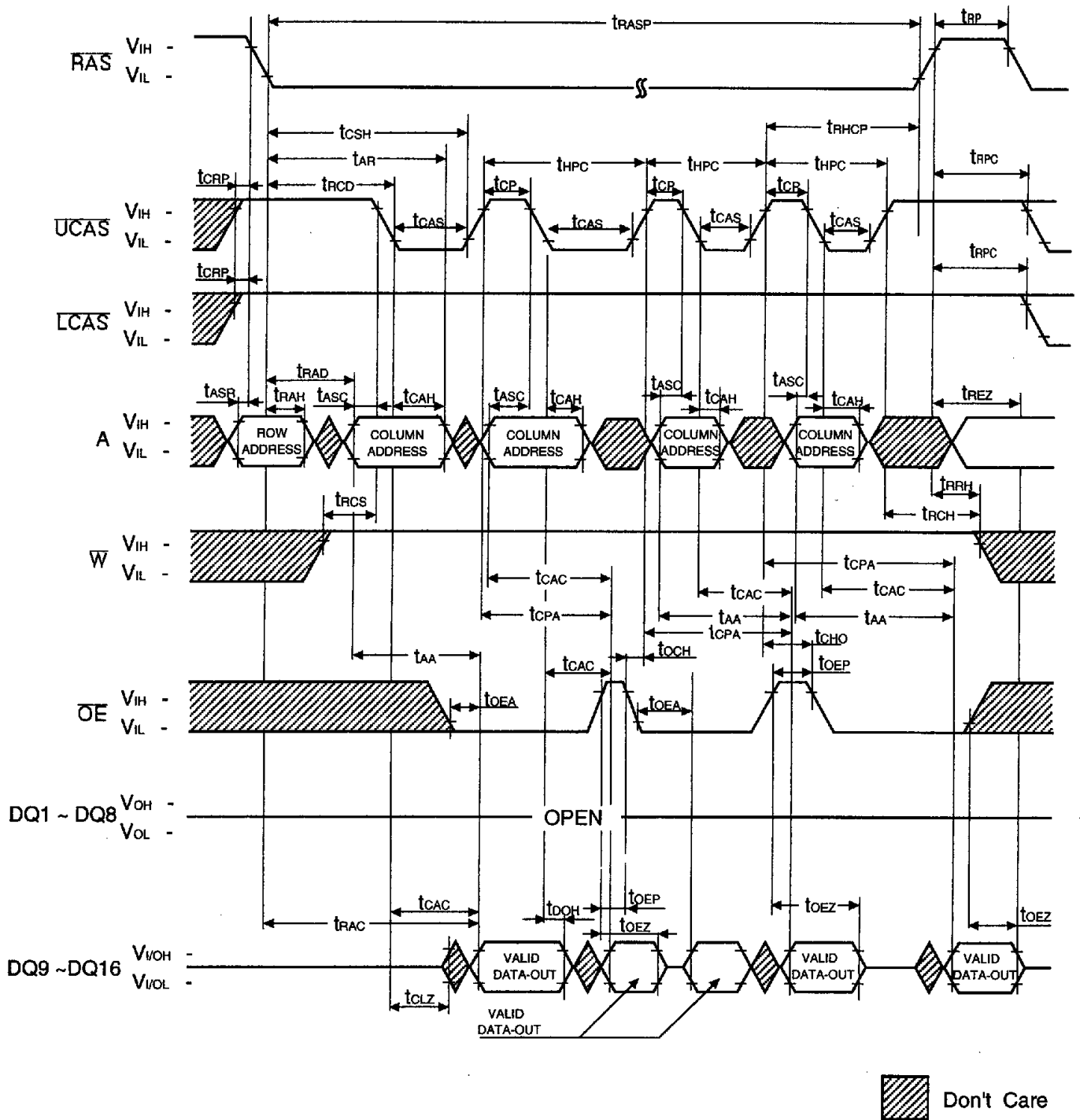
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HYPER PAGE MODE WORD READ CYCLE



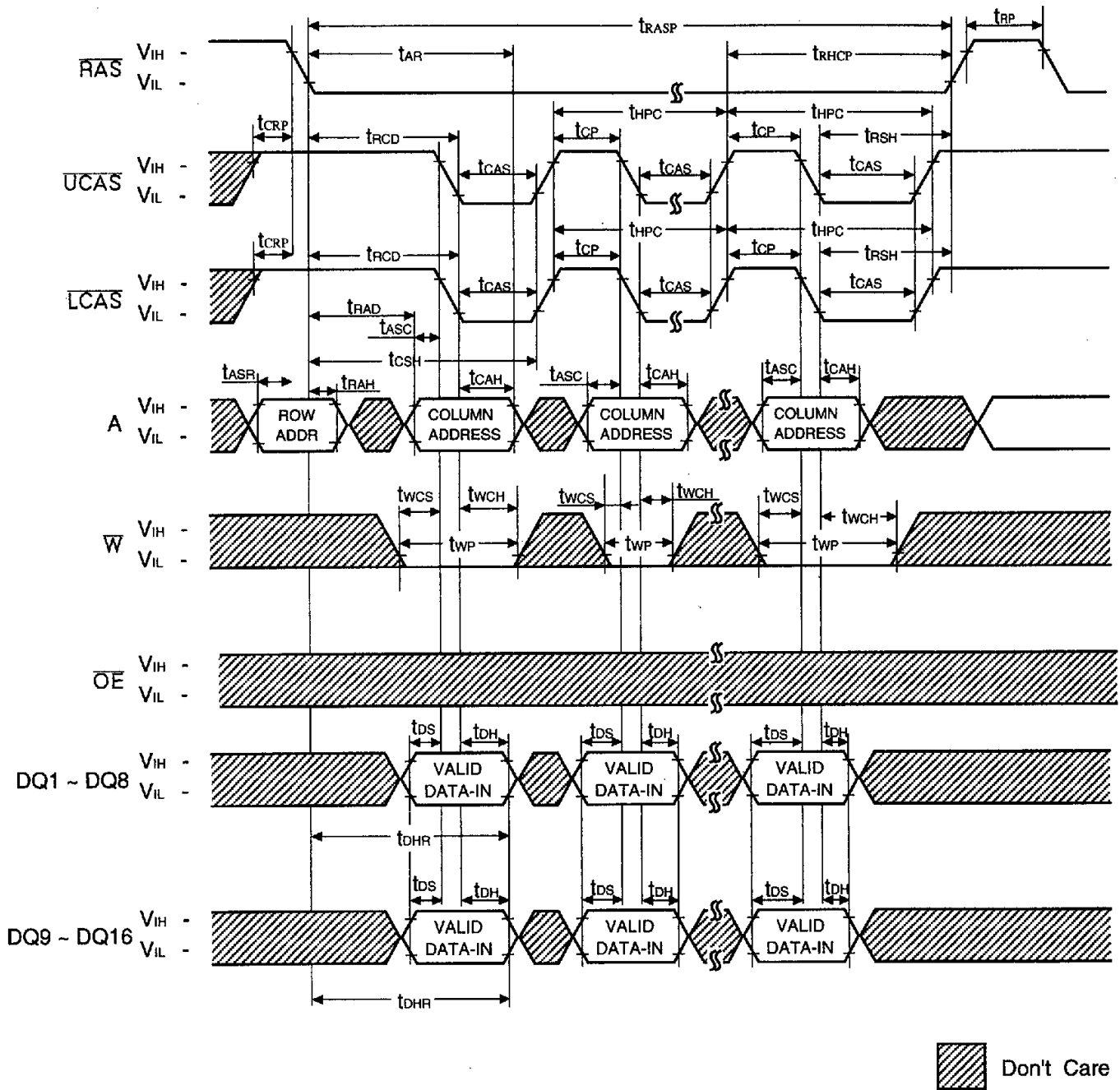


HYPER PAGE MODE UPPER BYTE READ CYCLE



HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

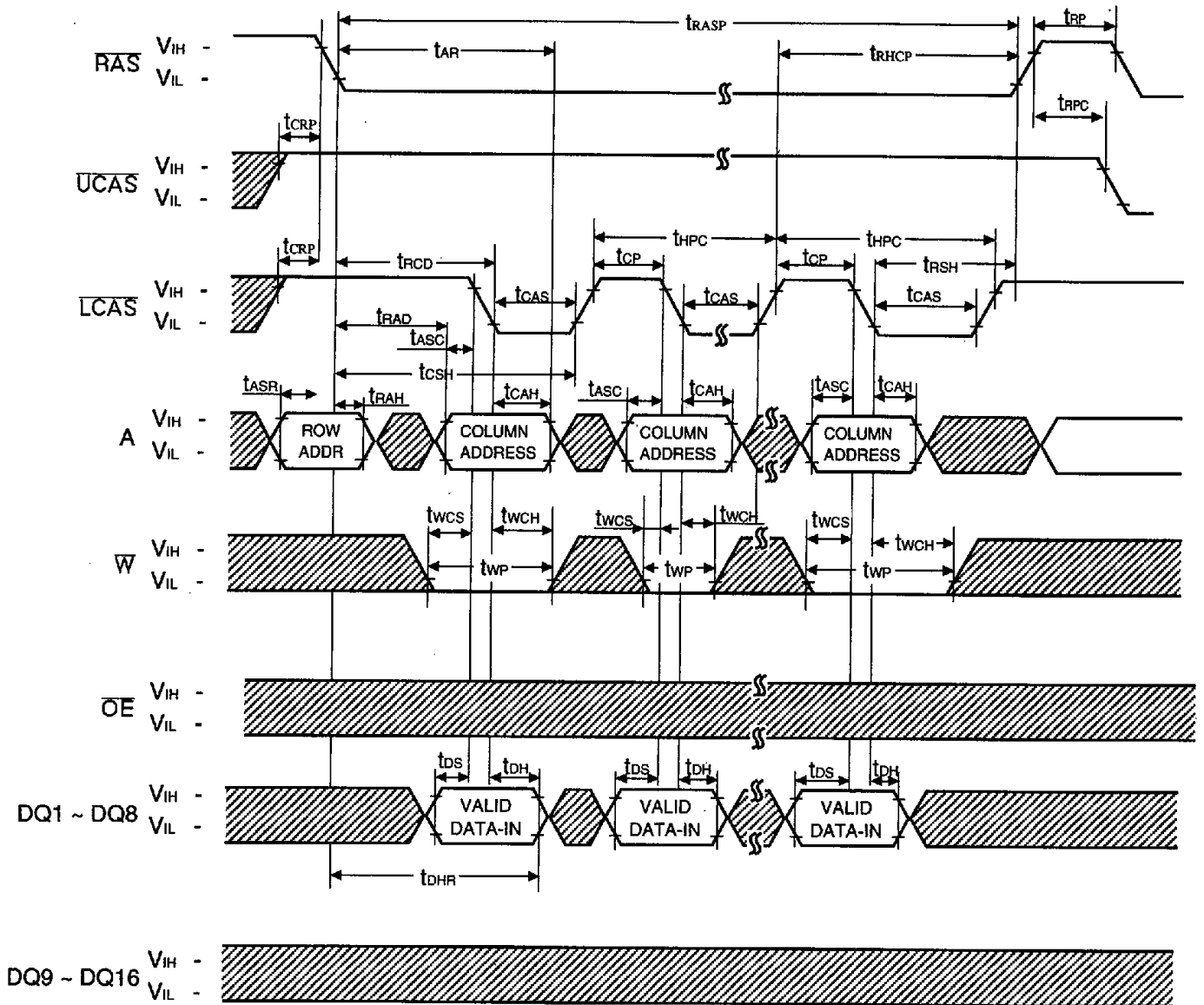
NOTE : Dout = Open



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**HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)**

NOTE : Dout = Open

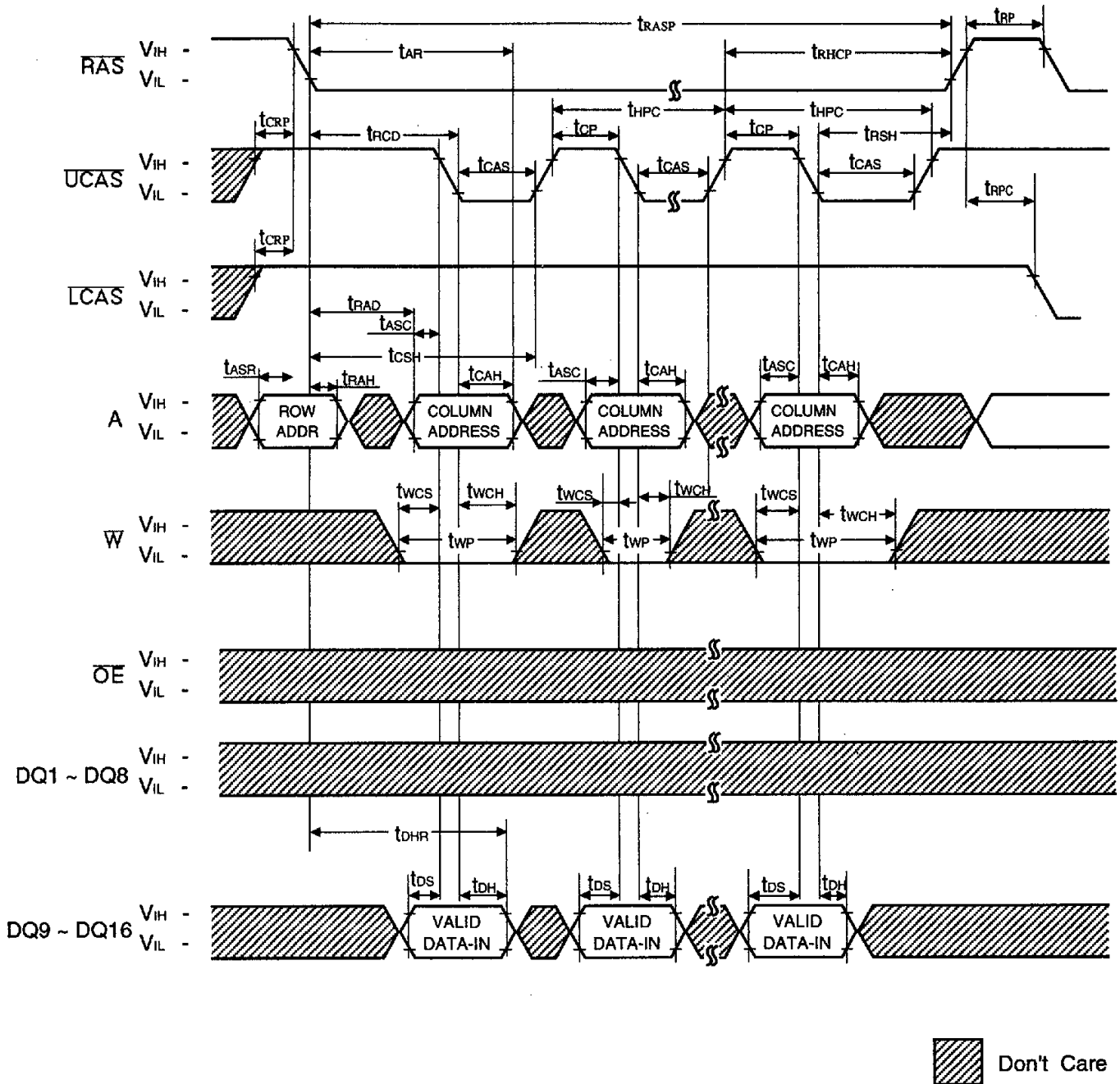


 Don't Care



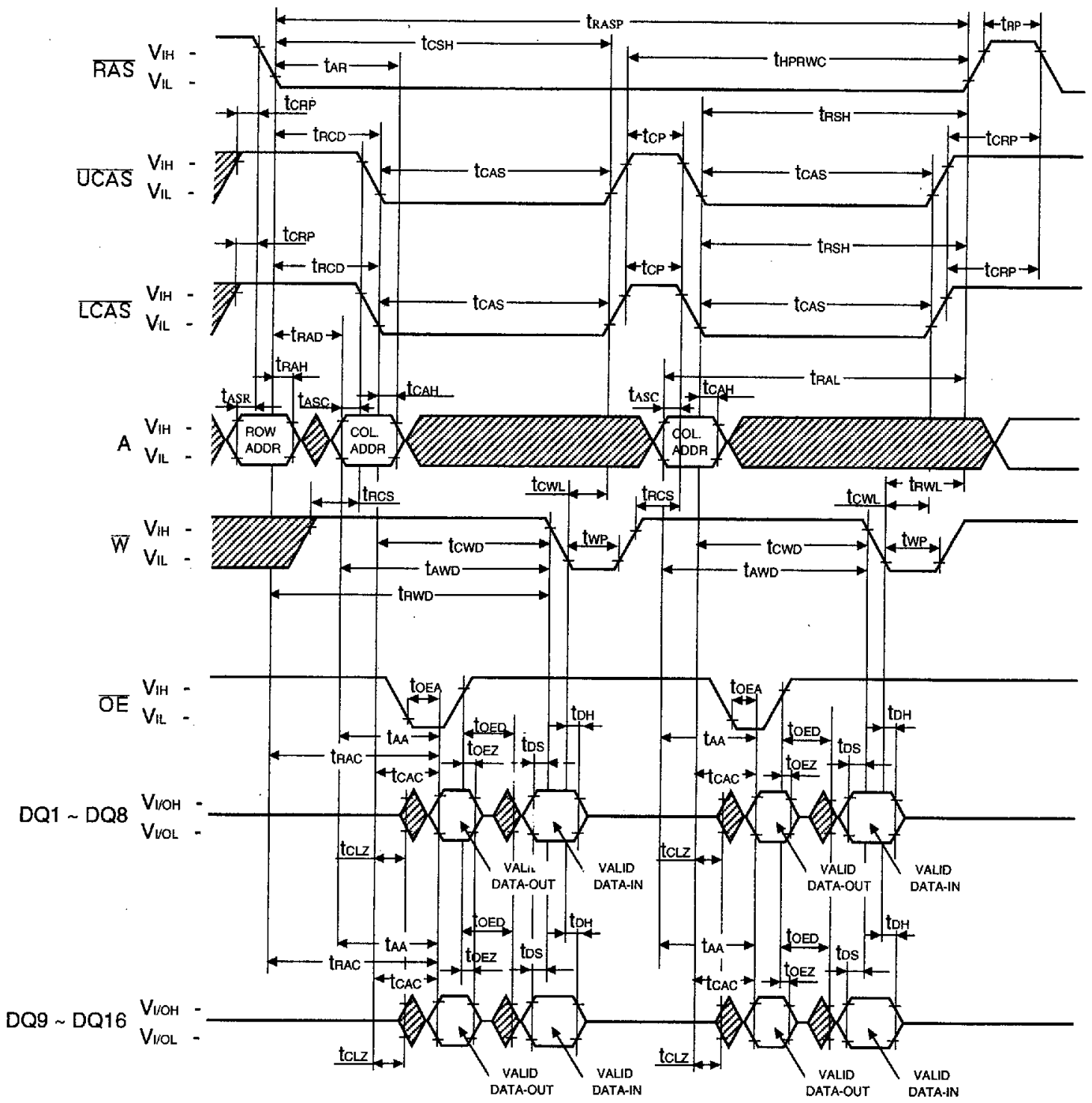
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : Dout = Open



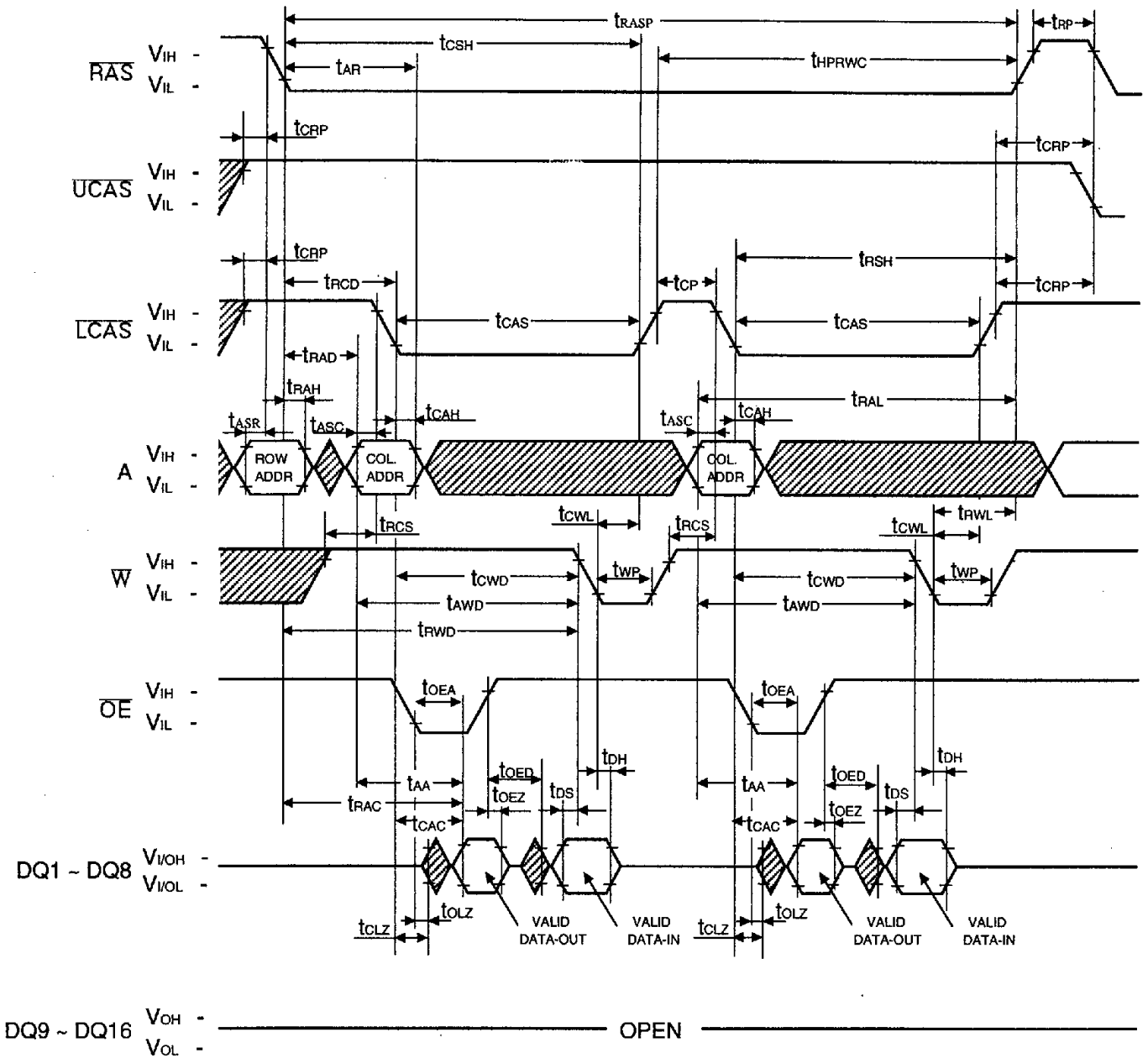
6

HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE




Don't Care

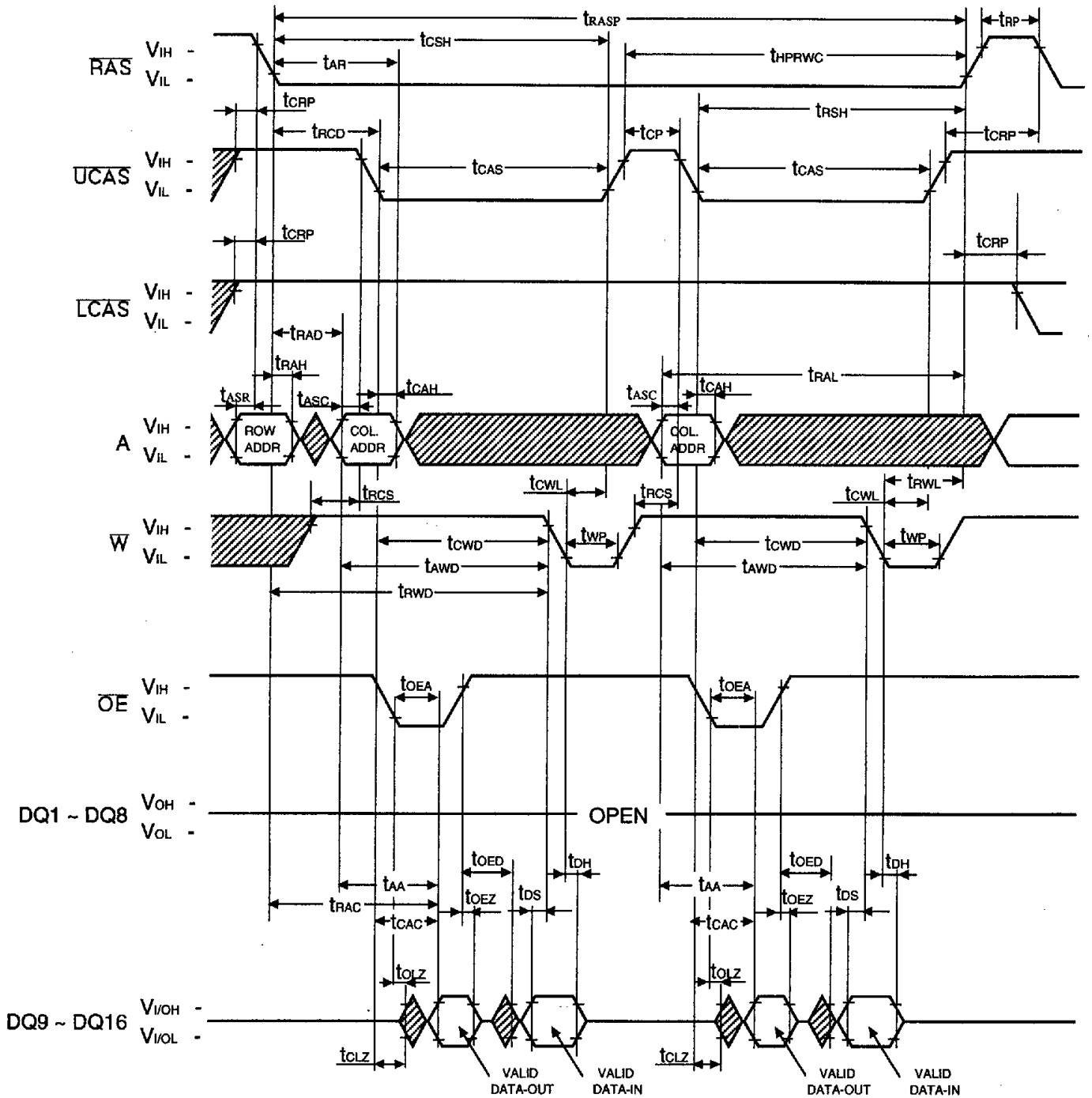
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



6

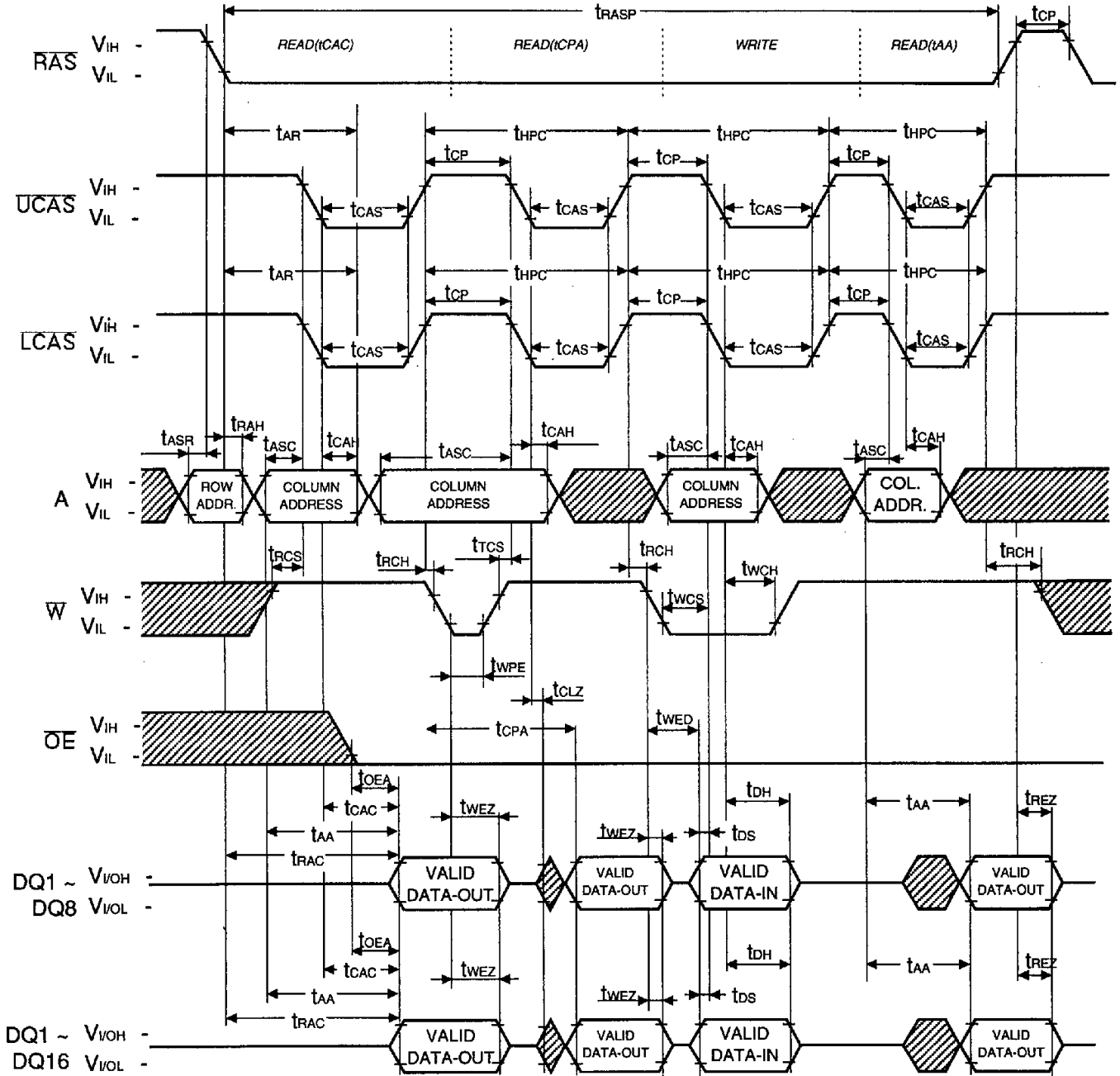
 Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



 Don't Care

HYPER PAGE READ AND WRITE MIXED CYCLE

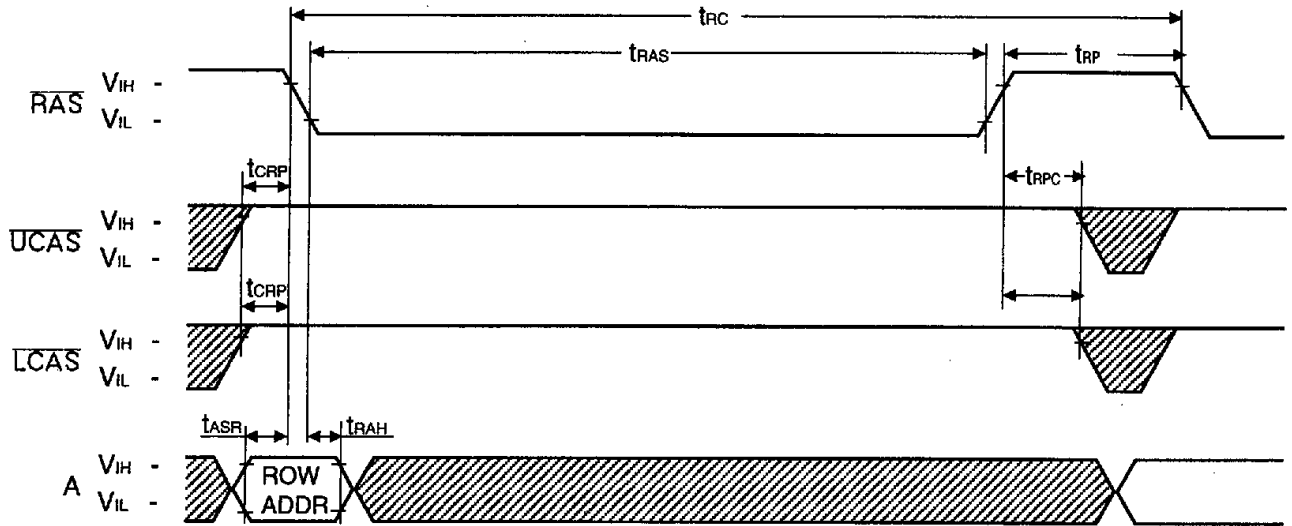


6

Don't Care

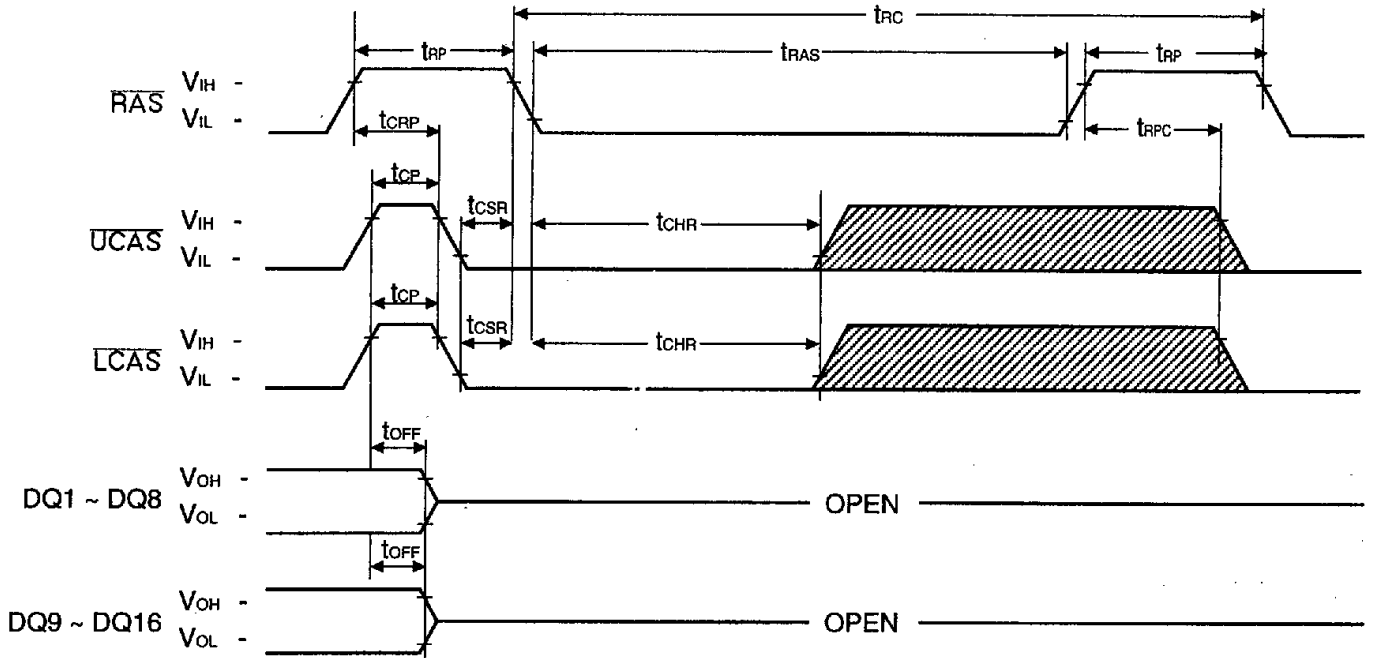
**RAS-ONLY REFRESH CYCLE**

NOTE :  $\bar{W}$ ,  $\bar{OE}$ ,  $D_{IN}$  = Don't care  
 $D_{OUT}$  = Open



**CAS-BEFORE-RAS REFRESH CYCLE**

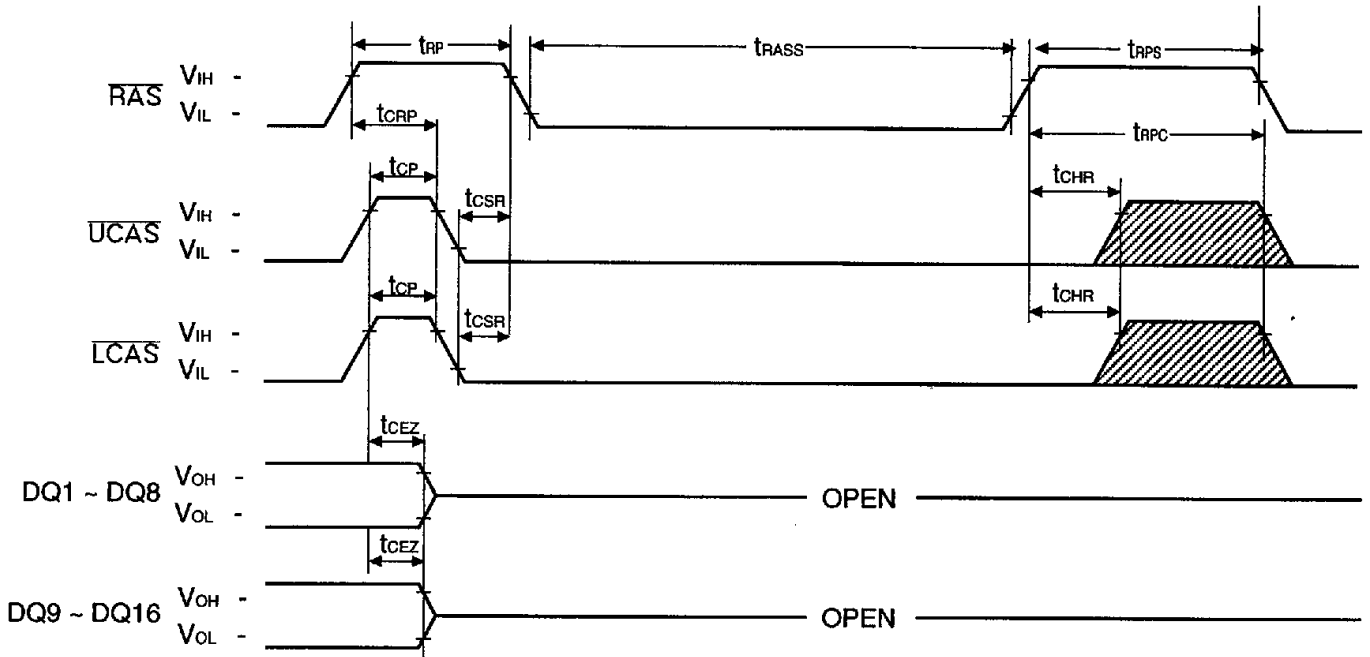
NOTE :  $\bar{W}$ ,  $\bar{OE}$ , A = Don't Care



 Don't Care

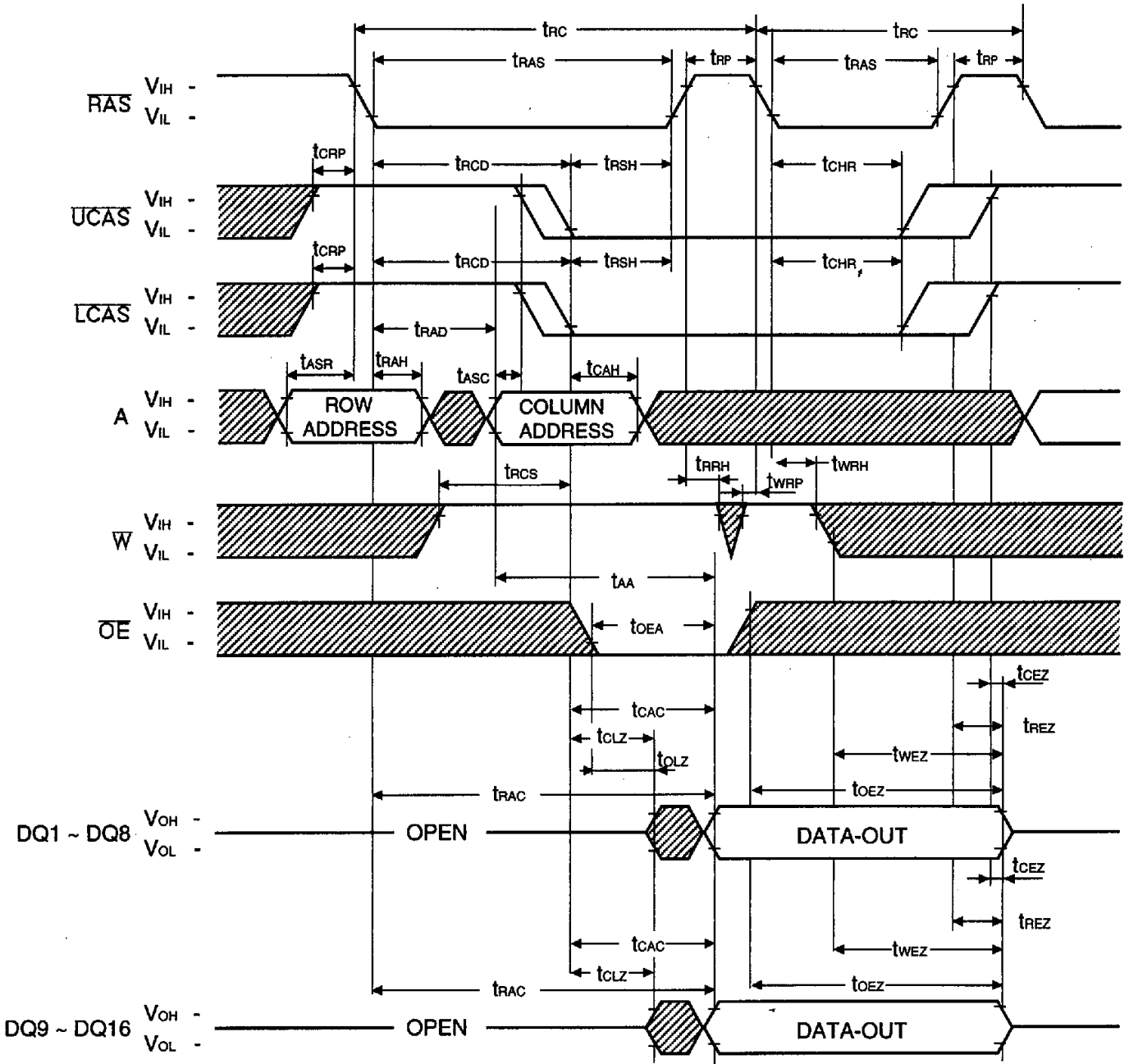
**CAS-BEFORE-RAS SELF REFRESH CYCLE(LL-version)**

NOTE :  $\overline{W}$ ,  $\overline{OE}$ , A = Don't Care



 Don't Care

HIDDEN REFRESH CYCLE ( READ )

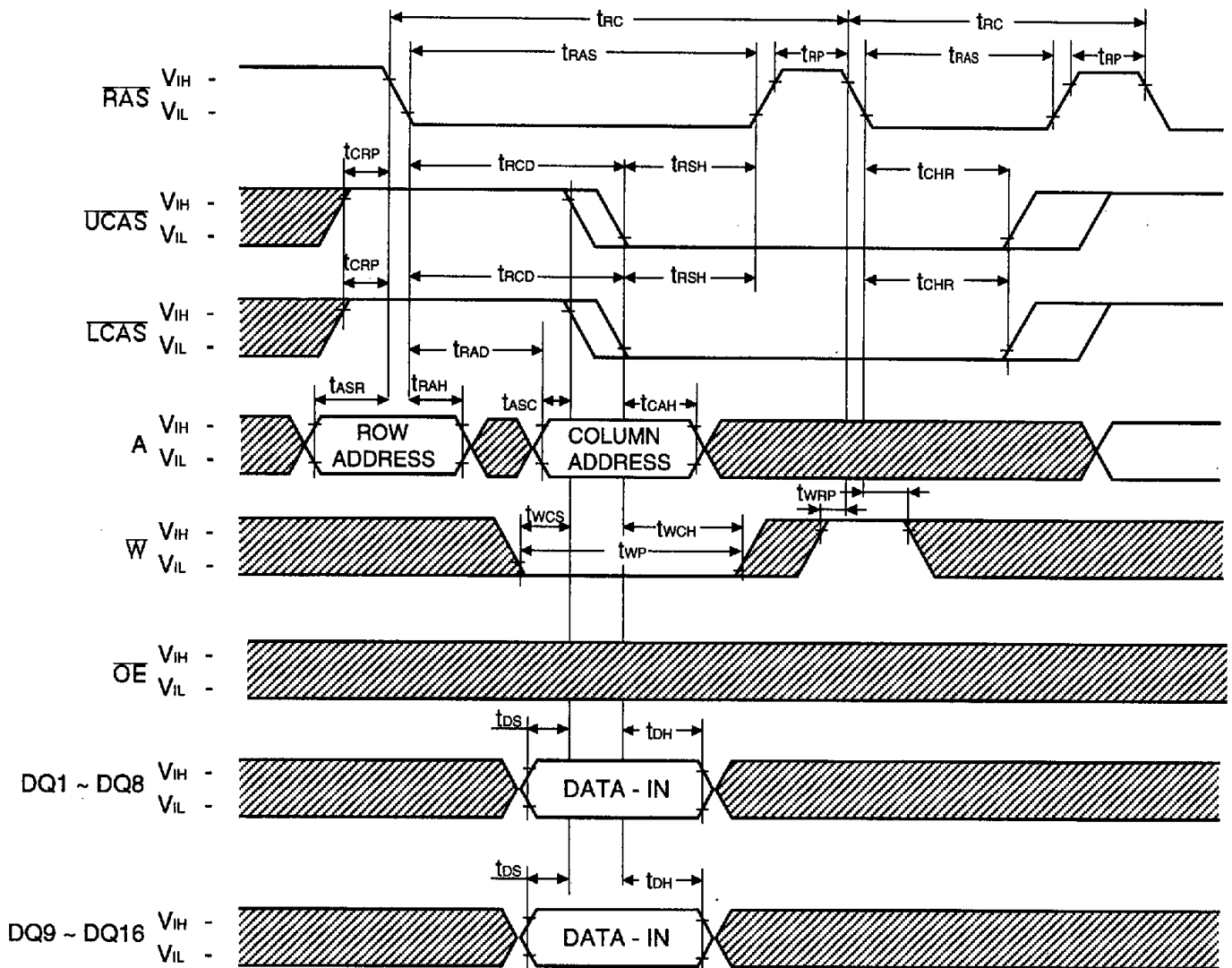


 Don't Care



HIDDEN REFRESH CYCLE (WRITE)

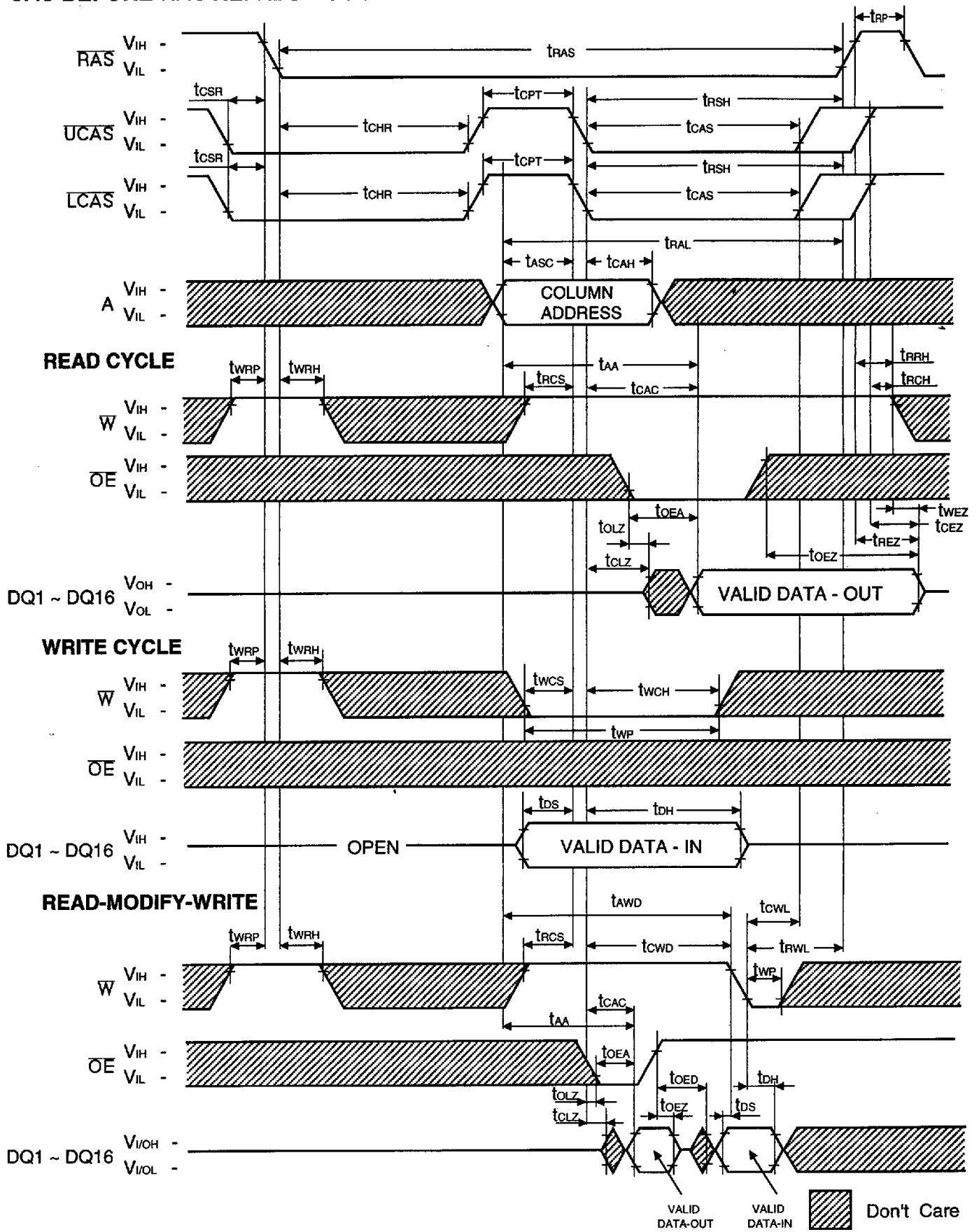
NOTE : D<sub>out</sub> = OPEN



 Don't Care

6

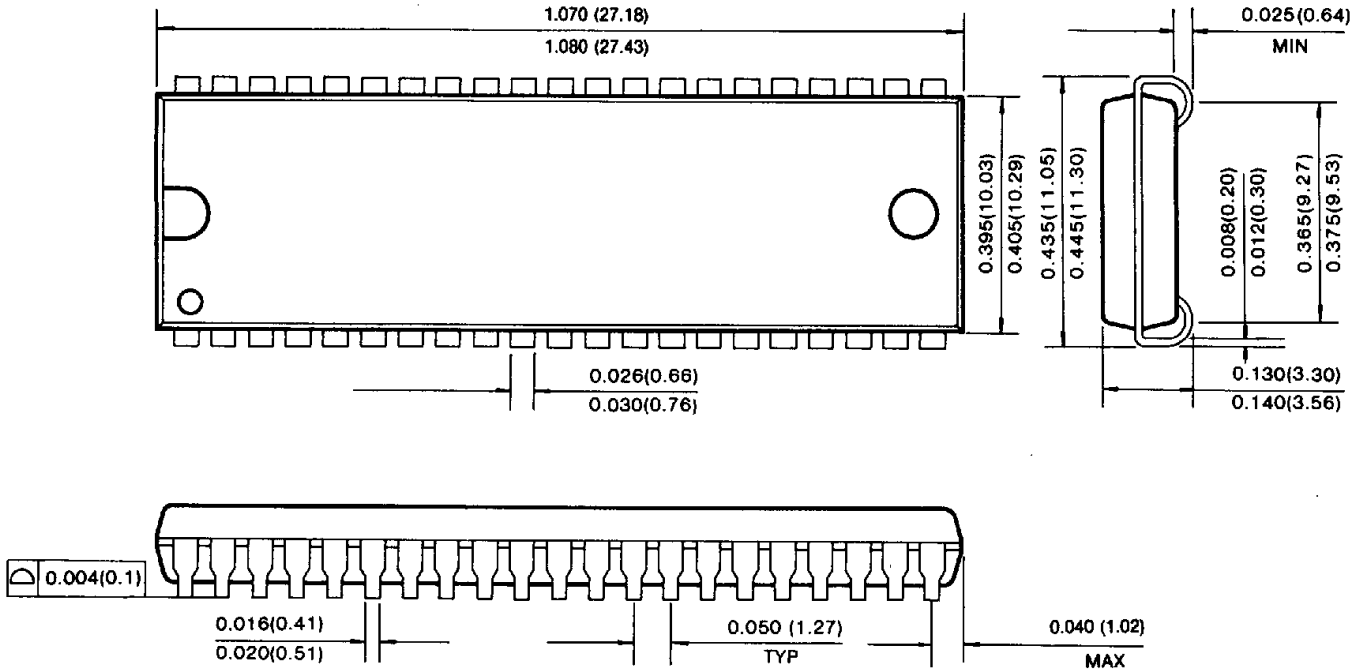
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

