SSD1810
SSD1810A

Advance Information

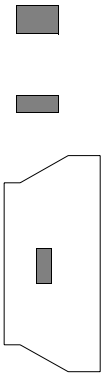
LCD Segment / Common Driver with Controller

CMOS

SSD1810 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It consists of 133 high voltage driving output pins supporting driving 98 Segments, 34 Commons and 1icon driving-Common or 100 Segments, 32 Commons and 1icon driving-Common.

SSD1810 displays data directly from its internal Graphic RAM (100x66). Data/ Command are sent from general MCU through a software selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD1810 embeds a DC-DC Converter, an On-chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1810 is suitable for any portable battery-driven application requiring long operation period and compact size.



Bare Die

Gold Bump Die

TAB

ORDERING INFORMATION

SSD1810V	Bare Die
SSD1810AZ	Gold BumpDie
SSD1810ATR1	TAB

- 98x34 or 100x32 Graphic Display Modes with a Icon Line
- Single Supply Operation, 2.4V - 3.5V
- Low Current Sleep Mode
- On Chip Voltage Generator / External Power Supply
- 2X / 3X / 4X On chip DC-DC Converter
- On chip Oscillator
- On Chip Smart Bias Divider
- 1:4 / 1:5 / 1:6 / 1:7 Bias Ratio
- Maximum -12.0V LCD Driving Output Voltage
- Built-in Temperature Compensation Circuit
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
- On Chip 100 x 66 Graphic Display Data RAM
- Four grey level control in 32-mux mode
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Internal Regulator Resistors Control
- External Contrast Control
- 32 level Internal Contrast Control
- Available in Bare Die, Gold Bump Die or TAB (Tape Automated Bonding) package

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM

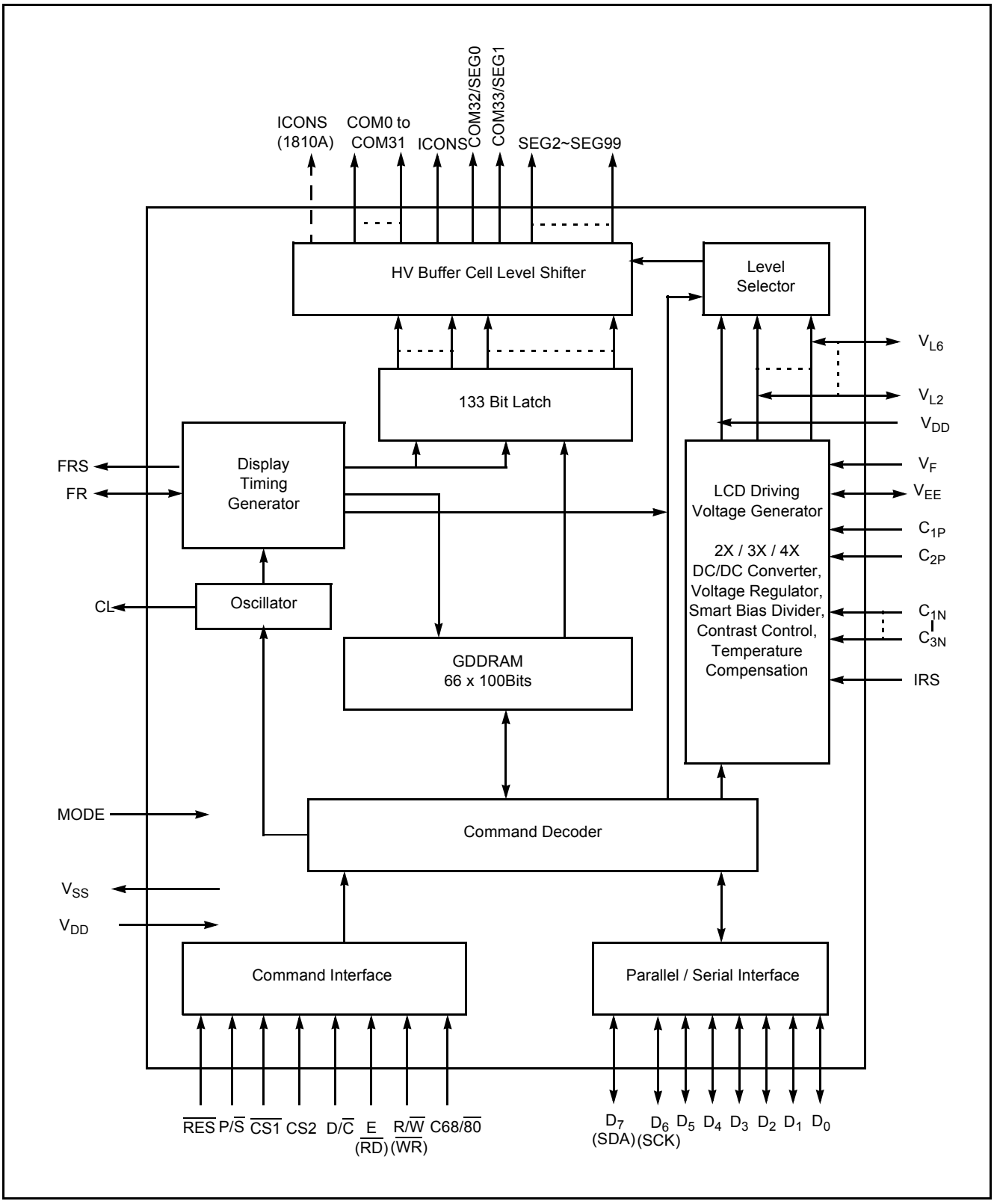
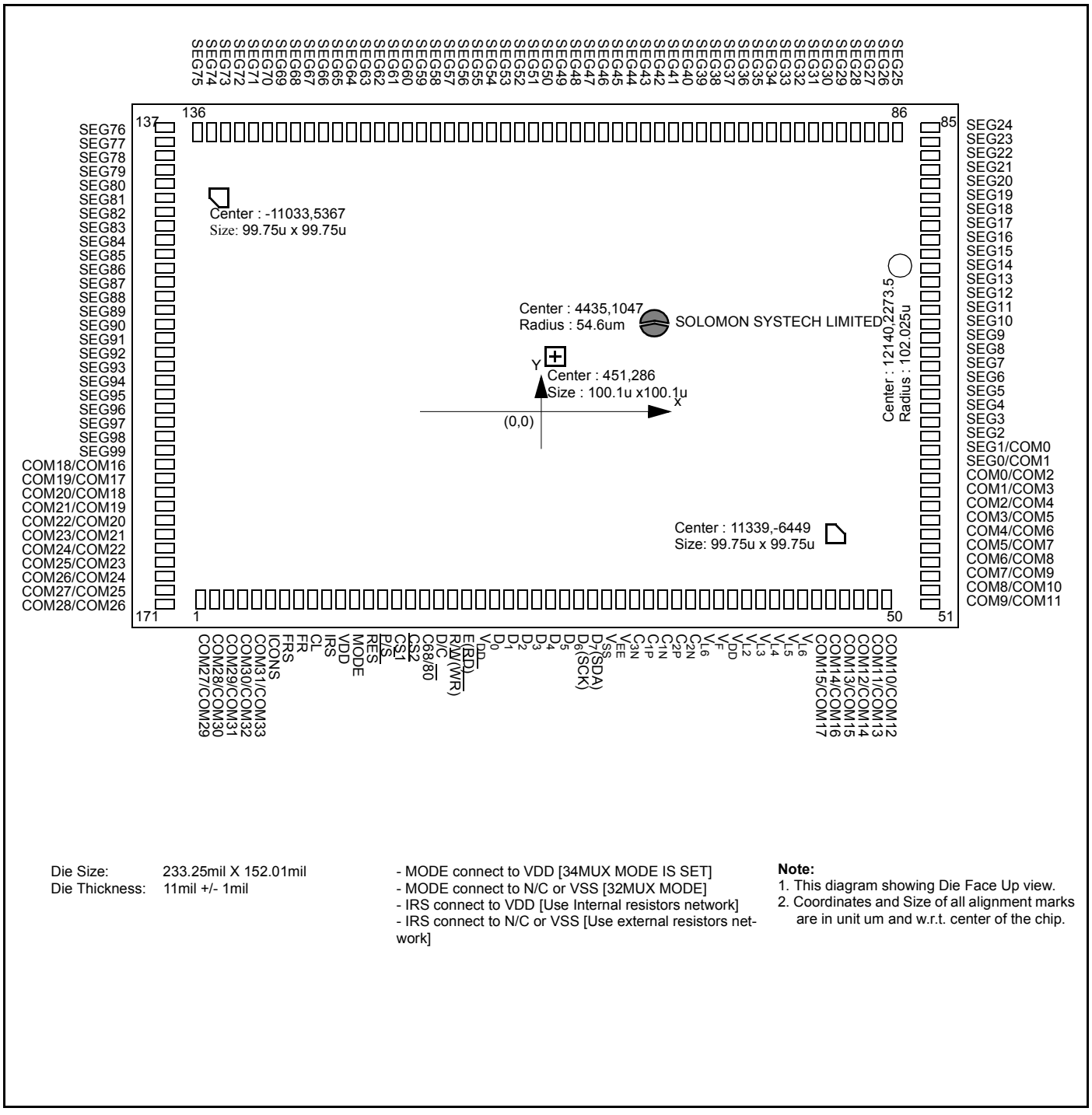


Figure 1 SSD1810/A Block Diagram

PIN ARRANGEMENT



Die Size: 233.25mil X 152.01mil
Die Thickness: 11mil +/- 1mil

- MODE connect to VDD [34MUX MODE IS SET]
- MODE connect to N/C or VSS [32MUX MODE]
- IRS connect to VDD [Use Internal resistors network]
- IRS connect to N/C or VSS [Use external resistors network]

Note:
1. This diagram showing Die Face Up view.
2. Coordinates and Size of all alignment marks are in unit um and w.r.t. center of the chip.

Figure 2 SSD1810V Bare Die Pin Arrangement

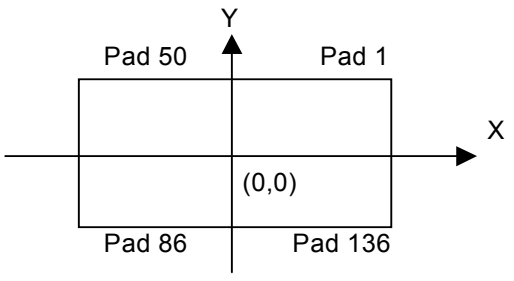
Table 1 SSD1810's Output Relation between SEG and Column Address at different MODE

Pad #	MODE=VDD	MODE=NC/	COL ADDRESS HEX		Pad #	MODE=VDD	MODE=NC	COL ADDRESS HEX		Pad #	MODE=VDD	MODE=NC	COL ADDRESS HEX	
		MODE=Vss	Normal	Re-map			MODE=Vss	Normal	Re-map			MODE=Vss	Normal	Re-map
					94	SEG33	SEG33	31	52	144	SEG83	SEG83	63	20
45	COM17	COM15			95	SEG34	SEG34	32	51	145	SEG84	SEG84	64	1F
46	COM16	COM14			96	SEG35	SEG35	33	50	146	SEG85	SEG85	65	1E
47	COM15	COM13			97	SEG36	SEG36	34	4F	147	SEG86	SEG86	66	1D
48	COM14	COM12			98	SEG37	SEG37	35	4E	148	SEG87	SEG87	67	1C
49	COM13	COM11			99	SEG38	SEG38	36	4D	149	SEG88	SEG88	68	1B
50	COM12	COM10			100	SEG39	SEG39	37	4C	150	SEG89	SEG89	69	1A
51	COM11	COM9			101	SEG40	SEG40	38	4B	151	SEG90	SEG90	6A	19
52	COM10	COM8			102	SEG41	SEG41	39	4A	152	SEG91	SEG91	6B	18
53	COM9	COM7			103	SEG42	SEG42	3A	49	153	SEG92	SEG92	6C	17
54	COM8	COM6			104	SEG43	SEG43	3B	48	154	SEG93	SEG93	6D	16
55	COM7	COM5			105	SEG44	SEG44	3C	47	155	SEG94	SEG94	6E	15
56	COM6	COM4			106	SEG45	SEG45	3D	46	156	SEG95	SEG95	6F	14
57	COM5	COM3			107	SEG46	SEG46	3E	45	157	SEG96	SEG96	70	13
58	COM4	COM2			108	SEG47	SEG47	3F	44	158	SEG97	SEG97	71	12
59	COM3	COM1			109	SEG48	SEG48	40	43	159	SEG98	SEG98	72	11
60	COM2	COM0			110	SEG49	SEG49	41	42	160	SEG99	SEG99	73	10
61	COM1	SEG0	10	73	111	SEG50	SEG50	42	41	161	COM18	COM16		
62	COM0	SEG1	11	72	112	SEG51	SEG51	43	40	162	COM19	COM17		
63	SEG2	SEG2	12	71	113	SEG52	SEG52	44	3F	163	COM20	COM18		
64	SEG3	SEG3	13	70	114	SEG53	SEG53	45	3E	164	COM21	COM19		
65	SEG4	SEG4	14	6F	115	SEG54	SEG54	46	3D	165	COM22	COM20		
66	SEG5	SEG5	15	6E	116	SEG55	SEG55	47	3C	166	COM23	COM21		
67	SEG6	SEG6	16	6D	117	SEG56	SEG56	48	3B	167	COM24	COM22		
68	SEG7	SEG7	17	6C	118	SEG57	SEG57	49	3A	168	COM25	COM23		
69	SEG8	SEG8	18	6B	119	SEG58	SEG58	4A	39	169	COM26	COM24		
70	SEG9	SEG9	19	6A	120	SEG59	SEG59	4B	38	170	COM27	COM25		
71	SEG10	SEG10	1A	69	121	SEG60	SEG60	4C	37	171	COM28	COM26		
72	SEG11	SEG11	1B	68	122	SEG61	SEG61	4D	36	1	COM29	COM27		
73	SEG12	SEG12	1C	67	123	SEG62	SEG62	4E	35	2	COM30	COM28		
74	SEG13	SEG13	1D	66	124	SEG63	SEG63	4F	34	3	COM31	COM29		
75	SEG14	SEG14	1E	65	125	SEG64	SEG64	50	33	4	COM32	COM30		
76	SEG15	SEG15	1F	64	126	SEG65	SEG65	51	32	5	COM33	COM31		
77	SEG16	SEG16	20	63	127	SEG66	SEG66	52	31	6	ICONS	ICONS		
78	SEG17	SEG17	21	62	128	SEG67	SEG67	53	30					
79	SEG18	SEG18	22	61	129	SEG68	SEG68	54	2F					
80	SEG19	SEG19	23	60	130	SEG69	SEG69	55	2E					
81	SEG20	SEG20	24	5F	131	SEG70	SEG70	56	2D					
82	SEG21	SEG21	25	5E	132	SEG71	SEG71	57	2C					
83	SEG22	SEG22	26	5D	133	SEG72	SEG72	58	2B					
84	SEG23	SEG23	27	5C	134	SEG73	SEG73	59	2A					
85	SEG24	SEG24	28	5B	135	SEG74	SEG74	5A	29					
86	SEG25	SEG25	29	5A	136	SEG75	SEG75	5B	28					
87	SEG26	SEG26	2A	59	137	SEG76	SEG76	5C	27					
88	SEG27	SEG27	2B	58	138	SEG77	SEG77	5D	26					
89	SEG28	SEG28	2C	57	139	SEG78	SEG78	5E	25					
90	SEG29	SEG29	2D	56	140	SEG79	SEG79	5F	24					
91	SEG30	SEG30	2E	55	141	SEG80	SEG80	60	23					
92	SEG31	SEG31	2F	54	142	SEG81	SEG81	61	22					
93	SEG32	SEG32	30	53	143	SEG82	SEG82	62	21					

Table 2 SSD1810 Pad Coordinates

Pad #	Name	X	Y	Pad #	Name	X	Y
1	COM27/COM29	2450	1649.025	51	COM9/COM11	-2744.35	1664.95
2	COM28/COM30	2347.8	1649.025	52	COM8/COM10	-2744.35	1562.75
3	COM29/COM31	2245.6	1649.025	53	COM7/COM9	-2744.35	1460.55
4	COM30/COM32	2143.4	1649.025	54	COM6/COM8	-2744.35	1358.35
5	COM31/COM33	2041.2	1649.025	55	COM5/COM7	-2744.35	1256.15
6	ICONS	1939	1649.025	56	COM4/COM6	-2744.35	1153.95
7	FRS	1790.775	1649.025	57	COM3/COM5	-2744.35	1051.75
8	FR	1688.575	1649.025	58	COM2/COM4	-2744.35	949.55
9	CL	1586.375	1649.025	59	COM1/COM3	-2744.35	847.35
10	IRS	1492.225	1649.025	60	COM0/COM2	-2744.35	753.2
11	VDD	1398.075	1649.025	61	SEG0/COM1	-2744.35	659.05
12	MODE	1303.925	1649.025	62	SEG1/COM0	-2744.35	564.9
13	/RES	1209.775	1649.025	63	SEG2	-2744.35	470.75
14	P/S	1115.625	1649.025	64	SEG3	-2744.35	376.6
15	/CS1	1021.475	1649.025	65	SEG4	-2744.35	282.45
16	CS2	927.325	1649.025	66	SEG5	-2744.35	188.3
17	C68/80	833.175	1649.025	67	SEG6	-2744.35	94.15
18	D/C	739.025	1649.025	68	SEG7	-2744.35	0
19	R/W	641.375	1649.025	69	SEG8	-2744.35	-94.15
20	E/RD	543.725	1649.025	70	SEG9	-2744.35	-188.3
21	VDD	446.075	1649.025	71	SEG10	-2744.35	-282.45
22	D0	348.425	1649.025	72	SEG11	-2744.35	-376.6
23	D1	250.775	1649.025	73	SEG12	-2744.35	-470.75
24	D2	153.125	1649.025	74	SEG13	-2744.35	-564.9
25	D3	55.475	1649.025	75	SEG14	-2744.35	-659.05
26	D4	-42.175	1649.025	76	SEG15	-2744.35	-753.2
27	D5	-139.825	1649.025	77	SEG16	-2744.35	-847.35
28	D6	-237.475	1649.025	78	SEG17	-2744.35	-949.55
29	D7	-335.125	1649.025	79	SEG18	-2744.35	-1051.75
30	VSS	-460.6	1649.025	80	SEG19	-2744.35	-1153.95
31	VEE	-558.25	1649.025	81	SEG20	-2744.35	-1256.15
32	C3N	-655.9	1649.025	82	SEG21	-2744.35	-1358.35
33	C1P	-753.55	1649.025	83	SEG22	-2744.35	-1460.55
34	C1N	-851.2	1649.025	84	SEG23	-2744.35	-1562.75
35	C2P	-948.85	1649.025	85	SEG24	-2744.35	-1664.95
36	C2N	-1046.5	1649.025				
37	VL6	-1144.15	1649.025				
38	VF	-1241.8	1649.025				
39	VDD	-1339.45	1649.025				
40	VL2	-1437.1	1649.025				
41	VL3	-1534.75	1649.025				
42	VL4	-1632.4	1649.025				
43	VL5	-1734.6	1649.025				
44	VL6	-1836.8	1649.025				
45	COM15/COM17	-1939	1649.025				
46	COM14/COM16	-2041.2	1649.025				
47	COM13/COM15	-2143.4	1649.025				
48	COM12/COM14	-2245.6	1649.025				
49	COM11/COM13	-2347.8	1649.025				
50	COM10/COM12	-2450	1649.025				

Remark:
MODE connect to VDD : MUX33 mode(COM0~COM33);
MODE connect to VSS/NC: MUX32 mode(COM0~COM31);



Pad #	Name	X	Y
86	SEG25	-2430.225	-1649.025
87	SEG26	-2328.025	-1649.025
88	SEG27	-2225.825	-1649.025
89	SEG28	-2123.625	-1649.025
90	SEG29	-2021.425	-1649.025
91	SEG30	-1919.225	-1649.025
92	SEG31	-1817.025	-1649.025
93	SEG32	-1714.825	-1649.025
94	SEG33	-1612.625	-1649.025
95	SEG34	-1510.425	-1649.025
96	SEG35	-1412.25	-1649.025
97	SEG36	-1318.1	-1649.025
98	SEG37	-1223.95	-1649.025
99	SEG38	-1129.8	-1649.025
100	SEG39	-1035.65	-1649.025
101	SEG40	-941.5	-1649.025
102	SEG41	-847.35	-1649.025
103	SEG42	-753.2	-1649.025
104	SEG43	-659.05	-1649.025
105	SEG44	-564.9	-1649.025
106	SEG45	-470.75	-1649.025
107	SEG46	-376.6	-1649.025
108	SEG47	-282.45	-1649.025
109	SEG48	-188.3	-1649.025
110	SEG49	-94.15	-1649.025
111	SEG50	0	-1649.025
112	SEG51	94.15	-1649.025
113	SEG52	188.3	-1649.025
114	SEG53	282.45	-1649.025
115	SEG54	376.6	-1649.025
116	SEG55	470.75	-1649.025
117	SEG56	564.9	-1649.025
118	SEG57	659.05	-1649.025
119	SEG58	753.2	-1649.025
120	SEG59	847.35	-1649.025
121	SEG60	941.5	-1649.025
122	SEG61	1035.65	-1649.025
123	SEG62	1129.8	-1649.025
124	SEG63	1223.95	-1649.025
125	SEG64	1318.1	-1649.025
126	SEG65	1412.25	-1649.025
127	SEG66	1510.425	-1649.025
128	SEG67	1612.625	-1649.025
129	SEG68	1714.825	-1649.025
130	SEG69	1817.025	-1649.025
131	SEG70	1919.225	-1649.025
132	SEG71	2021.425	-1649.025
133	SEG72	2123.625	-1649.025
134	SEG73	2225.825	-1649.025
135	SEG74	2328.025	-1649.025
136	SEG75	2430.225	-1649.025
137	SEG76	2744.35	-1664.95
138	SEG77	2744.35	-1562.75
139	SEG78	2744.35	-1460.55
140	SEG79	2744.35	-1358.35
141	SEG80	2744.35	-1256.15
142	SEG81	2744.35	-1153.95
143	SEG82	2744.35	-1051.75
144	SEG83	2744.35	-949.55
145	SEG84	2744.35	-847.35
146	SEG85	2744.35	-753.2
147	SEG86	2744.35	-659.05
148	SEG87	2744.35	-564.9
149	SEG88	2744.35	-470.75
150	SEG89	2744.35	-376.6
151	SEG90	2744.35	-282.45
152	SEG91	2744.35	-188.3
153	SEG92	2744.35	-94.15
154	SEG93	2744.35	0
155	SEG94	2744.35	94.15
156	SEG95	2744.35	188.3
157	SEG96	2744.35	282.45
158	SEG97	2744.35	376.6
159	SEG98	2744.35	470.75
160	SEG99	2744.35	564.9
161	COM16/COM18	2744.35	659.05
162	COM17/COM19	2744.35	753.2
163	COM18/COM20	2744.35	847.35
164	COM19/COM21	2744.35	949.55
165	COM20/COM22	2744.35	1051.75
166	COM21/COM23	2744.35	1153.95
167	COM22/COM24	2744.35	1256.15
168	COM23/COM25	2744.35	1358.35
169	COM24/COM26	2744.35	1460.55
170	COM25/COM27	2744.35	1562.75
171	COM26/COM28	2744.35	1664.95

Pad Size

Pad #	X	Y
1 - 8	3.4 mil	4.3 mil
9 - 42	3.1 mil	4.3 mil
43 - 50	3.4 mil	4.3 mil
51 - 58	4.3 mil	3.4 mil
59 - 77	4.3 mil	3.1 mil
78 - 85	4.3 mil	3.4 mil
86 - 95	3.4 mil	4.3 mil
96 - 126	3.1 mil	4.3 mil
127 - 136	3.4 mil	4.3 mil
137 - 144	4.3 mil	3.4 mil
145 - 163	4.3 mil	3.1 mil
164 - 171	4.3 mil	3.4 mil

PIN ARRANGEMENT

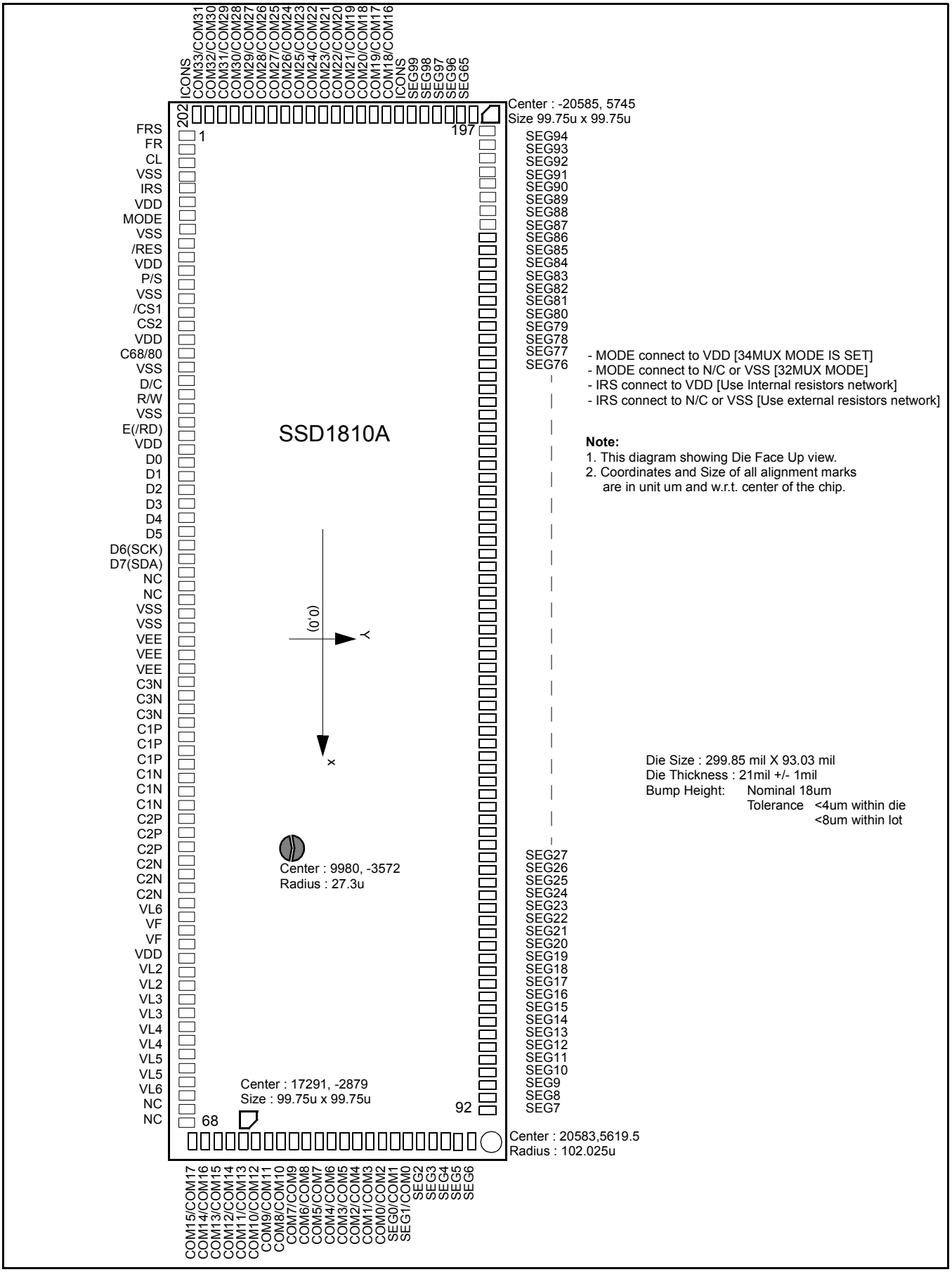


Figure 3 SSD1810A Gold Bump Die Pin Arrangement

Table 3 SSD1810A's Output Relation between SEG and colomn address at different MODE

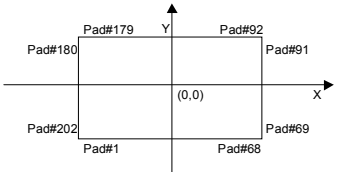
Pad #	MODE=VDD	MODE=NC	COL ADDRESS HEX		Pad #	MODE=VDD	MODE=NC	COL ADDRESS HEX		Pad #	MODE=VDD	MODE=NC	COL ADDRESS HEX	
			Normal	Re-map				Normal	Re-map				Normal	Re-map
					118	SEG31	SEG33	31	52	168	SEG81	SEG83	63	20
69	COM17	COM15			119	SEG32	SEG34	32	51	169	SEG82	SEG84	64	1F
70	COM16	COM14			120	SEG33	SEG35	33	50	170	SEG83	SEG85	65	1E
71	COM15	COM13			121	SEG34	SEG36	34	4F	171	SEG84	SEG86	66	1D
72	COM14	COM12			122	SEG35	SEG37	35	4E	172	SEG85	SEG87	67	1C
73	COM13	COM11			123	SEG36	SEG38	36	4D	173	SEG86	SEG88	68	1B
74	COM12	COM10			124	SEG37	SEG39	37	4C	174	SEG87	SEG89	69	1A
75	COM11	COM9			125	SEG38	SEG40	38	4B	175	SEG88	SEG90	6A	19
76	COM10	COM8			126	SEG39	SEG41	39	4A	176	SEG89	SEG91	6B	18
77	COM9	COM7			127	SEG40	SEG42	3A	49	177	SEG90	SEG92	6C	17
78	COM8	COM6			128	SEG41	SEG43	3B	48	178	SEG91	SEG93	6D	16
79	COM7	COM5			129	SEG42	SEG44	3C	47	179	SEG92	SEG94	6E	15
80	COM6	COM4			130	SEG43	SEG45	3D	46	180	SEG93	SEG95	6F	14
81	COM5	COM3			131	SEG44	SEG46	3E	45	181	SEG94	SEG96	70	13
82	COM4	COM2			132	SEG45	SEG47	3F	44	182	SEG95	SEG97	71	12
83	COM3	COM1			133	SEG46	SEG48	40	43	183	SEG96	SEG98	72	11
84	COM2	COM0			134	SEG47	SEG49	41	42	184	SEG97	SEG99	73	10
85	COM1	SEG0	10	73	135	SEG48	SEG50	42	41	185	ICONS	ICONS		
86	COM0	SEG1	11	72	136	SEG49	SEG51	43	40	186	COM18	COM16		
87	SEG0	SEG2	12	71	137	SEG50	SEG52	44	3F	187	COM19	COM17		
88	SEG1	SEG3	13	70	138	SEG51	SEG53	45	3E	188	COM20	COM18		
89	SEG2	SEG4	14	6F	139	SEG52	SEG54	46	3D	189	COM21	COM19		
90	SEG3	SEG5	15	6E	140	SEG53	SEG55	47	3C	190	COM22	COM20		
91	SEG4	SEG6	16	6D	141	SEG54	SEG56	48	3B	191	COM23	COM21		
92	SEG5	SEG7	17	6C	142	SEG55	SEG57	49	3A	192	COM24	COM22		
93	SEG6	SEG8	18	6B	143	SEG56	SEG58	4A	39	193	COM25	COM23		
94	SEG7	SEG9	19	6A	144	SEG57	SEG59	4B	38	194	COM26	COM24		
95	SEG8	SEG10	1A	69	145	SEG58	SEG60	4C	37	195	COM27	COM25		
96	SEG9	SEG11	1B	68	146	SEG59	SEG61	4D	36	196	COM28	COM26		
97	SEG10	SEG12	1C	67	147	SEG60	SEG62	4E	35	197	COM29	COM27		
98	SEG11	SEG13	1D	66	148	SEG61	SEG63	4F	34	198	COM30	COM28		
99	SEG12	SEG14	1E	65	149	SEG62	SEG64	50	33	199	COM31	COM29		
100	SEG13	SEG15	1F	64	150	SEG63	SEG65	51	32	200	COM32	COM30		
101	SEG14	SEG16	20	63	151	SEG64	SEG66	52	31	201	COM33	COM31		
102	SEG15	SEG17	21	62	152	SEG65	SEG67	53	30	202	ICONS	ICONS		
103	SEG16	SEG18	22	61	153	SEG66	SEG68	54	2F					
104	SEG17	SEG19	23	60	154	SEG67	SEG69	55	2E					
105	SEG18	SEG20	24	5F	155	SEG68	SEG70	56	2D					
106	SEG19	SEG21	25	5E	156	SEG69	SEG71	57	2C					
107	SEG20	SEG22	26	5D	157	SEG70	SEG72	58	2B					
108	SEG21	SEG23	27	5C	158	SEG71	SEG73	59	2A					
109	SEG22	SEG24	28	5B	159	SEG72	SEG74	5A	29					
110	SEG23	SEG25	29	5A	160	SEG73	SEG75	5B	28					
111	SEG24	SEG26	2A	59	161	SEG74	SEG76	5C	27					
112	SEG25	SEG27	2B	58	162	SEG75	SEG77	5D	26					
113	SEG26	SEG28	2C	57	163	SEG76	SEG78	5E	25					
114	SEG27	SEG29	2D	56	164	SEG77	SEG79	5F	24					
115	SEG28	SEG30	2E	55	165	SEG78	SEG80	60	23					
116	SEG29	SEG31	2F	54	166	SEG79	SEG81	61	22					
117	SEG30	SEG32	30	53	167	SEG80	SEG82	62	21					

Table 4 SSD1810A Pad Coordinates

PAD#	PAD NAME	X/um	Y/um	PAD#	PAD NAME	X/um	Y/um	PAD#	PAD NAME	X/um	Y/um
1	FRS	-3046.05	-997.675	69	COM15/COM17	3604.3	-1005.2	137	SEG52	-114.975	979.475
2	FR	-2957.15	-997.675	70	COM14/COM16	3604.3	-928.9	138	SEG53	-191.275	979.475
3	CL	-2868.25	-997.675	71	COM13/COM15	3604.3	-852.6	139	SEG54	-267.575	979.475
4	VSS	-2779.35	-997.675	72	COM12/COM14	3604.3	-776.3	140	SEG55	-343.875	979.475
5	IRS	-2690.45	-997.675	73	COM11/COM13	3604.3	-700	141	SEG56	-420.175	979.475
6	VDD	-2601.55	-997.675	74	COM10/COM12	3604.3	-623.7	142	SEG57	-496.475	979.475
7	MODE	-2512.65	-997.675	75	COM9/COM11	3604.3	-547.4	143	SEG58	-572.775	979.475
8	VSS	-2423.75	-997.675	76	COM8/COM10	3604.3	-471.1	144	SEG59	-649.075	979.475
9	/RES	-2334.85	-997.675	77	COM7/COM9	3604.3	-394.8	145	SEG60	-725.375	979.475
10	VDD	-2245.95	-997.675	78	COM6/COM8	3604.3	-318.5	146	SEG61	-801.675	979.475
11	P/S	-2157.05	-997.675	79	COM5/COM7	3604.3	-242.2	147	SEG62	-877.975	979.475
12	VSS	-2068.15	-997.675	80	COM4/COM6	3604.3	-165.9	148	SEG63	-954.275	979.475
13	/CS1	-1979.25	-997.675	81	COM3/COM5	3604.3	-89.6	149	SEG64	-1030.575	979.475
14	CS2	-1890.35	-997.675	82	COM2/COM4	3604.3	-13.3	150	SEG65	-1106.875	979.475
15	VDD	-1801.45	-997.675	83	COM1/COM3	3604.3	63	151	SEG66	-1183.175	979.475
16	C68/80	-1712.55	-997.675	84	COM0/COM2	3604.3	139.3	152	SEG67	-1259.475	979.475
17	VSS	-1623.65	-997.675	85	SEG0/COM1	3604.3	215.6	153	SEG68	-1335.775	979.475
18	D/C	-1534.75	-997.675	86	SEG1/COM0	3604.3	291.9	154	SEG69	-1412.075	979.475
19	R/W	-1445.85	-997.675	87	SEG2	3604.3	368.2	155	SEG70	-1488.375	979.475
20	VSS	-1356.95	-997.675	88	SEG3	3604.3	444.5	156	SEG71	-1564.675	979.475
21	E/RD	-1268.05	-997.675	89	SEG4	3604.3	520.8	157	SEG72	-1640.975	979.475
22	VDD	-1179.15	-997.675	90	SEG5	3604.3	597.1	158	SEG73	-1717.275	979.475
23	D0	-1090.25	-997.675	91	SEG6	3604.3	673.4	159	SEG74	-1793.575	979.475
24	D1	-1001.35	-997.675	92	SEG7	3318.525	979.475	160	SEG75	-1869.875	979.475
25	D2	-912.45	-997.675	93	SEG8	3242.225	979.475	161	SEG76	-1946.175	979.475
26	D3	-823.55	-997.675	94	SEG9	3165.925	979.475	162	SEG77	-2022.475	979.475
27	D4	-734.65	-997.675	95	SEG10	3089.625	979.475	163	SEG78	-2098.775	979.475
28	D5	-645.75	-997.675	96	SEG11	3013.325	979.475	164	SEG79	-2175.075	979.475
29	D6	-556.85	-997.675	97	SEG12	2937.025	979.475	165	SEG80	-2251.375	979.475
30	D7	-467.95	-997.675	98	SEG13	2860.725	979.475	166	SEG81	-2327.675	979.475
31	NC	-323.05	-997.675	99	SEG14	2784.425	979.475	167	SEG82	-2403.975	979.475
32	NC	-205.45	-997.675	100	SEG15	2708.125	979.475	168	SEG83	-2480.275	979.475
33	VSS	-116.55	-997.675	101	SEG16	2631.825	979.475	169	SEG84	-2556.575	979.475
34	VSS	-27.65	-997.675	102	SEG17	2555.525	979.475	170	SEG85	-2632.875	979.475
35	VEE	61.25	-997.675	103	SEG18	2479.225	979.475	171	SEG86	-2709.175	979.475
36	VEE	150.15	-997.675	104	SEG19	2402.925	979.475	172	SEG87	-2785.475	979.475
37	VEE	239.05	-997.675	105	SEG20	2326.625	979.475	173	SEG88	-2861.775	979.475
38	C3N	327.95	-997.675	106	SEG21	2250.325	979.475	174	SEG89	-2938.075	979.475
39	C3N	416.85	-997.675	107	SEG22	2174.025	979.475	175	SEG90	-3014.375	979.475
40	C3N	505.75	-997.675	108	SEG23	2097.725	979.475	176	SEG91	-3090.675	979.475
41	C1P	594.65	-997.675	109	SEG24	2021.425	979.475	177	SEG92	-3166.975	979.475
42	C1P	683.55	-997.675	110	SEG25	1945.125	979.475	178	SEG93	-3243.275	979.475
43	C1P	772.45	-997.675	111	SEG26	1868.825	979.475	179	SEG94	-3319.575	979.475
44	C1N	861.35	-997.675	112	SEG27	1792.525	979.475	180	SEG95	-3604.3	673.4
45	C1N	950.25	-997.675	113	SEG28	1716.225	979.475	181	SEG96	-3604.3	597.1
46	C1N	1039.15	-997.675	114	SEG29	1639.925	979.475	182	SEG97	-3604.3	520.8
47	C2P	1128.05	-997.675	115	SEG30	1563.625	979.475	183	SEG98	-3604.3	444.5
48	C2P	1216.95	-997.675	116	SEG31	1487.325	979.475	184	SEG99	-3604.3	368.2
49	C2P	1305.85	-997.675	117	SEG32	1411.025	979.475	185	ICONS	-3604.3	291.9
50	C2N	1394.75	-997.675	118	SEG33	1334.725	979.475	186	COM16/COM18	-3604.3	215.6
51	C2N	1483.65	-997.675	119	SEG34	1258.425	979.475	187	COM17/COM19	-3604.3	139.3
52	C2N	1572.55	-997.675	120	SEG35	1182.125	979.475	188	COM18/COM20	-3604.3	63
53	VL6	1661.45	-997.675	121	SEG36	1105.825	979.475	189	COM19/COM21	-3604.3	-13.3
54	VDD	1750.35	-997.675	122	SEG37	1029.525	979.475	190	COM20/COM22	-3604.3	-89.6
55	VF	1839.25	-997.675	123	SEG38	953.225	979.475	191	COM21/COM23	-3604.3	-165.9
56	VF	1928.15	-997.675	124	SEG39	876.925	979.475	192	COM22/COM24	-3604.3	-242.2
57	VDD	2017.05	-997.675	125	SEG40	800.625	979.475	193	COM23/COM25	-3604.3	-318.5
58	VL2	2105.95	-997.675	126	SEG41	724.325	979.475	194	COM24/COM26	-3604.3	-394.8
59	VL2	2194.85	-997.675	127	SEG42	648.025	979.475	195	COM25/COM27	-3604.3	-471.1
60	VL3	2283.75	-997.675	128	SEG43	571.725	979.475	196	COM26/COM28	-3604.3	-547.4
61	VL3	2372.65	-997.675	129	SEG44	495.425	979.475	197	COM27/COM29	-3604.3	-623.7
62	VL4	2461.55	-997.675	130	SEG45	419.125	979.475	198	COM28/COM30	-3604.3	-700
63	VL4	2550.45	-997.675	131	SEG46	342.825	979.475	199	COM29/COM31	-3604.3	-776.3
64	VL5	2639.35	-997.675	132	SEG47	266.525	979.475	200	COM30/COM32	-3604.3	-852.6
65	VL5	2728.25	-997.675	133	SEG48	190.225	979.475	201	COM31/COM33	-3604.3	-928.9
66	VL6	2817.15	-997.675	134	SEG49	113.925	979.475	202	ICONS	-3604.3	-1005.2
67	NC	2906.05	-997.675	135	SEG50	37.625	979.475				
68	NC	2994.95	-997.675	136	SEG51	-38.675	979.475				

BUMP SIZE		
PAD#	X/um	Y/um
1 - 68	60.2	60.2
69 - 91	100.1	42.0
92 - 179	42.0	100.1
180 - 202	100.1	42.0

Remark:
MODE connect to VDD : MUX33 mode(COM0~COM33);
MODE connect to VSS/NC: MUX32 mode(COM0~COM31);



Die Size: 299.85 mil X 93.03 mil
Bumps face up

PIN DESCRIPTIONS

MODE

This pin is display mode select input.
MODE = 1: Set to 34-mux display.
MODE = 0 or N/C: Set to 32-mux display.

FR

This pin is the frame signal output. The voltage output from this pin is either V_{SS} or V_{DD}. This voltage will toggle once per frame.

FRS

This pin is used together with FR in for static drive (indicator) output. Voltage level output from this pin is also either V_{SS} or V_{DD}. After power-on or after Set Indicator Off command is issued, this pin will be same phase signal to FR. If Set Indicator On command is sent to the chip, a out-of-phase to FR signal will be output.

CL

This pin is the display clock output.

$\overline{CS1}$, CS2

These pin are chip select inputs. The chip is enabled for MCU communication only when both $\overline{CS1}$ is pulled low and CS2 is pulled high.

$\overline{RES}$

This pin is reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset procedure is 1μs.

D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. Details relationship with other MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/$\overline{W}$($\overline{WR}$)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/$\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When interfacing to an 8080-microprocessor, this pin will be the Write ($\overline{WR}$) input. Data write operation is initiated when this pin is pulled low when the chip is selected.

E($\overline{RD}$)

This pin is MCU interface input. When interfacing to an 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high when the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read ($\overline{RD}$) signal. Data read operation is initiated when this pin is pulled low when the chip is selected.

D_7-D_0

These pins are the 8-bit bi-directional data bus to be connected to the MCU in parallel interface mode. D_7 is the MSB while D_0 is the LSB.

When serial mode is selected, D_7 is the serial data input (SDA) and D_6 is the serial clock input (SCK).

V_{DD}

Chip's Power Supply pin. This is also the reference for the DC-DC Converter output and LCD driving voltages.

V_{SS}

Ground. A reference for the logic pins.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter, by turning on the **internal voltage booster** option in the **Set Power Control Register** command.

When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C_{3N}, C_{1P}, C_{1N}, C_{2N} and C_{2P}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected between these pins. Different connection will result in different DC-DC converter multiple factor, 2X, 3X or 4X. Detail connections please refer to voltage converter section in the functional block description.

V_{L2}, V_{L3}, V_{L4} and V_{L5}

These are the LCD driving voltage levels. All these levels are referenced to V_{DD}.

They can be supplied externally or generated by the internal bias divider, by turning on the **output op-amp buffers** option in the **Set Power Control Register** command.

The potential relation of these pins are given as:

$$V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$$

and with bias factor, a,

$$V_{L2} - V_{DD} = 1/a * (V_{L6} - V_{DD})$$
$$V_{L3} - V_{DD} = 2/a * (V_{L6} - V_{DD})$$
$$V_{L4} - V_{DD} = (a-2)/a * (V_{L6} - V_{DD})$$
$$V_{L5} - V_{DD} = (a-1)/a * (V_{L6} - V_{DD})$$

V_{L6}

This pin is the most negative LCD driving voltage. It can be supplied externally or generated by turning on the **internal regulator** option in the **Set Power Control Register** command.

V_F

This pin is the input of the built-in voltage regulator for generating V_{L6}.

When external resistor network is selected (IRS pulled low) to generate the LCD driving level, V_{L6}, two external resistors, R_1 and R_2, should be connected between V_{DD} and V_F, and V_F and V_{L6}, respectively (see application circuit diagrams).

C68/$\overline{80}$

This pin is MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series interface is selected.

If Serial Interface is selected (P/$\overline{S}$ pulled low), the setting of this pin is ignored, but must be connected to a known logic (either high or low).

P/$\overline{S}$

This pin is serial/parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When it is pulled low, serial interface will be selected.

Note1: For serial mode, D0, D1, D2, D3, D4, D5, R/W/(WR), E/(RD) is recommended to be connected to Vss.

Note2: Read Back operation is only available in parallel mode.

IRS

This is the input pin to enable the internal resistors network for the voltage regulator. When this pin is pulled high, the internal feedback resistors of the internal regulator for generating V_{L6} will be enabled.

When it is pulled low, external resistors, R_1 and R_2, should be connected to V_{DD} and V_F, and V_F and V_{L6}, respectively (see application circuit diagrams).

COM0 - COM33

These pins provide the row driving signal to the LCD panel. The output voltage level of these pins is V_{DD} during sleep mode and standby mode.

SEG0 - SEG99

These pins provide the LCD column driving signals. The output voltage level of these pins is V_{DD} during sleep mode and standby mode.

ICONS

This pin is the special icon or indicator line. There are two ICONS pins (SSD1810A) on the chip. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the LCD layout.

Note: SSD1810V has only one ICONS pin.

NC

These are the No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether D_0 ~ D_7 input is interpreted as data or command, based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ is high, the input at D_0 ~ D_7 is written to Graphic Display Data RAM (GDDRAM). If D/$\overline{C}$ is low, the input at D_0-D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once $\overline{RES}$ receives a reset pulse (pull low) of about 1us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, E($\overline{RD}$), $\overline{CS1}$ and CS2. R/$\overline{W}$($\overline{WR}$) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$($\overline{WR}$) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E($\overline{RD}$) input serves as data latch signal (clock) when high provided that $\overline{CS1}$ and CS2 are low and high respectively. Refer to Figure 10 on page 26 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessor

In order to match the operating frequency of display RAM with that of the microprocessor, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read form the driver. This is shown in Figure 4 below.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), E($\overline{RD}$), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, $\overline{CS1}$ and CS2. E($\overline{RD}$) input serves as data read latch signal (clock) when low provided that $\overline{CS1}$ and CS2 are low and high respectively. Whether it is display data or status register read is controlled by D/$\overline{C}$. R/$\overline{W}$($\overline{WR}$) input serves as data write latch signal(clock) when high provided that $\overline{CS1}$ and CS2 are low and high respectively. Whether it is display data or command register write is controlled by D/$\overline{C}$. Refer to Figure 11 on page 27 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read form the driver.

MPU Serial interface

The serial interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$, $\overline{CS1}$ and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D_7, D_6,... D_0. D/$\overline{C}$ is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

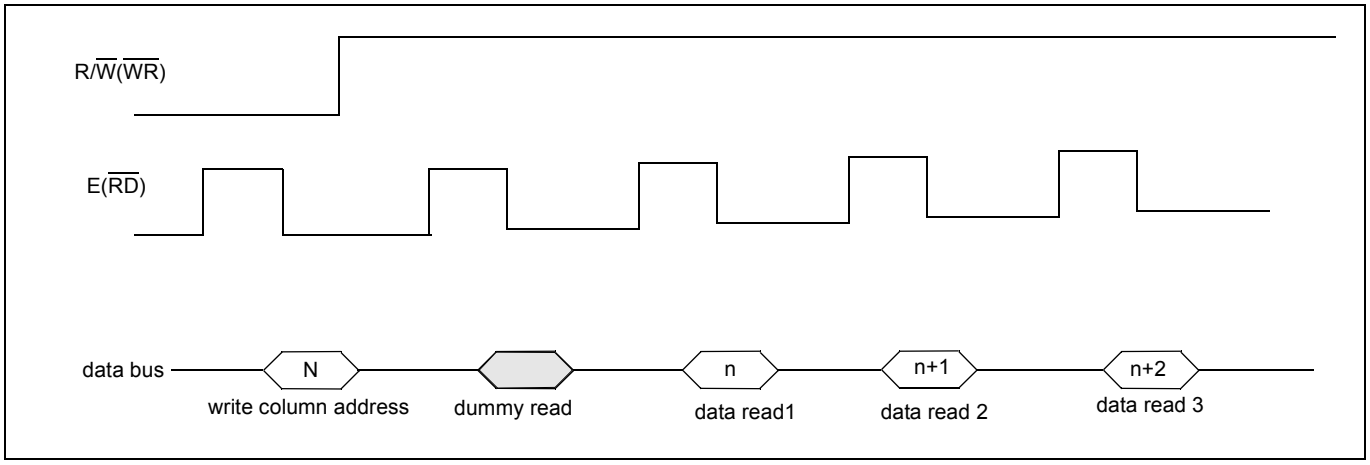


Figure 4 Display data read with the insertion of dummy read

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry(Figure 5) . The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

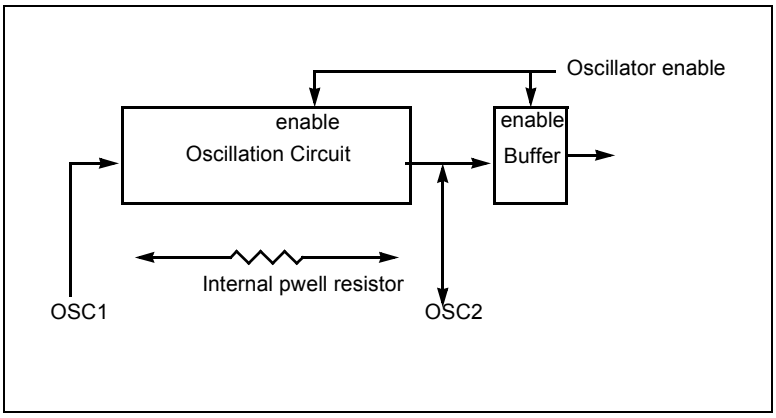


Figure 5 Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. With reference to V_{DD}, it takes a single supply input, V_{SS}, and generate necessary voltage levels. This block consists of:

1. 2X, 3X and 4X DC-DC voltage converter

The built-in DC-DC voltage converter is used to generate the large negative voltage supply with reference to VDD from the voltage input (VSS). It is possible to produce 2X, 3X or 4X boosting from the potential different between V_{SS} - V_{DD}.

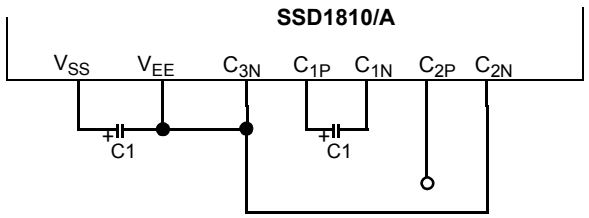
Detail configurations of the DC-DC converter for different boosting multiples are given in Figure 6.

2. Voltage Regulator (Voltages referenced to V_{DD})

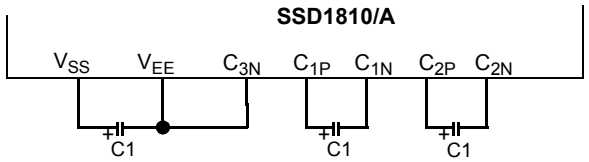
Internal (IRS pin = H) or external (IRS pin = L) feedback gain can control the LCD driving contrast curves.

If internal resistor network is enabled, eight settings can be selected through software command.

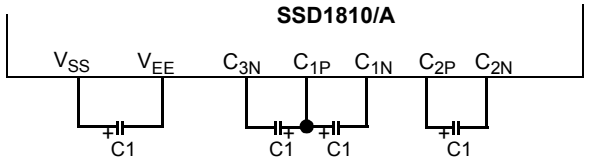
If external control is selected, external resistors are required to be connected between V_{DD} and V_F (R1), and between V_F and V_{L6} (R2). See application circuit diagrams for detail connections.



2X Boosting Configuration



3X Boosting Configuration



4X Boosting Configuration

Remarks:
1. C1 = 0.47 - 1.0uF
2. Boosting input from V_{SS}.
3. 4. All voltages are referenced to V_{DD}

Figure 6 DC-DC Converter Configurations

3. Contrast Control (Voltages referenced to V_{DD})

Software control of the 32 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$$V_{L6} - V_{DD} = Gain * (1 + \frac{Contrast}{\beta}) * V_{ref}$$

$$V_{ref} = (\frac{V_{BE} + R * (V_{DD} - V_{SS})}{1 + R})$$

where

	Ext. Resistor
Gain	$-(1+R_2/R_1)$
β	52.8

and

TC	0 (-0.00%/°C)	2 (-0.15%/°C)	4 (-0.23%/°C)	7 (-0.31%/°C)
V_{BE}	-0.012	0.492	0.490	0.487
R	1.0	0.472	0.269	0.154

*Note: There may be a calculation error of max. 6% when comparing with measurement values.

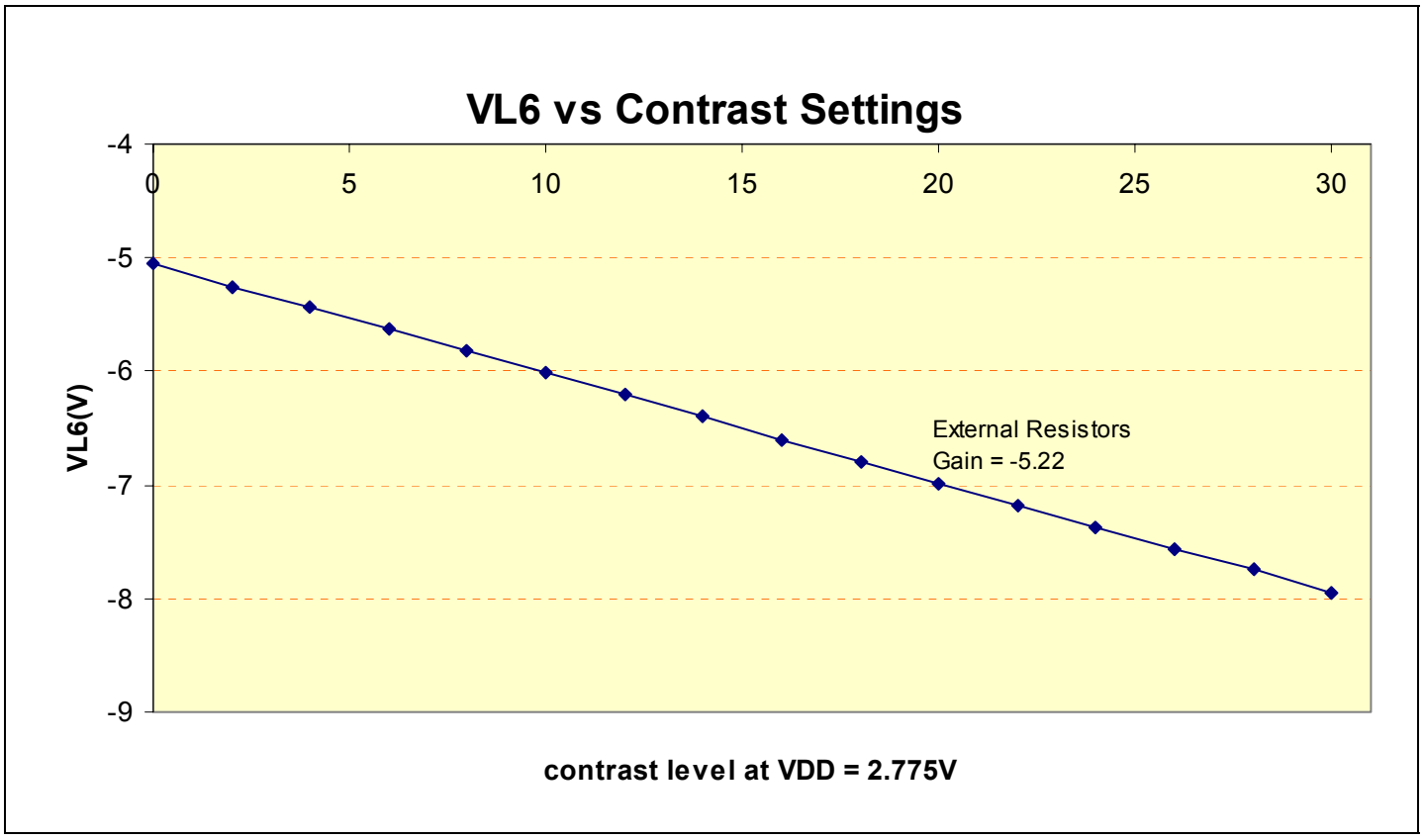


Figure 7 Voltage Regulator Output for Different Contrast Settings (Vop depends on V_{DD})

3. Smart Bias Divider
   Divide the regulator output to give the LCD driving voltages (V_{L2} - V_{L5}). This is a low power consumption circuit which saves most of the display current.
4. Contrast Control (Voltages referenced to V_{DD})
   Software control of 32 voltage levels of LCD voltage.
5. Bias Ratio Selection circuitry
   Software control of 1/4, 1/5, 1/6 and 1/7 bias ratio to match the characteristic of LCD panel.
6. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.23%/^{o}C.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 100x 65= 6500 bits. RAM columns 00H to 0FH are reserved for future use. Only columns 10H to 73H are mapped to segment outputs. Figure 8 on page 16 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided. For vertical scrolling of display, an internal initial line register can be set to control the portion of the RAM data to be mapped to the display. Figure 8 on page 16 shows the case in which the initial line register is set at 38H. No display data will be written when a column address less than 10H is set.

133 Bit Latch

A register carries the display signal information. In 98 X 35 display mode, first 35 bits are Common driving signals and other 98 bits are Segment driving signals. Data will be fed to the HV-buffer Cell and level-shifted to the required level.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

Reset Circuit

When $\overline{RES}$ input is low, the chip is initialized with the following status:

- Display is OFF
- 98X34 Display Display Mode with a Icon Line is set
- Normal segment and display data column address mapping(Mode = 1,SEG0 mapped to address 12H; Mode = 0 SEG0 mapped to address 10H) is set
- Read-modify-write mode is OFF
- Power control register is set at zero
- Shift register data clear in serial interface
- Bias ratio is set at 1/6
- Static indicator is OFF
- Vertical scroll value register is set at 0
- Column address counter is set at 0
- Page address is set at 0
- COM outputs is normal scan direction
- Contrast control register is set at zero
- Test mode is OFF
- Temperature Coefficient is set to TC5
- Smart Icon Mode is disabled.

		Pin Name	SEG0	SEG1	SEG2	.....	SEG98	SEG99
RAM	RAM	Normal	10h	11h	12h	.....	72h	73h
COM	Column	Remapped	73h	72h	71h	.....	11h	10h

00h	Page 0	D0 (LSB)				.....		
01h		D1				.....		
02h		D2				.....		
03h		D3				.....		
04h		D4				.....		
05h		D5				.....		
06h		D6				.....		
07h		D7 (MSB)				.....		
08h	Page 1	D0 (LSB)				.....		
09h		D1				.....		
0Ah		D2				.....		
0Bh		D3				.....		
0Ch		D4				.....		
0Dh		D5				.....		
0Eh		D6				.....		
0Fh		D7 (MSB)				.....		
10h	Page 2	D0 (LSB)				.....		
11h		D1				.....		
12h		D2				.....		
13h		D3				.....		
14h		D4				.....		
15h		D5				.....		
16h		D6				.....		
17h		D7 (MSB)				.....		
18h	Page 3	D0 (LSB)				.....		
19h		D1				.....		
1Ah		D2				.....		
1Bh		D3				.....		
1Ch		D4				.....		
1Dh		D5				.....		
1Eh		D6				.....		
1Fh		D7 (MSB)				.....		
20h	Page 4	D0 (LSB)				.....		
21h		D1				.....		
22h		D2				.....		
23h		D3				.....		
24h		D4				.....		
25h		D5				.....		
26h		D6				.....		
27h		D7 (MSB)				.....		
28h	Page 5	D0 (LSB)				.....		
29h		D1				.....		
2Ah		D2				.....		
2Bh		D3				.....		
2Ch		D4				.....		
2Dh		D5				.....		
2Eh		D6				.....		
2Fh		D7 (MSB)				.....		
30h	Page 6	D0 (LSB)				.....		
31h		D1				.....		
32h		D2				.....		
33h		D3				.....		
34h		D4				.....		
35h		D5				.....		
36h		D6				.....		
37h		D7 (MSB)				.....		
38h	Page 7	D0 (LSB)				.....		
39h		D1				.....		
3Ah		D2				.....		
3Bh		D3				.....		
3Ch		D4				.....		
3Dh		D5				.....		
3Eh		D6				.....		
3Fh		D7 (MSB)				.....		
	Page 8	D0(MSB)				.....		
		D1 (LSB)				.....		

initial line register			
POR		38H	
Normal	Remapped	Normal	Remapped
0	31	8	23
1	30	9	22
2	29	10	21
3	28	11	20
4	27	12	19
5	26	13	18
6	25	14	17
7	24	15	16
8	23	16	15
9	22	17	14
10	21	18	13
11	20	19	12
12	19	20	11
13	18	21	10
14	17	22	9
15	16	23	8
16	15	24	7
17	14	25	6
18	13	26	5
19	12	27	4
20	11	28	3
21	10	29	2
22	9	30	1
23	8	31	0
24	7	x	x
25	6	x	x
26	5	x	x
27	4	x	x
28	3	x	x
29	2	x	x
30	1	x	x
31	0	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	x	x
x	x	0	31
x	x	1	30
x	x	2	29
x	x	3	28
x	x	4	27
x	x	5	26
x	x	6	25
x	x	7	24
ICONS	ICONS	ICONS	ICONS

Note:
In Grey Scale Mode,
MSB is from Page 0 to Page 3
LSB is form Page 4 to Page 7.
In Icons line,
MSB is from the bit 0 of page 8 and
LSB is from the bit 1 of page 8.

Example: (In Grey Mode)

Page 0	D0 (LSB)	0	0	0	....
	D1	0	0	0	....
	D2	0	0	0	....
	D3	0	0	0	....
	D4	1	1	1	....
	D5	1	1	1	....
	D6	1	1	1	....
	D7 (MSB)	1	1	1	....
⋮	⋮	⋮	⋮	⋮	⋮
Page 4	D0 (LSB)	0	0	0	....
	D1	0	0	0	....
	D2	1	1	1	....
	D3	1	1	1	....
	D4	0	0	0	....
	D5	0	0	0	....
	D6	1	1	1	....
	D7 (MSB)	1	1	1	....

LINE 0	BI	BI	BI	....
LINE 1	BI	BI	BI	....
LINE 2	A	A	A	....
LINE 3	A	A	A	....
LINE 4	B	B	B	....
LINE 5	B	B	B	....
LINE 6	C	C	C	....
LINE 7	C	C	C	....
⋮	⋮	⋮	⋮	⋮

Page 8	D0(MSB)	0	0	1	....
	D1 (LSB)	0	1	0	....

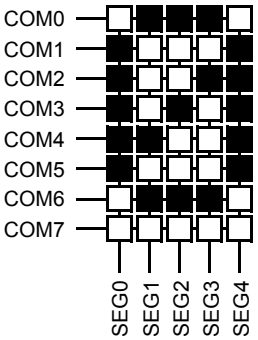
Icons	BI	A	B	....

BI : BLANK (00)
A : COLOR A (01)
B : COLOR B (10)
C : COLOR C (11)

Figure 8 Graphic Display Data RAM (GDDRAM) Address Map

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to LCD panel. The waveforms shown in Figure 6a and 6b illustrate the desired multiplex scheme.



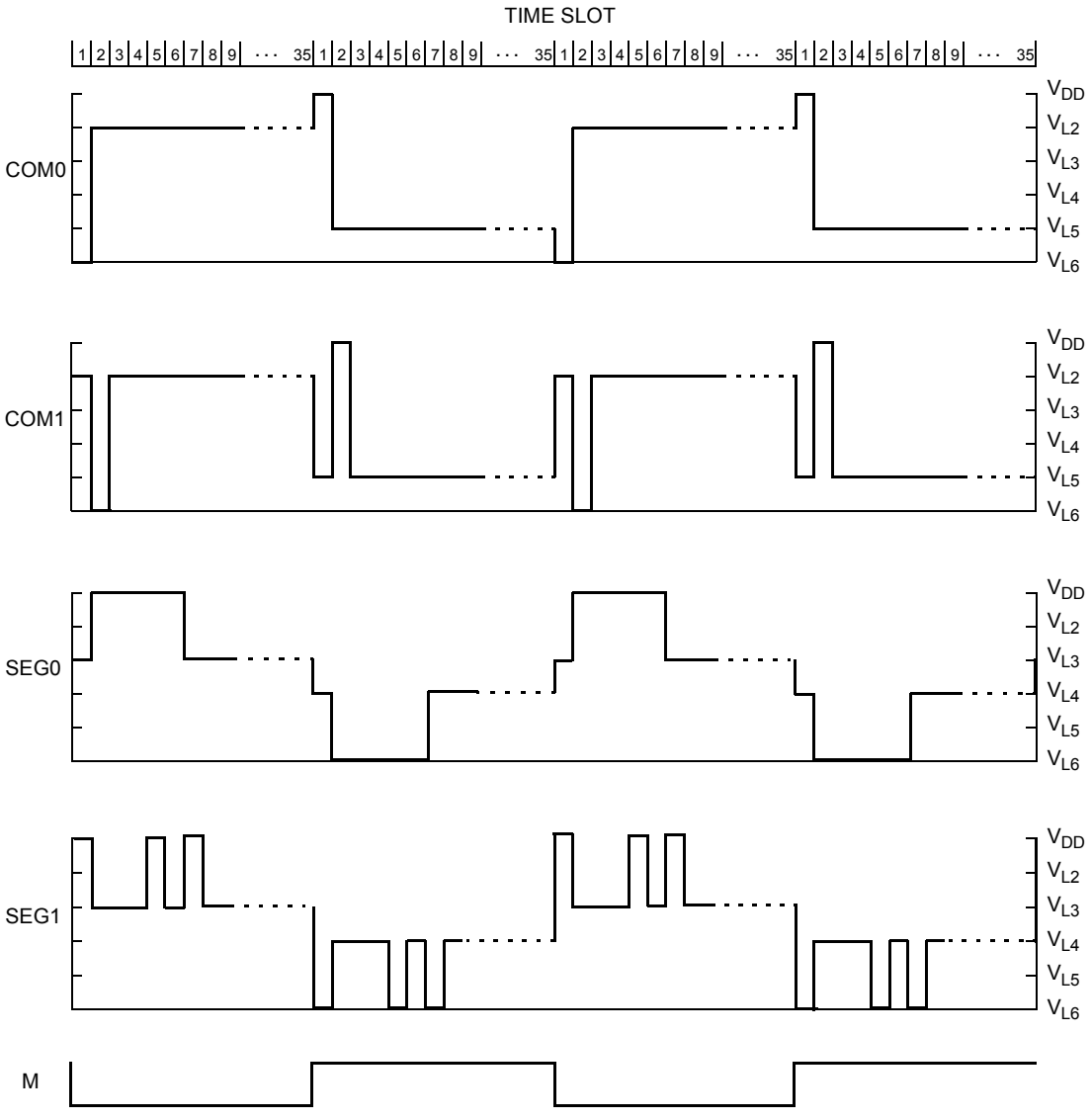


Figure 9 LCD Driving Signal from SSD1810/A

COMMAND TABLE

Table 5 Write Command Table (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=0, E($\overline{RD}$)=1

Bit Pattern	Command	Comment
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the colume address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$00100X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Feedback gain of the internal regulator generating V_{L6} increases as $X_2X_1X_0$ increased from 000b to 111b. After POR, $X_2X_1X_0$ = 100b.
$00101X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
$100X_4X_3X_2X_1X_0$	Set Contrast Control Register	Sets one of 32 available values to the internal contrast control register using $X_4X_3X_2X_1X_0$. Maximum ± 4% V_{L6} output variation among the 32 levels should be considered. Recommend to use level 10010000b [90] as the center contrast control for smaller output variance. The contrast control register is reset to 10000000b after POR.
$1010000X_0$	Set Segment Re-map	When Mode = 1: (34 mux) X_0=0: column address 12H is mapped to SEG2 (POR) X_0=1: column address 71H is mapped to SEG2 When Mode = 0 or NC (32 mux) X_0=0: column address 10H is mapped to SEG0 (POR) X_0=1: column address 73H is mapped to SEG0 See Table 1 on page 4 for detail
$1010001X_0$	Set LCD Bias	X_0=0: 1/6 bias (POR) X_0=1: 1/5 bias
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0~8) for read/write using $X_3X_2X_1X_0$
$1100X_3$***	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode. COM0-33 become COM33-0. See Figure 8 on page 16 for detail mapping
11100000	Set Read-Modify-Write Mode	Read-modify-write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF.
11100010	Software Reset	Initialize the internal status
11101110	Set End of Read-Modify-Write Mode	Exit Read-modify-write mode. Column address before entering the mode will be restored.After POR, Read-modify-write mode is turned OFF.
$1010110X_0$	Set Indicator On/Off	X_0=0: indicator off (POR) X_0=1: indicator on
1111****	Set Test Mode	Reserved for IC testing. Do NOT use
********	Set Power Save Mode (Standby or Sleep)	Standby or sleep mode will be entered using compound commands. Issue compound commands “Set Display Off” followed by “Set Entire display On”.
$01X_5X_4X_3X_2X_1X_0$	Set Vertical Scroll Register	Set the vertical scroll value from 0-63 using $01X_5X_4X_3X_2X_1X_0$ when Vertical Scroll Value Range Register is set to 0. The Vertical Scroll Register is reset to 01000000 after POR.

Table 6 Extended Command Table

Bit Pattern	Command	Description
10101001 $011X_4X_3X_2X_1X_0$	Set Bias Ratio (X_1X_0)	X_1X_0 = 00 : 1/5 or 1/6 X_1X_0 = 01 : 1/7 bias X_1X_0 = 10 : 1/4 bias X_1X_0 = 11 : Reserved for IC testing. Do NOT use
	Set Temperature Coefficient	$X_4X_3X_2$ = 000 : 0.0%/^{o}C (TC0) $X_4X_3X_2$ = 010 : -0.15%/^{o}C (TC2) $X_4X_3X_2$ = 101 : -0.23%/^{o}C (TC5,POR) $X_4X_3X_2$ = 111 : -0.31%/^{o}C (TC7) $X_4X_3X_2$ = 001, 011, 100, 110 : Reserved
$1010101X_0$	Set Grey scale / mono display mode	X_0 = 0 : mono (POR) X_0 = 1 : Grey Scale If Grey scale mode is selected, there are four grey level which can be selected by two bits. The MSB is from page 0 to page 3, bit 0 of page 8 and the LSB is from page 4 to page 7, bit 1 of page 8. The grey level of the 3 color (Color A, B, C) is defined by another separated command (Set Grey Level Control). example: MSB, LSB = 00 : Blank (1/16) MSB, LSB = 01 : Color A (5/16) MSB, LSB = 10 : Color B (11/16) MSB, LSB = 11 : Color C (16/16) See Figure 8 on page 16 for detail.
$1101X_3X_2X_1X_0$ $****X_dX_cX_bX_a$	Set Grey Level Control	Select a color $X_3X_2X_1X_0$ = 0111 Color A (POR 16/16) $X_3X_2X_1X_0$ = 1000 Color B (POR 16/16) $X_3X_2X_1X_0$ = 1001 Color C (POR 16/16) Set the Grey level of a color $X_dX_cX_bX_a$ = 0000 1/16 $X_dX_cX_bX_a$ = 0001 2/16 : : : $X_dX_cX_bX_a$ = 1110 15/16 $X_dX_cX_bX_a$ = 1111 16/16 See an example on page 22 for setting grey level control.
11010010 $0X_6X_500100$	Set 4- / 6-Phases Smart-Icon Mode	X_6X_5 = 00 : 4 phases (1.8V to 2.2V) X_6X_5 = 01 : 6 phases (2.2V to 2.6V) POR X_6X_5 = 10 : Reserved for IC testing. Do NOT use X_6X_5 = 11 : Reserved for IC testing. Do NOT use
$1101000X_0$	Set Smart Icon Mode On/OFF	X_0 = 0 : normal display mode X_0 = 1 : smart icon mode
11011100 $0000000X_0$	Option for Vop dependent V_{DD}	X_0 = 0 : Vop dependent V_{DD} (POR) X_0 = 1 : Vop independent V_{DD}

Table 7 Read Command Table (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=1, E=1($\overline{RD}$=0))

$D_7D_6D_5D_4D_3D_2D_1D_0$	Read Status Register	D_7=0: indicates the driver is ready for command. D_7=1: indicates the driver is Busy. D_6=0: indicates normal segment mapping with column address D_6=1: indicates reverse segment mapping with column address D_5=0: indicates the display is ON. D_5=1: indicates the display is OFF. D_4=0: initialization is completed. D_4=1: initialization process is in progress after $\overline{RES}$ or software reset. $D_3D_2D_1D_0$ = 1010, these 4-bit is fixed to 1010 which could be used to identify as Solomon Systech Device.

Note : Patterns other than that given in Command Table and Extended Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided in serial interface mode.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode.

Also, a dummy read is required before first valid data is read. See Figure 4 on page 12 in Functional Block Descriptions section for detail waveform diagram.

To write data to the GDDRAM, input Low to R/$\overline{W}$($\overline{WR}$) pin and High to D/$\overline{C}$ pin for both 6800-series and 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

It should be noted that, after the automatic column address increment, the pointer will NOT wrap round to 0 when overflow (>97 when mode is 0 or >99 when mode is 1). The increment of the pointer stops at 97 or 99, so manual adjustment may be needed to set column address pointer.

Table 8 Automatic Address Increment

D/$\overline{C}$	R/$\overline{W}$($\overline{WR}$)	Action	Auto Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

*1. If read data is issued in read-modify-write mode, address pointer will not be increased automatically.

Command Description

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power relating sub-circuits could be turned on/off by this command.

Internal voltage booster is used to generated the large negative voltage supply (V_{EE}) from the voltage input (V_{SS} - V_{DD}). An external negative power supply is required if this option is turned off.

Internal regulator is used to generate the LCD driving voltage. V_{L6}, from the negative power supply, V_{EE}.

Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, V_{L6}. External voltage sources should be fed into this driver if this circuit is turned off.

Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing the LCD drive voltage, V_{L6}, provided by the On-Chip power circuits. V_{L6} is set with 32 steps (5-bit) in the contrast control register by a compound commands.

Set Segment Re-map

This command changes the mapping between the display data column addresses and segment drivers. It allows flexibility in mechanical layout of LCD glass design. Please refer to Figure 8 on page 16 for example.

Set LCD Bias

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use.

The selectable values of this command is 1/6 or 1/5.

For other bias ratio settings, extended commands should be used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be selected regardless of the contents of the GDDRAM. In addition, this command has higher priority than the normal/inverse display.

This command is used together with “Set Display Display ON/OFF” command to form a compound command for entering power save mode. See “Set Power Save Mode” later in this section.

Set Normal/Inverse Display

This command turns the display to be either normal or inversed. In normal display, RAM data of 1 indicates an illumination on the corresponding pixel, while in inversed display, RAM data of 0 will turn on the pixel.

It should be noted that the icon line will not affect, that is not be reversed, by this command.

Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered. See “Set Power Save Mode” later in this section for details.

Set Page Address

This command enters the page address from 0 to 8 to the RAM pager register for read/write operations. Please refer to Figure 8 on page 16.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. See Figure 8 on page 16 for the relationship between turning on or off of this feature.

In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. column address is saved before entering the mode
2. column address is increased only after display data write but not after display data read.

This Ready-Modify-Write mode is used to save the MCU’s loading when a very portion of display area is being updated frequently.

As reading the data will not change the column address, it could be get back from the chip and do some operation in the MCU. Then the updated data could be write back to the GDDRAM with automatic address increment.

After updating the area, “Set End of Read-Modify-Write Mode” is sent to restore the column address and ready for next update sequence.

Software Reset

Issuing this command causes some of the chip’s internal status registers to be initialized:

- Static indicator is OFF
- Vertical scroll register is set at zero
- Column address counter is set at zero
- Page address is set at zero
- Normal scan direction of the COM outputs
- Contrast control register is set at zero
- Test mode is OFF

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address before entering read-modify-write mode will be restored no matter how much modification during the read-modify-write mode.

Set Indicator On/Off

This command turns on or off the drive indicators.

When the “Set Indicator On” command is sent, the second command byte “Indicator Display Mode” must follow. However, the “Set Indicator Off” command is a single byte command and no second byte command is required.

The status of static indicator also controls whether standby mode or sleep mode will be entered, after issuing the power save compound command. See “Set Power Save Mode” later in this section.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, users should NOT apply this command.

Set Power Save Mode

Entering Standby or Sleep Mode should be done by using a compound command composed of “Set Display ON/OFF” and “Set Entire Display ON/OFF” commands. When “Set Entire Display ON” is issued when display is OFF, either Standby Mode or Sleep Mode will be entered.

The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

- Internal oscillator and LCD power supply circuits are stopped
- Segment and Common drivers output V_{DD} level
- The display data and operation mode before sleep are held
- Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except:

- Internal oscillator is on
- Static icon is on

Please also be noted that during Standby Mode, if the software reset command is issued, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

Status register Read

This command is issued by pulling D/$\overline{C}$ Low during a data read (refer to Figure 10 on page 26 and Figure 11 on page 27 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip.

No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

Set Temperature Coefficient (TC) Value

4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades. Please refer to the extended command table, Table 6 on page 19 for detail TC values.

Set Grey scale / mono display mode

This command is used to set the grey scale or mono display mode. If grey scale mode is set, the grey level is selected by two bits. The MSB is from page 0 to page 3, bit 0 of page 8 and the LSB is from page 4 to page 7, bit 1 of page 8

Set Grey Level Control

This command is to set the grey level of the three color(A, B and C). There can be adjusted to 15 grey scale levels form 1/16 to 16/16 (1/16 is lightest, 16/16 is the darkest).

Set 4- / 6-Phase Smart-Icon Mode

This command is to set 4-Phase or 6-Phase smart icon modes which for lower V_{DD} or higher V_{on} of panel.

Set Smart Icon Mode ON/OFF

This command is to switch on/off the low-current Icon Display Mode.

Set Vertical Scroll Register

This command is used to scroll the screen vertically by selecting a scroll value from 0 to 63. With scroll value equals to 0, D0 of Page 0 is mapped to COM0. With scroll value equals to 1, D1 of Page0 is mapped to COM0. The vertical scroll values of 0 to 63 are assigned to Page 0 to 7. ICONs is not affected by this command. Refer toFigure 8 on page 16.

Example for setting grey level control

Command	Remark:
1. 10101011	set grey scale mode
2. 11010111	Select color A
3. 00000000	set the grey level to 1/16
4. 11011000	Select color B
5. 00000110	set the grey level to 7/16
6. 11011001	Select color C
7. 00001111	set the grey level to 16/16

- Fill display data into Graphic Display RAM

MAXIMUM RATINGS

Table 9 MAXIMUM RATINGS* (Voltages Reference to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{EE}		-2.4 to -12	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS

Table 10 ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Voltage Reference to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=-30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range Voltage Generator Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.4	3.0	3.5	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 3.0V, Voltage Generator On, 4X Converter Enabled, Write accessing, T_{cyc} = 3.3MHz, Osc. Freq.=22kHz, Display On.	-	200	400	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 3.0V, V_{EE} = -8V, Voltage Generator On, DC-DC Converter Disabled, R/$\overline{W}$($\overline{WR}$) Halt, Osc. Freq. = 22kHz, Display On, V_{L6} - V_{DD} = -8V.	-	25	70	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 3.0V, V_{EE} = -5V, Voltage Generator On, DC-DC Converter Enabled, R/$\overline{W}$($\overline{WR}$) Halt, Osc. Freq. = 22kHz, Display On, V_{L6} - V_{DD} = -8V.	-	120	200	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD}=3.0V, LCD Driving Waveform Off, Osc. Freq. = 22kHz, R/$\overline{W}$($\overline{WR}$) halt.	-	5	10	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 3.0V, LCD Driving Waveform Off, Oscillator Off, R/$\overline{W}$($\overline{WR}$) halt.	-	0.2	5	µA
I_{ICON}	Icon Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 3.0V, Voltage Generator On, Osc. Freq. = 22kHz, Display On. V_{L6} - V_{DD} = -8V.	-	7	15	µA
V_{EE}	LCD Driving Voltage Generator Output (V_{EE} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	-12.0	-	-2.4	V
V_{LCD}	LCD Driving Voltage Input (V_{EE} Pin)	Voltage Generator Disabled.	-12.0	-	-2.4	V
V_{OH1}	Logic High Voltage	I_{out}=-100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Voltage	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control)	V_{EE}-0.5	-	V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disabled	-	Floating	-	V

Table 10 ELECTRICAL CHARACTERISTICS(Unless otherwise specified, Voltage Reference to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=-30 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Logic High Input voltage ($\overline{RES}$, D_0-D_7,R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage ($\overline{RES}$, $\overline{CE}$, D_0-D_7, R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, S/$\overline{P}$)		0	-	0.2*V_{DD}	V
V_{L2}	LCD Display Voltage Output	Voltage reference to V_{DD}, Smart Bias Divider Enabled, 1:a bias ratio	-	1/a*V_{L6}	-	V
V_{L3}	(V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)		-	2/a*V_{L6}	-	V
V_{L4}			-	(a-2)/a*V_{L6}	-	V
V_{L5}			-	(a-1)/a*V_{L6}	-	V
V_{L6}			-	V_{L6}	-	V
V_{L2}	LCD Display Voltage Input	Voltage reference to V_{DD}, External Voltage Generator, Smart Bias Divider Disabled	V_{L3}	-	V_{DD}	V
V_{L3}	(V_{L2}, V_{L3},V_{L4}, V_{L5}, V_{L6} Pins)		V_{L4}	-	V_{L2}	V
V_{L4}			V_{L5}	-	V_{L3}	V
V_{L5}			V_{L6}	-	V_{L4}	V
V_{L6}			-12V	-	V_{L5}	V
I_{OH}	Logic High Output Current Source (D_0-D_7, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain (D_0-D_7, OSC2)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source (D_0-D_7, OSC2)		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current ($\overline{RES}$, D_0-D_7, R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, S/$\overline{P}$)		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
ΔV_{L6}	Variation of V_{L6} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	± 4	-	%
	Temperature Coefficient Compensation					
TC0	Flat Temperature Coefficient	Voltage Regulator Enabled	-	0.0	-0.075	%/°C
TC2	Temperature Coefficient 2*	Voltage Regulator Enabled	-0.075	-0.15	-0.18	%/°C
TC5	Temperature Coefficient 5* (POR)	Voltage Regulator Enabled	-0.18	-0.23	-0.27	%/°C
TC7	Temperature Coefficient 7*	Voltage Regulator Enabled	-0.27	-0.31	-	%/°C

* The formula for the temperature coefficient is:

$$TC(\%)= \frac{V_{ref} \text{ at } 50°C - V_{ref} \text{ at } 0°C}{50°C - 0°C} \times \frac{1}{V_{ref} \text{ at } 25°C} \times 100\%$$

Table 11 AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage reference to V_{SS}, AV_{DD}=DV_{DD}=3V: unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	Internal Oscillator Enabled	15	17.5	20	kHz
F_{FRM}	Frame Frequency	Display ON, Set 98 X 34 Graphic Display Mode with a Icon Line	-	$\frac{F_{OSC}}{8*35}$	-	Hz
		Display ON, Set 100 X 32 Graphic Display Mode with a Icon Line	-	$\frac{F_{OSC}}{8*33}$	-	Hz

Table 12 6800-Series MPU Parallel Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	450	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	140 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	140 200	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

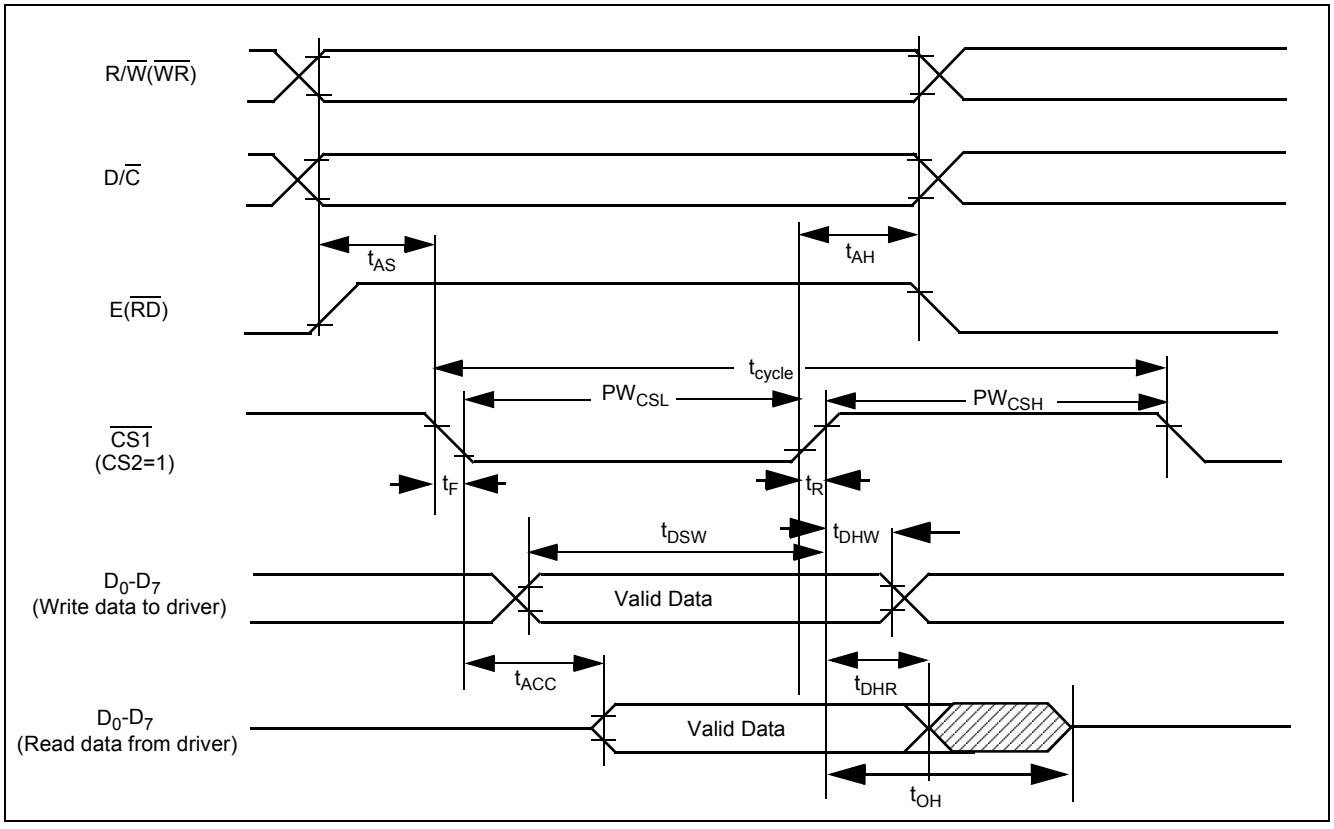


Figure 10 Parallel 6800-series Interface Timing Characteristics

Table 13 8080-Series MUP Parallel Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	450	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{DSW}	Write Data Setup Time	20	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	140	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	140	-	-	ns
	Chip Select High Pulse Width (write)	200	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

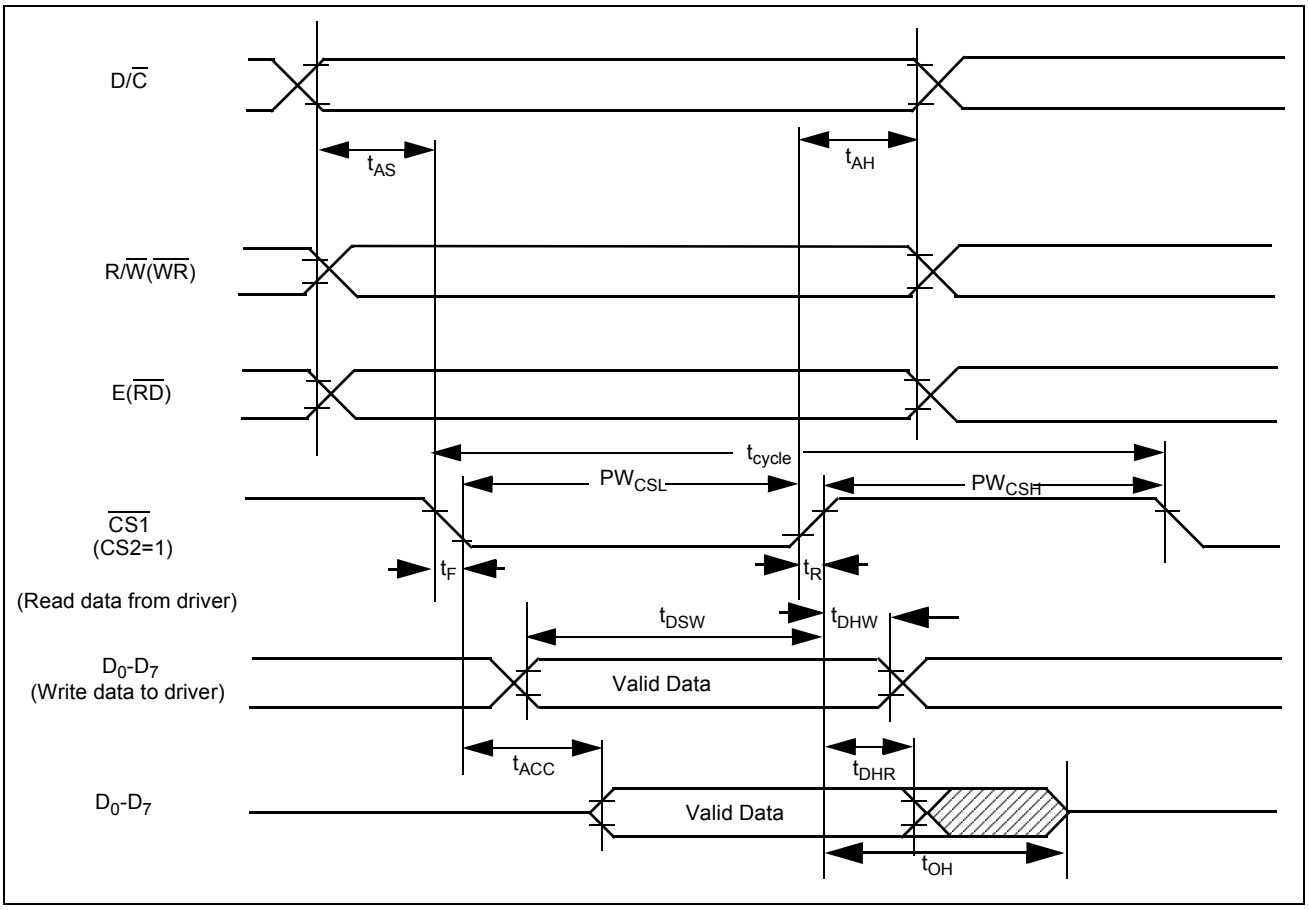


Figure 11 8080-series Parallel Interface Timing Characteristics

Table 14 Serial Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	1000	-	-	ns
t_{AS}	Address Setup Time	500	-	-	ns
t_{AH}	Address Hold Time	500	-	-	ns
t_{CSS}	Chip Select Setup Time	60	-	-	ns
t_{CSH}	Chip Select Hold Time	800	-	-	ns
t_{DSW}	Write Data Setup Time	250	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	300	-	-	ns
t_{CLKH}	Clock High Time	300	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

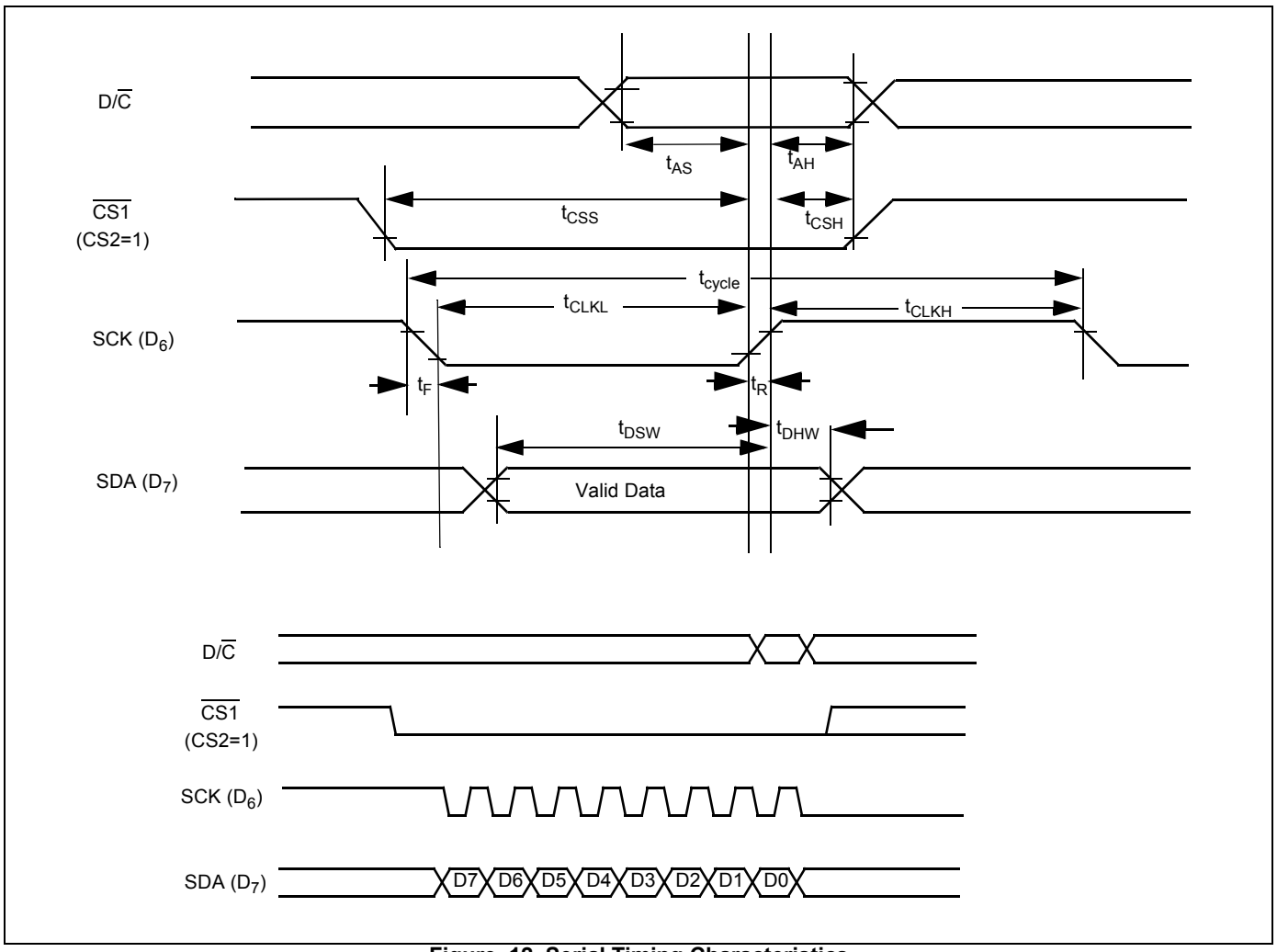
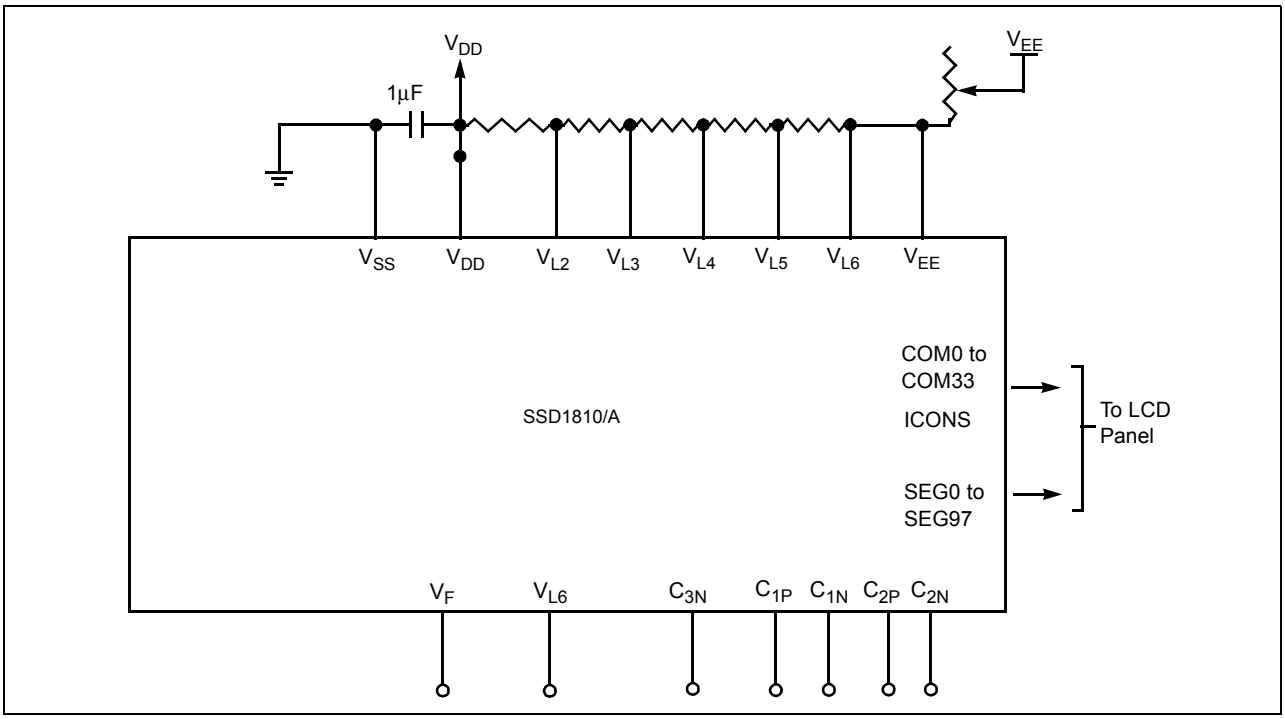


Figure 12 Serial Timing Characteristics

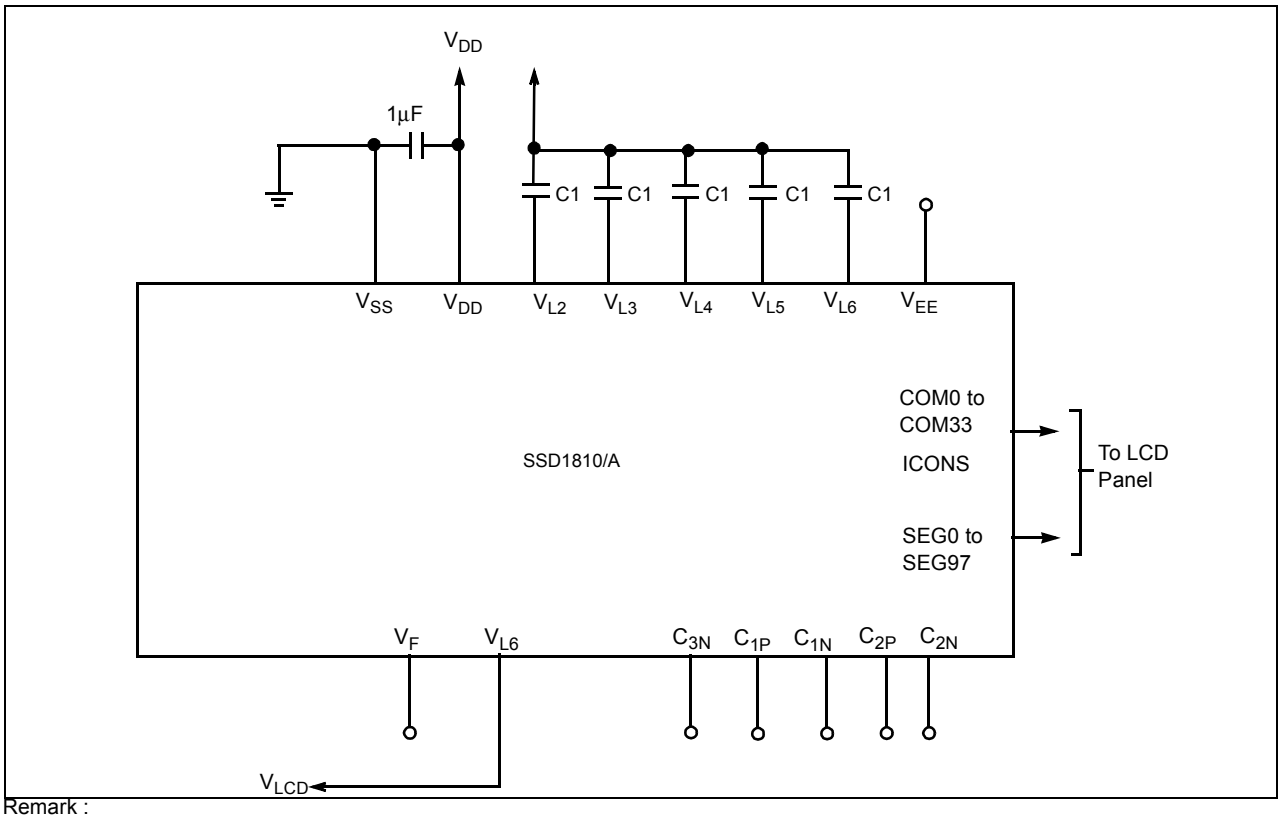
APPLICATIN EXAMPLES

Figure 13 All External Power Supply

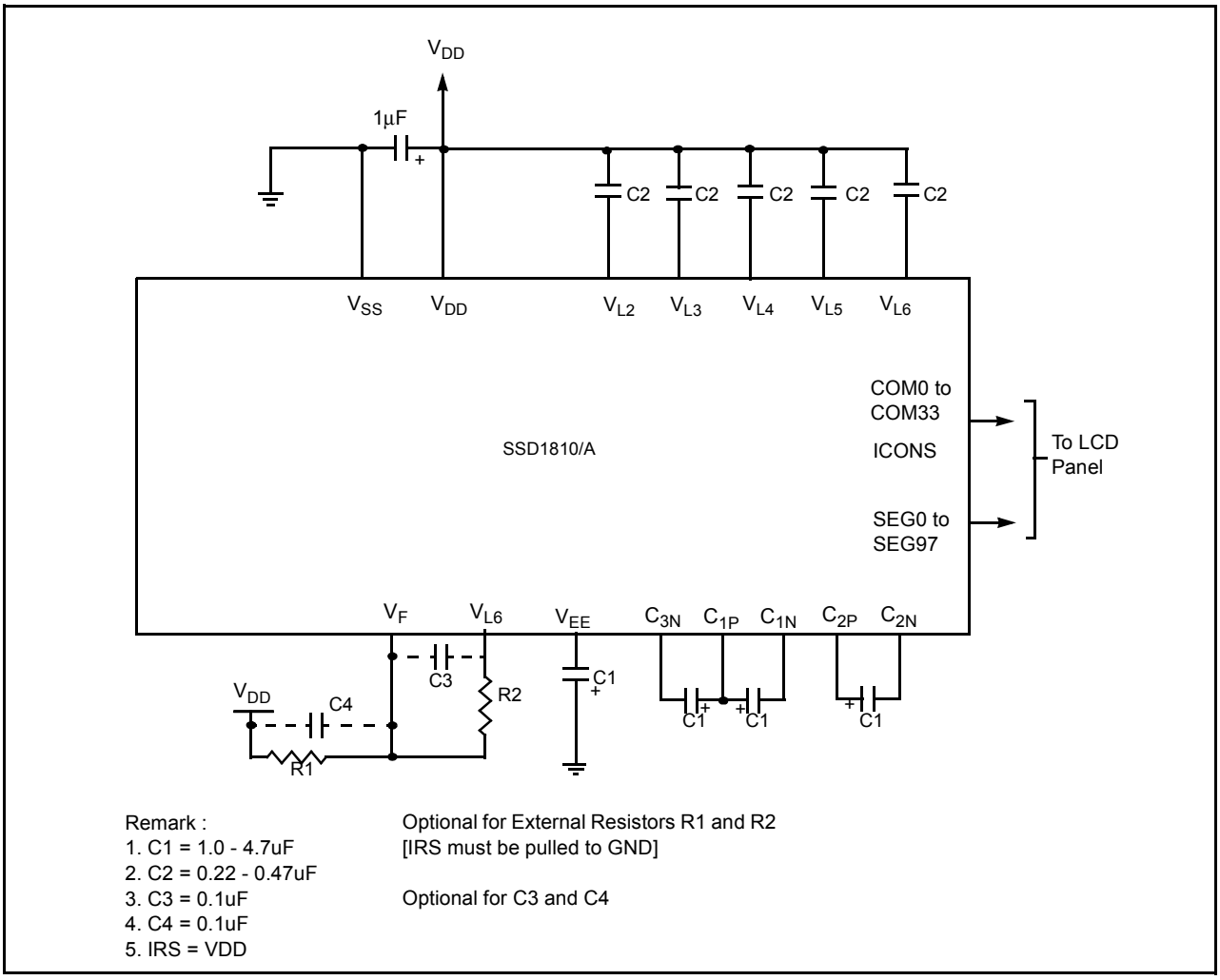


Remark :
1. $\overline{RES}$ should be at a known state.
2. R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, D_0-D_2 and D_5-D_6 can be open for SPI serial mode.

Figure 14 Internal Divider Only



Remark :
1. C1 = 0.22 - 0.47uF

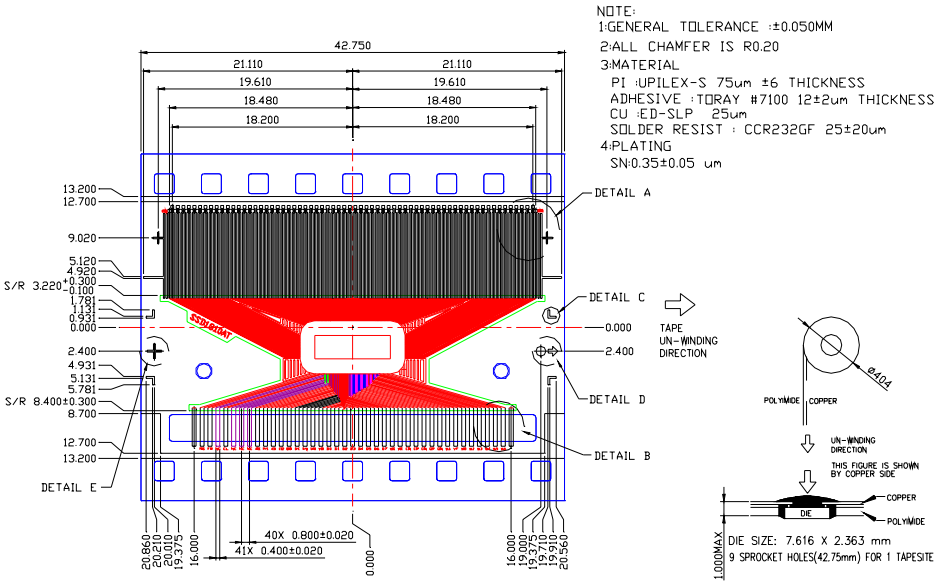


Remark :
1. C1 = 1.0 - 4.7uF
2. C2 = 0.22 - 0.47uF
3. C3 = 0.1uF
4. C4 = 0.1uF
5. IRS = VDD

Optional for External Resistors R1 and R2
[IRS must be pulled to GND]

Optional for C3 and C4

Figure 15 Application Circuit (4x DC-DC Converter)



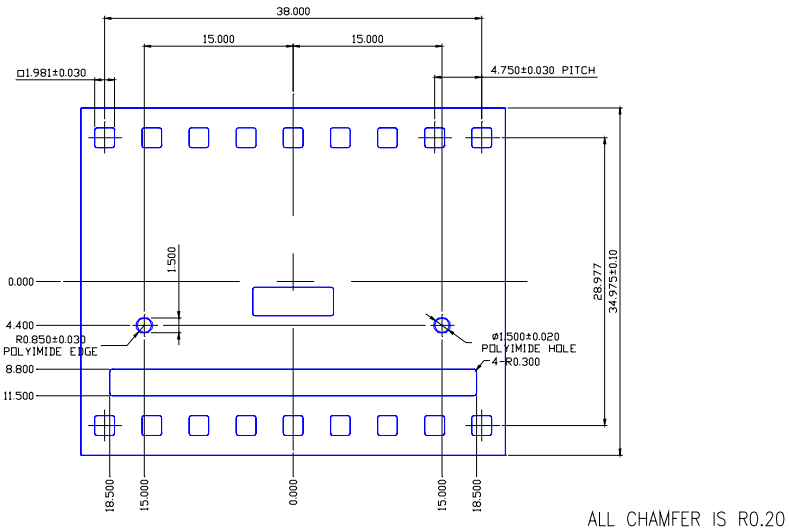


Figure 16 SSD1810AT TAB Drawing 1/2

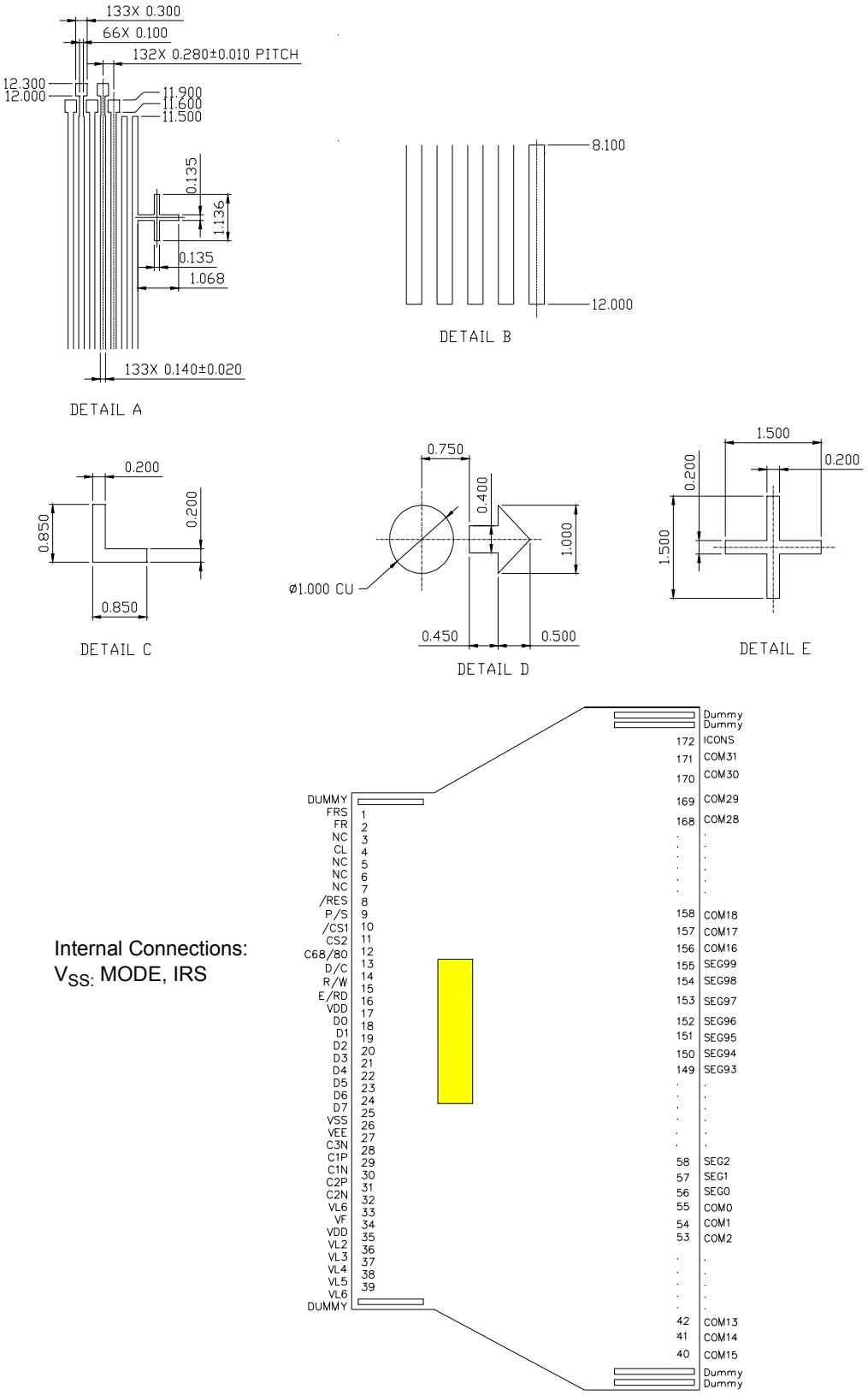
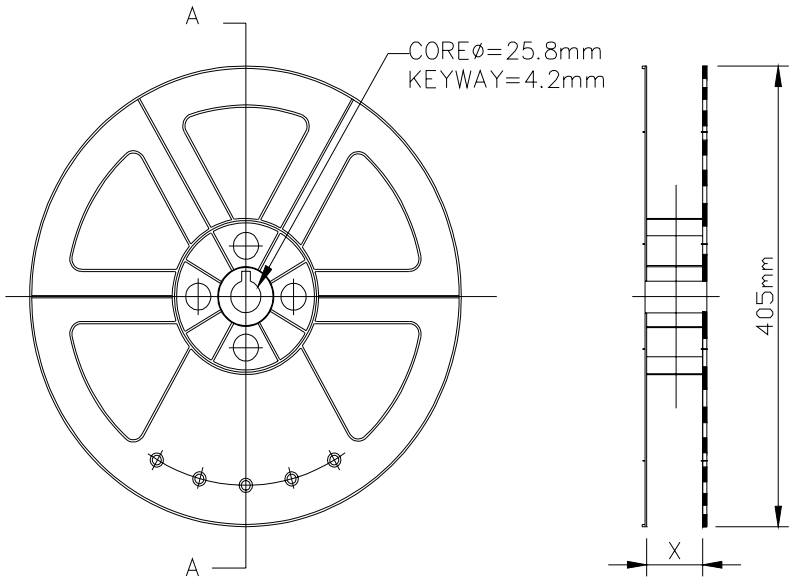


Figure 17 SSD1810AT TAB Drawing 2/2



FORMAT	35mm	48mm	70mm
X(±0.5)	37mm	50mm	72mm

TAPE LENGTH=40m

MATERIAL: HIGH IMPACT POLYSTYRENE (HIPS)

SURFACE RESISTIVITY: $1X10^{5}$ OHM MIN
$1X10^{9}$ OHM MAX

Figure 18 TAB Wheel Mechanical Drawing