

## TABLE OF CONTENTS

1	GENERAL DESCRIPTION.....	1
2	FEATURES .....	1
3	ORDERING INFORMATION .....	1
4	BLOCK DIAGRAM.....	2
5	SSD1882Z DIE PAD COORDINATE .....	3
6	SSD1882T1 TAB PIN ASSIGNMENT.....	6
7	PIN DESCRIPTION .....	8
	VDD_ROW.....	8
	+V1, VC, -V1 .....	8
	YD .....	8
	LP.....	8
	FR .....	8
	F1, F2.....	8
	DOFF# .....	8
	SEL .....	8
	CIO1, CIO2 .....	8
	SHL .....	8
	LSEL.....	9
	CSEL.....	9
	TEST1 .....	9
	TEST2.....	9
	COM0 – COM239 .....	9
8	FUNCTIONAL BLOCK DESCRIPTIONS .....	10
8.1	Controller and Data Register .....	10

8.2	Bi-directional Shift Register.....	10
8.3	Common Cell Level Shifter .....	10
9	MAXIMUM RATINGS .....	15
10	DC CHARACTERISTICS .....	16
11	AC CHARACTERISTICS .....	17
12	PRECAUTION .....	19
13	APPLICATION EXAMPLE.....	21
14	SSD1882T1 TAB PACKAGE DRAWING .....	23

# SSD1882

## *Advance Information*

### **240 Outputs MLA Row (Common) Driver CMOS**

#### **1 General Description**

The SSD1882 is an MLA (Multi Line Addressing) common driver equipped with 240 low resistance triple-value outputs. Combining with MLA power chip and MLA column driver (\*), an MLA LCD module system having high picture quality, high speed responses and low power consumption can be produced.

(\*) Please refer to SSL MLA product list or application note for the MLA chipset product information.

#### **2 FEATURES**

- 4-line MLA driving scheme
- Power supply to logic system, 2.7V - 5.5V
- LCD drive voltage, 14V - 30V
- 200 or 240 common outputs
- 1/2P and 1P operation mode
- Adjustable LCD power source offset bias
- Non-biased display off function
- Pin selectable output shift direction
- Cascade supported
- Available in TAB (Tape Automated Bonding) and Gold bump die package

#### **3 ORDERING INFORMATION**

**Table 1 - Ordering Information**

Ordering Part Number	Outer lead pitch	Package Form
SSD1882Z	N/A	Gold Bump Die
SSD1882T1R1	0.21mm	TAB

This document contains information on a new product. Specifications and information herein are subject to change without notice.  
IC manufactured under Motif license including U.S. Patent No. 5,420,604

## 4 BLOCK DIAGRAM

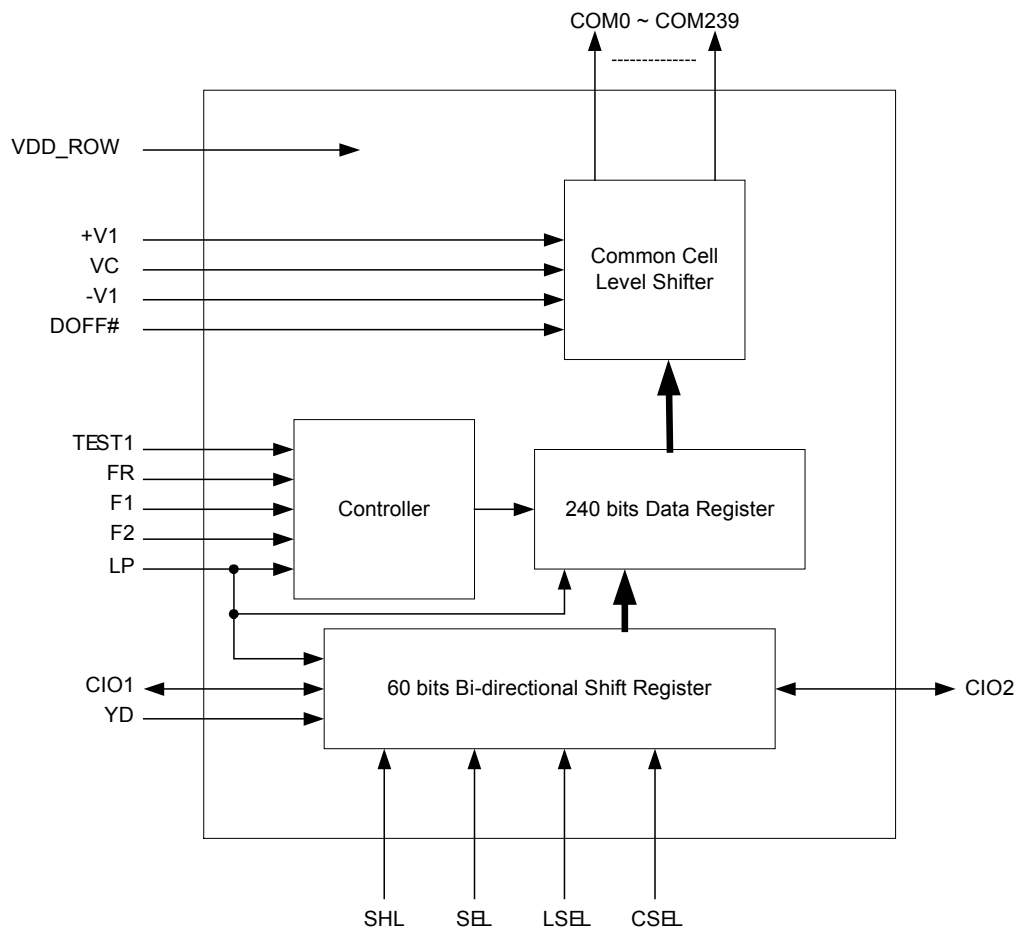


Figure 1 – SSD1882 Block Diagram

## 5 SSD1882Z Die Pad Coordinate

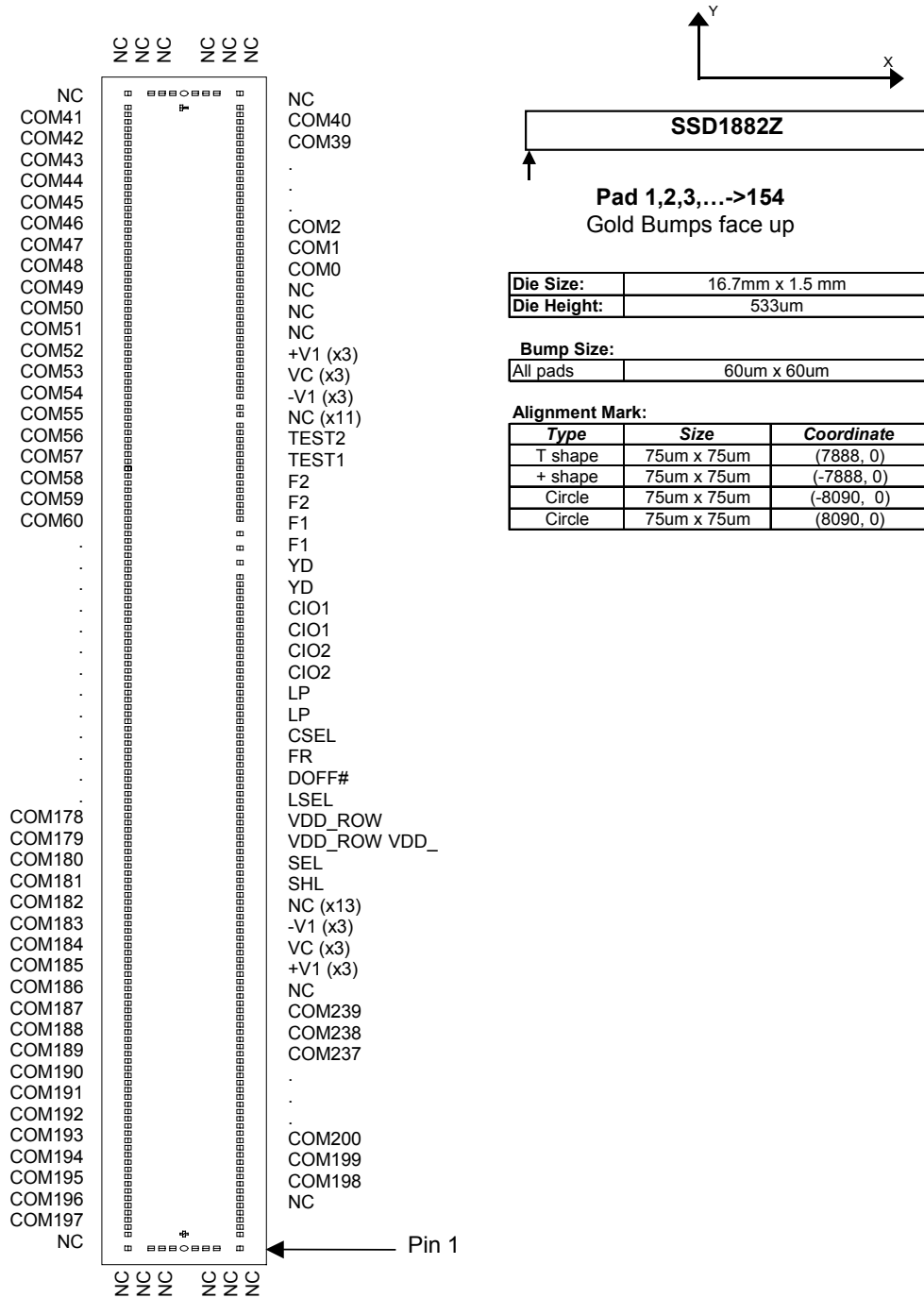


Figure 2 - SSD1882Z Die Pad Assignment

**Table 2 - SSD1882Z Die Pad Coordinates**

PAD #	PIN NAME	X-POS	Y-POS	PAD #	PIN NAME	X-POS	Y-POS	PAD #	PIN NAME	X-POS	Y-POS
1	NC	-8090.3	-526.6	61	NC	-1922.8	-526.6	121	COM8	4655.2	-526.6
2	COM198	-7893.6	-526.6	62	NC	-1821.6	-526.6	122	COM9	4756.4	-526.6
3	COM199	-7792.4	-526.6	63	NC	-1720.4	-526.6	123	COM10	4857.6	-526.6
4	COM200	-7691.2	-526.6	64	NC	-1619.2	-526.6	124	COM11	4958.8	-526.6
5	COM201	-7590.0	-526.6	65	NC	-1518.0	-526.6	125	COM12	5060.0	-526.6
6	COM202	-7488.8	-526.6	66	NC	-1416.8	-526.6	126	COM13	5161.2	-526.6
7	COM203	-7387.6	-526.6	67	SHL	-1315.6	-526.6	127	COM14	5262.4	-526.6
8	COM204	-7286.4	-526.6	68	SEL	-1214.4	-526.6	128	COM15	5363.6	-526.6
9	COM205	-7185.2	-526.6	69	VDD ROW	-1113.2	-526.6	129	COM16	5464.8	-526.6
10	COM206	-7084.0	-526.6	70	VDD ROW	-1012.0	-526.6	130	COM17	5566.0	-526.6
11	COM207	-6982.8	-526.6	71	VDD ROW	-910.8	-526.6	131	COM18	5667.2	-526.6
12	COM208	-6881.6	-526.6	72	LSEL	-809.6	-526.6	132	COM19	5768.4	-526.6
13	COM209	-6780.4	-526.6	73	DOFF#	-708.4	-526.6	133	COM20	5869.6	-526.6
14	COM210	-6679.2	-526.6	74	FR	-607.2	-526.6	134	COM21	5970.8	-526.6
15	COM211	-6578.0	-526.6	75	CSEL	-506.0	-526.6	135	COM22	6072.0	-526.6
16	COM212	-6476.8	-526.6	76	LP	-404.8	-526.6	136	COM23	6173.2	-526.6
17	COM213	-6375.6	-526.6	77	LP	-303.6	-526.6	137	COM24	6274.4	-526.6
18	COM214	-6274.4	-526.6	78	CIO2	-202.4	-526.6	138	COM25	6375.6	-526.6
19	COM215	-6173.2	-526.6	79	CIO2	-101.2	-526.6	139	COM26	6476.8	-526.6
20	COM216	-6072.0	-526.6	80	CIO1	0.0	-526.6	140	COM27	6578.0	-526.6
21	COM217	-5970.8	-526.6	81	CIO1	101.2	-526.6	141	COM28	6679.2	-526.6
22	COM218	-5869.6	-526.6	82	YD	202.4	-526.6	142	COM29	6780.4	-526.6
23	COM219	-5768.4	-526.6	83	YD	303.6	-526.6	143	COM30	6881.6	-526.6
24	COM220	-5667.2	-526.6	84	F1	404.8	-526.6	144	COM31	6982.8	-526.6
25	COM221	-5566.0	-526.6	85	F1	506.0	-526.6	145	COM32	7084.0	-526.6
26	COM222	-5464.8	-526.6	86	F2	607.2	-526.6	146	COM33	7185.2	-526.6
27	COM223	-5363.6	-526.6	87	F2	708.4	-526.6	147	COM34	7286.4	-526.6
28	COM224	-5262.4	-526.6	88	TEST1	809.6	-526.6	148	COM35	7387.6	-526.6
29	COM225	-5161.2	-526.6	89	TEST2	910.8	-526.6	149	COM36	7488.8	-526.6
30	COM226	-5060.0	-526.6	90	NC	1012.0	-526.6	150	COM37	7590.0	-526.6
31	COM227	-4958.8	-526.6	91	NC	1113.2	-526.6	151	COM38	7691.2	-526.6
32	COM228	-4857.6	-526.6	92	NC	1214.4	-526.6	152	COM39	7792.4	-526.6
33	COM229	-4756.4	-526.6	93	NC	1315.6	-526.6	153	COM40	7893.6	-526.6
34	COM230	-4655.2	-526.6	94	NC	1518.0	-526.6	154	NC	8090.3	-526.6
35	COM231	-4554.0	-526.6	95	NC	1720.4	-526.6	155	NC	8090.3	-308.2
36	COM232	-4452.8	-526.6	96	NC	1922.8	-526.6	156	NC	8090.3	-207.0
37	COM233	-4351.6	-526.6	97	NC	2125.2	-526.6	157	NC	8090.3	-105.8
38	COM234	-4250.4	-526.6	98	NC	2226.4	-526.6	158	NC	8090.3	105.8
39	COM235	-4149.2	-526.6	99	NC	2327.6	-526.6	159	NC	8090.3	207.0
40	COM236	-4048.0	-526.6	100	NC	2428.8	-526.6	160	NC	8090.3	308.2
41	COM237	-3946.8	-526.6	101	-V1	2530.0	-526.6	161	NC	8090.3	526.6
42	COM238	-3845.6	-526.6	102	-V1	2631.2	-526.6	162	COM41	7893.6	526.6
43	COM239	-3744.4	-526.6	103	-V1	2732.4	-526.6	163	COM42	7792.4	526.6
44	NC	-3643.2	-526.6	104	VC	2833.6	-526.6	164	COM43	7691.2	526.6
45	+V1	-3542.0	-526.6	105	VC	2934.8	-526.6	165	COM44	7590.0	526.6
46	+V1	-3440.8	-526.6	106	VC	3036.0	-526.6	166	COM45	7488.8	526.6
47	+V1	-3339.6	-526.6	107	+V1	3137.2	-526.6	167	COM46	7387.6	526.6
48	VC	-3238.4	-526.6	108	+V1	3238.4	-526.6	168	COM47	7286.4	526.6
49	VC	-3137.2	-526.6	109	+V1	3339.6	-526.6	169	COM48	7185.2	526.6
50	VC	-3036.0	-526.6	110	NC	3440.8	-526.6	170	COM49	7084.0	526.6
51	-V1	-2934.8	-526.6	111	NC	3542.0	-526.6	171	COM50	6982.8	526.6
52	-V1	-2833.6	-526.6	112	NC	3643.2	-526.6	172	COM51	6881.6	526.6
53	-V1	-2732.4	-526.6	113	COM0	3845.6	-526.6	173	COM52	6780.4	526.6
54	NC	-2631.2	-526.6	114	COM1	3946.8	-526.6	174	COM53	6679.2	526.6
55	NC	-2530.0	-526.6	115	COM2	4048.0	-526.6	175	COM54	6578.0	526.6
56	NC	-2428.8	-526.6	116	COM3	4149.2	-526.6	176	COM55	6476.8	526.6
57	NC	-2327.6	-526.6	117	COM4	4250.4	-526.6	177	COM56	6375.6	526.6
58	NC	-2226.4	-526.6	118	COM5	4351.6	-526.6	178	COM57	6274.4	526.6
59	NC	-2125.2	-526.6	119	COM6	4452.8	-526.6	179	COM58	6173.2	526.6
60	NC	-2024.0	-526.6	120	COM7	4554.0	-526.6	180	COM59	6072.0	526.6

PAD #	PIN NAME	X-POS	Y-POS
181	COM60	5970.8	526.6
182	COM61	5869.6	526.6
183	COM62	5768.4	526.6
184	COM63	5667.2	526.6
185	COM64	5566.0	526.6
186	COM65	5464.8	526.6
187	COM66	5363.6	526.6
188	COM67	5262.4	526.6
189	COM68	5161.2	526.6
190	COM69	5060.0	526.6
191	COM70	4958.8	526.6
192	COM71	4857.6	526.6
193	COM72	4756.4	526.6
194	COM73	4655.2	526.6
195	COM74	4554.0	526.6
196	COM75	4452.8	526.6
197	COM76	4351.6	526.6
198	COM77	4250.4	526.6
199	COM78	4149.2	526.6
200	COM79	4048.0	526.6
201	COM80	3946.8	526.6
202	COM81	3845.6	526.6
203	COM82	3744.4	526.6
204	COM83	3643.2	526.6
205	COM84	3542.0	526.6
206	COM85	3440.8	526.6
207	COM86	3339.6	526.6
208	COM87	3238.4	526.6
209	COM88	3137.2	526.6
210	COM89	3036.0	526.6
211	COM90	2934.8	526.6
212	COM91	2833.6	526.6
213	COM92	2732.4	526.6
214	COM93	2631.2	526.6
215	COM94	2530.0	526.6
216	COM95	2428.8	526.6
217	COM96	2327.6	526.6
218	COM97	2226.4	526.6
219	COM98	2125.2	526.6
220	COM99	2024.0	526.6
221	COM100	1922.8	526.6
222	COM101	1821.6	526.6
223	COM102	1720.4	526.6
224	COM103	1619.2	526.6
225	COM104	1518.0	526.6
226	COM105	1416.8	526.6
227	COM106	1315.6	526.6
228	COM107	1214.4	526.6
229	COM108	1113.2	526.6
230	COM109	1012.0	526.6
231	COM110	910.8	526.6
232	COM111	809.6	526.6
233	COM112	708.4	526.6
234	COM113	607.2	526.6
235	COM114	506.0	526.6
236	COM115	404.8	526.6
237	COM116	303.6	526.6
238	COM117	202.4	526.6
239	COM118	101.2	526.6
240	COM119	0.0	526.6

PAD #	PIN NAME	X-POS	Y-POS
241	COM120	-101.2	526.6
242	COM121	-202.4	526.6
243	COM122	-303.6	526.6
244	COM123	-404.8	526.6
245	COM124	-506.0	526.6
246	COM125	-607.2	526.6
247	COM126	-708.4	526.6
248	COM127	-809.6	526.6
249	COM128	-910.8	526.6
250	COM129	-1012.0	526.6
251	COM130	-1113.2	526.6
252	COM131	-1214.4	526.6
253	COM132	-1315.6	526.6
254	COM133	-1416.8	526.6
255	COM134	-1518.0	526.6
256	COM135	-1619.2	526.6
257	COM136	-1720.4	526.6
258	COM137	-1821.6	526.6
259	COM138	-1922.8	526.6
260	COM139	-2024.0	526.6
261	COM140	-2125.2	526.6
262	COM141	-2226.4	526.6
263	COM142	-2327.6	526.6
264	COM143	-2428.8	526.6
265	COM144	-2530.0	526.6
266	COM145	-2631.2	526.6
267	COM146	-2732.4	526.6
268	COM147	-2833.6	526.6
269	COM148	-2934.8	526.6
270	COM149	-3036.0	526.6
271	COM150	-3137.2	526.6
272	COM151	-3238.4	526.6
273	COM152	-3339.6	526.6
274	COM153	-3440.8	526.6
275	COM154	-3542.0	526.6
276	COM155	-3643.2	526.6
277	COM156	-3744.4	526.6
278	COM157	-3845.6	526.6
279	COM158	-3946.8	526.6
280	COM159	-4048.0	526.6
281	COM160	-4149.2	526.6
282	COM161	-4250.4	526.6
283	COM162	-4351.6	526.6
284	COM163	-4452.8	526.6
285	COM164	-4554.0	526.6
286	COM165	-4655.2	526.6
287	COM166	-4756.4	526.6
288	COM167	-4857.6	526.6
289	COM168	-4958.8	526.6
290	COM169	-5060.0	526.6
291	COM170	-5161.2	526.6
292	COM171	-5262.4	526.6
293	COM172	-5363.6	526.6
294	COM173	-5464.8	526.6
295	COM174	-5566.0	526.6
296	COM175	-5667.2	526.6
297	COM176	-5768.4	526.6
298	COM177	-5869.6	526.6
299	COM178	-5970.8	526.6
300	COM179	-6072.0	526.6

PAD #	PIN NAME	X-POS	Y-POS
301	COM180	-6173.2	526.6
302	COM181	-6274.4	526.6
303	COM182	-6375.6	526.6
304	COM183	-6476.8	526.6
305	COM184	-6578.0	526.6
306	COM185	-6679.2	526.6
307	COM186	-6780.4	526.6
308	COM187	-6881.6	526.6
309	COM188	-6982.8	526.6
310	COM189	-7084.0	526.6
311	COM190	-7185.2	526.6
312	COM191	-7286.4	526.6
313	COM192	-7387.6	526.6
314	COM193	-7488.8	526.6
315	COM194	-7590.0	526.6
316	COM195	-7691.2	526.6
317	COM196	-7792.4	526.6
318	COM197	-7893.6	526.6
319	NC	-8090.3	526.6
320	NC	-8090.3	308.2
321	NC	-8090.3	207.0
322	NC	-8090.3	105.8
323	NC	-8090.3	-105.8
324	NC	-8090.3	-207.0
325	NC	-8090.3	-308.2

## 6 SSD1882T1 TAB Pin Assignment

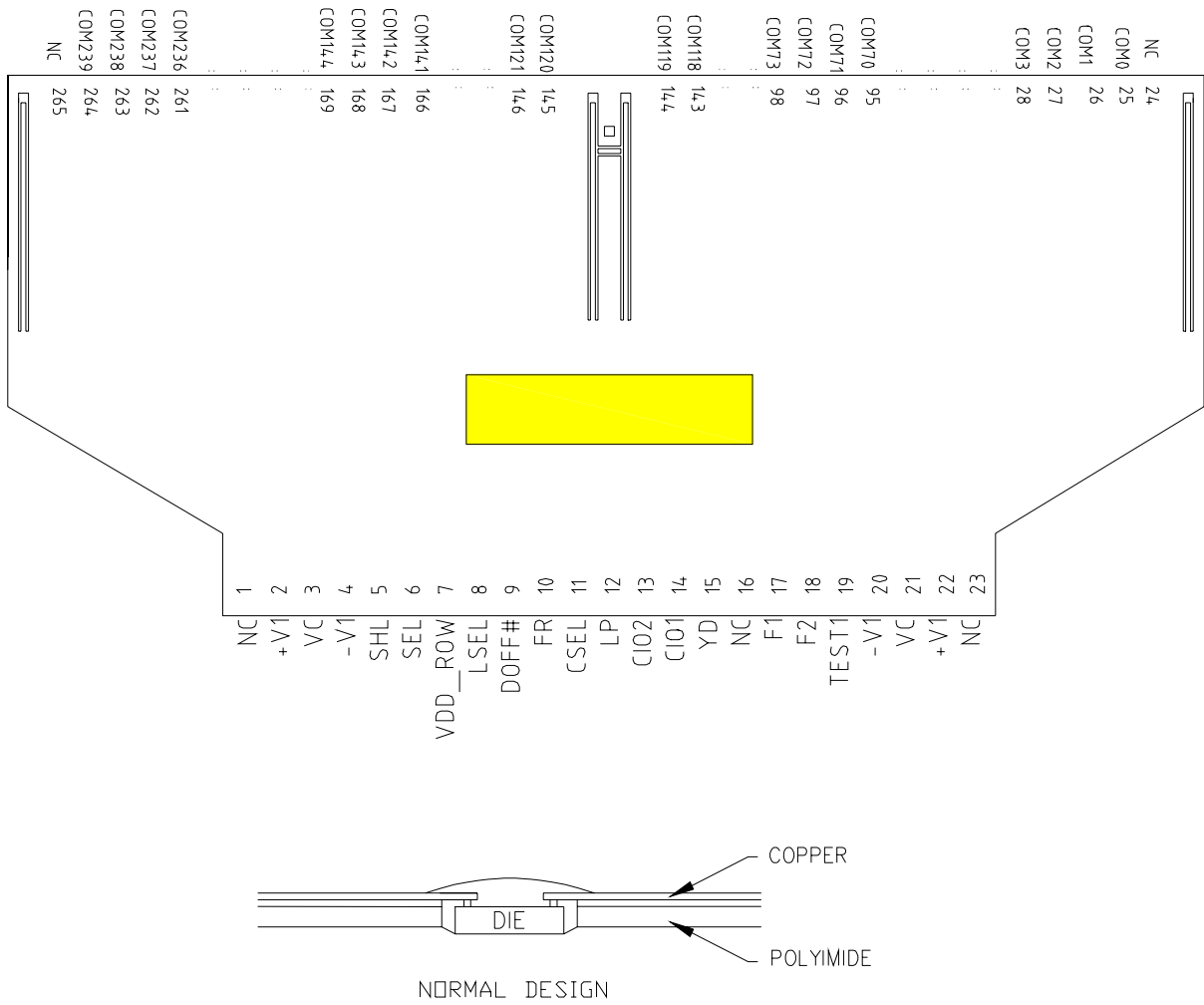


Figure 3 – SSD1882T1 Pin Assignment (Copper View, Normal TAB Design)



**Table 3 - SSD1882T1 Pin assignment Table**

TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name
1	NC	61	COM36	121	COM96	181	COM156	241	COM216
2	+V1	62	COM37	122	COM97	182	COM157	242	COM217
3	VC	63	COM38	123	COM98	183	COM158	243	COM218
4	-V1	64	COM39	124	COM99	184	COM159	244	COM219
5	SHL	65	COM40	125	COM100	185	COM160	245	COM220
6	SEL	66	COM41	126	COM101	186	COM161	246	COM221
7	VDD_ROW	67	COM42	127	COM102	187	COM162	247	COM222
8	LSEL	68	COM43	128	COM103	188	COM163	248	COM223
9	DOFF#	69	COM44	129	COM104	189	COM164	249	COM224
10	FR	70	COM45	130	COM105	190	COM165	250	COM225
11	CSEL	71	COM46	131	COM106	191	COM166	251	COM226
12	LP	72	COM47	132	COM107	192	COM167	252	COM227
13	CIO2	73	COM48	133	COM108	193	COM168	253	COM228
14	CIO1	74	COM49	134	COM109	194	COM169	254	COM229
15	YD	75	COM50	135	COM110	195	COM170	255	COM230
16	NC	76	COM51	136	COM111	196	COM171	256	COM231
17	F1	77	COM52	137	COM112	197	COM172	257	COM232
18	F2	78	COM53	138	COM113	198	COM173	258	COM233
19	TEST1	79	COM54	139	COM114	199	COM174	259	COM234
20	-V1	80	COM55	140	COM115	200	COM175	260	COM235
21	VC	81	COM56	141	COM116	201	COM176	261	COM236
22	+V1	82	COM57	142	COM117	202	COM177	262	COM237
23	NC	83	COM58	143	COM118	203	COM178	263	COM238
24	NC	84	COM59	144	COM119	204	COM179	264	COM239
25	COM0	85	COM60	145	COM120	205	COM180	265	NC
26	COM1	86	COM61	146	COM121	206	COM181		
27	COM2	87	COM62	147	COM122	207	COM182		
28	COM3	88	COM63	148	COM123	208	COM183		
29	COM4	89	COM64	149	COM124	209	COM184		
30	COM5	90	COM65	150	COM125	210	COM185		
31	COM6	91	COM66	151	COM126	211	COM186		
32	COM7	92	COM67	152	COM127	212	COM187		
33	COM8	93	COM68	153	COM128	213	COM188		
34	COM9	94	COM69	154	COM129	214	COM189		
35	COM10	95	COM70	155	COM130	215	COM190		
36	COM11	96	COM71	156	COM131	216	COM191		
37	COM12	97	COM72	157	COM132	217	COM192		
38	COM13	98	COM73	158	COM133	218	COM193		
39	COM14	99	COM74	159	COM134	219	COM194		
40	COM15	100	COM75	160	COM135	220	COM195		
41	COM16	101	COM76	161	COM136	221	COM196		
42	COM17	102	COM77	162	COM137	222	COM197		
43	COM18	103	COM78	163	COM138	223	COM198		
44	COM19	104	COM79	164	COM139	224	COM199		
45	COM20	105	COM80	165	COM140	225	COM200		
46	COM21	106	COM81	166	COM141	226	COM201		
47	COM22	107	COM82	167	COM142	227	COM202		
48	COM23	108	COM83	168	COM143	228	COM203		
49	COM24	109	COM84	169	COM144	229	COM204		
50	COM25	110	COM85	170	COM145	230	COM205		
51	COM26	111	COM86	171	COM146	231	COM206		
52	COM27	112	COM87	172	COM147	232	COM207		
53	COM28	113	COM88	173	COM148	233	COM208		
54	COM29	114	COM89	174	COM149	234	COM209		
55	COM30	115	COM90	175	COM150	235	COM210		
56	COM31	116	COM91	176	COM151	236	COM211		
57	COM32	117	COM92	177	COM152	237	COM212		
58	COM33	118	COM93	178	COM153	238	COM213		
59	COM34	119	COM94	179	COM154	239	COM214		
60	COM35	120	COM95	180	COM155	240	COM215		

## 7 PIN DESCRIPTION

### **VDD\_ROW**

VDD\_ROW is the power supply pin to the logic system. The voltage range is 2.7V to 5.5V with respect to the -V1 pin.

### **+V1, VC, -V1**

+V1, VC and -V1 are power supply pins to the LCD driving system. -V1 pin also serves as the logic ground of chip.

Their relationship is  $+V1 \geq VC \geq VDD\_ROW \geq -V1$ .

### **YD**

This input pin is used as a signal to start a frame and to reset the column address for writing. (Note 1)

### **LP**

This is an input pin for display data latch clock. The display data is latched at the falling edge of LP. (Note 1)

### **FR**

This is an input pin and is used to change the LCD driving waveform polarity. If MLA power chip is used, the output FR from the power chip should be connected to the FR pin of the row driver. (Note 1)

### **F1, F2**

These are input pins and are used as driver pattern select signals. These two signals are generated by a column driver. If the display system is formed by the MLA column driver and the MLA row driver, outputs F10 and F20 from the column driver should be connected to F1 and F2 of the row driver respectively. (Note 1)

### **DOFF#**

This is an input pin and is used to control the display. When it is set at "L" level, all common outputs are forced to VC level and the LC display will be forced to blank, however, the contents of the latches are maintained. In normal display operation, it is set to "H" level. (Note 1)

### **SEL**

SSD1882 can be configured as 200 or 240 common outputs depending on the logic level of input pin SEL.

When SEL is set at "L" level, 240 outputs are chosen and COM0 to COM239 will be used. When SEL is set at "H" level, 200 outputs are chosen and only COM20 to COM219 will be used.

### **CIO1, CIO2**

These are I/O pins and they can be configured as an input or an output by the signal SHL. When SHL is set at "L" level, CIO1 is input and CIO2 is output. When SHL is set at "H" level, CIO1 is output and CIO2 is input. The output transition occurs on the falling edge of LP. (Note 1)

### **SHL**

This is an input pin and is used to select the output shift direction and to configure CIO1 and CIO2. The following table shows the relationship between SEL, SHL, CIO1, CIO2 and the output shift direction.

SEL = L (240 common outputs)			
SHL	Output Shift Direction	CIO1	CIO2
L	COM0 -----> COM239	Input	Output
H	COM239 -----> COM0	Output	Input
SEL = H (200 common outputs)			
SHL	Output Shift Direction	CIO1	CIO2
L	COM20 -----> COM219	Input	Output
H	COM219 -----> COM20	Output	Input

### LSEL

This is an input pin to select 1P Operation or 1/2P Operation. That can cope with different LCD having different response time.

When LSEL is set at "L" level, 1P Normal Operation is selected. When LSEL is set at "H" level, 1/2P Operation is selected.

### CSEL

This is a chip select signal input. When only one common driver is used, CSEL should be set at "L" level. When multiple common drivers are used, CSEL of the leading chip must be tied to "L" level and that of other chips must be tied to "H" level.

### TEST1

This is a reserved pin and it must be set at "L" level in the normal operation.

### TEST2

This is a reserved pin and it must be set at "L" level in the normal operation.

### COM0 – COM239

These are output pins and provide common driving signals to the LCD panel. Output transition occurs at the falling edge of LP.

Note 1 : If an MLA LCD system is formed by SSD1882 row driver, MLA column driver and MLA power chip, 1nF capacitors are necessary for capacitor coupling between SSD1882 and MLA column driver signals. Refer to the Application Examples for circuit connection.

## 8 FUNCTIONAL BLOCK DESCRIPTIONS

### 8.1 Controller and Data Register

Based on the input signal of FR, F1, F2 and LP, this Controller will generate signals to control the Data Register. Then, the Data Register will latch the data to the Common Cell Level Shifter according to the signals from the Controller and the data from the Shift Register. The data is latched to the Common Cell Level Shifter at the falling edge of LP.

### 8.2 Bi-directional Shift Register

This Shift Register shifts the input signals YD and CIO input according to the setting of SHL, SEL, LSEL and CSEL. When SHL is set at "L" level, CIO1 is input and CIO2 is output. When SHL is set at "H" level, CIO1 is output and CIO2 is input. The output transition occurs on the falling edge of LP.

### 8.3 Common Cell Level Shifter

This is a level interface circuit which converts the signal voltage level from a logic system level to the LCD driver system voltage level. When DOFF# is at "L" level, all common output voltage will be at VC level. When DOFF# is at "H" level, the common output voltage will be changed according to the status of input signals of FR, F1 and F2. Table 5 and Table 6 show the relationship between the common output voltage values and the input signals FR, F1 and F2.

**Table 4 - Relationship between COM voltage and F1 & F2 when FR = L**

When DOFF# = H and FR = L				
F1	1	0	1	0
F2	1	1	0	0
line r	+V1	+V1	-V1	+V1
line (r + 1)	-V1	+V1	+V1	+V1
line (r + 2)	+V1	-V1	+V1	+V1
line (r + 3)	+V1	+V1	+V1	-V1

**Table 5 - Relationship between COM voltage and F1 & F2 when FR = H**

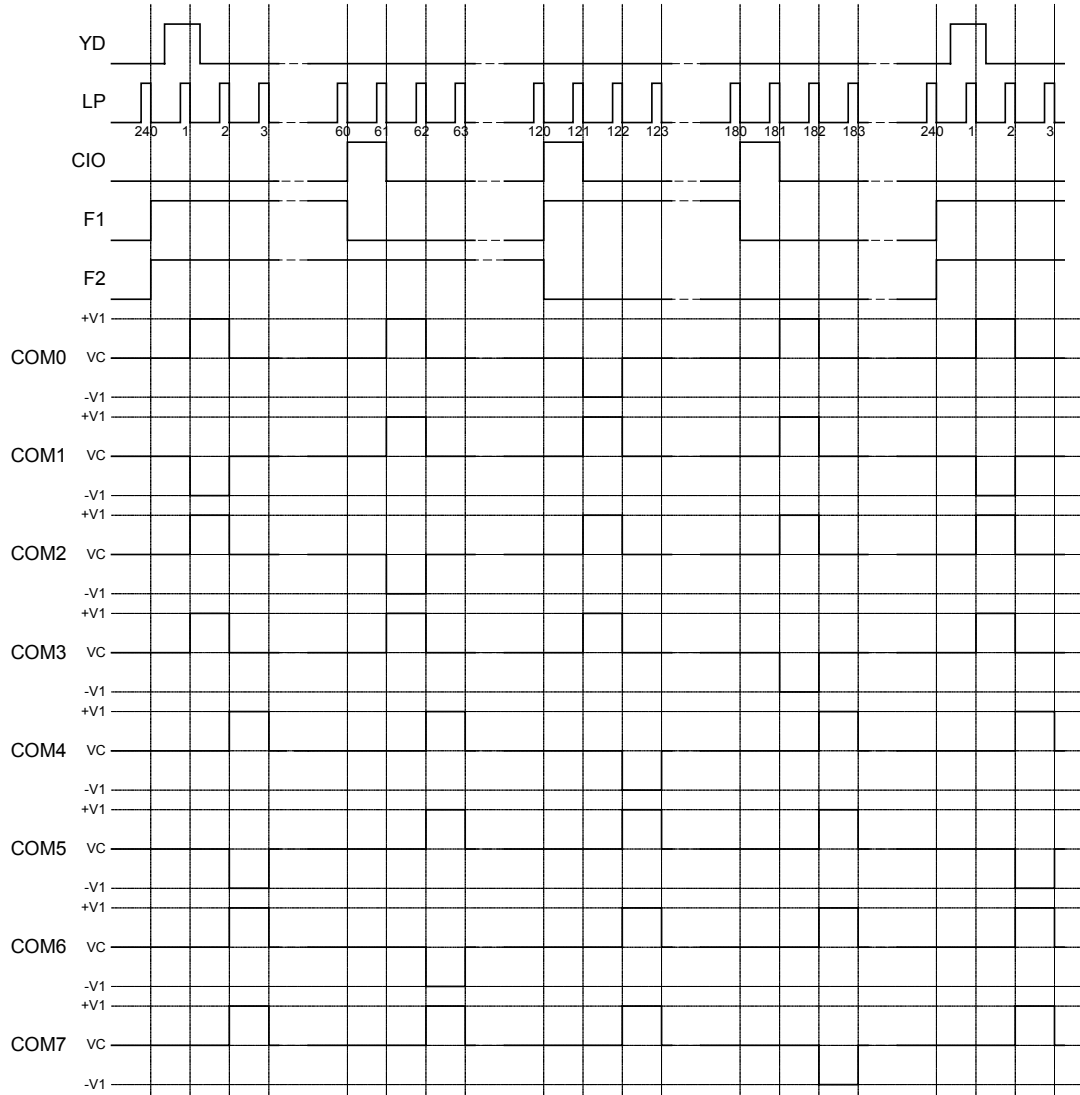
When DOFF# = H and FR = H				
F1	1	0	1	0
F2	1	1	0	0
line r	-V1	-V1	+V1	-V1
line (r + 1)	+V1	-V1	-V1	-V1
line (r + 2)	-V1	+V1	-V1	-V1
line (r + 3)	-V1	-V1	-V1	+V1

**Table 6 - Relationship between Line# and Common**

Line#	Formula	Common
r	Multiples of 4	0, 4, 8, 12, ... , 228, 232, 236
r + 1	1 + multiples of 4	1, 5, 9, 13, ... , 229, 233, 237
r + 2	2 + multiples of 4	2, 6, 10, 14, ... , 230, 234, 238
r + 3	3 + multiples of 4	3, 7, 11, 15, ... , 231, 235, 239

**Timing diagram for 1/240 duty and 1P operation (DOFF# = H and FR = L)**

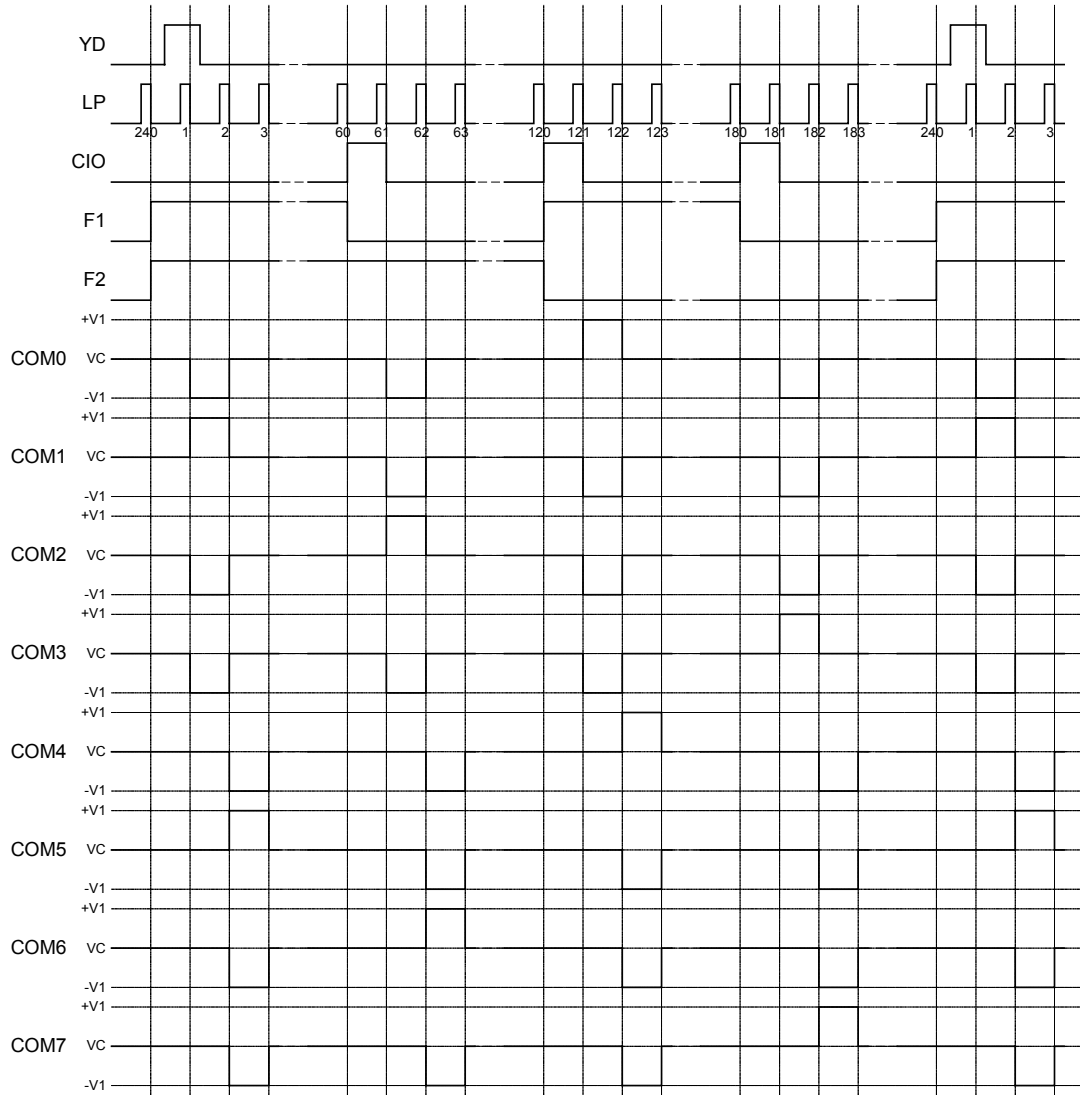
This diagram is only for reference. Below diagram is at the conditions of SHL = L, SEL = L, LSEL = L, CSEL = L



**Figure 4 - Timing diagram for 1/240 duty and 1P operation (DOFF# = H and FR = L)**

**Timing diagram for 1/240 duty and 1P operation (DOFF# = H and FR = H)**

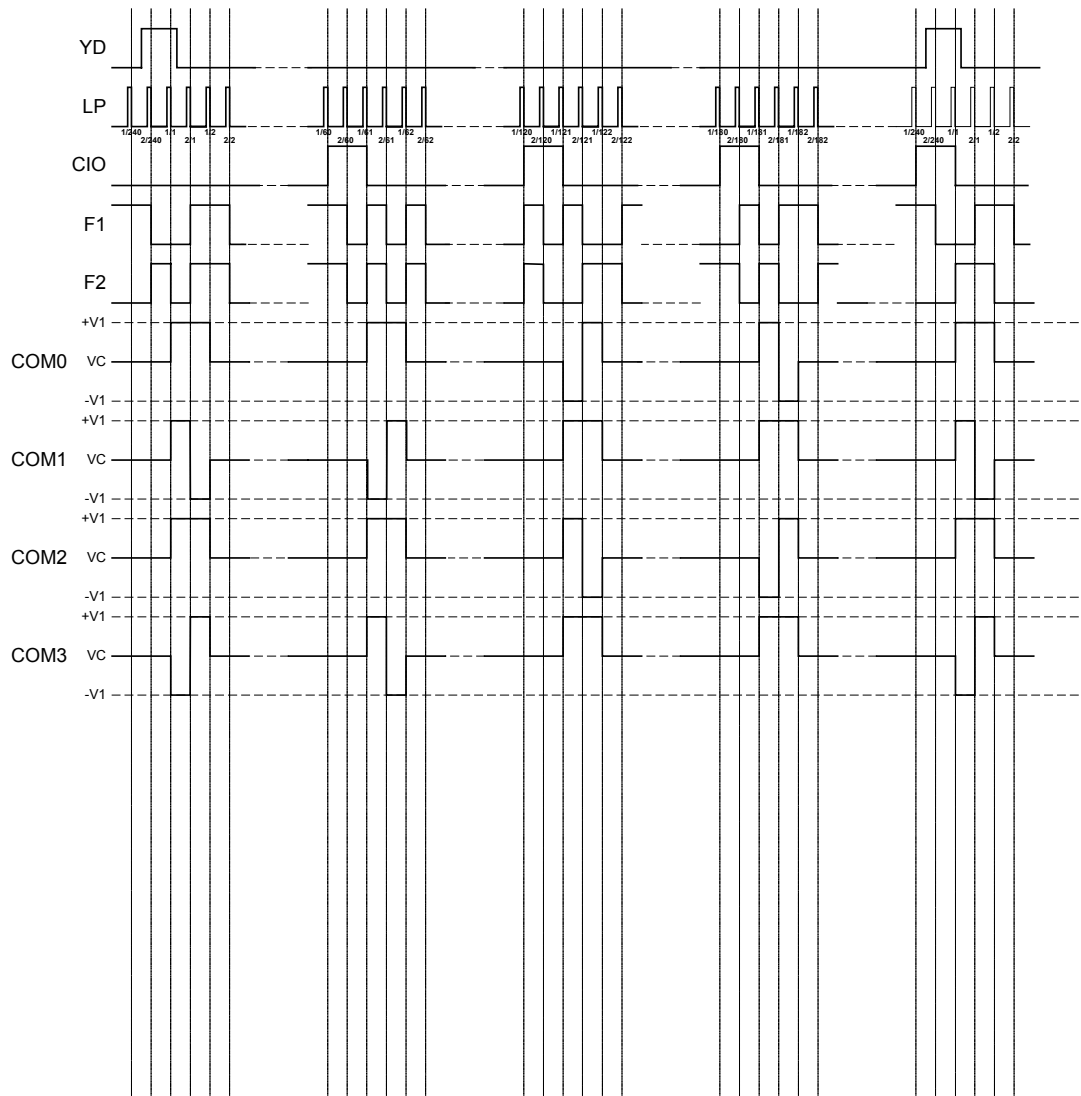
This diagram is only for reference. Below diagram is at the conditions of SHL = L, SEL = L, LSEL = L, CSEL = L



**Figure 5 - Timing diagram for 1/240 duty and 1P operation (DOFF# = H and FR = H)**

**Timing diagram for 1/240 duty and 1/2P operation (DOFF# = H and FR = L)**

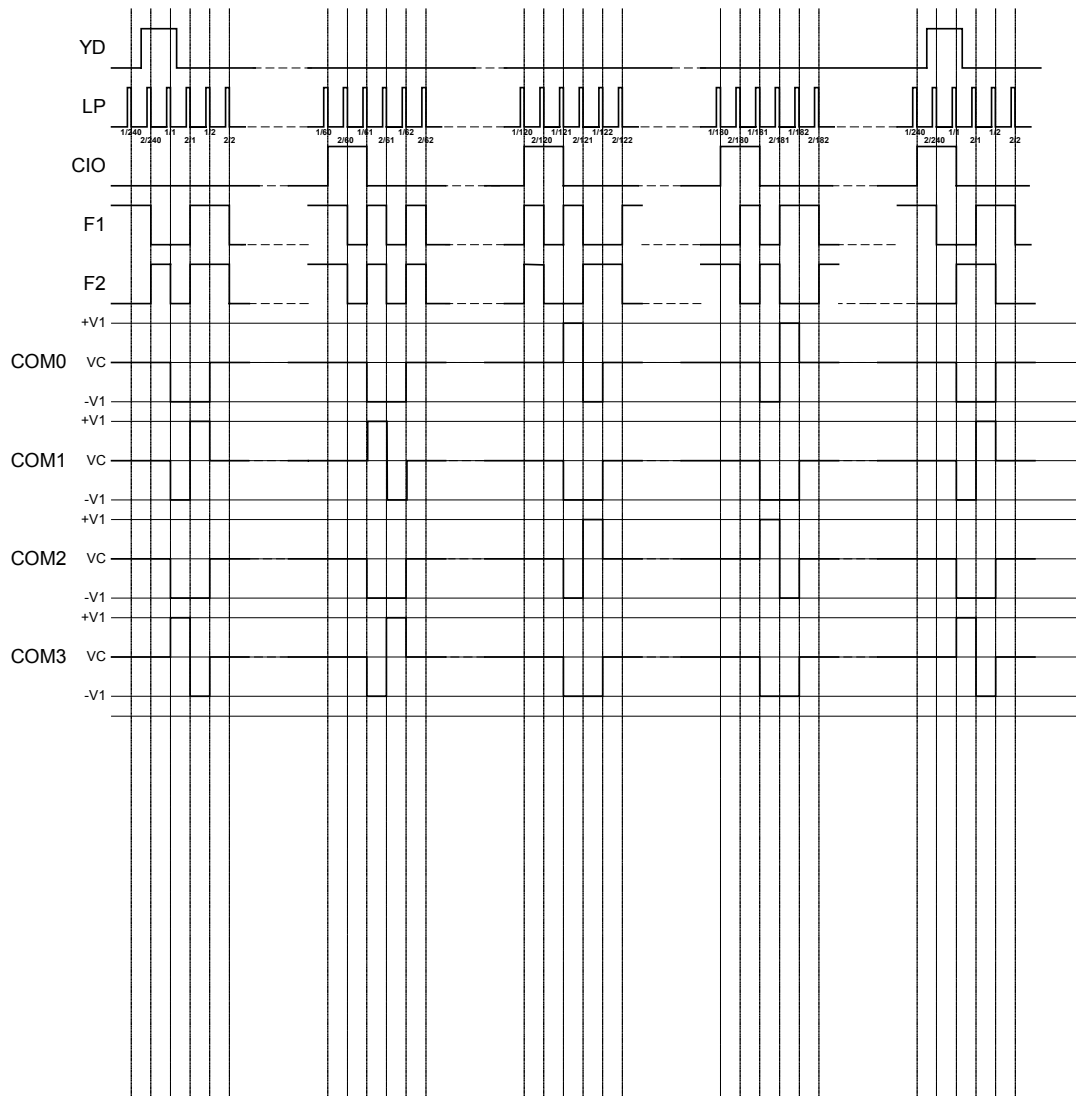
This diagram is only for reference. Below diagram is at the conditions of SHL = L, SEL = L, LSEL = H, CSEL = L



**Figure 6 - Timing diagram for 1/240 duty and 1/2P operation (DOFF# = H and FR = L)**

**Timing diagram for 1/240 duty and 1/2P operation (DOFF# = H and FR = H)**

This diagram is only for reference. Below diagram is at the conditions of SHL = L, SEL = L, LSEL = H, CSEL = L



**Figure 7 - Timing diagram for 1/240 duty and 1/2P operation (DOFF# = H and FR = H)**



## 9 MAXIMUM RATINGS

Table 7 - Maximum Ratings (Voltage Referenced to  $-V1 = 0.0V$ )

Symbol	Parameter	Value	Unit
VDD_ROW	Power Voltage	-0.3 to +7.0	V
+V1		-0.3 to 33	V
V <sub>IN</sub>	Input Voltage	$-V1 - 0.3$ to $+V1 + 0.3$	V
V <sub>o</sub>	Output Voltage	$-V1 - 0.3$ to $+V1 + 0.3$	V
I	Output current at CIO	20	mA
T <sub>A</sub>	Operating temperature	-30 to +85	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits shown in the DC characteristics section and the relationship between +V1, VC and -V1 must be  $+V1 \geq VC \geq VDD\_ROW \geq -V1$ . All voltages are referenced to  $-V1 = 0V$ .

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. All dummy pins and NC pins must be left open & unconnected. Don't group the dummy pins or the NC pins together. The device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

## 10 DC CHARACTERISTICS

**Table 8 - DC Characteristics (-V1 = 0.0V, VDD\_ROW = 5.0V, TA = 25°C)**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD_ROW	Power supply voltage for logic system		2.7	5.0	5.5	V
+V1 VC	Power supply voltage for LCD	-V1 = 0.0, VDD_ROW = 5.0V	14 --	-- +V1/2	30 --	V V
IDP1	Current drain from Pin VDD_ROW	VDD_ROW = 5.0V, VIN = VDD_ROW, VIL = -V1, freq of LP = 14.4kHz and freq of FR = 70Hz, no loading	--	5	25	uA
IDP2	Current drain from Pin +V1	+V1 = 30V, VC = +V1/2, -V1 = 0.0V, VDD_ROW = 5.0V, VIN = VDD_ROW, VIL = -V1, freq of LP = 14.4kHz and freq of FR = 70Hz, no loading	--	35	100	uA
ISB	Static current drain from Pin VDD_ROW	+V1 = 14.0V to 30.0V, VIN = VDD_ROW, VIL = -V1	--	1	5	uA
VIH	Input High voltage at pins: CIO1, CIO2, SHL, SEL, LSEL, CSEL, FR, YD, LP, F1, F2, TEST1 & DOFF#	VDD_ROW = 2.7V to 5.5V	0.8xVDD_ROW	--	--	V
VIL	Input Low voltage at pins: CIO1, CIO2, SHL, SEL, LSEL, CSEL, FR, YD, LP, F1, F2, TEST1 & DOFF#		--	--	0.2xVDD_ROW	V
VOH	Output High voltage at pins: CIO1 & CIO2	VDD_ROW = 2.7V to 5.5V, IOH = -0.3mA	VDD_ROW - 0.4	--	--	V
VOL	Output Low voltage at pins: CIO1 & CIO2	VDD_ROW = 2.7V to 5.5V, IOL = 0.3mA	--	--	0.4	V
IL1	Input leakage current at pins: SHL, SEL, LSEL, CSEL, FR, YD, LP, F1, F2, TEST1 & DOFF#		--	--	2	uA
IL2	I/O leakage current at pins: CIO1 & CIO2		--	--	5	uA
ROut	Output resistance of pins: COM0 - COM239	-V1 = 0.0, VDD_ROW = 5.0V	--	--	1000	Ω

## 11 AC CHARACTERISTICS

Table 9 - Input Timing Characteristics (-V1 = 0.0V, VDD\_ROW = 5.0V, T<sub>A</sub> = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>LPcyc</sub>	LP period	500	--	--	ns
t <sub>LPHi</sub>	LP pulse width (High level)	55	--	--	ns
t <sub>LPLo</sub>	LP pulse width (Low level)	330	--	--	ns
t <sub>YDs</sub>	YD, CIO setup time	100	--	--	ns
t <sub>YDh</sub>	YD, CIO hold time	40	--	--	ns
t <sub>YDset</sub>	YD, CIO setup time	80	--	--	ns
t <sub>F12s</sub>	F1, F2 setup time	100	--	--	ns
t <sub>F12h</sub>	F1, F2 hold time	40	--	--	us
t <sub>FRs</sub>	FR setup time	100	--	--	ns
t <sub>FRh</sub>	FR hold time	40	--	--	ns
t <sub>r</sub>	Input signal rise time	--	--	50	ns
t <sub>f</sub>	Input signal fall time	--	--	50	ns

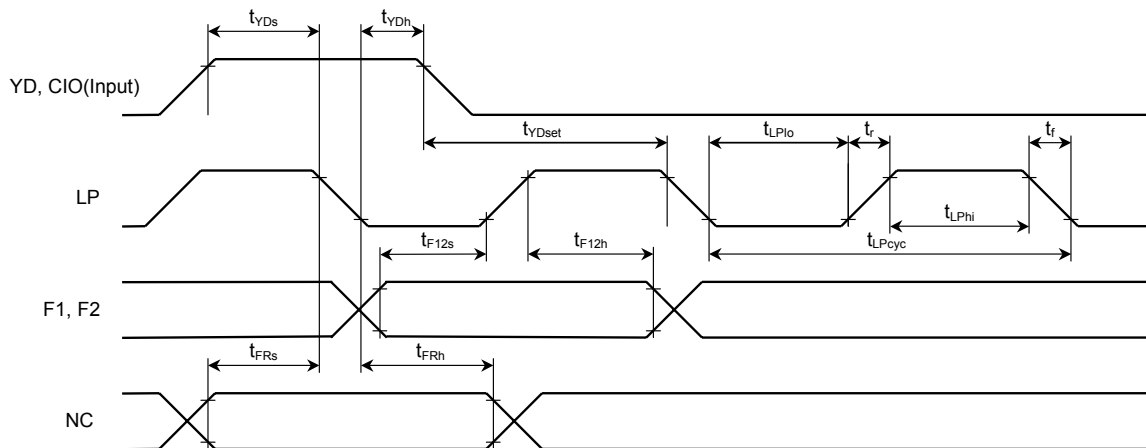
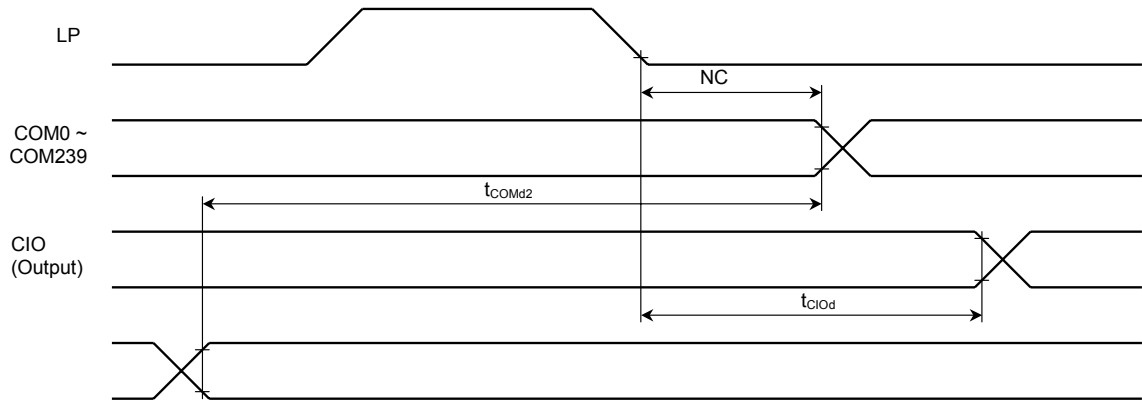


Figure 8 - Input Timing Characteristics

**Table 10 - Output Timing Characteristics -V1 = 0.0V, VDD\_ROW = 5.0V, T<sub>A</sub> = 25°C**

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>COMd1</sub>	Delay time from LP to COM	--	--	300	ns
t <sub>COMd2</sub>	Delay time from DOFF# to COM	--	--	350	ns
t <sub>CIOd</sub>	Delay time from LP to CIO output	--	--	700	ns



**Figure 9 - Output Timing Characteristics**

## 12 PRECAUTION

When SSD1882 is used with MLA column driver and MLA power chip to form a low power display system, the power supply of SSD1882 is actually coming from the MLA power chip outputs. Proper power up and power down sequence must be followed to protect and to ensure proper functioning of the system.

The recommended power up and down sequence is as follow:

Power up:

- Pull DOFF# to L
- Provide power to the MLA power chip and MLA column driver.
- Provide LP pulses chain with other controller signals while keeping DOFF# at "L".
- Wait for a minimum of 150ms to allow the MLA power chip building up appropriate power levels of the display system.
- Pull DOFF# to H to turn on the display

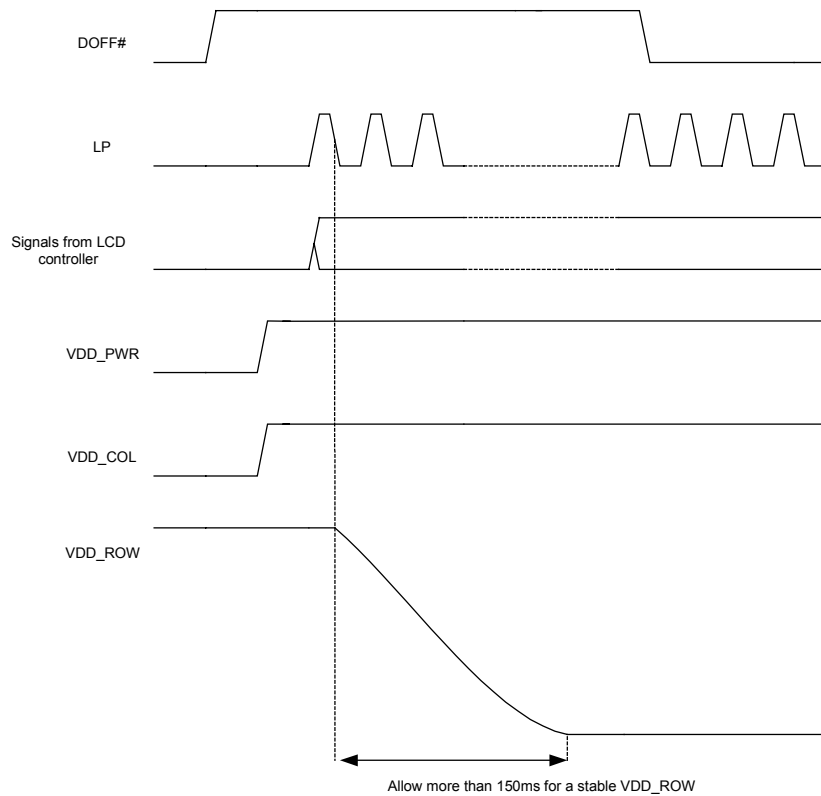
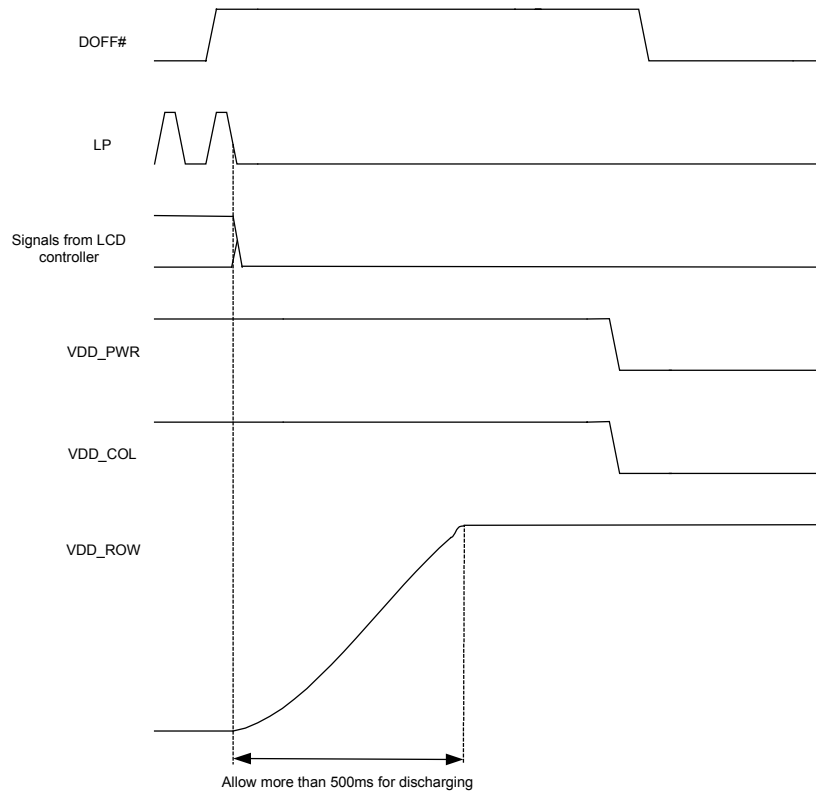


Figure 10 – Recommended power up sequence

Power down:

- Pull DOFF# to L to turn off the display
- Stop providing controller signals and LP pulses chain.
- Wait for a minimum of 500ms to allow the discharging of the power levels.
- Disconnect power from MLA column driver and MLA power chip.



**Figure 11 – Recommended power down sequence**

### 13 APPLICATION EXAMPLE

Below figure shows an example of a 160 x 240 LCD system with using the Power Chip SSD1730, the Row Driver SSD1882 and the Column Driver SSD1870. In order to operate the system, power source is applied to VDD\_PWR & VSS and a controller is used to issue signals to DOFF#, YD, LP, XSCL and data bus D0-D7.

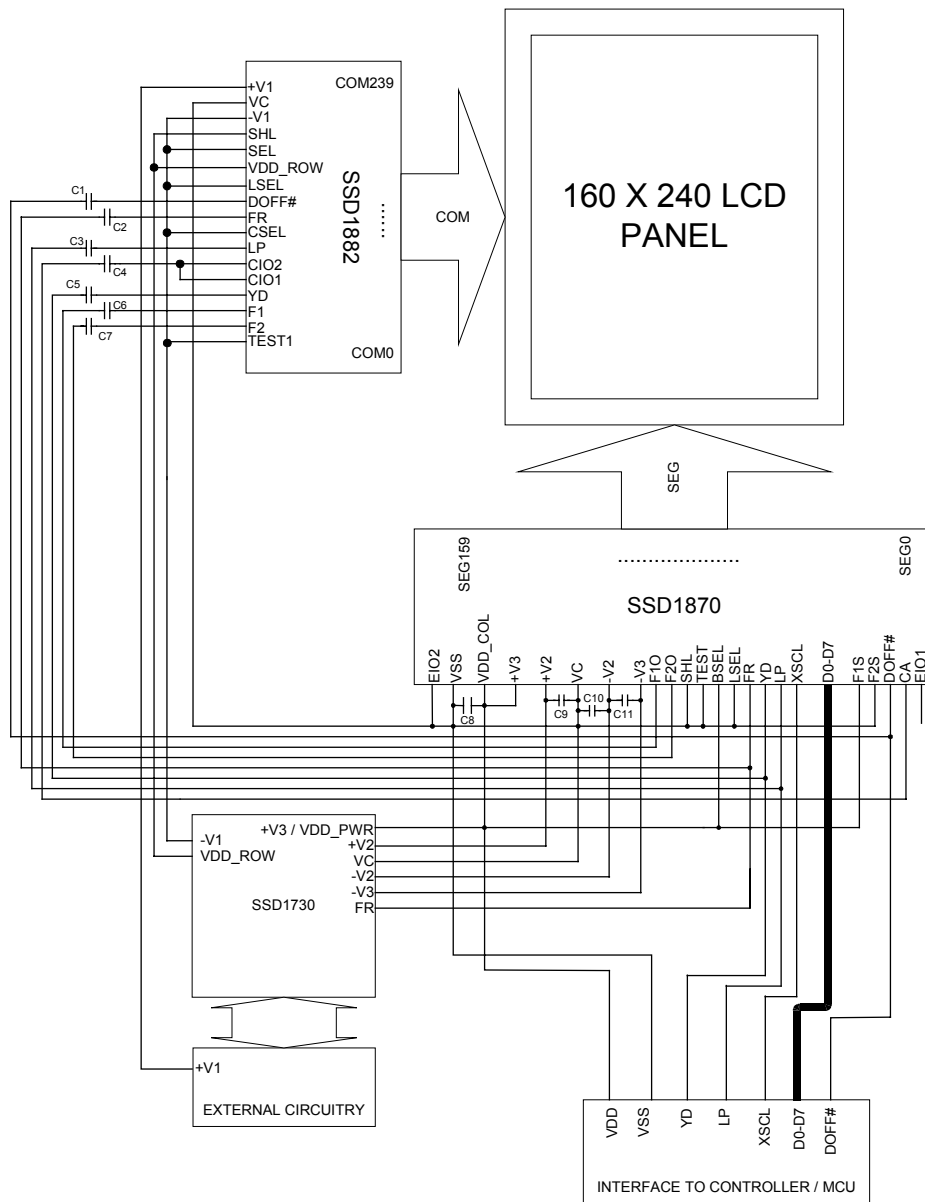


Figure 12 - Typical 160x240 MLA system

Below figure shows an example of a 320 x 240 LCD system with using the Power Chip SSD1730, the Row Driver SSD1882 and the Column Driver SSD1873.

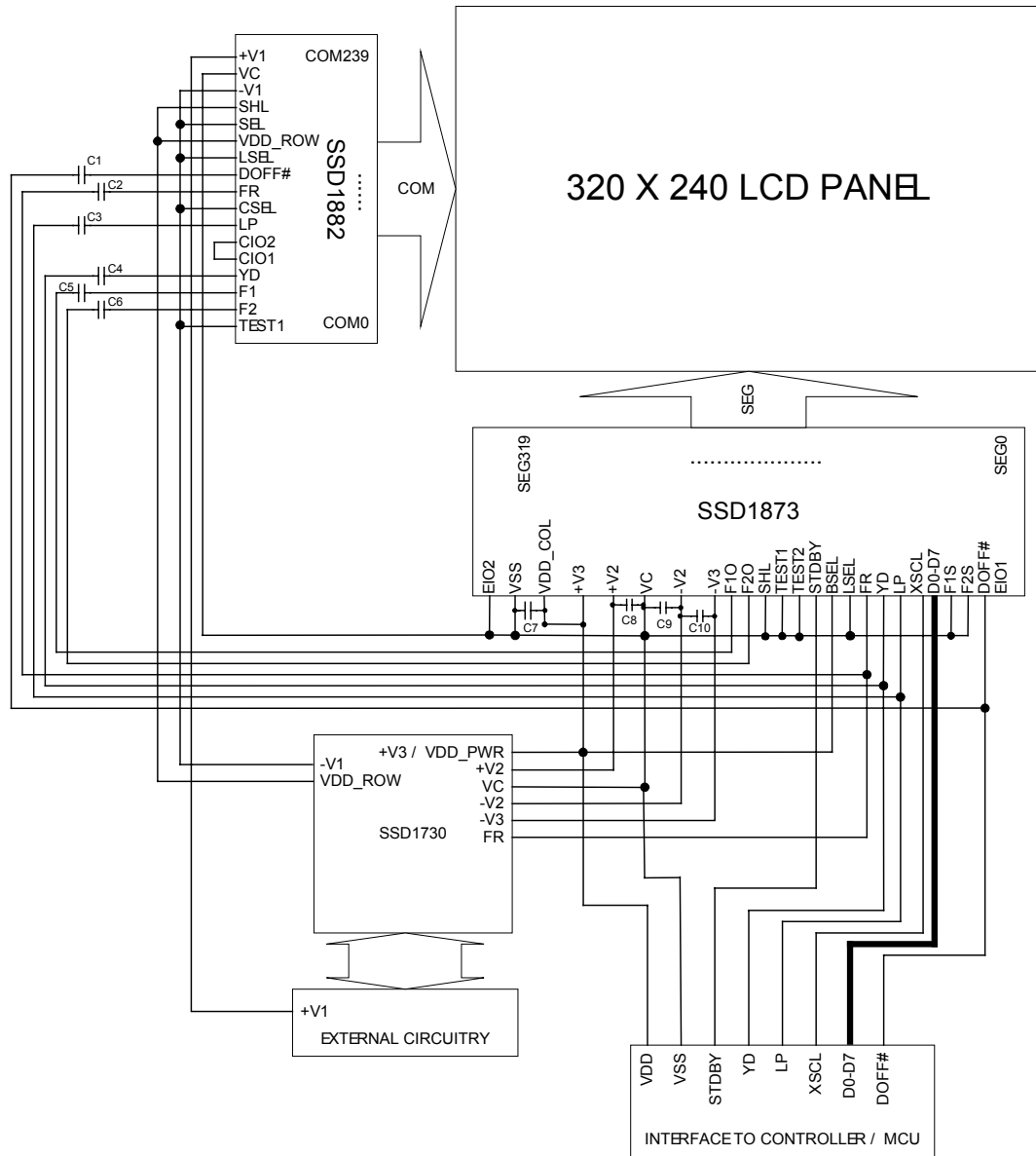
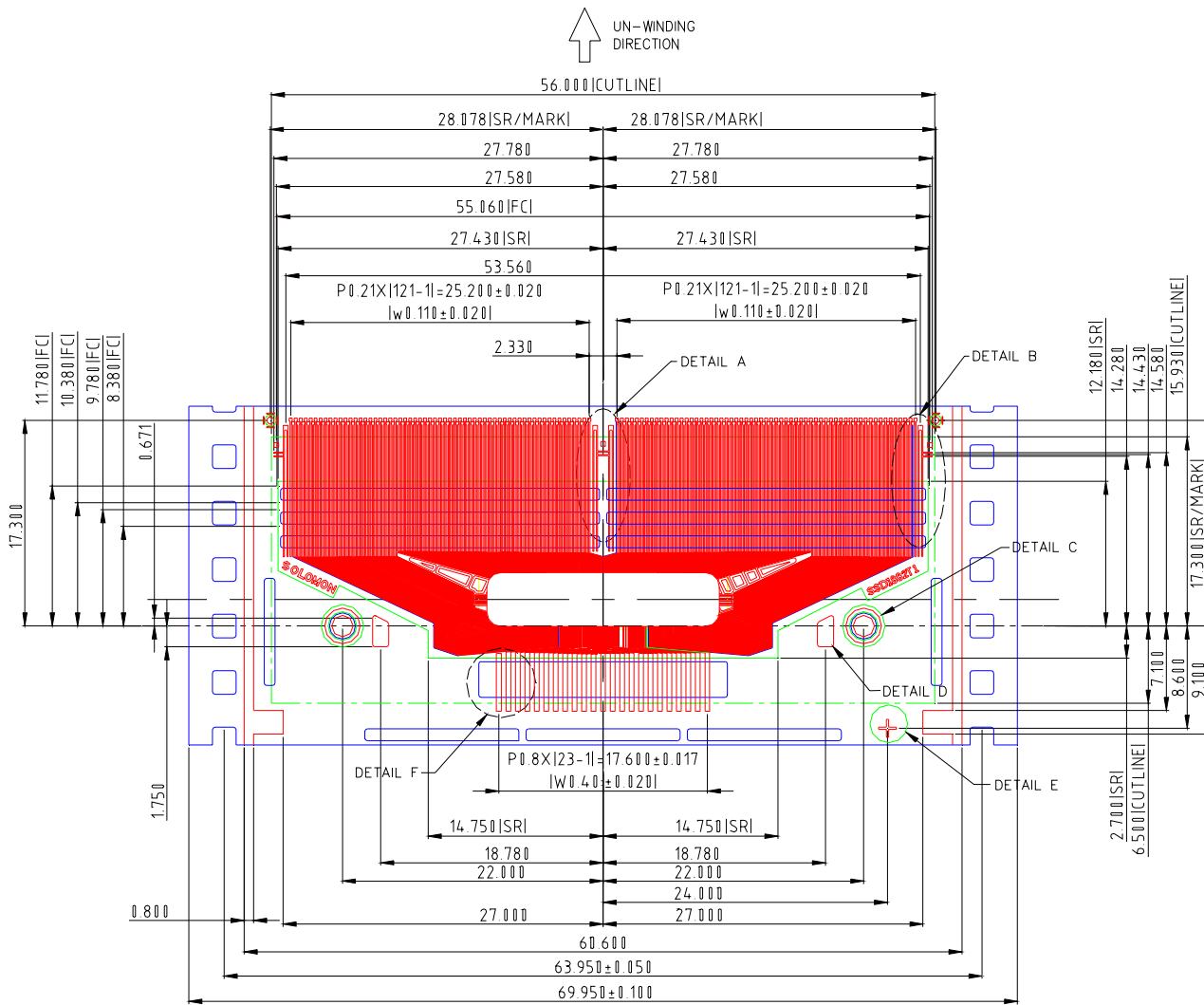


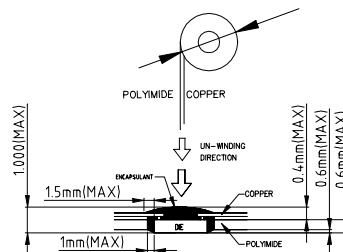
Figure 13 - Typical 320x240 MLA system

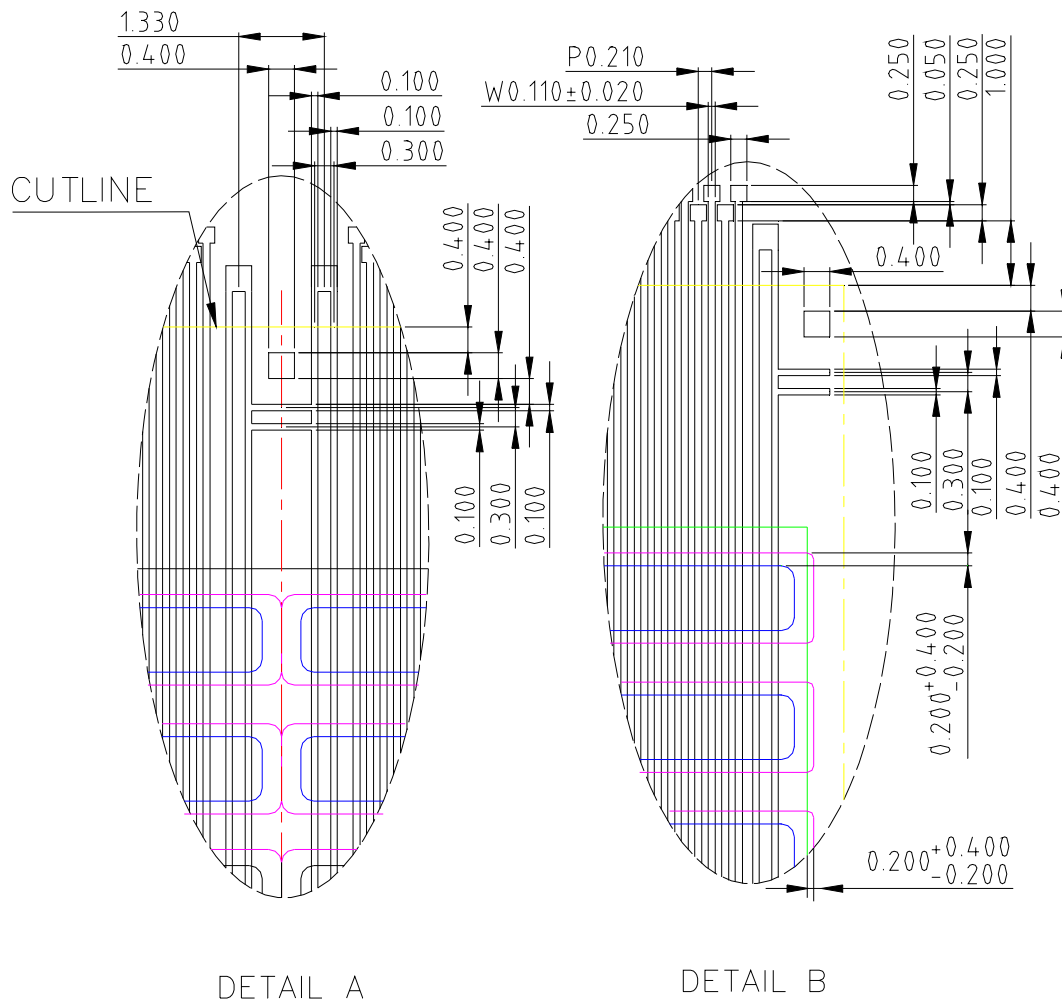


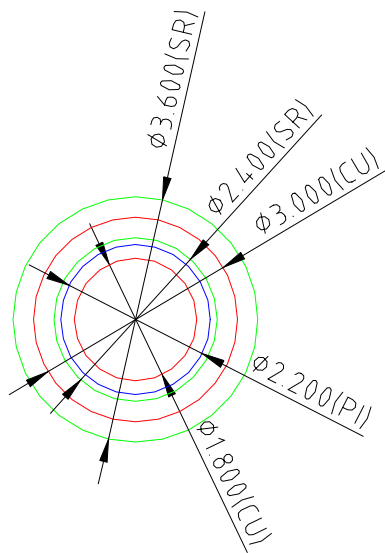
# 14 SSD1882T1 TAB Package Drawing



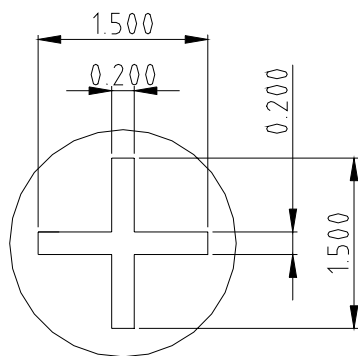
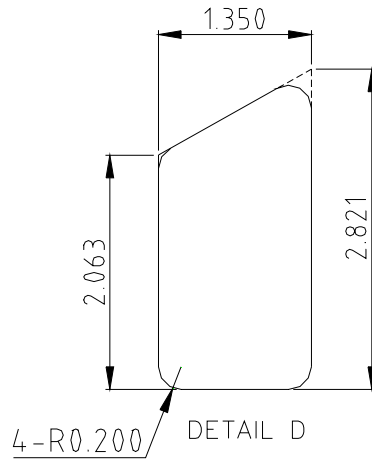
- NOTE:  
 1.GENERAL TOLERANCE:±0.05mm  
 2.MATERIALS  
 PI:75um±6um THICKNESS  
 ADHESIVE:12um±2um  
 CU:FQ-VLP 18um  
 FLEX COATING: MIN 10um  
 SOLDER RESIST:26um±14um  
 3.PLATING SN:0.25±0.050um  
 4.TAPSITE: 6 SPROCKET HOLE 28.5mm  
 5.ALL CHAMFER IS R2.00mm



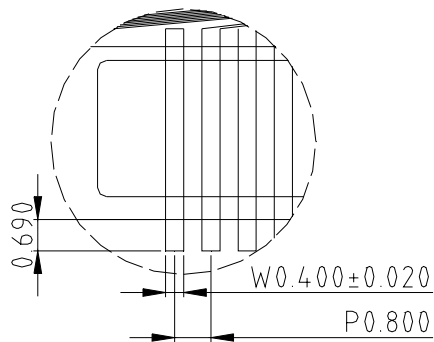




DETAIL C



DETAIL E



DETAIL F

Solomon Systech reserves the right to make changes without further notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.