SONY

CXA3197R

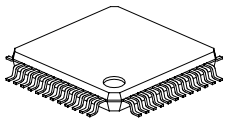
10-bit 125MSPS D/A Converter

Description

The CXA3197R is a high-speed D/A converter which can perform multiplexed input of two system 10-bit data.

This IC realizes a maximum conversion rate of 125MSPS. Multiplexed operation is possible by inputing the 1/2 frequency-divided clock or by halving the frequency of the clock internally with the clock frequency divider circuit having the reset pin. The data input is at TTL level, and the clock input and reset input can select either TTL or PECL level according to the application.

48 pin LQFP (Plastic)



LEAD TREATMENT: PALLADIUM PLATING

Features

- Maximum conversion rate:
  - During PECL operation: 125MSPS
  - During TTL operation: 100MSPS
- Resolution: 10 bits
- Low power consumption: 480mW (typ.)
- Data input level: TTL
- Clock, reset input level: TTL and PECL compatible
- 2:1 multiplexed input function
- 1/2 frequency-divided clock output possible by the built-in clock frequency divider circuit
- Voltage output (50Ω load drive possible)
- Single power supply or ±dual power supply operation
- Reset signal polarity switching function

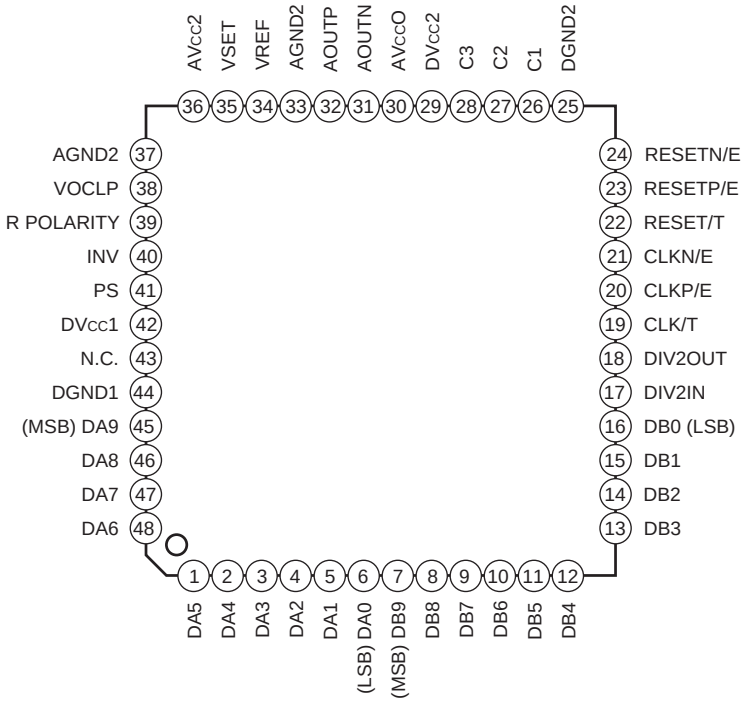
Structure

Bipolar silicon monolithic IC

Applications

- LCD
- DDS
- HDTV
- Communications (QPSK, QAM)
- Measuring devices

Pin Configuration



E97639-PS

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV$_{CC}$O, AV$_{CC}$2, DV$_{CC}$2	–0.5 to +6.0	V
	AGND2, DGND2	–6.0 to +0.5	V
	DV$_{CC}$1	–0.5 to +6.0	V
	AV$_{CC}$2 – AGND2	–0.5 to +6.0	V
	AV$_{CC}$O – AGND2	–0.5 to +6.0	V
	DV$_{CC}$2 – DGND2	–0.5 to +6.0	V
• Input voltage			
(Analog)	VSET	AGND2 – 0.5 to AV$_{CC}$2 + 0.5	V
(Digital)	TTL input pin	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
	PECL input pin	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
	PS	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
(Others)	VOCLP	DGND1 – 0.5 to DV$_{CC}$1 + 0.5	V
• Storage temperature	Tstg	– 65 to +150	°C
• Allowable power dissipation	Pd	1.4	W

(when mounted on a two-layer glass fabric base epoxy board with dimensions of 76mm × 114mm, t = 1.6mm)

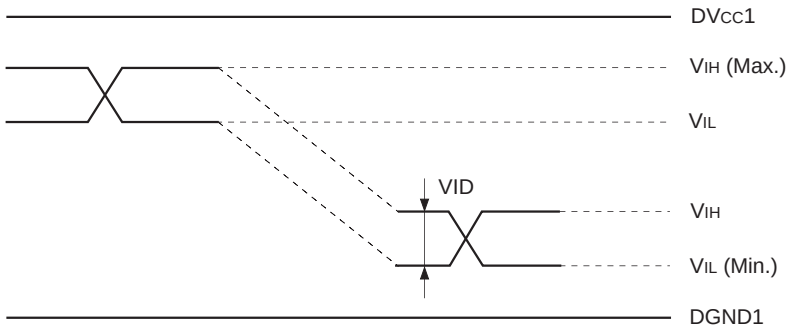
Recommended Operating Conditions

		[Single power supply]			[Dual power supply]			
• Supply voltage		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	AV$_{CC}$O	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
	AV$_{CC}$2	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
	AGND2	–0.05	0.0	+0.05	–5.50	–5.0	–4.75	V
	DV$_{CC}$1	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
	DGND1	–0.05	0.0	+0.05	–0.05	0.0	+0.05	V
	DV$_{CC}$2	+4.75	+5.0	+5.25	–0.05	0.0	+0.05	V
	DGND2	–0.05	0.0	+0.05	–5.50	–5.0	–4.75	V

			Min.	Typ.	Max.	Unit
• Input voltage						
(Analog)	VSET		AGND2 + 0.65		AGND2 + 1.03	V
(Digital)	TTL input pin	V_{IH}	DGND1 + 2.0			V
		V_{IL}			DGND1 + 0.8	V
	PECL input pin	V_{IH}	DV$_{CC}$1 – 1.05		DV$_{CC}$1 – 0.5	V
		V_{IL}	DV$_{CC}$1 – 3.2		DV$_{CC}$1 – 1.4	V
	VID*1		0.5	0.8		V
(Others)	VOCLP		DGND1 + 2.4		DV$_{CC}$1	V
• CLK pulse width (for RECL CLK)		tpw1	3.5			ns
		tpw0	3.5			ns
• Maximum conversion rate	During PECL operation	Fc	125			MSPS
	During TTL operation	Fc	100			MSPS
• Load resistance		R_L	50	50	≥ 10k	Ω
• Analog output full-scale voltage						
R_L ≥ 10kΩ		V_{FS}	1.5	2.0	2.1	V
R_L = 50Ω		V_{FS}	0.75	1.0	1.05	V
• Operating temperature		Ta	–20		+75	°C

*1 VID: Input Voltage Differential

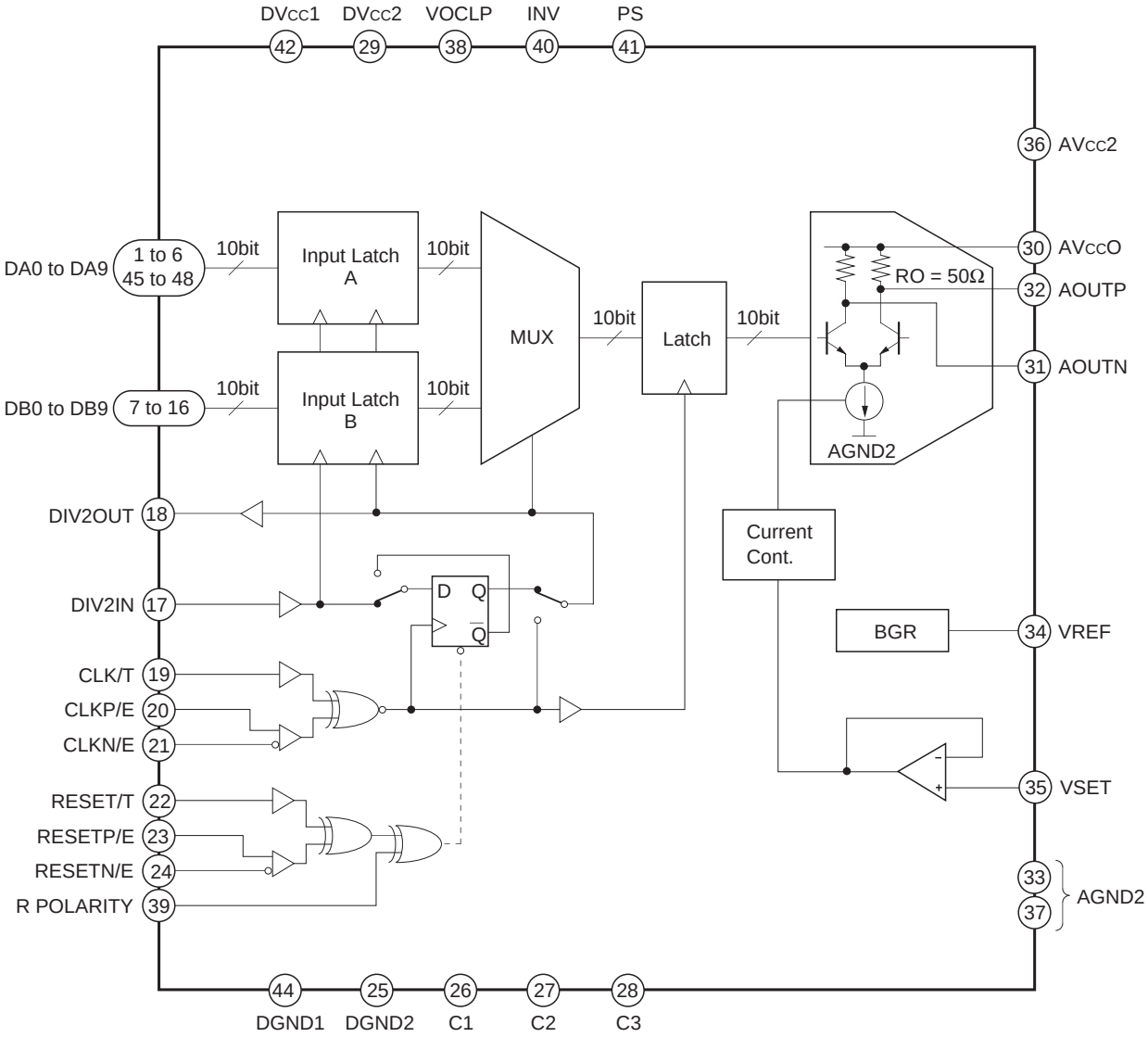
PECL input signal switching level



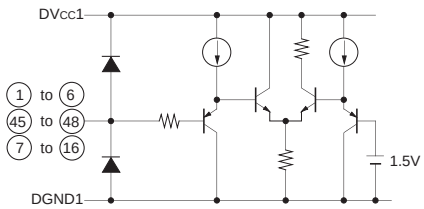
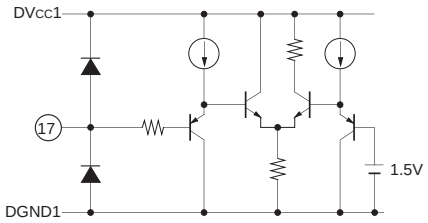
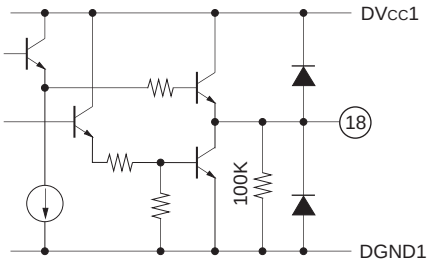
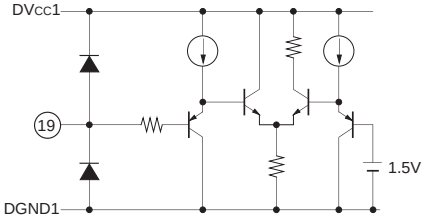
Pin Description

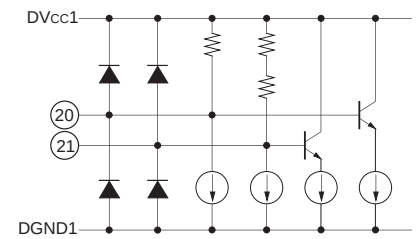
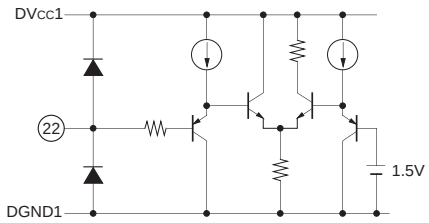
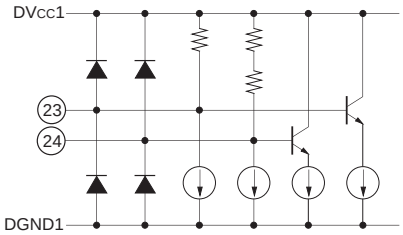
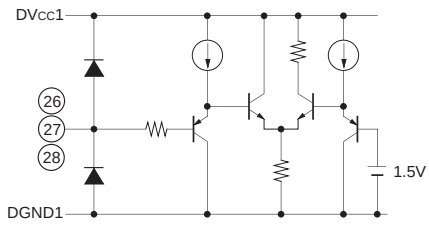
[Symbol]	[Pin No.]	[Description]	[Typical voltage level for a single power supply]	[Typical voltage level for dual power supply]
DA0 to DA9	1 to 6, 45 to 48	Side A data input.	TTL	TTL
DB0 to DB9	7 to 16	Side B data input.	TTL	TTL
DIV2IN	17	1/2 frequency-divided clock input.	TTL	TTL
DIV2OUT	18	1/2 frequency-divided clock output.	TTL	TTL
CLK/T	19	TTL clock input.	TTL	TTL
CLKP/E	20	PECL clock input.	PECL	PECL
CLKN/E	21	PECL clock input.	PECL	PECL
RESET/T	22	TTL reset input.	TTL	TTL
RESETP/E	23	PECL reset input.	PECL	PECL
RESETN/E	24	PECL reset input.	PECL	PECL
DGND2	25	Digital ground.	0V	–5V
C1	26	Function setting.	TTL	TTL
C2	27	Function setting.	TTL	TTL
C3	28	Function setting.	TTL	TTL
$DV_{CC}2$	29	Digital power supply.	5V	0V
$AV_{CC}O$	30	Analog output power supply.	5V (typ.)	0V (typ.)
AOUTN	31	Negative analog output.	$AV_{CC}O - V_{FS}$	$AV_{CC}O - V_{FS}$
AOUTP	32	Positive analog output.	$AV_{CC}O - V_{FS}$	$AV_{CC}O - V_{FS}$
AGND2	33	Analog ground.	0V	–5V
VREF	34	Analog reference voltage.	AGND2 + 1.25V	AGND2 + 1.25V
VSET	35	Full-scale adjustment.	AGND2 + 0.65V to AGND2 + 1.03V	AGND2 + 0.65V to AGND2 + 1.03V
$AV_{CC}2$	36	Analog power supply.	5V	0V
AGND2	37	Analog ground.	0V	–5V
VOCLP	38	TTL High level clamp.	Clamp voltage	Clamp voltage
R POLARITY	39	Reset signal polarity switching.	TTL	TTL
INV	40	Analog output inversion.	TTL	TTL
PS	41	Power saving.	TTL	TTL
$DV_{CC}1$	42	Digital power supply.	5V	5V
N.C.	43	Not connected.	—	—
DGND1	44	Digital ground.	0V	0V

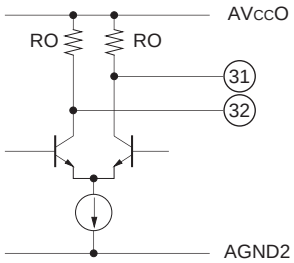
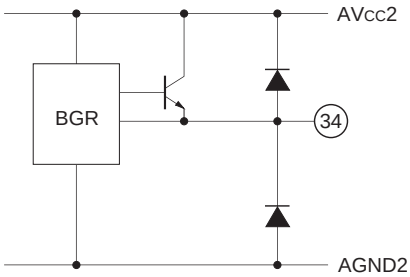
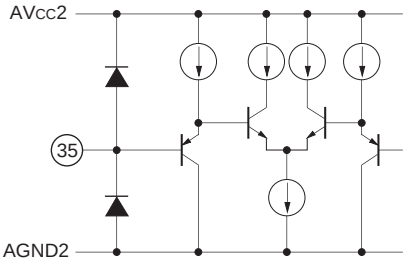
Block Diagram

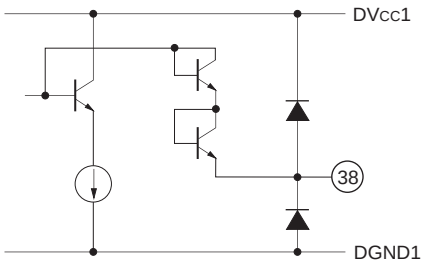
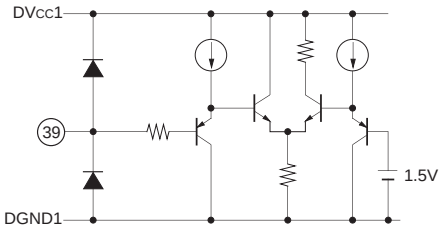
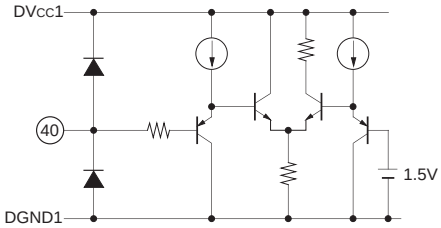
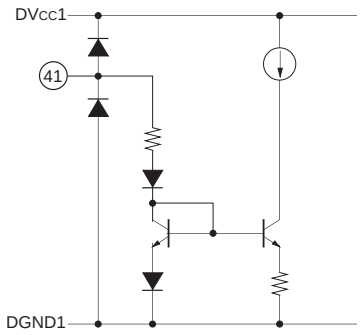


Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
1 to 6 45 to 48	DA0 to DA9	I	TTL		Side A data input.
7 to 16	DB0 to DB9	I	TTL		Side B data input.
17	DIV2IN	I	TTL		1/2 frequency-divided clock input. Use this pin in MUX.1A or MUX.2 mode. Leave open for other modes.
18	DIV2OUT	O	TTL		1/2 frequency-divided clock output. The 1/2 frequency-divided clock signal (DIV2OUT) is output in MUX.1A mode. Set to high impedance for other modes.
19	CLK/T	I	TTL		Clock input. Use this pin when the clock is input at TTL level. At this time, leave Pins 20 and 21 open.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
20	CLKP/E	I	PECL		Clock input. Use this pin when the clock is input at PECL level. At this time, leave Pin 19 open. CLKP/E and CLKN/E are complementary and should be used together.
21	CLKN/E	I	PECL		CLKP/E complementary input.
22	RESET/T	I	TTL		Reset signal input. When multiple CXA3197R are operated at the same time in MUX.1A or MUX.1B mode, the start timing of the internal 1/2 frequency divider circuits should be matched. At this time, the reset signal is used; when the reset signal is at TTL level, Pin 22 is used and Pins 23 and 24 are left open. When the reset signal is at PECL level, Pins 23 and 24 are used and Pin 22 is left open. The reset signal polarity can be set by Pin 39 (R POLARITY). Leave the reset pin open when other modes are used. RESETP/E and RESETN/E are complementary and should be used together.
23	RESETP/E	I	PECL		
24	RESETN/E	I	PECL		
25	DGND2		Single power supply: GND Dual power supply: –5V		Digital power supply.
26	C1	I	TTL		Function setting.
27	C2	I	TTL		Function setting.
28	C3	I	TTL		Function setting.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
29	DVcc2		Single power supply: +5V Dual power supply: GND		Digital power supply.
30	AVccO		Single power supply: +5V Dual power supply: GND		Analog output power supply. The AVccO pin voltage can be varied within the range that satisfies the analog output compliance voltage.
31	AOUTN	O	AVccO – VFS		Negative analog output. The inverse of the positive analog output pin is output. When the positive output is terminated with 50Ω, the inverse output pin should also be terminated with 50Ω even if the inverse output is not used.
32	AOUTP	O	AVccO – VFS		Positive analog output.
33	AGND2		Single power supply: GND Dual power supply: –5V		Analog ground.
34	VREF	O	AGND + 1.25V (Typ.)		Reference voltage output.
35	VSET	I	AGND2 + 0.65V to AGND2 + 1.03V		Analog output full-scale adjustment.
36	AVcc2		Single power supply: +5V Dual power supply: GND		Analog power supply.

Pin No.	Symbol	I/O	Typical voltage level	Equivalent circuit	Description
37	AGND2		Single power supply: GND Dual power supply: –5V		Analog power supply.
38	VOCLP	I	Clamp voltage		TTL output High level clamp. A TTL level signal is output from the DIV2OUT pin in MUX.1A mode. The TTL High level voltage can be clamped to the value approximately equivalent to the voltage applied to this pin. Leave the VOCLP pin open for other modes.
39	R POLARITY	I	TTL		Reset signal polarity switching. At High level, the reset polarity is active Low; at Low level, active High.
40	INV	I	TTL		Analog output polarity inversion. The analog output is inverted at Low level.
41	PS	I	TTL		Power saving. Power saving mode is activated at Low level. Normally pull up the PS pin to High level as this pin is open Low.
42	DVcc1		5V		Digital power supply.
43	N.C.				Not connected.
44	DGND1		0V		Digital ground.

Electrical Characteristics

(DVcc1, DVcc2, AVcc2, AVccO = +5V, DGND1, DGND2 = 0V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		10	10	10	bit
Differential linearity error	DLE	VFS = 1000mV *2			–0.85/+0.5	LSB
					–1.2/+0.5	LSB
Integral linearity error	ILE				±1.2	LSB
Digital input (PECL)						
Digital input voltage	VIH		DVcc1 – 1.05		DVcc1 – 0.5	V
	VIL		DVcc1 – 3.2		DVcc1 – 1.4	V
Digital input current	IIH	VIH = DVcc1 – 0.8V	0		20	µA
	IIL	VIL = DVcc1 – 1.6V	–30		0	µA
Digital input capacitance					5	pF
Digital input (TTL)						
Digital input voltage	VIH		2			V
	VIL				0.8	V
Threshold voltage	VTH			1.5		V
Digital input current	IIH	VIH = 3.5V	–1		1	µA
	IIL	VIL = 0.2V	–2		0	µA
Digital input capacitance					5	pF
Digital output (TTL)						
Digital output voltage	VOH	IOH = –2.0mA	2.4			V
	VOL	IOL = 1.0mA			0.5	V
Leak current at high impedance		When VO = 5V	10		100	µA
		When VO = 0V	–1		1	µA
Digital output rise time	Tr	0.8 to 2.4V (CL = 10pF)	1		1.5	ns
Digital output fall time	Tf	0.8 to 2.4V (CL = 10pF)	0.6		1.2	ns
PS pin input (PS)						
PS pin input voltage	VIH		2			V
	VIL				0.8	V
PS pin input current	IIH	VIH = 3.5V	1		100	µA
	IIL	VIL = 0.2V	–1		0	µA
Clamp pin (VOCLP)						
VOCLP pin input current	IVOCLP	VOCLP = DVcc1	0		5	µA
	IVOCLP	VOCLP = 2.4V	–60		–10	µA
Analog output characteristics						
Output full-scale voltage						
: RL ≥ 10kΩ	VFS		1.5	2	2.1	V
: RL = 50Ω	VFS		0.75	1	1.05	V
Output zero offset voltage						
: RL ≥ 10kΩ	VOF	} VSET = AGND2 + 937.5mV	0		20	mV
: RL = 50Ω	VOF		0		10	mV
Analog output resistance	RO			50		Ω
Analog output capacitance	CO			10		pF
Absolute amplitude error	EG	VSET = AGND2 + 937.5mV	–4.0		4.0	% of F.S.
Absolute amplitude error temperature characteristics	TCG	VFS = 1000mV at 25°C			60	ppm/°C
Analog output rise time	Tr	} When RL = 50Ω,	0.85		1.05	ns
Analog output fall time	Tf	} VFS = 1V,10 – 90%	0.75		0.85	ns
Settling time	tSET				3.5	ns
Glitch energy	GE				5	pVsec
Compliance voltage	VOC	Mesured to DVcc2 *3	–2.1		1.5	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference/control amplifier characteristics						
VREF pin output voltage	V_{REF}	} I_{REFOUT} = 1mA	AGND2 + 1.18	AGND2 + 1.25	AGND2 + 1.32	V
VREF pin output voltage in PS mode	V_{REF}		AGND2 + 1.18	AGND2 + 1.25	AGND2 + 1.32	V
VREF voltage drift coefficient					250	ppm/°C
VSET pin input current	I_{SET}		–5		0	µA
Multiplying bandwidth		100mVp-p, SIN, at –3dB	50			MHz
Current consumption	I_{CC}	Total current consumption	63	96	129	mA
	$DI_{CC}1$	DIcc1 current consumption	7	15.5	24	mA
	$DI_{CC}2$	DIcc2 current consumption	13	19	25	mA
	$AI_{CC}2$	AIcc2 current consumption	6	8.5	11	mA
	$AI_{CC}O$	AIccO current consumption	37	53	69	mA
Current consumption in PS mode *4	I_{CC}	Total current consumption in PS mode		0.432	4	mA
	$DI_{CC}1$	DIcc1 current consumption in PS mode		0.38	1.5	mA
	$DI_{CC}2$	DIcc2 current consumption in PS mode		0.001	0.2	mA
	$AI_{CC}2$	AIcc2 current consumption in PS mode		0.05	0.3	mA
	$AI_{CC}O$	AIccO current consumption in PS mode		0.001	2	mA

*2 64-step D.L.E. This indicates the D.L.E. when the INV pin is High and the data input code changes between:

(MSB) (LSB) (MSB) (LSB)
0 0 0 0 1 1 1 1 1 1 ⟷ 0 0 0 1 0 0 0 0 0 0

at the AOUTP side output or between:

(MSB) (LSB) (MSB) (LSB)
1 1 1 1 0 0 0 0 0 0 ⟷ 1 1 1 0 1 1 1 1 1 1

at the AOUTN side output.

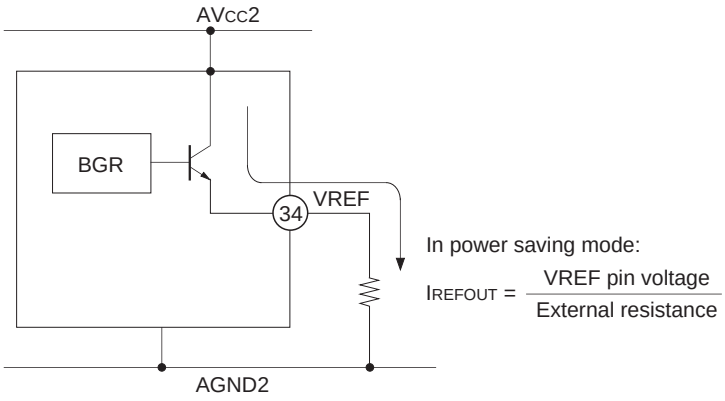
*3 When using the analog output within the compliance voltage range, set $AV_{CC}O$ so that it satisfies the following equations.

V_{OC} (min) = ($AV_{CC}O$ – VFS) – $DV_{CC}2 \geq -2.1V$

V_{OC} (max) = ($AV_{CC}O$ – VOF) – $DV_{CC}2 \leq 1.5V$

*4 The current consumption in power saving mode does not include the VREF pin output current. When grounding the VREF pin to the AGND2 level using external resistance, a voltage of 1.18 to 1.32V is generated at the VREF pin even in power saving mode. Therefore, the current indicated by the following equation flows from the AVCC2 pin to the VREF pin. This value must be added to obtain the actual current consumption in power saving mode.

$$\frac{\text{VREF pin voltage}}{\text{External resistance}} = I_{REFOUT}$$



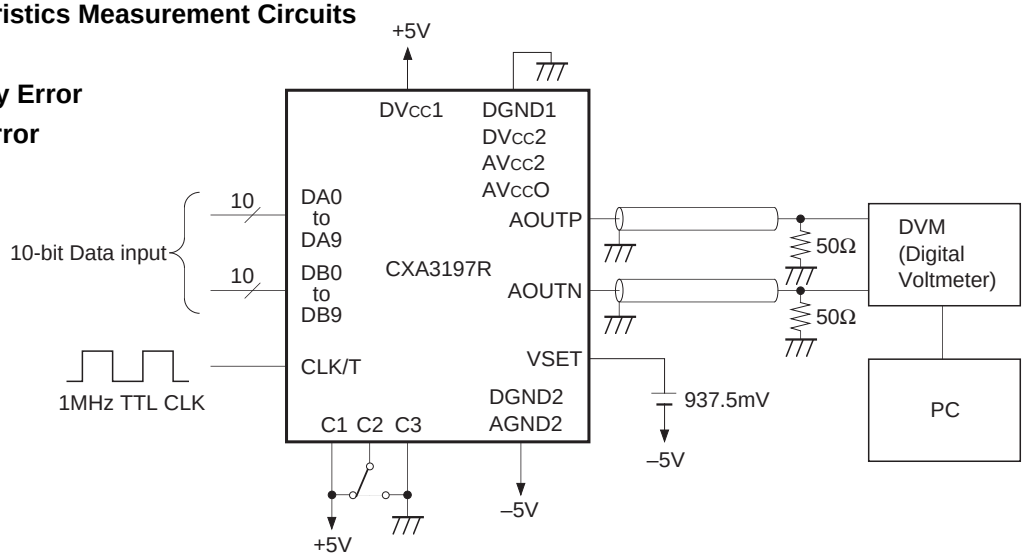
			CLK signal level		PECL			TTL			PECL			
			Reset signal level		PECL			TTL			TTL			
Item			Symbol	Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Switching characteristics	MUX.1A mode	Maximum conversion rate	FC		125			100			125			MSPS
		Clock High pulse width	Tpw1		3.5			4.5			3.5			ns
		Clock Low pulse width	Tpw0		3.5			3.0			3.5			ns
		Reset signal setup time	ts-rst		0			1.0			4.0			ns
		Reset signal hold time	th-rst		1.0			3.0			0			ns
		DIV2OUT output delay	td-DIV	C_L = 10pF	5.5	6.5	8	8.0	9.5	12.0	5.5	6.5	8	ns
		DIV2OUT to DIV2IN maximum delay time	2T-tm				2T – 7			2T – 7			2T – 7	ns
		Data input setup time	ts		1.0			1.0			1.0			ns
		Data input hold time	th		5.0			5.0			5.0			ns
		Analog output pipeline delay	t_{PD} (A)			4			4			4		CLK
			t_{PD} (B)			5			5			5		
		Analog output delay	tdo		5.0	5.5	6.0	6.5	7.5	8.5	5.0	5.5	6.0	ns
	MUX.1B mode	Maximum conversion rate	FC		125			100			125			MSPS
		Clock High pulse width	Tpw1		3.5			4.5			3.5			ns
		Clock Low pulse width	Tpw0		3.5			3.0			3.5			ns
		Reset signal setup time	ts-rst		0			1.0			4.0			ns
		Reset signal hold time	th-rst		1.0			3.0			0			ns
		Data input setup time	ts		1.0			1.0			1.0			ns
		Data input hold time	th		4.0			6.0			4.0			ns
		Analog output pipeline delay	t_{PD} (A)			2			2			2		CLK
			t_{PD} (B)			3			3			3		
		Analog output delay	tdo		5.0	5.5	6.0	6.5	7.5	8.5	5.0	5.5	6.0	ns

				CLK signal level	PECL			TTL			
				Reset signal level	— *4			— *4			
Item			Symbol	Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Switching characteristics	MUX.2 mode	Maximum conversion rate	FC		125			100			MSPS
		Clock High pulse width	Tpw1		3.5			4.5			ns
		Clock Low pulse width	Tpw0		3.5			3.0			ns
		DIV2IN setup time	ts-DIV		4.5			2.0			ns
		DIV2IN hold time	th-DIV		0			3.5			ns
		Data input setup time	ts		1.0			1.0			ns
		Data input hold time	th		5.0			5.0			ns
		Analog output pipeline delay	t_{PD} (A)			2			2		CLK
			t_{PD} (B)			3			3		
		Analog output delay	tdo		5.0	5.5	6.0	6.5	7.5	8.5	ns
	SELE.A, SELE.B modes	Maximum conversion rate	FC		125			100			MSPS
		Clock High pulse width	Tpw1		3.5			4.5			ns
		Clock Low pulse width	Tpw0		3.5			3.0			ns
		C2 signal setup time	ts-C2		1.0			1.0			ns
		C2 signal hold time	th-C2		2.5			3.5			ns
		Data input setup time	ts		1.0			1.5			ns
		Data input hold time	th		2.0			3.5			ns
		Analog output pipeline delay	t_{PD} (A)			1			1		CLK
			t_{PD} (B)			1			1		
		Analog output delay	tdo		5.0	5.5	6.0	6.5	7.5	8.5	ns

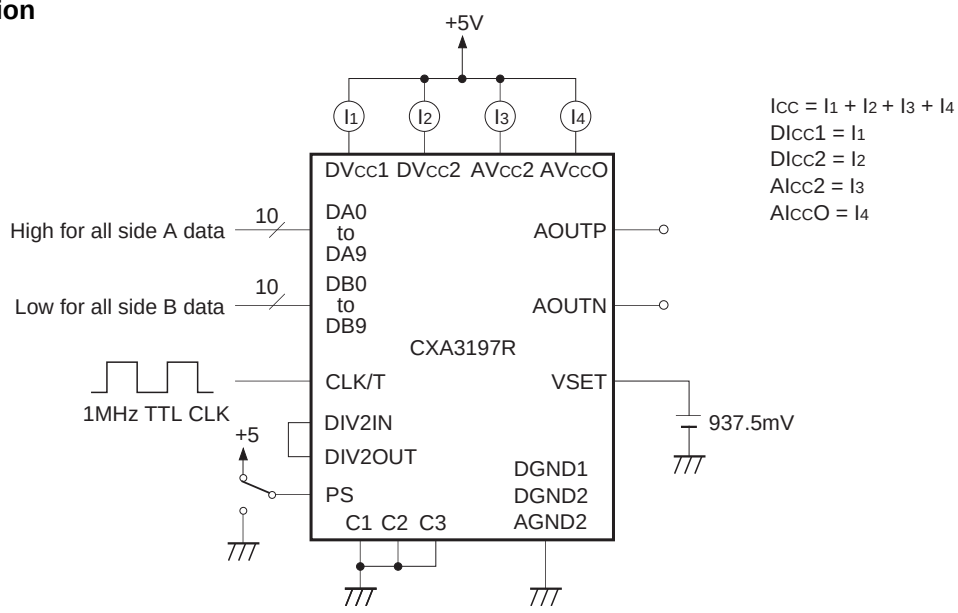
*4 The reset signal is not input in MUX.2, SELE.A or SELE.B mode.

Electrical Characteristics Measurement Circuits

Differential Linearity Error
Integral Linearity Error

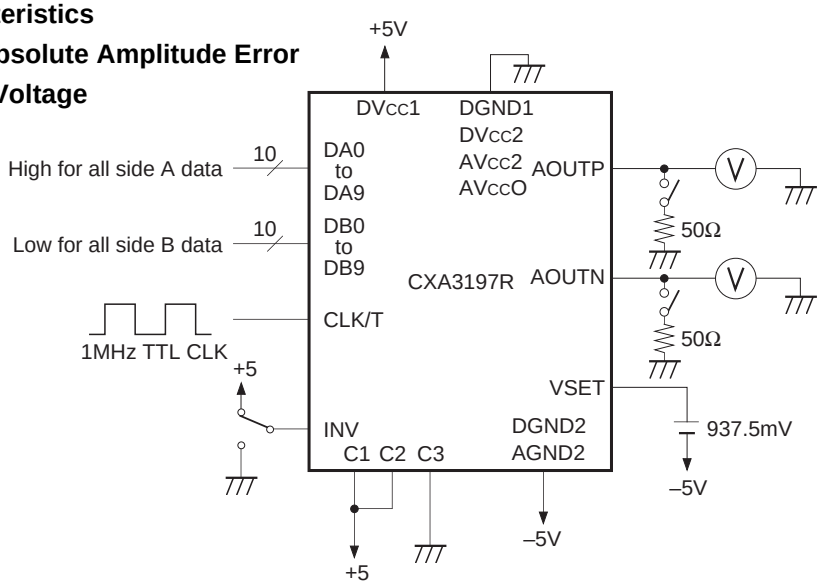


Current Consumption

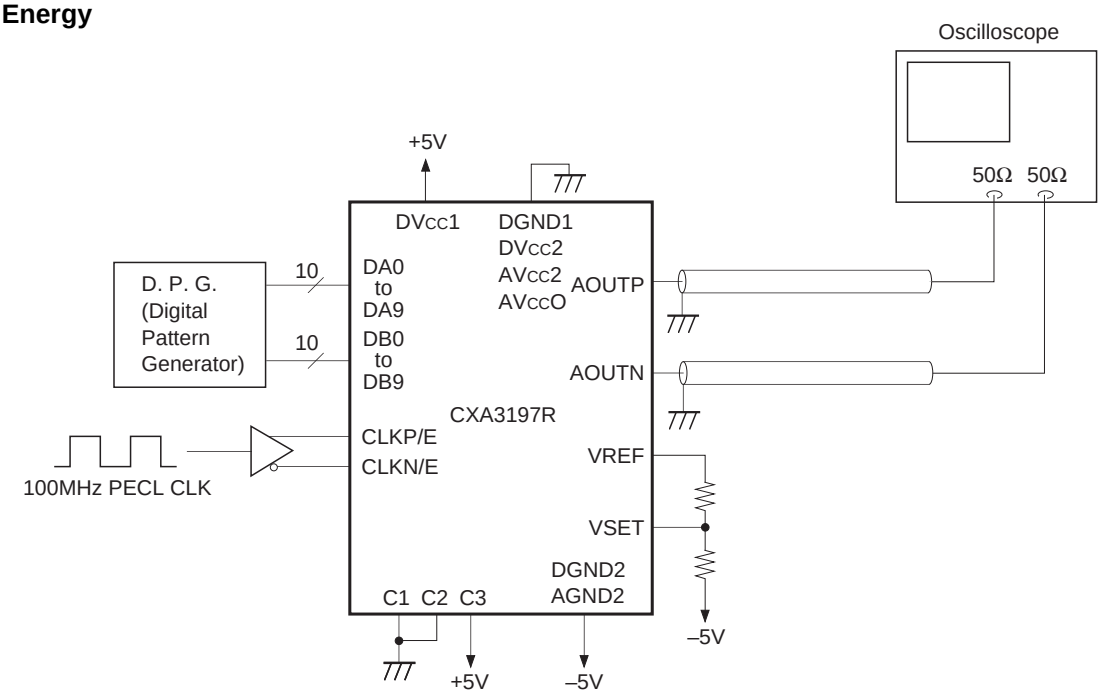


Analog Output Characteristics

Output Full-Scale Absolute Amplitude Error
Output Zero Offset Voltage

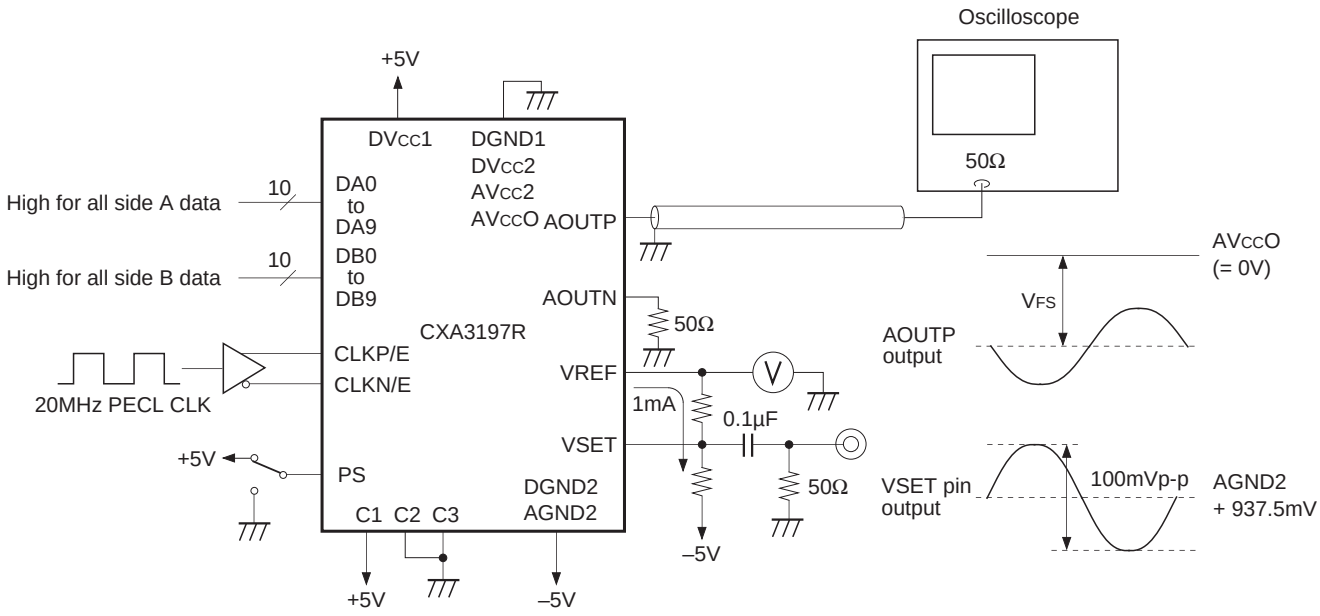


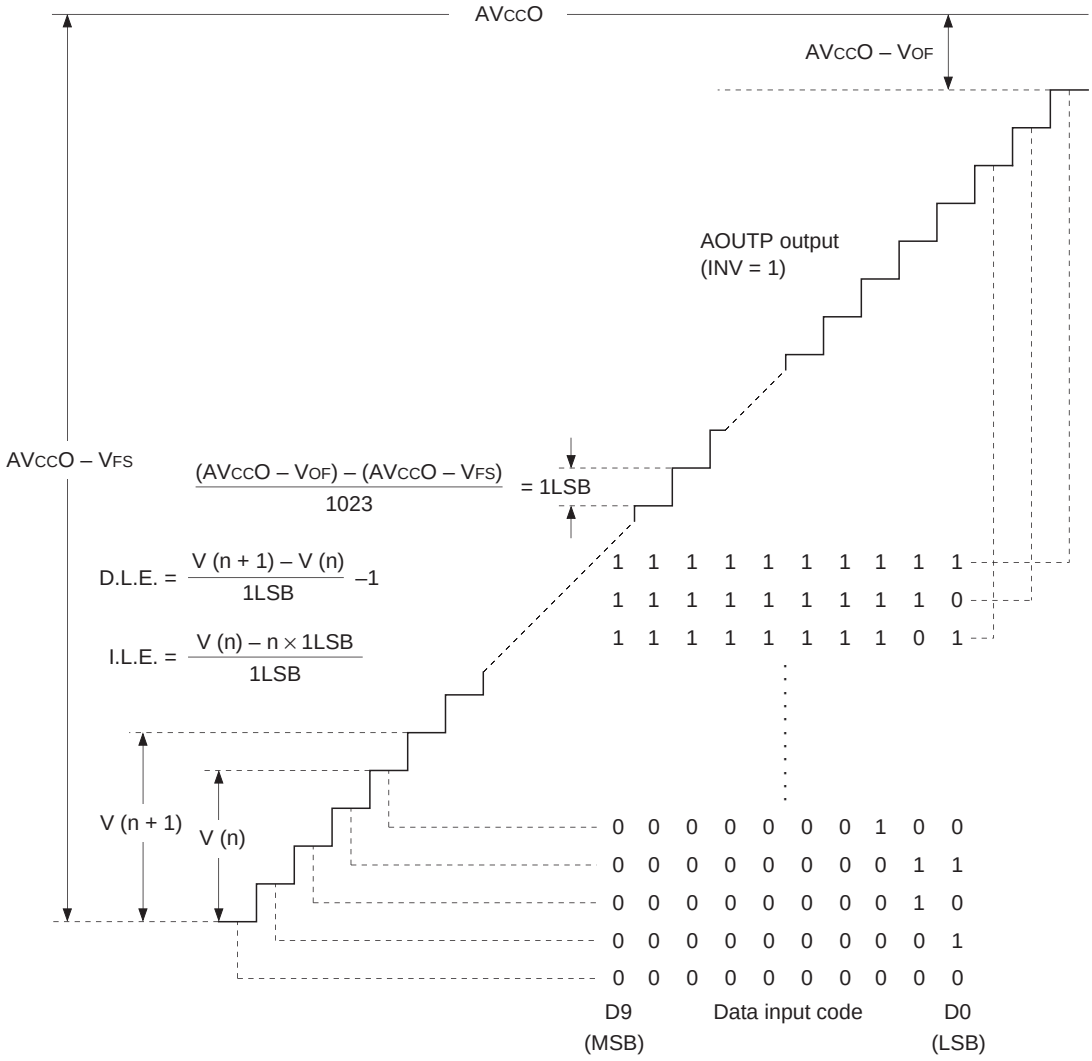
Analog Output Rise Time
Analog Output Fall Time
Settling Time
Glitch Energy



Reference/Control Amplifier Characteristics

VREF Pin Output Voltage
VREF Pin Output Voltage in Power Saving Mode
Multiplying Bandwidth





Data input code				Analog output level	
INV = 1		INV = 0		AOUTP	AOUTN
(MSB) D9	(LSB) D0	(MSB) D9	(LSB) D0		
1 1 1 1 1 1 1 1 1 1 : 0 0 0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0 0 0 : 1 1 1 1 1 1 1 1 1 1		AVCCO – VOF : AVCCO – VFS	AVCCO – VFS : AVCCO – VOF

Table 1. I/O Correspondence Table

Description of Operation

The CXA3197R has four types of operation modes to support various applications. The operation mode is set by switching the function setting pins (C1, C2 and C3).

Operation Mode Table

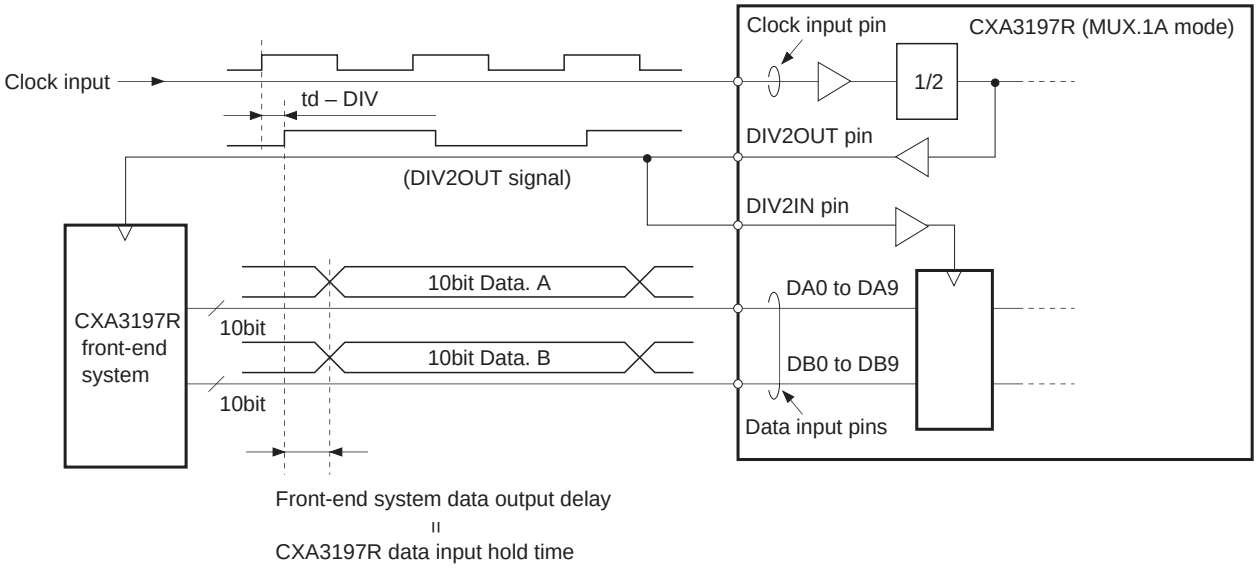
Mode	C1	C2	C3	CLK IN (MSPS)	Data IN (Mbps)	AOUT (Mbps)	DIV2OUT pin	Description of operation
MUX.1A	0	0	0	125	62.5	125	Outputs CLK/2 at TTL level	MUX operation by the internal CLK/2
MUX.1B	0	0	1				High impedance	MUX operation by the internal CLK/2
MUX.2	0	1	0				High impedance	MUX operation by DIV2IN
SELE.A	1	0	0		125		High impedance	D/A conversion of side A data input
SELE.B	1	1	0				High impedance	D/A conversion of side B data input

The CXA3197R can input data divided into two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplex the data, and output it as an analog signal, making it possible to halve the data rate. This lets the CXA3197R support the TTL data input level in contrast to the ECL data input level for conventional high-speed D/A converters. The clock signal and reset signal input levels can be selected from either TTL or PECL according to the application. (However, setting both signals to either TTL or PECL input level is recommended.)

1. MUX.1A mode

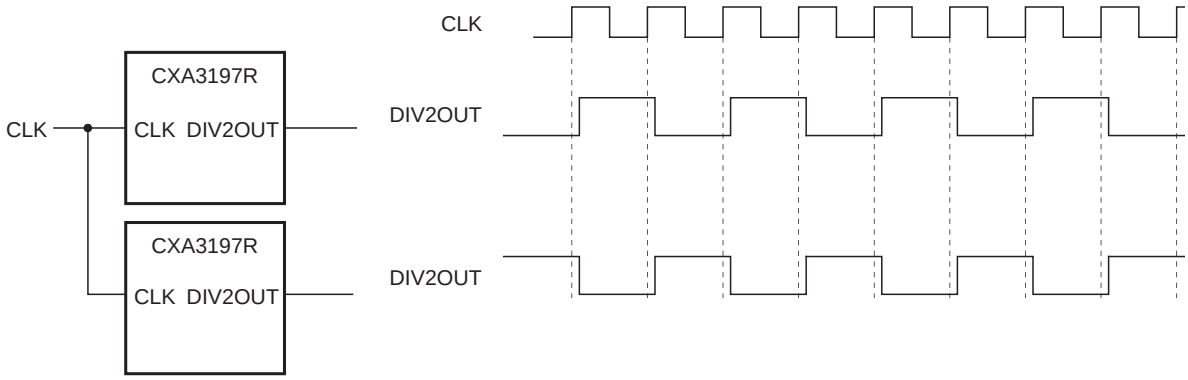
Set C1, C2 and C3 all Low for this mode.

In MUX.1A mode, the frequency of the clock input from the clock input pin is halved internally, and the 1/2 frequency-divided signal is output at TTL level from the DIV2OUT pin. Data synchronized with the DIV2OUT signal (the signal output from the DIV2OUT pin) can be obtained by operating the CXA3197R front-end system with the DIV2OUT signal. The timing at which the data output delay of the CXA3197R front-end system matches with the hold time during CXA3197R data input can be easily set by inputting this synchronized data to the data input pins and the DIV2OUT signal to the DIV2IN pin. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplexed, and extracted as analog output.

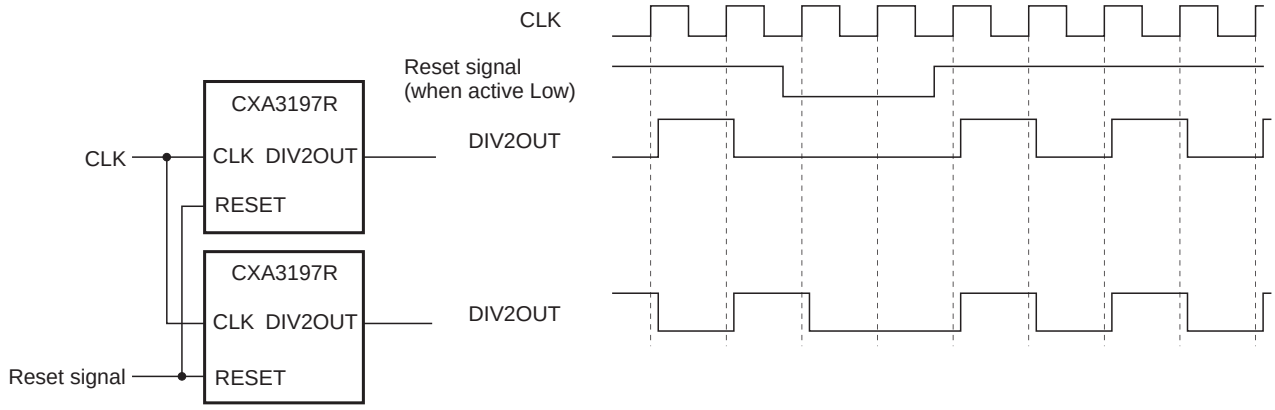


When using the multiple CXA3197R in MUX.1A mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example below. As a countermeasure, the MUX.1A mode has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See the timing chart for the detailed timing.

Example when not using the reset signal



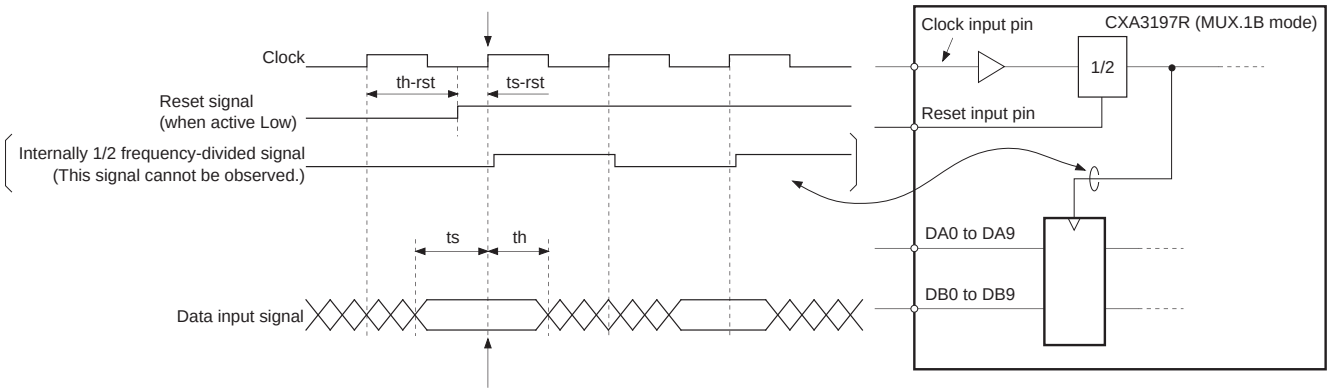
Example when using the reset signal



2. MUX.1B mode

Set C1 and C2 Low and C3 High for this mode.

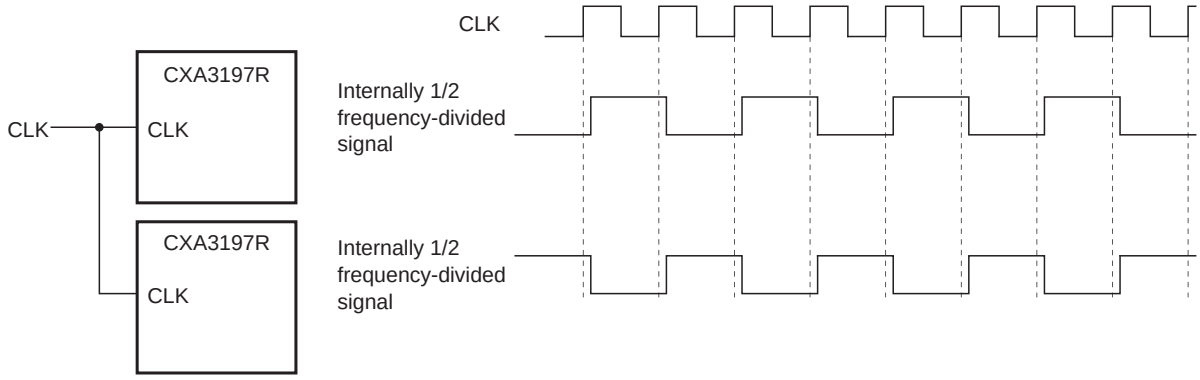
In MUX.1B mode, the frequency of the clock input from the clock input pin is halved internally, and the data is loaded by this 1/2 frequency-divided signal. The 1/2 frequency-divided signal cannot be observed at this time, so the data is actually loaded by observing the clock and reset signals to estimate the rising edge of the internally 1/2 frequency-divided signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay after loading by the clock.



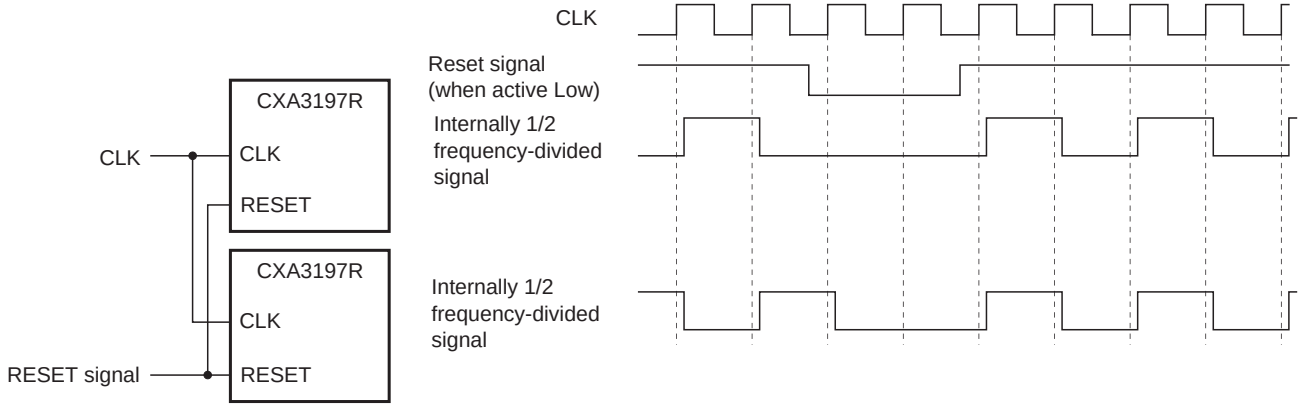
After the reset is released, the internal 1/2 frequency-divided signal commences at the first clock edge, so be sure to input the data in a manner that satisfies the setup time (ts) and hold time (th) with respect to this clock edge.

Like MUX.1A mode, when using the multiple CXA3197R in MUX.1B mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example below. As a countermeasure, the MUX.1B mode also has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See the timing chart for the detailed timing.

Example when not using the reset signal



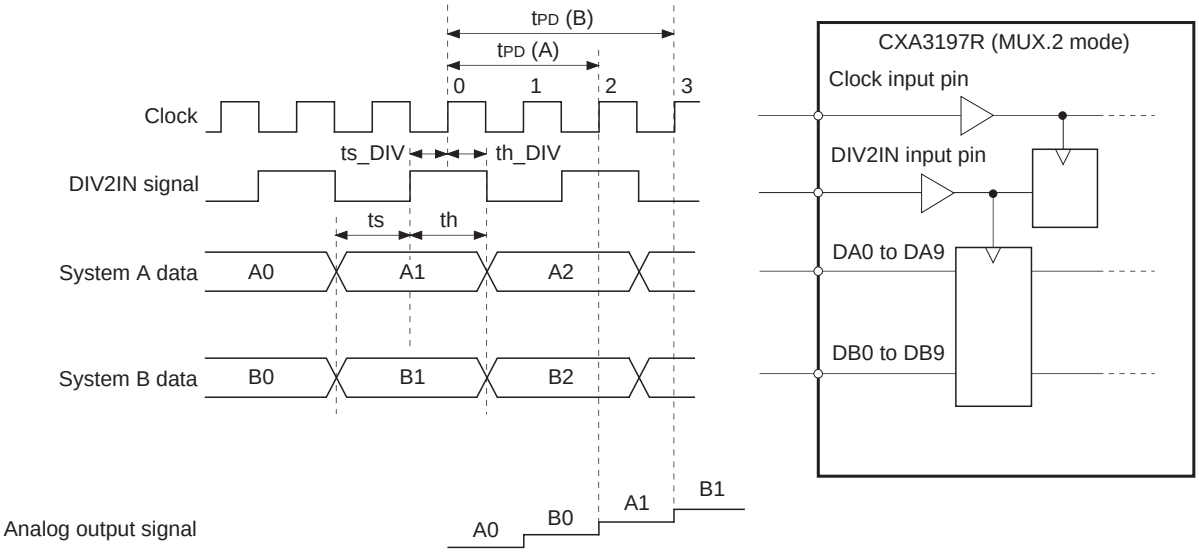
Example when using the reset signal



3. MUX.2 mode

Set C1 and C3 Low and C2 High for this mode.

In MUX.2 mode, the clock is input to the clock input pin, and the signal with a cycle half that of the clock (hereafter, DIV2IN signal) is input to the DIV2IN pin at TTL level. The DIV2IN signal is internally latched by the clock, so consideration must be given to the setup time (ts_DIV) and hold time (th_DIV) with respect to the clock. In addition, the data is loaded by the DIV2IN signal, so consideration must also be given to the setup time (ts) and hold time (th) with respect to the DIV2IN signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay from the clock that loads the DIV2IN signal. See the timing chart for the detailed timing.



4. SELE.A mode and SELE.B mode

Set C1 High and C2 and C3 Low for SELE.A mode.

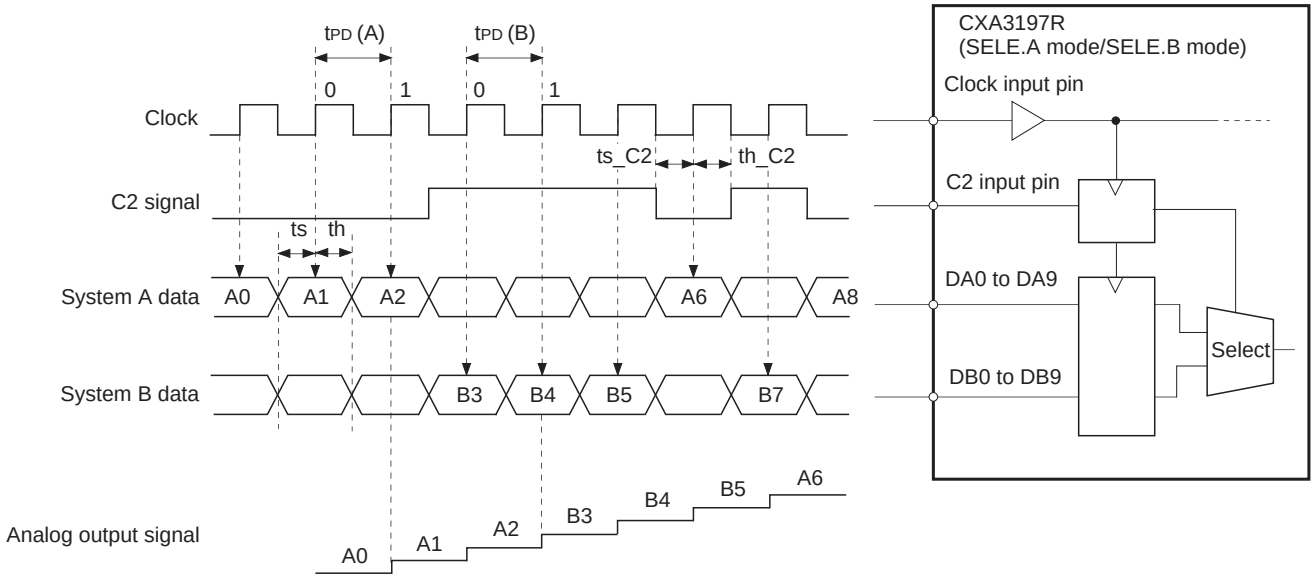
In SELE.A mode, the clock is input to the clock input pin, and the data is input to the system A (DA0 to DA9) data input pins.

Set C1 and C2 High and C3 Low for SELE.B mode.

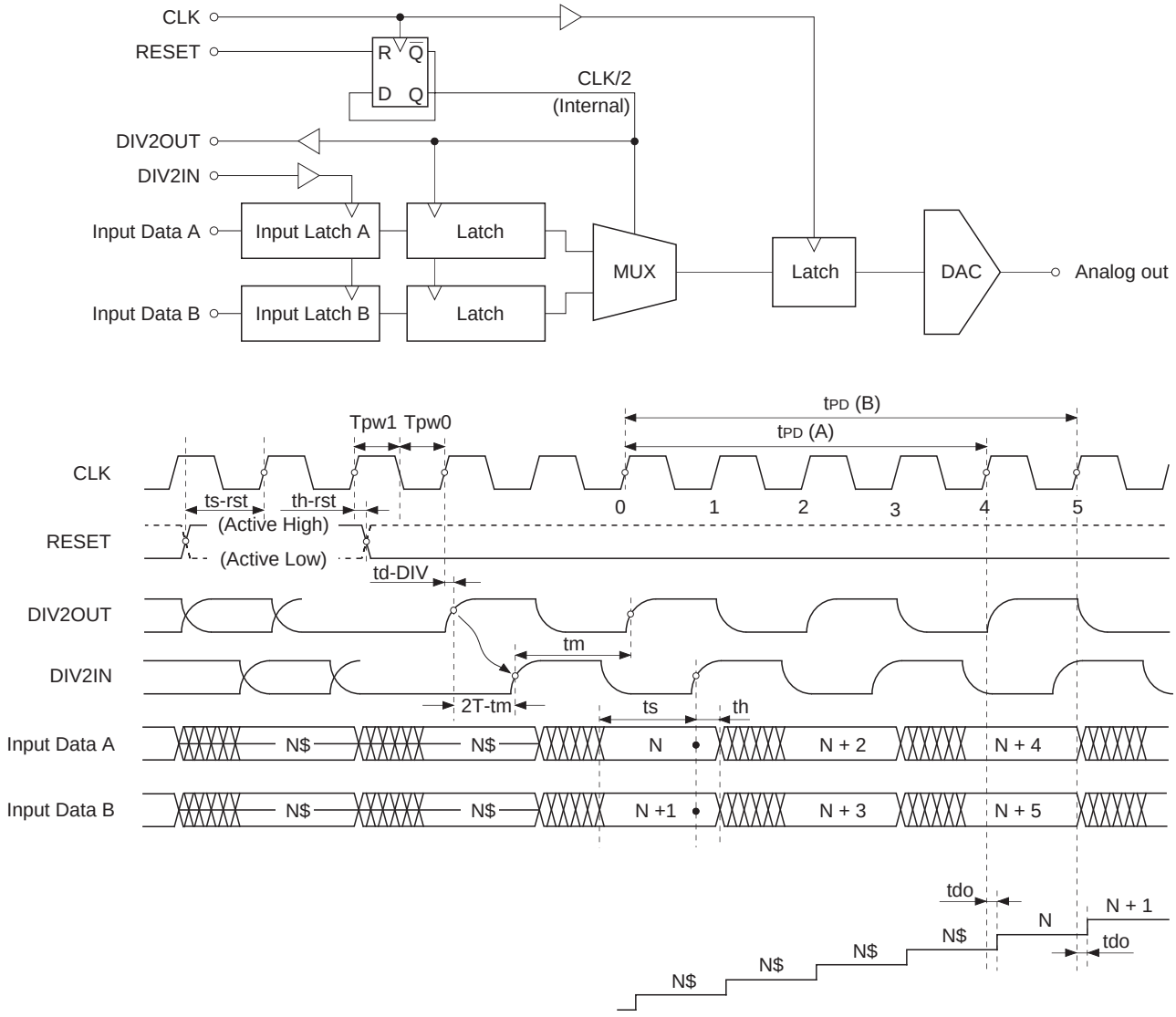
In SELE.B mode, the clock is input to the clock input pin, and the data is input to the system B (DB0 to DB9) data input pins.

In either mode, consideration must be given to the setup time (ts) and hold time (th) with respect to the clock. Also, the data is output as an analog signal with a 1-clock pipeline delay after loading by the clock.

Switching between SELE.A mode and SELE.B mode is done by switching the C2 pin between High and Low levels. Also, the mode can be switched at high speed in sync with the clock by inputting the switching signal (C2 signal) to the C2 pin. The C2 signal is internally latched by the clock, so consideration must be given to the setup time (ts_C2) and hold time (th_C2) with respect to the clock. See the timing chart for the detailed timing.

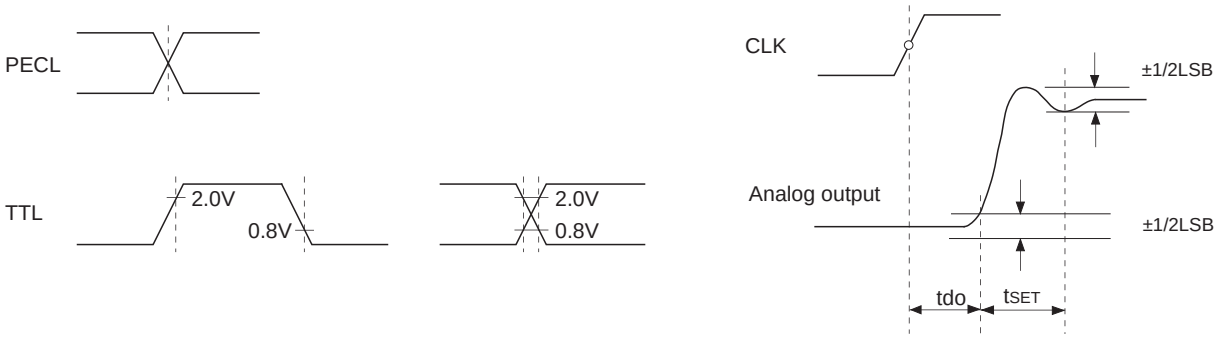


Block Diagram & Timing Chart (MUX.1A Mode)

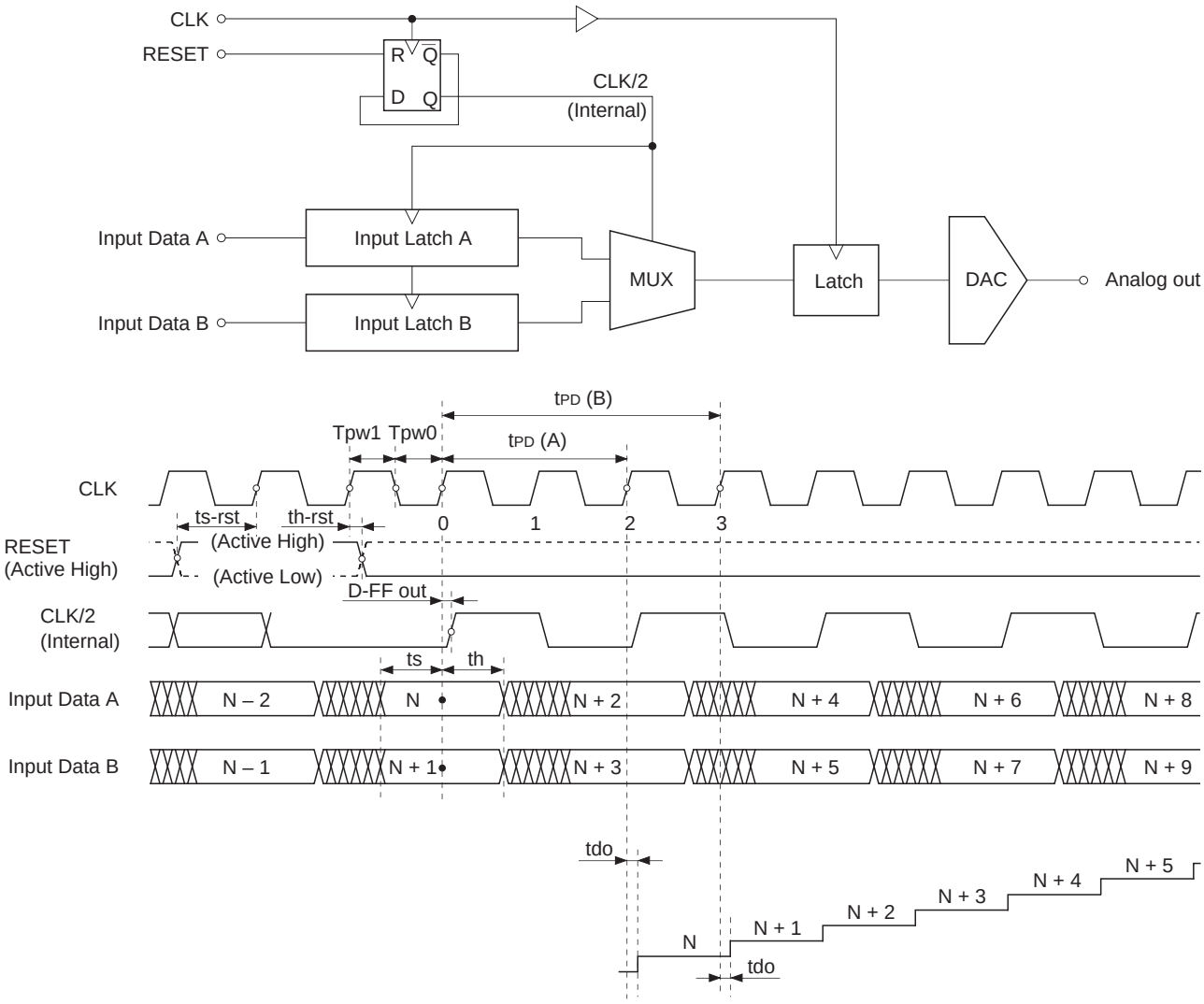


In MUX.1A mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit and the CLK/2 can be output at TTL level (DIV2OUT). CLK/2 can be reset by the reset signal.

(Timing judgment points)

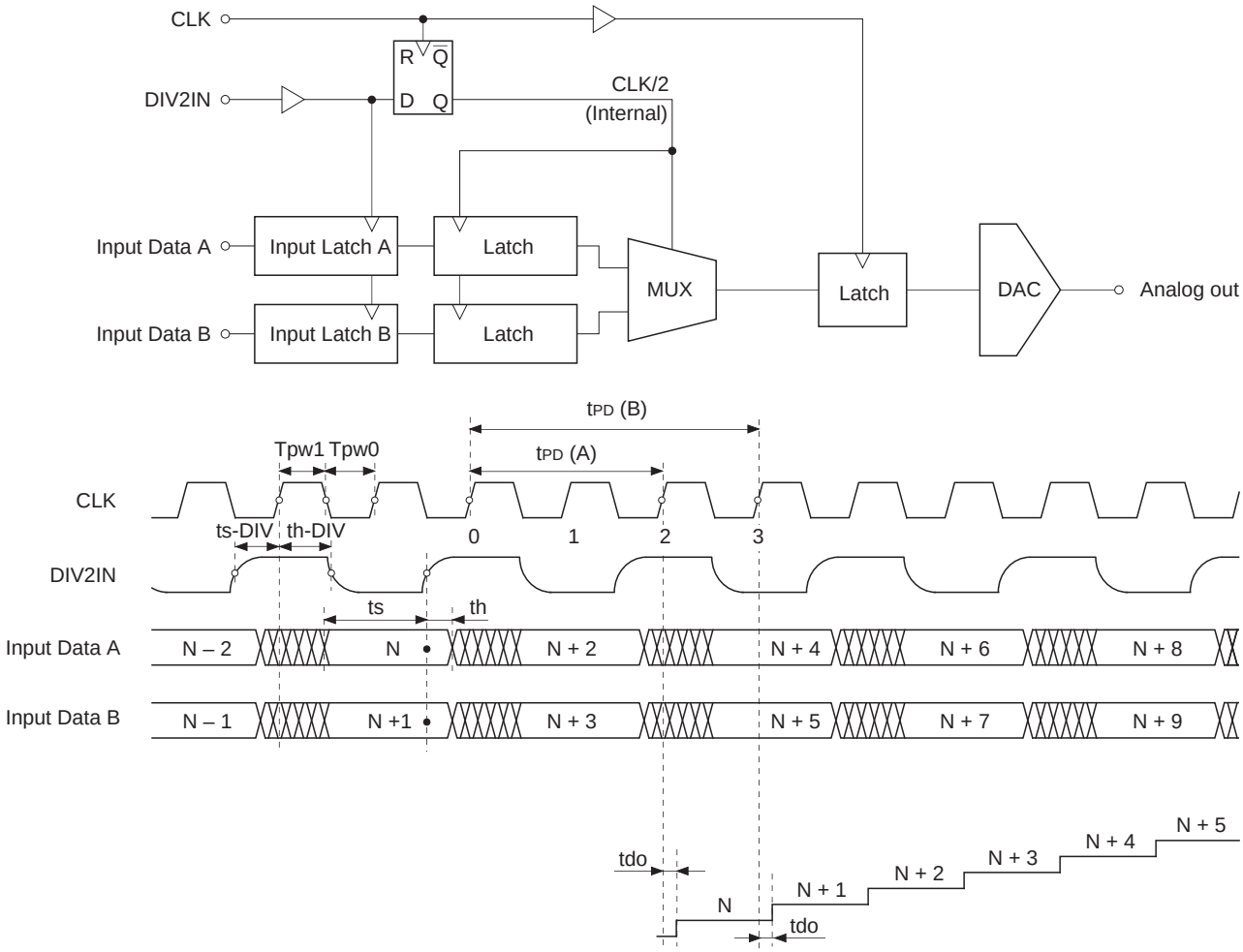


Block Diagram & Timing Chart (MUX.1B Mode)



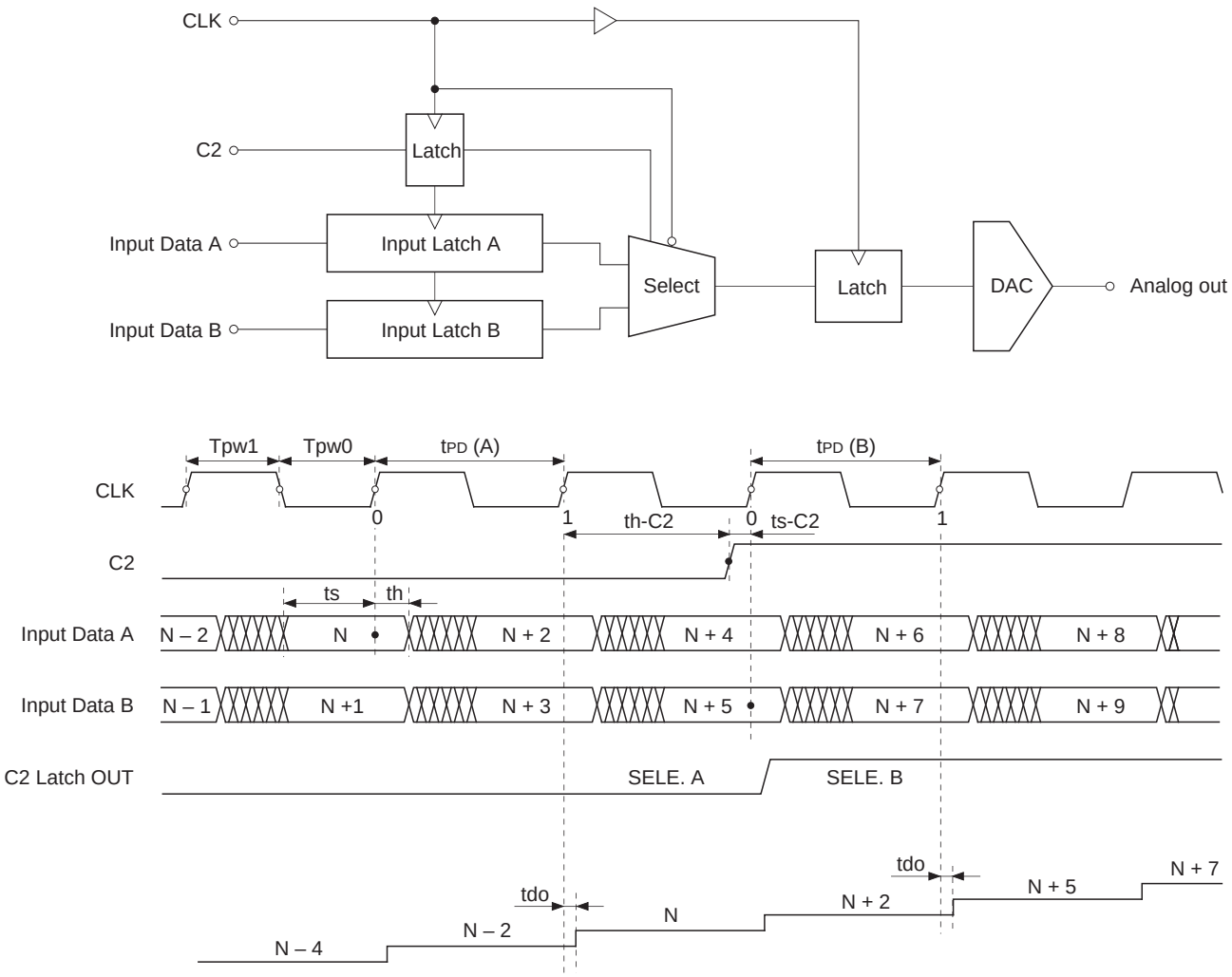
In MUX.1B mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit. CLK/2 can be reset by the reset signal.

Block Diagram & Timing Chart (MUX.2 Mode)



In MUX.2 mode, the 1/2 frequency-divided clock signal (DIV2IN) and Data A and Data B, which are synchronized with DIV2IN, are provided simultaneously. These signals are internally multiplexed and the resulting signal can be analog output.

Block Diagram & Timing Chart (SELE.A, SELE.B Mode)



In SELE.A and SELE.B modes, input Data A or Data B is selected and the selected data can be analog output. When C1 = 1 and C3 = 0, Data A is selected for C2 = 0, and Data B is selected for C2 = 1.

Application Circuit

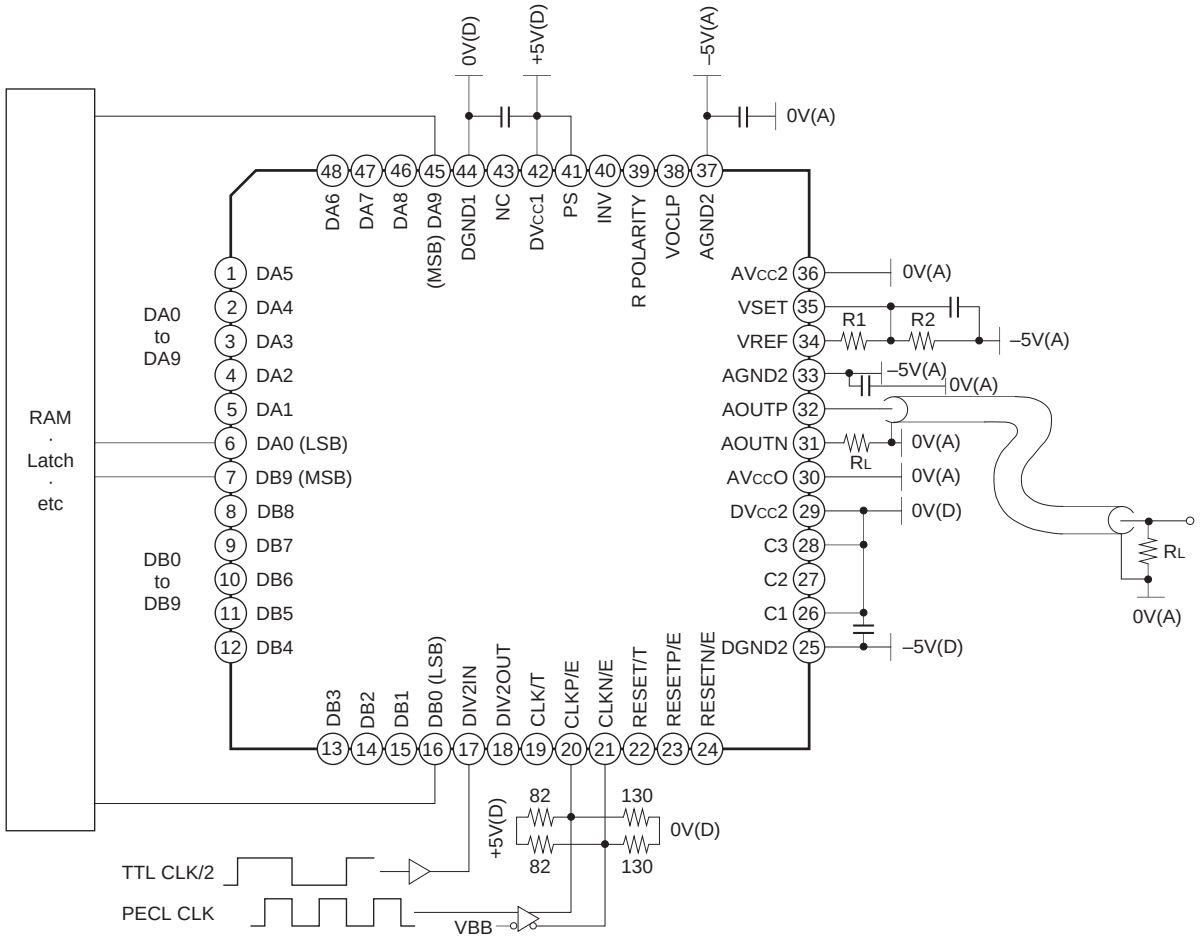
The circuit shown below is the basic circuit when the analog output is terminated with external resistance of 50Ω for operation with dual ±5V power supply in MUX.2 mode. The analog output uses AVCCO as the reference. The analog output full-scale voltage V_{FS} is obtained with the following equation.

$$V_{FS} = \frac{V_{SET}}{375} \times (15 + \frac{63}{64}) \times R$$

R = RO//RL
RO: Output impedance (= 50Ω)
RL: External termination resistance

$$\text{Here, } V_{SET} = \frac{R2}{R1 + R2} V_{REF}$$

($V_{REF} \approx 1.2V$)
($R1 + R2 \geq 1.2k\Omega$)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Use

- The CXA3197R has PECL and TTL input pins for the clock and reset inputs. When the clock is input at PECL level, it is recommended to also input the reset signal at PECL level. Likewise, when the clock is input at TTL level, it is recommended to also input the reset signal at TTL level.

- The input signal impedance should be properly matched to ensure the stable CXA3197R operation at high speed.
  Particularly when ringing appears in the input clock in the MUX.1A and MUX.1B modes, if this ringing exceeds the clock input threshold value, the internal 1/2 frequency divider circuit may misoperate.

- All TTL input pins of the CXA3197R except for the PS pin go to High level when left open, and only the PS pin goes to Low level when left open. Set the PS pin to High level to operate the IC.
  When the PECL input pins are left open, the P (positive) side goes to High level and the N (negative) side goes to Low level. The PECL input pins are complementary, so be sure to use the P and N sides together.

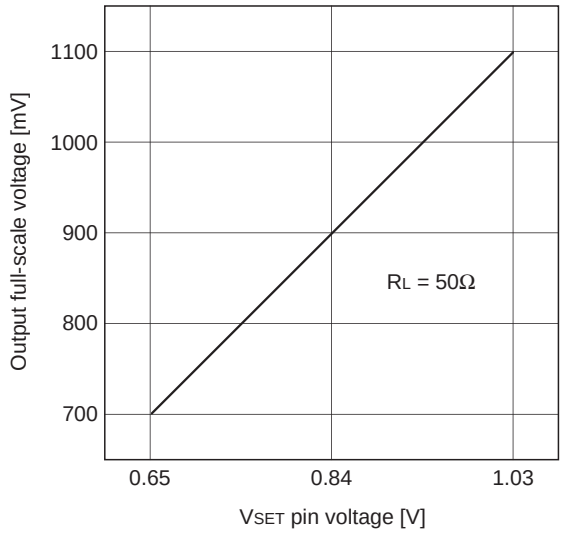
- When the clock and reset input signal level is TTL, ∗∗∗/T pins should be used and ∗∗∗/E pins left open. When the clock and reset input signal level is PECL, ∗∗∗/E pins should be used and ∗∗∗/T pins left open.

- The power supply and grounding have a profound influence on converter characteristics. The power supply and grounding method are particularly important during high-speed operation.
  General points for caution are as follows.
  — The ground pattern should be as wide as possible. It is recommended to make the power supply and ground wider at an inner layer using a multi-layer board.
  To prevent a DC offset from being generated between the analog and digital power supply patterns, it is recommended to connect the patterns at one point via a ferrite-bead filter, etc.
  — When using the CXA3197R with a single power supply, connect DGND1 and DGND2 to a common digital ground, and AGND2 to an analog ground. Also, $DV_{CC}1$ and $DV_{CC}2$ should use a common digital power supply, and $AV_{CC}2$ should be connected to an analog power supply. $AV_{CC}O$ serves as the analog output reference, so while it does not need to share the analog power supply, it should be used within the range that satisfies the analog output compliance voltage.
  — When using the CXA3197R with dual power supply, connect DGND1 and $DV_{CC}2$ to the digital ground, and $AV_{CC}2$ to the analog ground. $DV_{CC}1$ uses a positive digital power supply (+5V, typ.), DGND2 uses a negative digital power supply (–5V, typ.), and AGND2 uses a negative analog power supply (–5V, typ.). Like when using a single power supply, the $AV_{CC}O$ pin can be used within the range that satisfies the analog output compliance voltage. However, connecting it to the analog ground and using the analog ground as the reference for the analog output is recommended.
  — Ground the power supply pins as close to each pin as possible with a 0.1µF or more ceramic chip capacitor.
  When using a single power supply, connect $DV_{CC}1$ and $DV_{CC}2$ to the digital ground, and $AV_{CC}2$ and $AV_{CC}O$ to the analog ground.
  When using dual power supply, connect $DV_{CC}1$ and DGND2 to the digital ground, and AGND2 to the analog ground. In this case, when using $AV_{CC}O$ within the range that satisfies the compliance voltage, be sure to also connect the $AV_{CC}O$ pin to the analog ground using a ceramic chip capacitor.

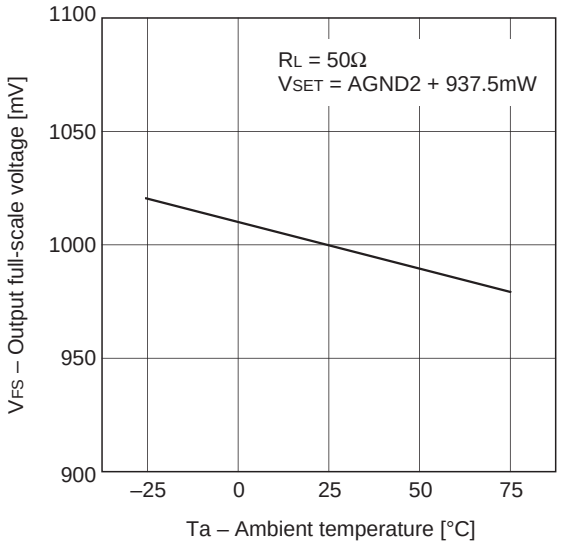
- The CXA3197R is designed with an analog output impedance of 50Ω. The analog outputs are wired with a characteristic impedance of 50Ω, and waveforms free of reflection can be obtained by terminating the analog outputs with 50Ω. Even when using only one of either AOUTP or AOUTN, if one analog output is terminated with 50Ω, be sure to also terminate the other analog output with 50Ω. (See the Application Circuit.)

Example of Representative Characteristics

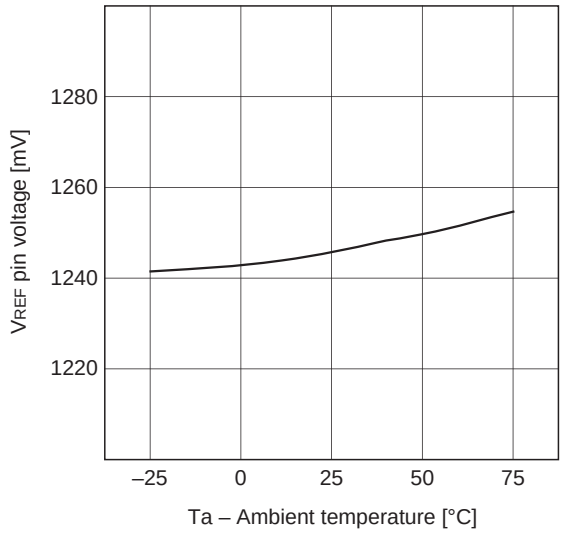
Output full-scale voltage vs. VSET pin voltage



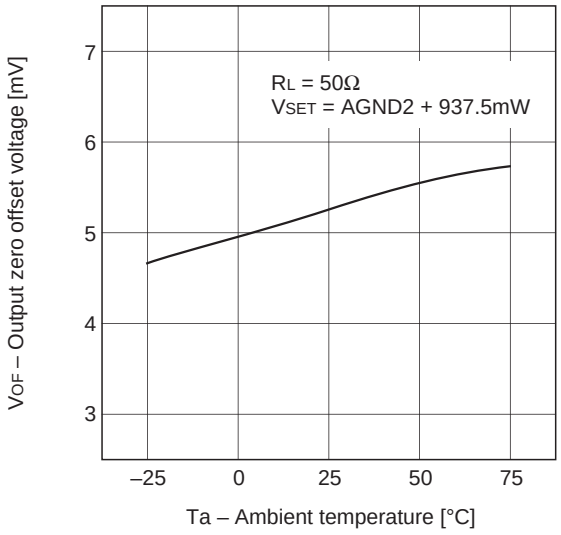
Output full-scale voltage vs. Ambient temperature



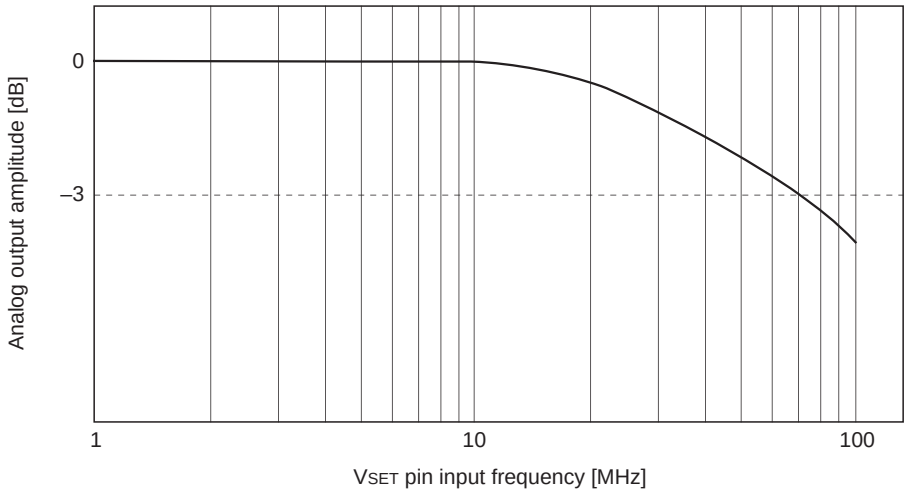
VREF pin voltage vs. Ambient temperature



Output zero offset voltage vs. Ambient temperature

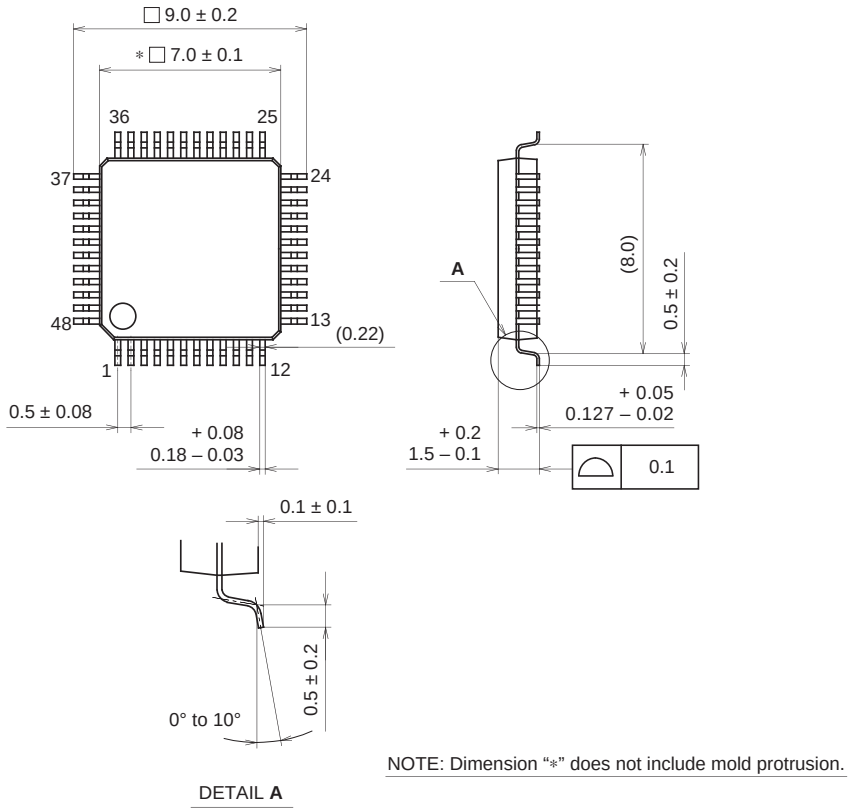


Multiplying bandwidth



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).