SONY

CXA3256R

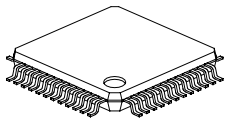
8-bit 120MSPS Flash A/D Converter

Description

The CXA3256R is an 8-bit high-speed flash A/D converter capable of digitizing analog signals at the maximum rate of 120MSPS. ECL, PECL or TTL can be selected as the digital input level in accordance with the application. The TTL digital output level allows 1: 2 demultiplexed output.

The CXA3256R is easier to be used by adding the new functions to the CXA3246Q and adopting a ultra-small package.

48 pin LQFP (Plastic)



LEAD TREATMENT: PALLADIUM PLATING

Features

- Differential linearity error: ±0.5LSB or less
- Integral linearity error: ±0.5LSB or less
- High-speed operation with a maximum conversion rate of 120MSPS
- Low input capacitance: 10pF
- Wide analog input bandwidth: 250MHz
- Low power consumption: 500mW
- Power saving function
- 1: 2 demultiplexed output
- 1/2 frequency-divided clock output (with reset function)
- Compatible with ECL, PECL and TTL digital input levels
- TTL output "H" levels: 2.8V (Typ.)
- Output voltage control function (VOCLP)
- +3.3V line CMOS IC direct connecting available
- Single +5V power supply operation available
- Ultra-small surface mounting package (48-pin LQFP)

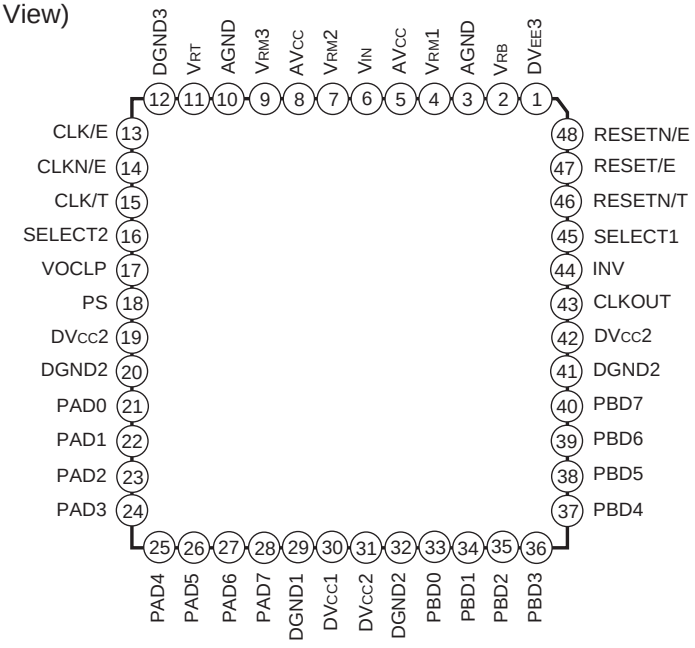
Structure

Bipolar silicon monolithic IC

Applications

- Magnetic recording (PRML)
- Communications (QPSK, QAM)
- LCDs
- Digital oscilloscopes

Pin Configuration (Top View)



E98305A8X-PS

Absolute Maximum Ratings (Ta = 25°C)

			Unit
• Supply voltage	AV_{CC}, $DV_{CC}1$, $DV_{CC}2$	–0.5 to +7.0	V
	DGND3	–0.5 to +7.0	V
	$DV_{EE}3$	–7.0 to +0.5	V
	DGND3 – $DV_{EE}3$	–0.5 to +7.0	V
• Analog input voltage	V_{IN}	V_{RT} – 2.7 to AV_{CC}	V
• Reference input voltage	V_{RT}	2.7 to AV_{CC}	V
	V_{RB}	V_{IN} – 2.7 to AV_{CC}	V
	$\|V_{RT} - V_{RB}\|$	2.5	V
• Digital input voltage	ECL/PECL input pin	$DV_{EE}3$ – 0.5 to DGND3 + 0.5	V
	TTL input pin	DGND1 – 0.5 to $DV_{CC}1$ + 0.5	V
	SELECT2 pin	DGND1 – 0.5 to $DV_{CC}1$ + 0.5	V
	VOCLP pin	DGND1 – 0.5 to $DV_{CC}1$ + 0.5	V
	VID*1 ($\|^{***}$/E – ***N/E$\|$)	2.7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.4	W

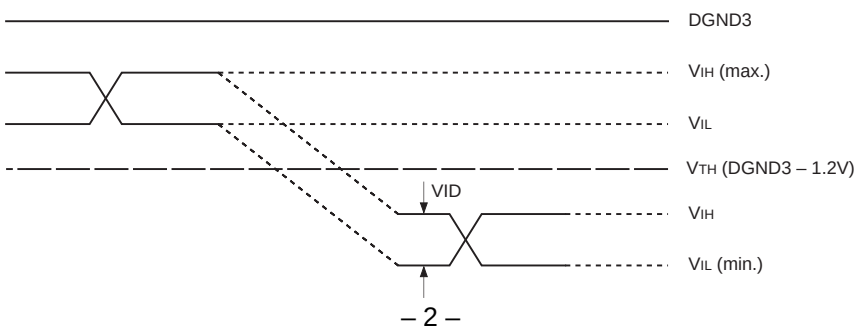
(when mounted on a two-layer glass fabric base epoxy board with dimentions of 50mm × 50mm, 1.6mm thick)

Recommended Operating Conditions

			With a single power supply			With dual power supply			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
• Supply voltage	$DV_{CC}1$, $DV_{CC}2$, AV_{CC}		+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
	DGND1, DGND2, AGND		–0.05	0	+0.05	–0.05	0	+0.05	V
	DGND3		+4.75	+5.0	+5.25	–0.05	0	+0.05	V
	$DV_{EE}3$		–0.05	0	+0.05	–5.5	–5.0	–4.75	V
• Analog input voltage	V_{IN}		V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
• Reference input voltage	V_{RT}		+2.9		+4.1	+2.9		+4.1	V
	V_{RB}		+1.4		+2.6	+1.4		+2.6	V
	$\|V_{RT} - V_{RB}\|$		1.5		2.1	1.5		2.1	V
• Digital input voltage	ECL/PECL input pin	: V_{IH}	$DV_{EE}3$ + 1.5		DGND3	$DV_{EE}3$ + 1.5		DGND3	V
		: V_{IL}	$DV_{EE}3$ + 1.1		V_{IH} – 0.4	$DV_{EE}3$ + 1.1		V_{IH} – 0.4	V
	TTL input pin	: V_{IH}	2.0			2.0			V
		: V_{IL}			0.8			0.8	V
	SELECT2 pin	: V_{IH}		$DV_{CC}1$			$DV_{CC}1$		V
		: V_{IL}		DGND1			DGND1		V
	VOCLP pin		DGND1 + 2.4		$DV_{CC}1$	DGND1 + 2.4		$DV_{CC}1$	V
	VID*1 ($\|^{***}$/E – ***N/E$\|$)		0.4	0.8		0.4	0.8		V
• Maximum conversion rate	Fc (Straight mode)		100			100			MSPS
	(DMUX mode)		120			120			MSPS
• Ambient temperature	Ta		–20		+75	–20		+75	°C

*1 VID: Input Voltage Differential

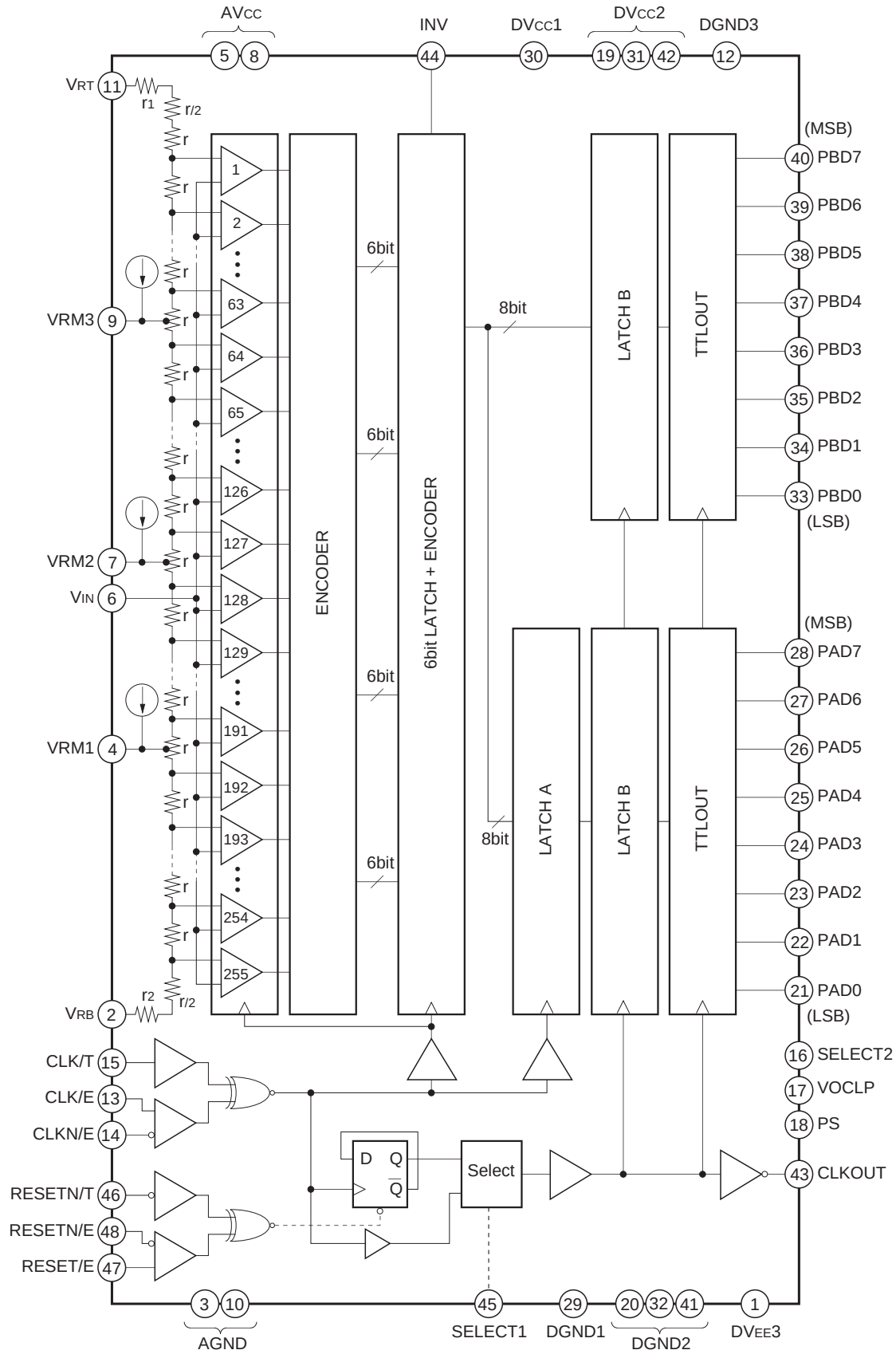
ECL and PECL switching level



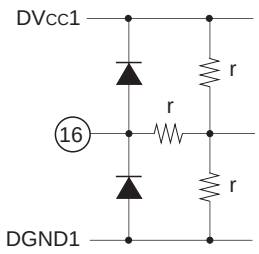
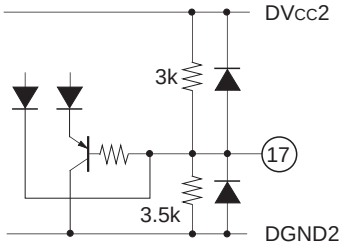
Pin Description

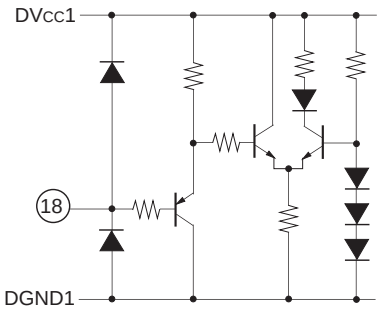
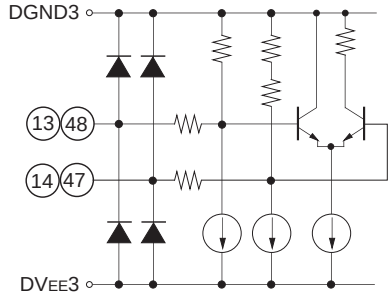
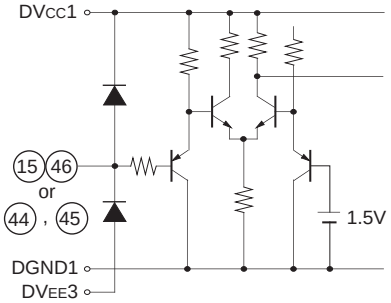
[Symbol]	[Pin No.]	[Description]	[Typical voltage level with a single power supply]	[Typical voltage level with dual power supply]
$DV_{EE}3$	1	Digital power supply	0V	–5.0V
V_{RB}	2	Bottom reference voltage	1.4 to 2.6V	1.4 to 2.6V
AGND	3	Analog ground	0V	0V
$V_{RM}1$	4	Reference voltage mid point	—	—
AV_{CC}	5	Analog power supply	+5V	+5V
V_{IN}	6	Analog signal input	V_{RB} to V_{RT}	V_{RB} to V_{RT}
$V_{RM}2$	7	Reference voltage mid point	—	—
AV_{CC}	8	Analog power supply	+5V	+5V
$V_{RM}3$	9	Reference voltage mid point	—	—
AGND	10	Analog ground	0V	0V
V_{RT}	11	Reference voltage (typ.)	2.9 to 4.1V	2.9 to 4.1V
DGND3	12	Digital power supply	+5V	0V
CLK/E	13	ECL/PECL clock input	PECL	ECL
CLKN/E	14	ECL/PECL clock input	PECL	ECL
CLK/T	15	TTL clock input	TTL	TTL
SELECT2	16	Data output switching	DGND1 or Open or DVcc1	DGND1 or Open or DVcc1
VOCLP	17	TTL high level clamp	Clamp voltage	Clamp voltage
PS	18	Power saving	TTL	TTL
$DV_{CC}2$	19	Digital power supply	+5V	+5V
DGND2	20	Digital ground	0V	0V
PAD0 to PAD7	21 to 28	PA side data output	TTL	TTL
DGND1	29	Digital ground	0V	0V
$DV_{CC}1$	30	Digital power supply	+5V	+5V
$DV_{CC}2$	31	Digital power supply	+5V	+5V
DGND2	32	Digital ground	0V	0V
PBD0 to PBD7	33 to 40	PB side data output	TTL	TTL
DGND2	41	Digital ground	0V	0V
$DV_{CC}2$	42	Digital power supply	+5V	+5V
CLKOUT	43	Clock output	TTL	TTL
INV	44	Data output polarity inversion	TTL	TTL
SELECT1	45	Output mode selection	TTL	TTL
RESETN/T	46	TTL reset input	TTL	TTL
RESET/E	47	ECL/PECL reset input	PECL	ECL
RESETN/E	48	ECL/PECL reset input	PECL	ECL

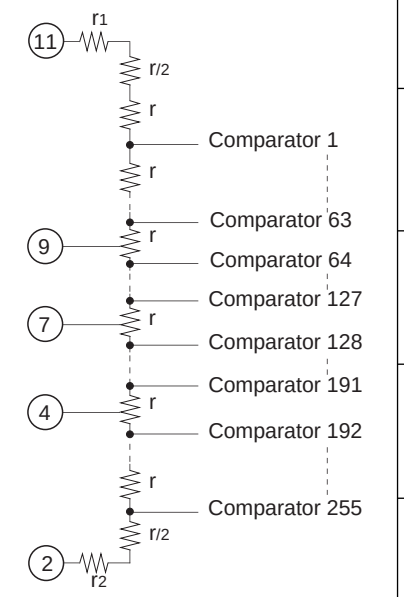
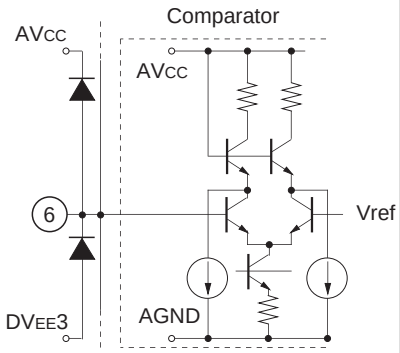
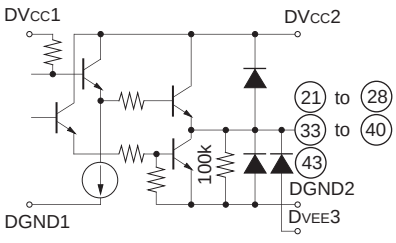
Block Diagram



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
3, 10	AGND		GND		Analog ground. Separated from the digital ground.
5, 8	AVCC		+5V (typ.)		Analog power supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital ground.
19, 30 31, 42	DVCC1 DVCC2		+5V (typ.)		Digital power supply.
12	DGND3		+5V (typ.) (With a single power supply) GND (With dual power supply)		Digital power supply. Ground for ECL input. +5V for PECL and TTL inputs.
1	DVEE3		GND (With a single power supply) –5V (typ.) (With dual power supply)		Digital power supply. –5V for ECL input. Ground for PECL and TTL inputs.
16	SELECT2	I	DVCC1 or Open or DGND1		Data output switching. Data is output from both the PA side and PB side by setting this pin open. When set to DVcc1 level, only the PA side output port outputs the data, makes the PB side high impedance. When set to DGND1 level, only the PB side output port outputs the data, makes the PA side high impedance.
17	VOCLP	I	Clamp voltage		TTL output high level clamp. The TTL high level voltage is clamped to the approximately same value as the voltage applied to this pin. Even if this pin is left open, the TTL high level is clamped to approximately 2.8V.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
18	PS	I	TTL		Power saving. When left open, this pin goes to high level. When set to low level, the power saving state is established.
13	CLK/E	I	ECL/ PECL		Clock input.
14	CLKN/E	I			CLK/E complementary input. When left open, this pin goes to the threshold voltage. Only CLK/E can be used for operation, but complementary inputs are recommended to attain fast and stable operation.
48	RESETN/E	I			Reset signal input. When set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E complementary input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.
15	CLK/T	I	TTL		Clock input.
46	RESETN/T	I			Reset signal input. When left open, this pin goes to high level. When set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data output polarity inversion input. When left open, this input goes to high level. (See Table 1. I/O Correspondence Table.)
45	SELECT1		Vcc or GND		Data output mode selection. (See Table 2. Operation Mode Table.)

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
11	V_{RT}	I	4.0V (typ.)		Top reference voltage. By-pass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
9	$V_{RM}3$		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1µF chip capacitor.
7	$V_{RM}2$		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1µF chip capacitor.
4	$V_{RM}1$		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1µF chip capacitor.
2	V_{RB}	I	2.0V (typ.)		Bottom reference voltage. By-pass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
6	V_{IN}	I	V_{RT} to V_{RB}		Analog input.
21 to 28	PAD0 to PAD7	O	TTL		Port A side data output. TTL output; the high level is clamped to approximately 2.8V.
33 to 40	PBD0 to PBD7	O			Port B side data output. TTL output; the high level is clamped to approximately 2.8V.
43	CLKOUT	O			Clock output. (See Table 2. Operation Mode Table.) TTL output; the high level is clamped to approximately 2.8V.

Electrical Characteristics

(AV_{CC}, $DV_{CC}1, 2$, DGND3 = +5V, AGND, DGND1, 2, $DV_{EE}3$ = 0V, V_{RT} = 4V, V_{RB} = 2V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC characteristics						
Integral linearity error	E_{IL}	V_{IN} = 2Vp-p, Fc = 5MSPS			±0.5	LSB
Differential linearity error	E_{DL}				±0.5	LSB
Analog input						
Analog input capacitance	C_{IN}	V_{IN} = +3.0V + 0.07Vrms		10		pF
Analog input resistance	R_{IN}		7	20	40	kΩ
Analog input current	I_{IN}		0	100	285	µA
Reference input						
Reference resistance	Rref*2		400	600	740	Ω
Reference current	Iref*3		2.7	3.3	5.0	mA
Offset voltage V_{RT} side	EOT		6	8	10	mV
V_{RB} side	EOB		0	1.5	3	mV
Digital input (ECL, PECL)						
Digital input voltage: High	V_{IH}		$DV_{EE}3$ + 1.5		DGND3	V
: Low	V_{IL}		$DV_{EE}3$ + 1.1		V_{IH} – 0.4	V
Threshold voltage	V_{TH}			DGND3 – 1.2		V
Digital input current: High	I_{IH}	V_{IH} = DGND3 – 0.8V	–50		20	µA
: Low	I_{IL}	V_{IL} = DGND3 – 1.6V	–50		20	µA
Digital input capacitance					5	pF
Digital input (TTL)						
Digital input voltage: High	V_{IH}		2.0			V
: Low	V_{IL}				0.8	V
Threshold voltage	V_{TH}			1.5		V
Digital input current: High	I_{IH}	V_{IH} = 3.5V	–10		5	µA
: Low	I_{IL}	V_{IL} = 0.2V	–20		0	µA
Digital input capacitance					5	pF
Digital output (TTL)						
Digital output voltage : High	V_{OH}	I_{OH} = –2mA	2.4			V
: Low	V_{OL}	I_{OL} = 1mA			0.5	V
Switching characteristics						
Maximum conversion rate	Fc	DMUX mode	120			MSPS
Aperture jitter	Taj			10		ps
Sampling delay	Tds		1.2	1.4	1.6	ns
Clock high pulse width	Tpw1	CLK	3.0			ns
Clock low pulse width	Tpw0	CLK	4.5			ns
Reset signal setup time	T_rs	RESETN – CLK	1.0			ns
Reset signal hold time	T_rh	RESETN – CLK	–0.5			ns
Clock output delay	Td_clk	(C_L = 5pF)	3.0	4.5	7.0	ns
Data output delay	Tdo1	DMUX mode (C_L = 5pF)		T*4 + 0.5		ns
	Tdo2	(C_L = 5pF)	3.5	5.0	7.5	ns
Output rise time	Tr	0.8 to 2.0V (C_L = 5pF)		1		ns
Output fall time	Tf	0.8 to 2.0V (C_L = 5pF)		1		ns

* These characteristics are for PECL input unless otherwise specified.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics						
Input bandwidth		V_{IN} = 2Vp-p, –3dB	250			MHz
SNR		Fc = 120MSPS, fin = 1kHz Fs DMUX mode		46		dB
		Fc = 120MSPS, fin = 29.999MHz Fs DMUX mode		42		dB
Error rate		Fc = 120MSPS, fin = 1kHz Fs DMUX mode Error > 16LSB			10^{-12}	TPS*5
		Fc = 120MSPS, fin = 29.999MHz Fs DMUX mode Error > 16LSB			10^{-9}	TPS
		Fc = 100MSPS, fin = 24.999MHz Fs Straight mode Error > 16LSB			10^{-9}	TPS
Power supply						
Supply current	I_{CC} + I_{EE}		70	98	140	mA
AVcc Pin supply current	AI_{CC}		45		87	mA
DVcc1 pin supply current	$DI_{CC}1$		20		36	mA
DVcc2 pin supply current	$DI_{CC}2$		5		15	mA
DGND3 pin supply current	I_{EE}		0.5		1.5	mA
Supply current for PS	I_{CC}+I_{EE}				5	mA
AVcc pin supply current for PS	AI_{CC}				1.5	mA
DVcc1 pin supply current for PS	$DI_{CC}1$				1.5	mA
DVcc2 pin supply current for PS	$DI_{CC}2$				1.5	mA
DGND3 pin supply current for PS	I_{EE}				0.5	mA
Power consumption	Pd*6		400	500	700	mW
Power consumption for PS	Pd*7		0.3		25	mW

*2 Rref: Resistance value between V_{RT} and V_{RB}

*3 $Iref = \frac{V_{RT} - V_{RB}}{Rref}$

*4 $T = \frac{1}{Fc}$

*5 TPS: Times Per Sample

*6 $Pd = (I_{CC} + I_{EE}) \cdot V_{CC} + \frac{(V_{RT} - V_{RB})^2}{Rref}$

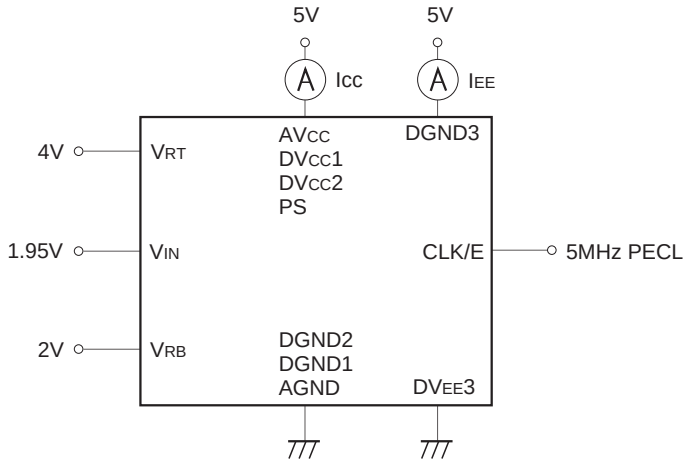
*7 $Pd = (I_{CC} + I_{EE}) \cdot V_{CC}$

V_{IN}	Step	INV															
		1								0							
		D7							D0	D7							D0
V_{RT}	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	⋮				⋮								⋮				
$V_{RM}2$	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	⋮				⋮								⋮				
	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
V_{RB}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

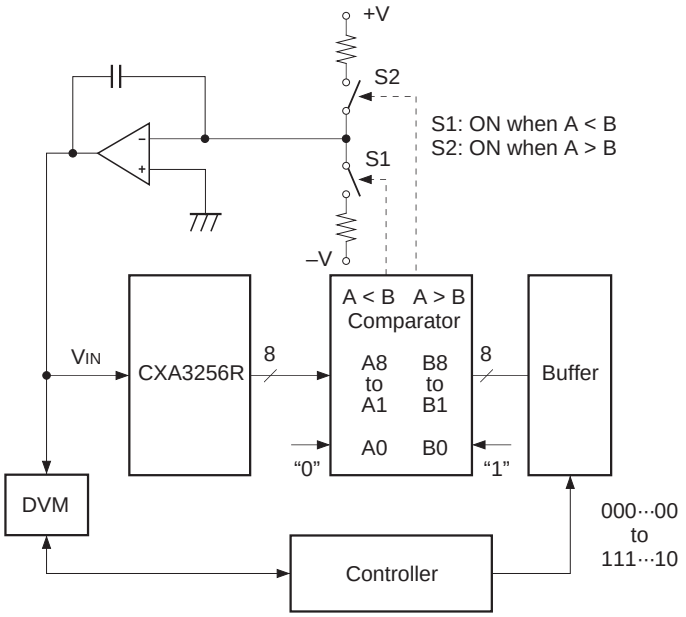
Table 1. I/O Correspondence Table

Electrical Characteristics Measurement Circuit

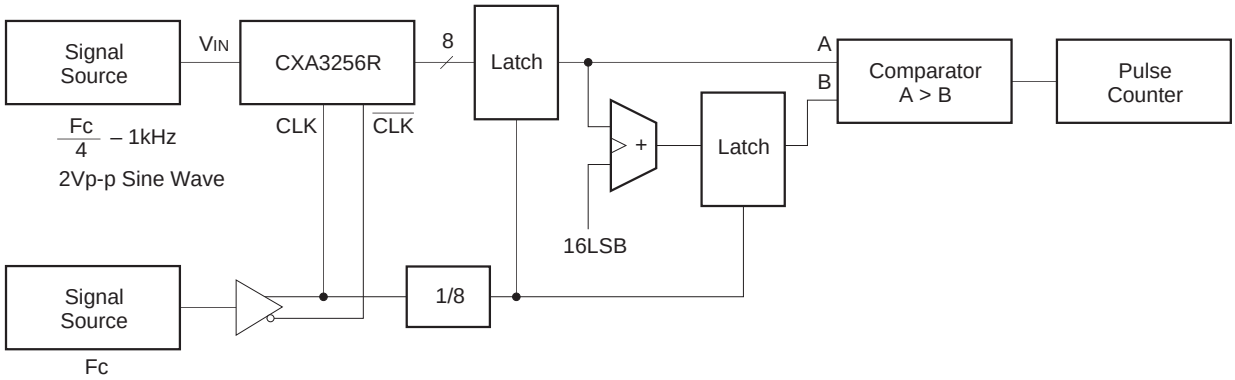
Current Consumption Measurement Circuit



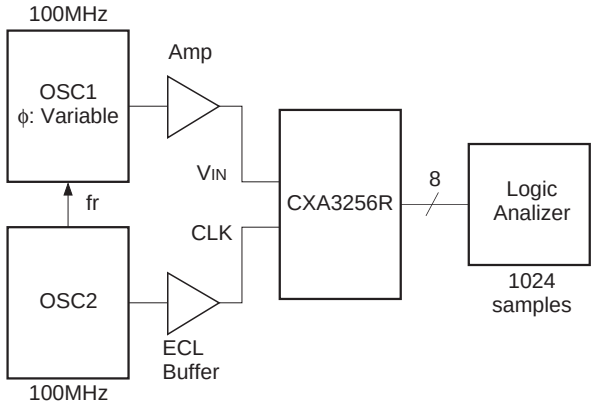
Integral Linearity Error Measurement Circuit
Differential Linearity Error Measurement Circuit



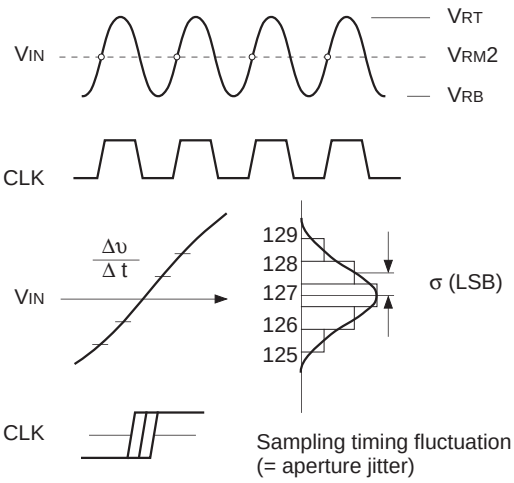
Error Rate Measurement Circuit



Sampling Delay Measurement Circuit
Aperture Jitter Measurement Circuit



Aperture Jitter Measurement Method



Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter Taj is:

$$Taj = \sigma / \frac{\Delta\upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

Description of Operation Modes

The CXA3256R has two types of operation modes which are selected with Pin 45 (SELECT).

Operation mode	SELECT1 pin	Maximum conversion rate	Data output	Clock output
DMUX mode	Vcc	120MSPS	Demultiplexed output 60Mbps	The input clock is 1/2 frequency divided and output. 60MHz
Straight mode	GND	100MSPS	Straight output 100Mbps	The input clock is inverted and output. 100MHz

Table 2. Operation Mode Table

1. DMUX mode (See Application Circuit 1-(1), (2) and (3).)

Set the SELECT1 pin to Vcc for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this 1/2 frequency-divided clock. The 1/2 frequency-divided clock, which has adequate setup time and hold time for the output data, is output from the clock output pin.

When using the multiple CXA3256R in DMUX mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example on the next page. As a countermeasure, the CXA3256R has a function that resets the 1/2 frequency-divided clocks.

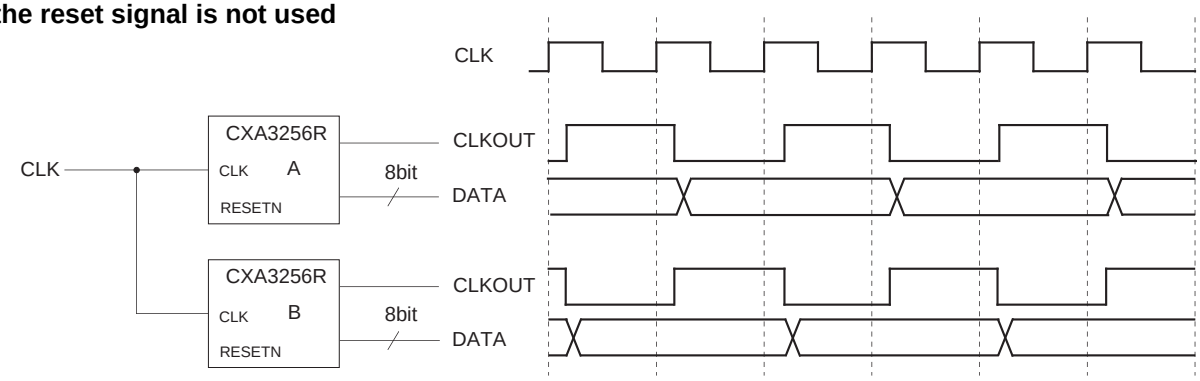
When resetting this 1/2 frequency-divided clock, the low level of the reset signal should be input to the RESETN pin (Pin 46 or 48). The reset signal requires the setup time ($T_{rs} \geq 1.0$ns) and hold time ($T_{rh} \geq -0.5$ns) to the clock rising edge because it is synchronized with and taken in the clock.

The reset period can be extended by making the low level period of the reset signal longer because the clock output pin is fixed to low (reset) during the low level period at the clock rising edge. If the reset start timing is regarded as not important, the timing where the reset signal is set from high to low is not so consequence. However, when the reset is released the timing where the reset signal is set from low to high must become significant because the timing is used to commence the 1/2 frequency-divided clock. In this case, the setup time (T_{rs}) is also necessary.

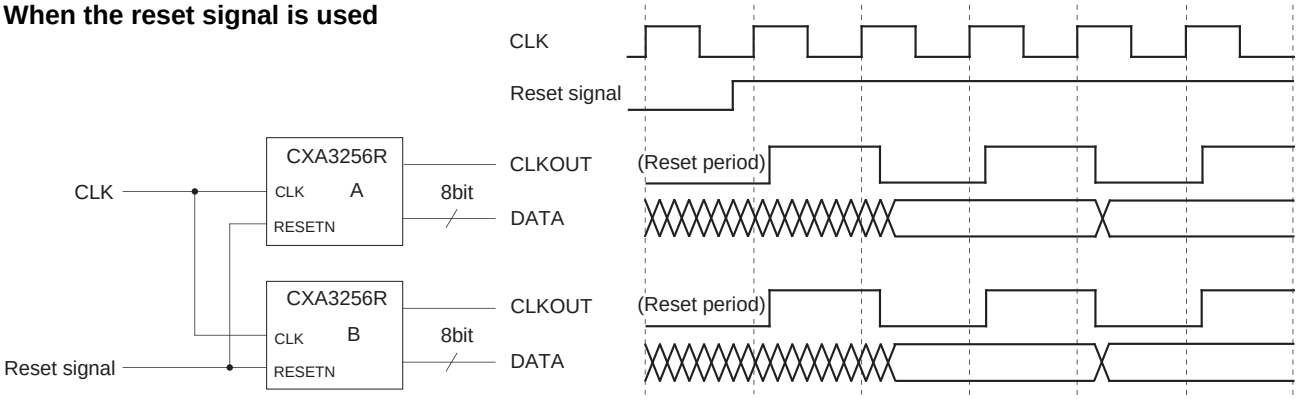
See the timing chart for detail. (This chart shows the example of reset for 2T.)

The A/D converter can operate at Fc (min.) = 120MSPS in this mode.

When the reset signal is not used



When the reset signal is used



2. Straight mode (See Application Circuits 1-(4), (5) and (6).)

Set the SELECT1 pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at Fc (min.) = 100MSPS in this mode.

Digital input level and supply voltage settings

The logic input level for the CXA3256R supports ECL, PECL and TTL levels.

The power supplies ($DV_{EE}3$, DGND3) for the logic input block must be set to match the logic input (CLK and reset signals) level.

Digital input level	$DV_{EE}3$	DGND3	Supply voltage	Application circuits
ECL	–5V	0V	±5V	(1) (4)
PECL	0V	+5V	+5V	(2) (5)
TTL	0V	+5V	+5V	(3) (6)

Table 3. Logic Input Level and Power Supply Settings

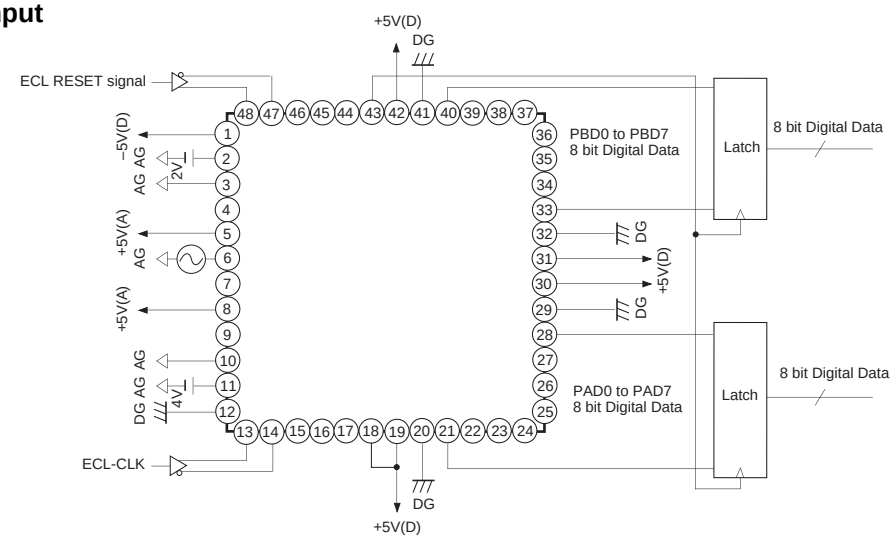
Description of SELECT2 pin

The CXA3256R has the two systems of data output. The SELECT2 pin is used to select the port where the data is output.

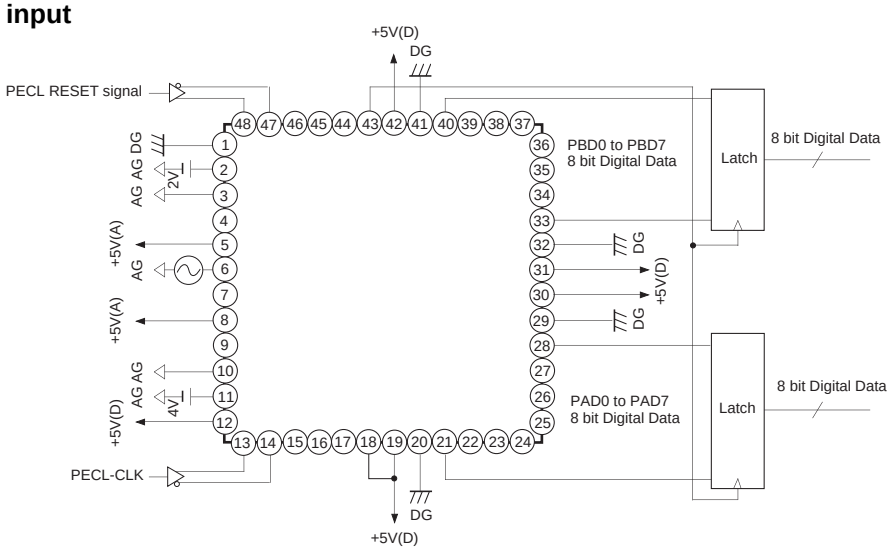
SELECT2 pin	Data output
Open	Output possible to both PA and PB
Vcc1	Output possible to PA, and PB output is high impedance.
GND1	Output possible to PB, and PA output is high impedance.

Application Circuit 1

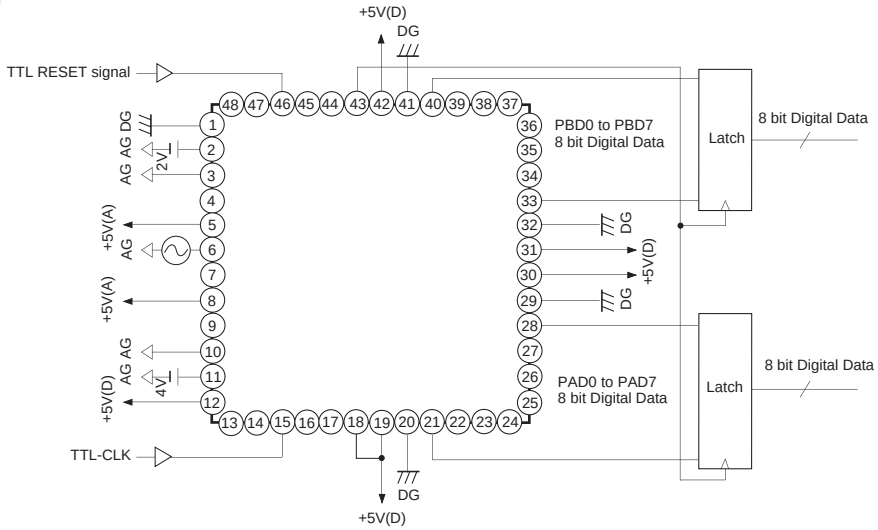
(1) DMUX ECL input



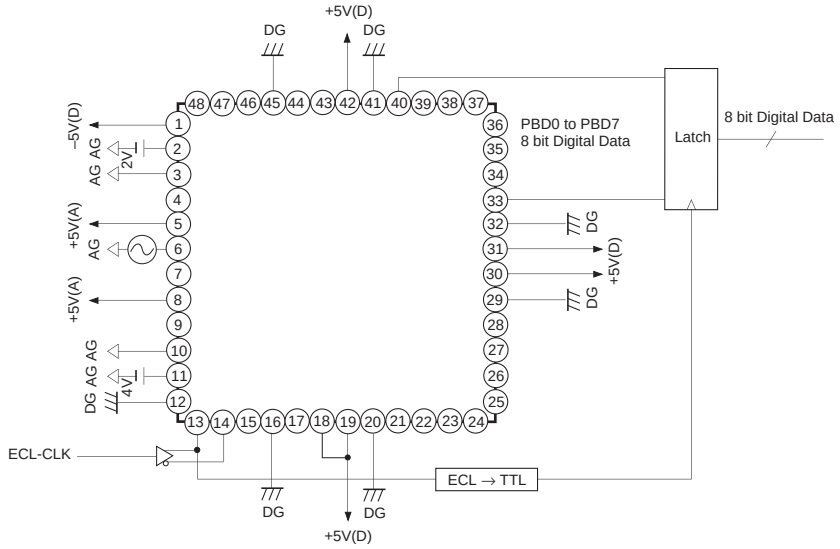
(2) DMUX PECL input



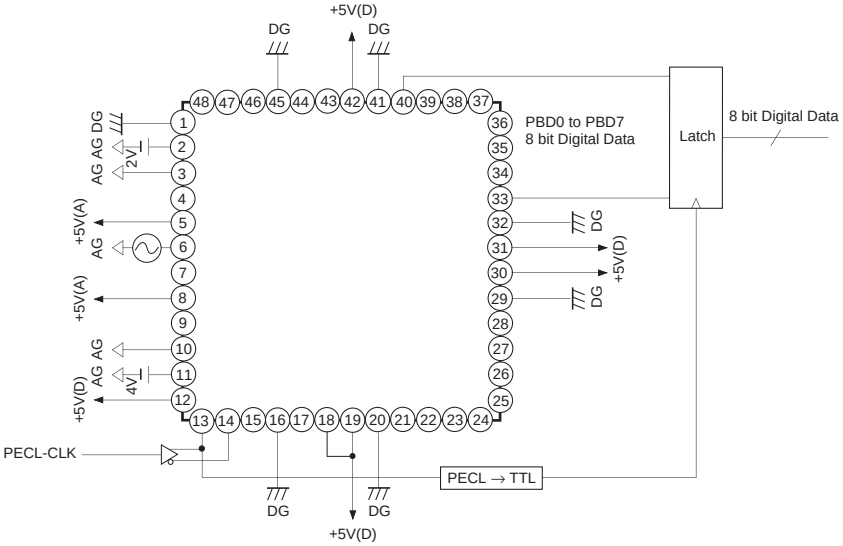
(3) DMUX TTL input



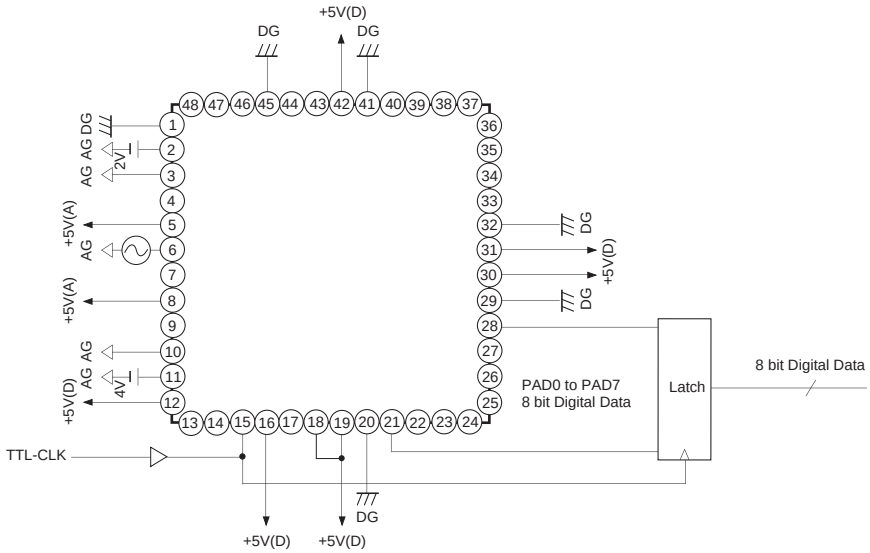
(4) Straight ECL input



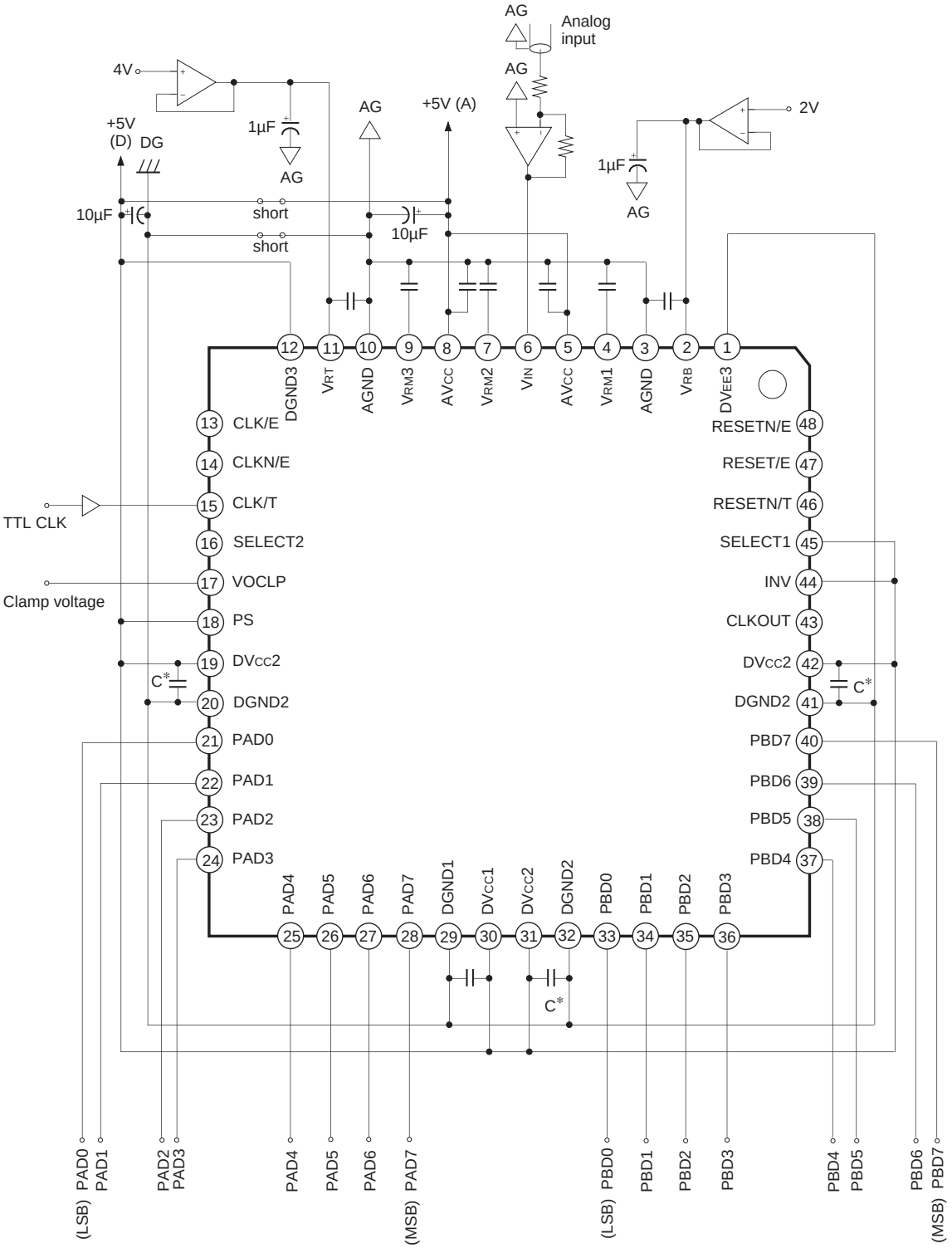
(5) Straight PECL input



(6) Straight TTL input



Application Circuit 2 DMUX Mode TTL I/O (When a single power supply is used)

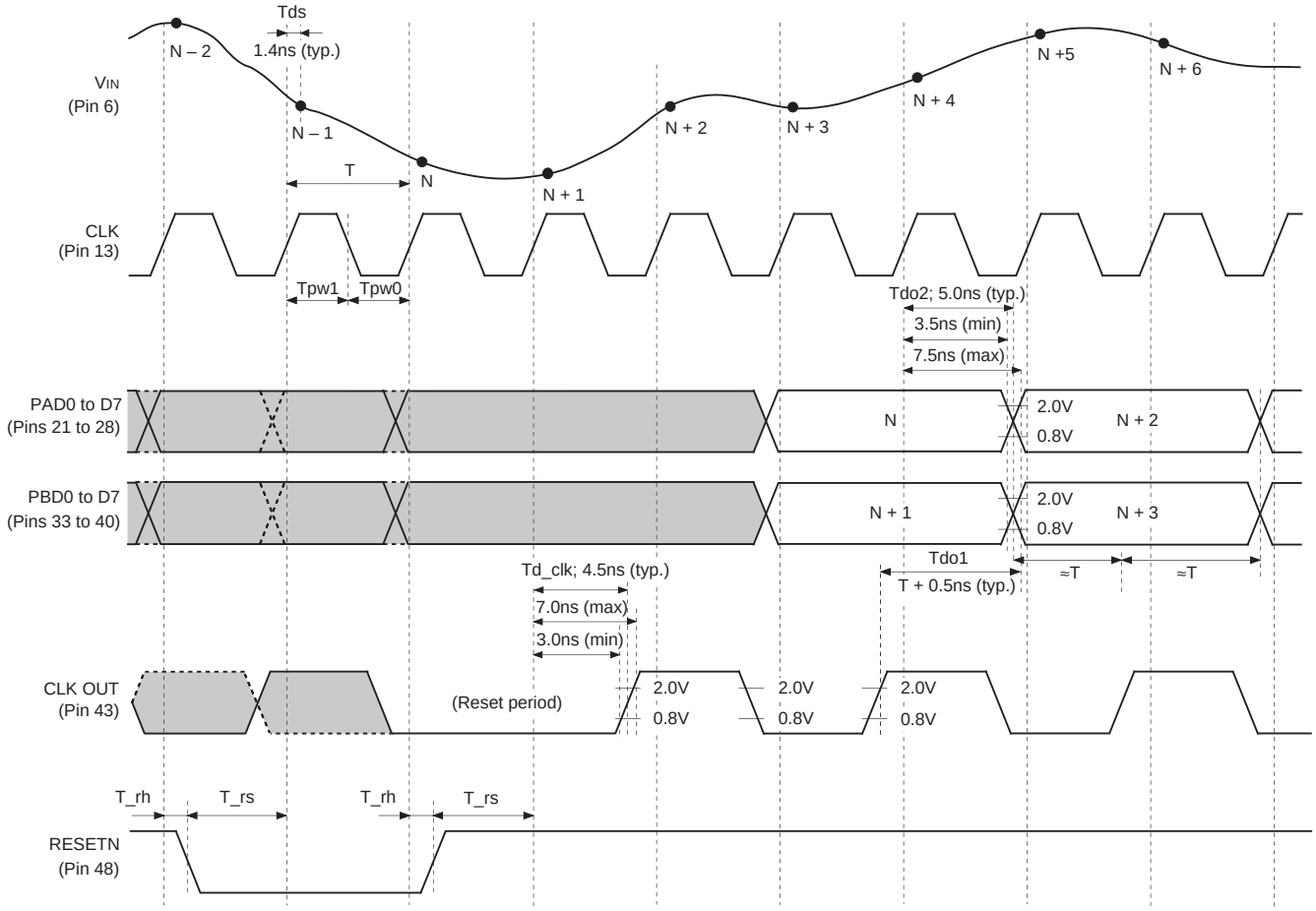


Short the analog system and digital system at one point immediately under the A/D converter. See the Notes on Operation.

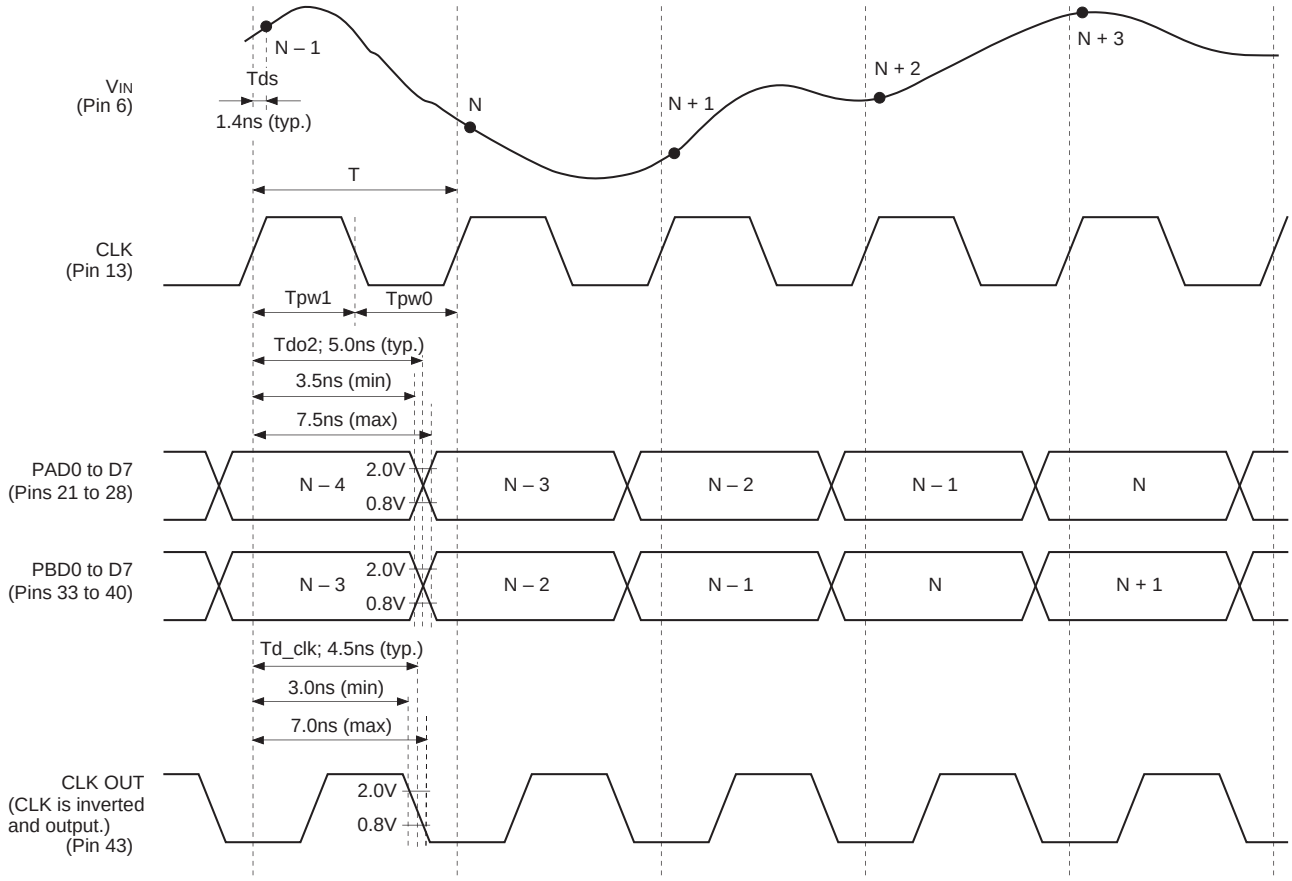
is the chip capacitor of 0.1µF. Also, C* is important to suppress the noise generated during the TTL output circuit is operating. Place C* at the fixed position between the pins with the shortest distance.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

DMUX Mode Timing Chart (Select = V_{CC})



Straight Mode Timing Chart (Select = GND)



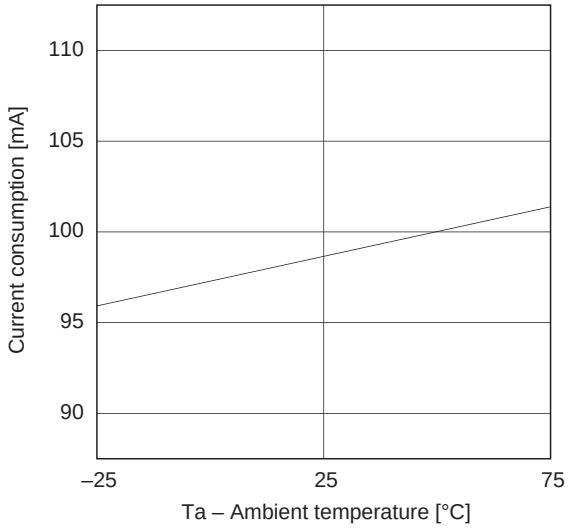
Notes on Operation

- The CXA3256R has the PECL and TTL input pins for the clock and reset input pins. When the clock is input in PECL level, inputting the reset signal in PECL level is recommended. Also, when the clock is input in TTL level, inputting the reset signal in TTL is recommended.
- The impedance of the input signal should be properly matched to ensure the CXA3256R's stable operation at the high speed.
- In the CXA3256R, all the TTL input pins become the high level when left open.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows.
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AVcc and DVcc, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AVcc and DVcc lines at one point each via a ferrite-bead filter, etc. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Be sure to turn the analog and digital power supplies on simultaneously. If not simultaneously, the IC does not operate correctly.
  - Ground the power supply pins (AVcc, DVcc1, DVcc2, $DV_{EE}3$) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor.
    (Connect the AVcc pin to the AGND pattern and the DVcc1, DVcc2 and $DV_{EE}3$ pins to the DGND pattern.)
  - It is recommended to place the ceramic chip capacitor of 0.1µF or more, in particular, between DVcc2 and DGND2 with the shortest distance. This has the effect to suppress the noise generated when the CXA3256R TTL output circuit operates.
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 10pF. To drive the A/D converter with the proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit, keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate by-pass to protect them from high-frequency noise. By-pass them to AGND with approximately 1µF tantal capacitor and 0.1µF chip capacitor as short as possible.
- If the CLKN/E pin is not used, by-pass this pin to DGND with an approximately 0.1µF capacitor. At this time, approximately DGND3 – 1.2V voltage is generated. However, this is not recommended for use as the threshold voltage V_{BB} because it is too weak.

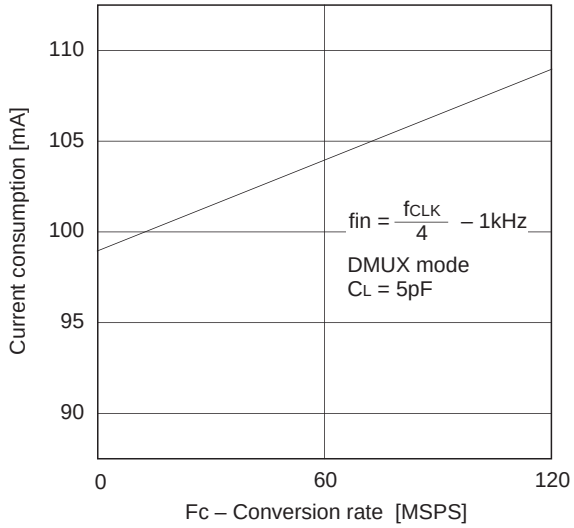
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and ***/E pins left open.
- The CXA3256R TTL output high level is clamped to approximately 2.8 V in the IC.This makes it possible to directly interface with the 3.3V system CMOS IC. However,the CXA3256R has the VOCLP pin which is used to clamp the TTL output high level. See the Example of Representative Characteristics for the relationship between the VOCLP pin and the TTL high level.
- The CXA3026Q has the output pins P1** and P2**. However, in the CXA3256R, these symbols are changed as PA**and PB**. At this time, the P1 side of the CXA3026Q is changed to the PB side for the CXA3256R; the P2 side of the CXA3026Q to the PA side for the CXA3256R.
- The pipeline delay of the CXA3256R is smaller by one clock, compared to that of CXA3026Q.

Example of Representative Characteristics

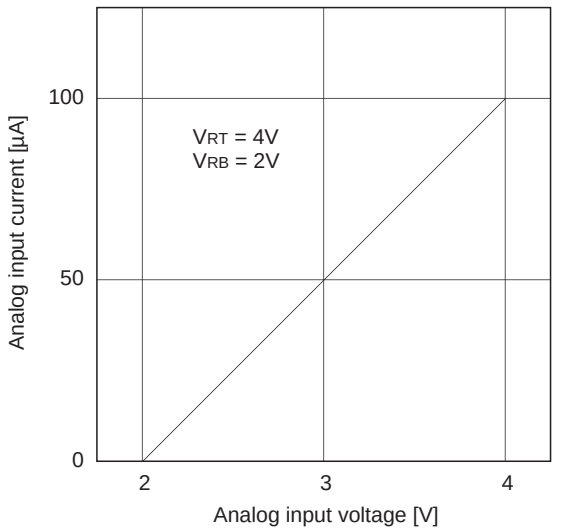
Current consumption vs. Ambient temperature characteristics



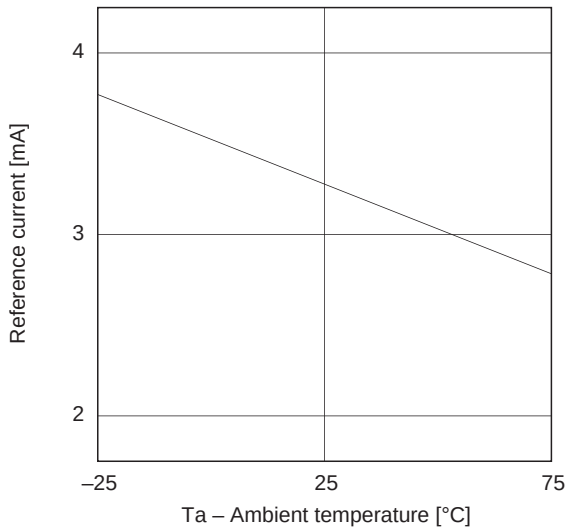
Current consumption vs. Conversion rate characteristics



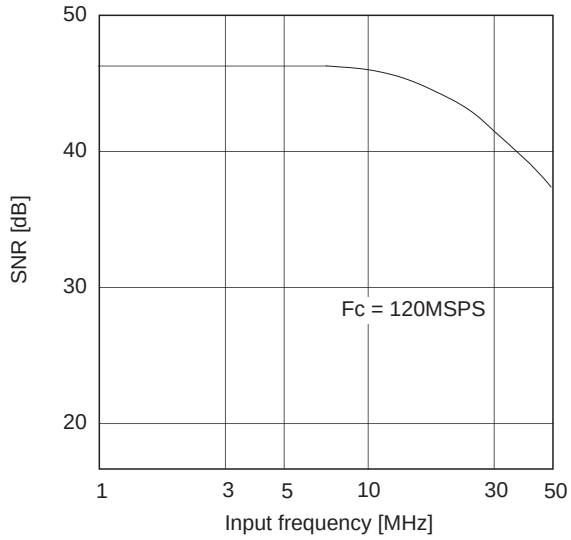
Analog input current vs. Analog input voltage characteristics



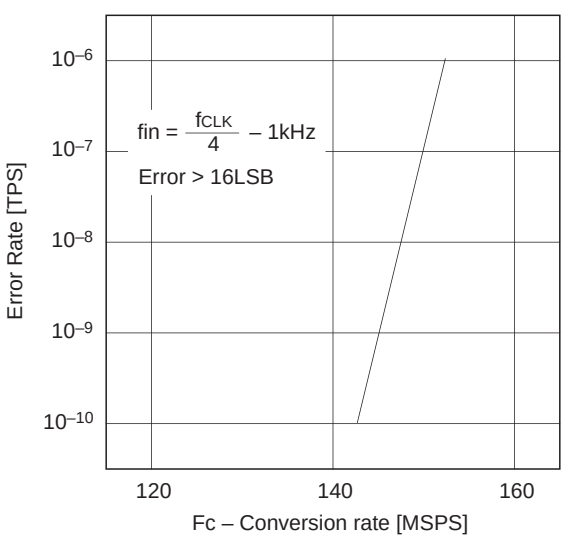
Reference current vs. Ambient temperature characteristics



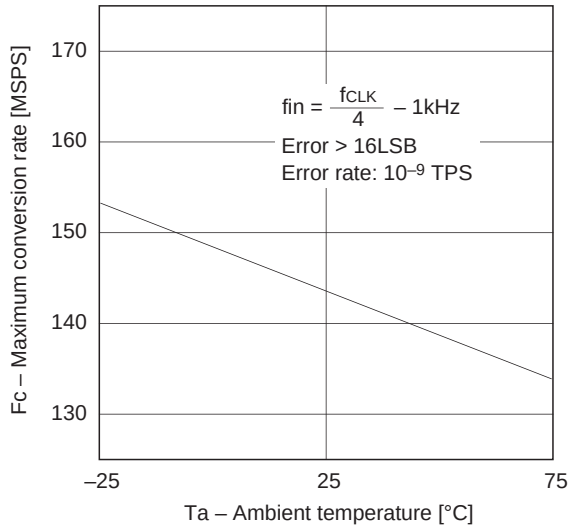
SNR vs. Input frequency response



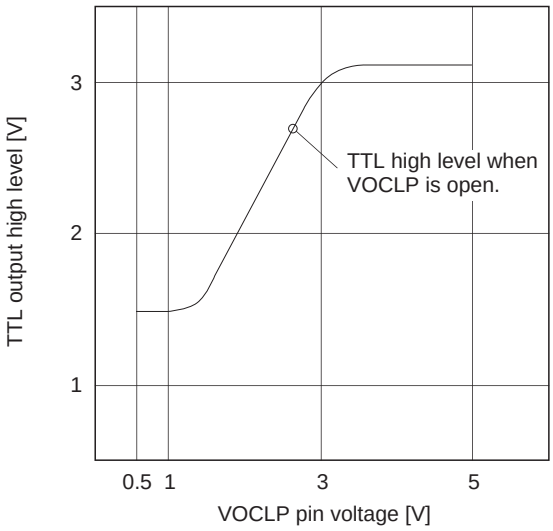
Error rate vs. Conversion rate characteristics



Maximum conversion rate vs. Ambient temperature characteristics

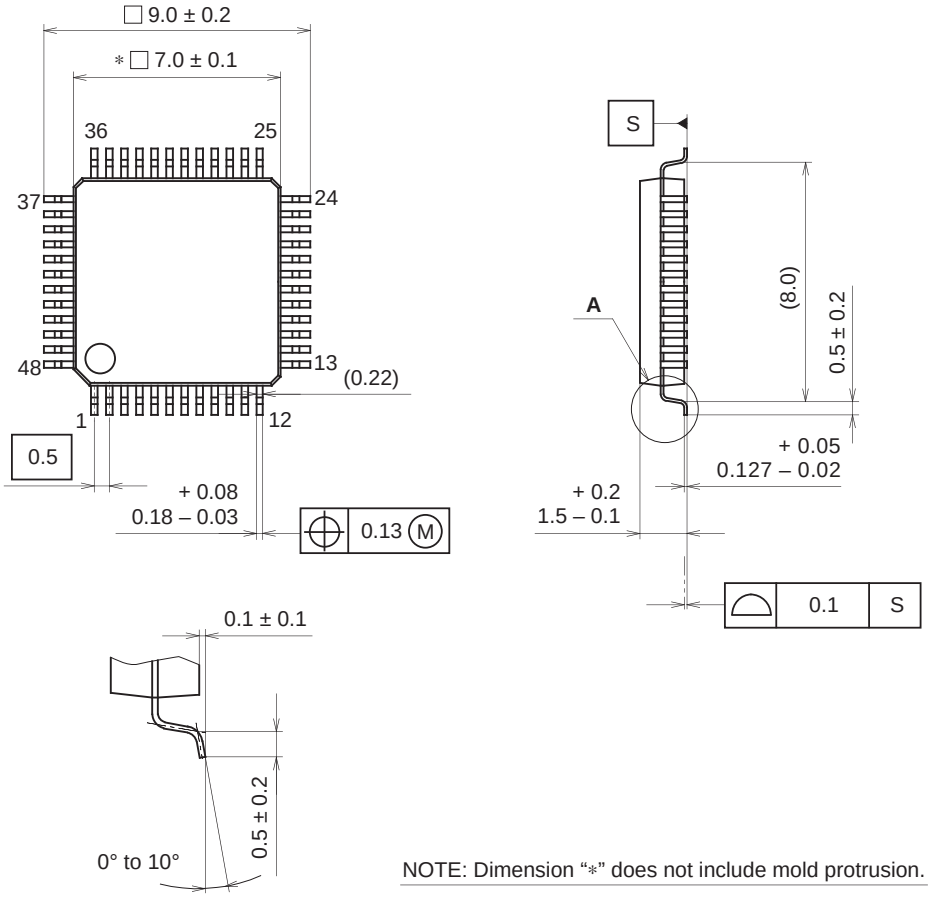


TTL output high level vs. VOCLP pin



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).