SONY

CXD2315Q

10-bit 80MSPS 1ch D/A Converter (Ultra-low Glitch Version)

Description

The CXD2315Q is a 1-ch 10-bit 80MSPS D/A converter for monitor and video. This IC achieves high specifications for the industrial and information equipment due to the reduction of the glitch energy.

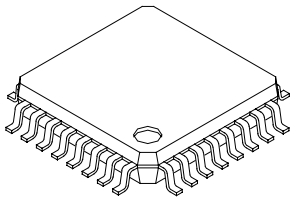
Features

- 10-bit resolution
- Maximum conversion rate 80MSPS
- Differential linearity error ±0.5LSB
- Low power consumption 150 mW (Max., When 80MSPS 200 Ω load, 2 Vp-p is output)
- Pin-compatible with CXD2306Q
- Single 5 V power supply
- Built-in independent constant-voltage source
- Ultra-low glitch
- Stand-by function

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

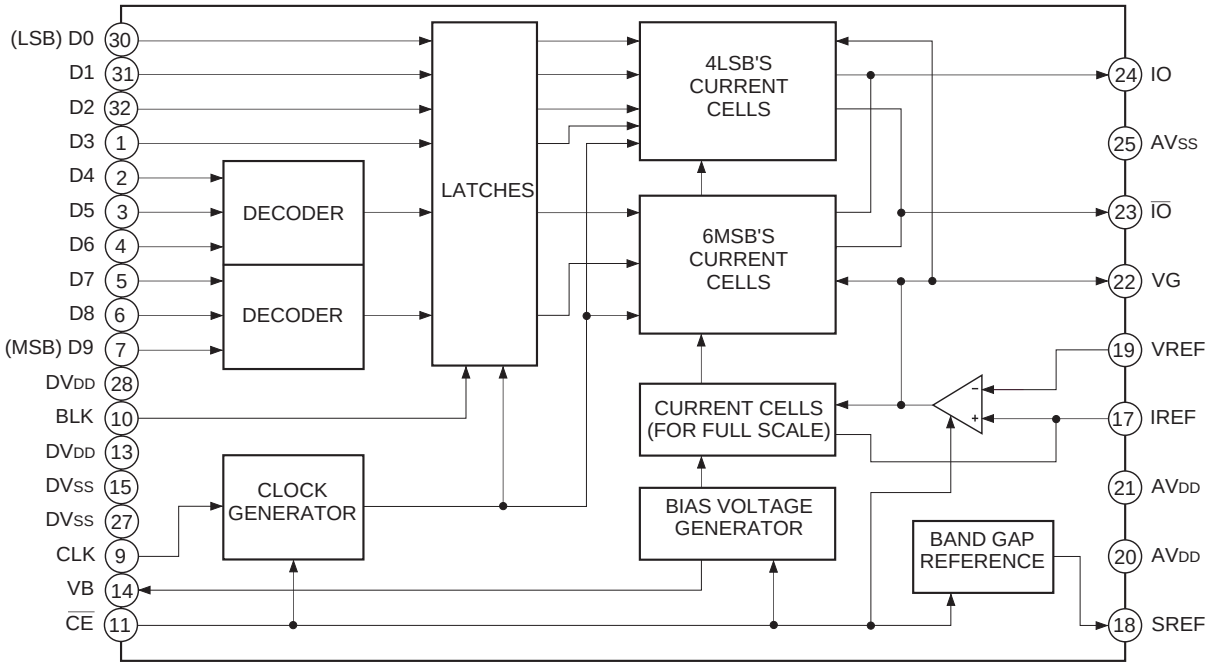
• Supply voltage	AV_{DD}, DV_{DD}	7	V
• Input voltage (All pins)	V_{IN}	V_{DD} +0.5 to V_{SS} –0.5	V
• Output voltage (for each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

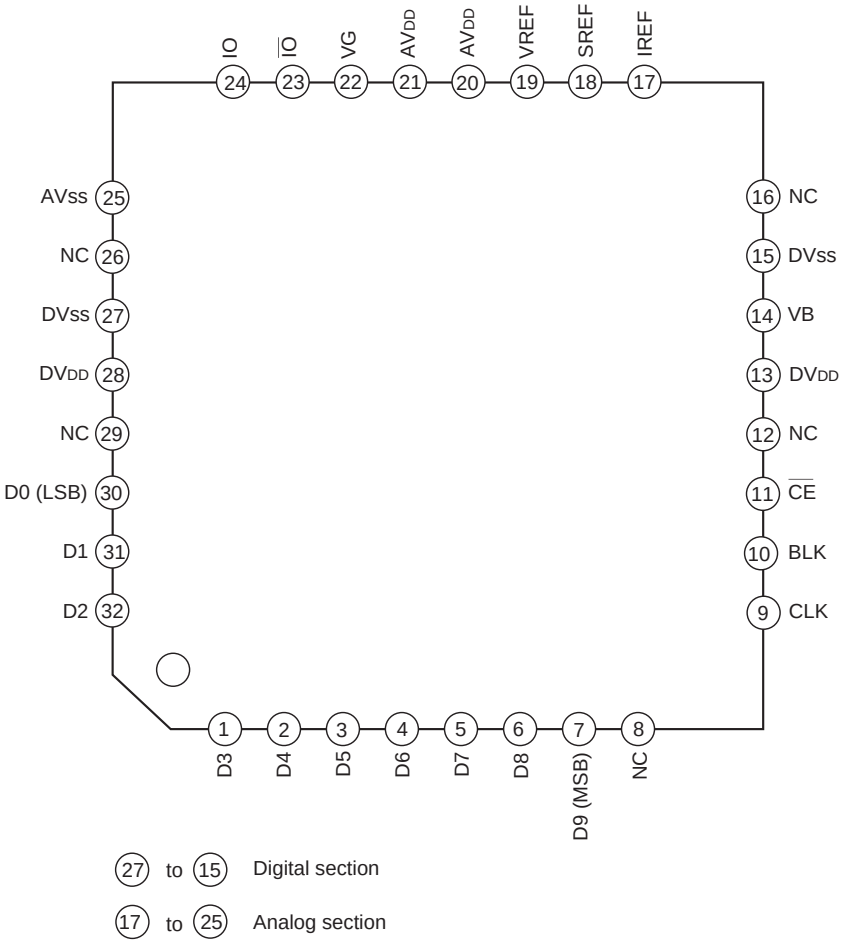
• Supply voltage	AV_{DD}, AV_{SS}	5.0 ± 0.25	V
	DV_{DD}, DV_{SS}	5.0 ± 0.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	tpw_1, tpw_0	5.6 (min.)	ns
• Operating temperature	Topr	–20 to +85	°C

E95704D01

Block Diagram



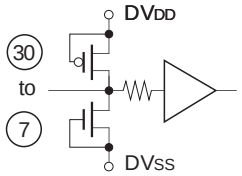
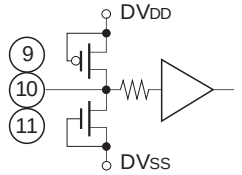
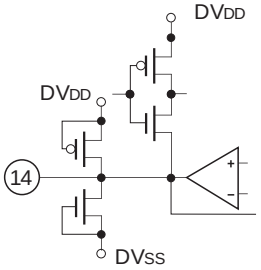
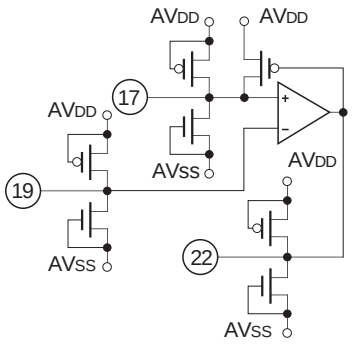
Pin Configuration

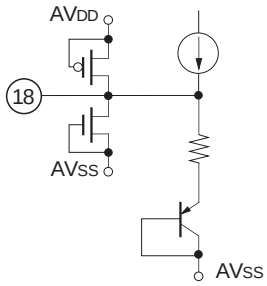
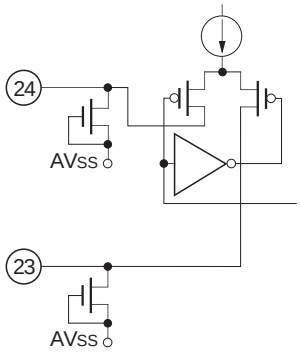


(27) to (15) Digital section

(17) to (25) Analog section

Pin Description and Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
30 to 32 1 to 7	D0 to D9	I		Digital input. 30 pin D0 (LSB) to 7 pin D9 (MSB)
8, 12, 16, 26, 29	NC	—		No connection.
9	CLK	I		Clock input.
10	BLK			Blanking input. This is synchronized with the clock input signal. No signal (0 V output) at high and output state at low.
11	$\overline{CE}$			Chip enable input. This is not synchronized with the clock input signal. No signal (0 V output) at high makes power consumption minimum.
13, 28	DVDD	—		Digital power supply.
14	VB	O		Connect a capacitor of approximately 0.1 µF.
15, 27	DVSS	—		Digital ground.
17	IREF	O		Reference current output. Connect resistance “RIR” which is 16 times output resistance “ROUT”.
19	VREF	I		Reference voltage input. Sets output full scale value.
22	VG	O		Connect a capacitor of approximately 0.1 µF.

Pin No.	Symbol	I/O	Equivalent circuit	Description
18	SREF	O		Independent constant-voltage source output pin using band gap reference. Stable voltage independent of the fluctuation for supply voltage can be get by connecting to VREF. See Application Circuit 2 for details.
20, 21	AVDD	—		Analog VDD
23	$\overline{IO}$	O		Inverted current output. Connect to GND normally.
24	IO			Current output. Output can be retrieved by connecting resistance. The standard is 200 Ω.
25	AVSS	—		Analog ground.

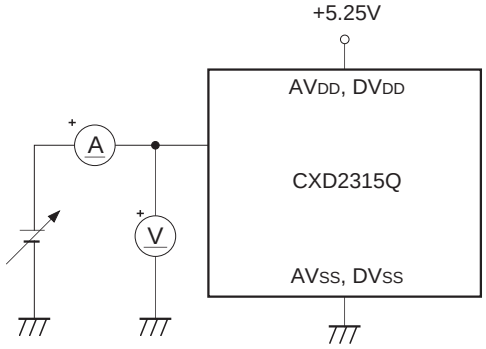
Electrical Characteristics (F_{CLK}=80 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, R_{IR}=3.3 kΩ, V_{REF}=2.0 V, Ta=25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Conversion speed	F_{CLK}	AV_{DD}=DV_{DD}=4.75 to 5.25 V Ta=–20 to +85 °C	0		80	MSPS
Integral non-linearity error	E_L	Endpoint	–1.5		1.5	LSB
Differential non-linearity error	E_D		–0.5		0.5	LSB
Precision guaranteed output voltage range	V_{OC}		1.8	1.94	2.0	V
Output full-scale voltage	V_{FS}		1.8	1.94	2.0	V
Output full-scale current	I_{FS}		9.0	9.7	10	mA
Output offset voltage	V_{OS}	When D0 to D9= “0000000000” input			1	mV
Glitch energy	GE				30	pV•s
Differential gain	DG				1.0	%
Differential phase	DP				1.0	deg
Supply current	I_{DD}	$\overline{CE}$= “L”			30	mA
	I_{STB}	$\overline{CE}$= “H”			1	
Analog input resistance	R_{IN}	VREF	1			MΩ
Input capacitance	C_I				9	pF
Digital input voltage	V_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V	2.45			V
	V_{IL}	Ta=–20 to +75 °C			0.85	
Digital input current	I_{IH}	AV_{DD}=DV_{DD}=4.75 to 5.25 V	–5		5	µA
	I_{IL}	Ta=–20 to +75 °C				
SREF output voltage	V_{SR}		1.0	1.2	1.45	V
Setup time	ts		3.0			ns
Hold time	th		3.0			ns
Rise time	tr		5			ns
Propagation delay time	t_{PD}			5		ns
$\overline{CE}$ enable time ∗	t_E	$\overline{CE}$= H→L		1	2	ms
$\overline{CE}$ disable time ∗	t_D	$\overline{CE}$= L→H		1	2	ms

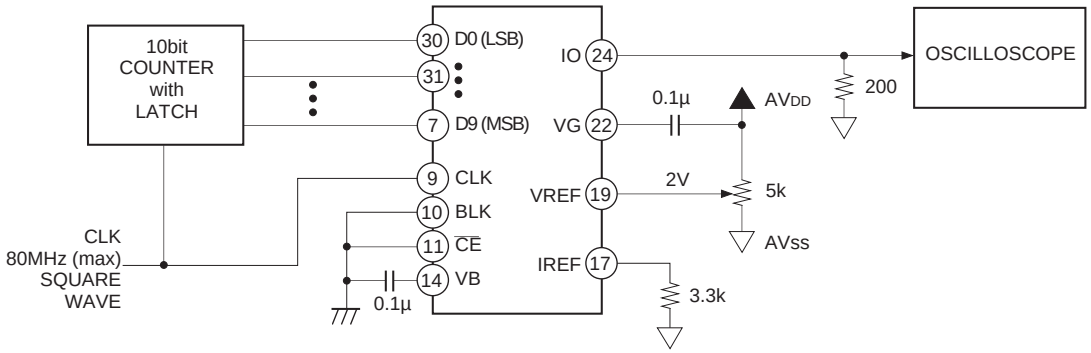
∗ When the external capacitor for the VGR,VGG and VGB pins are 0.1 µF.

Electrical Characteristics Measurement Circuit

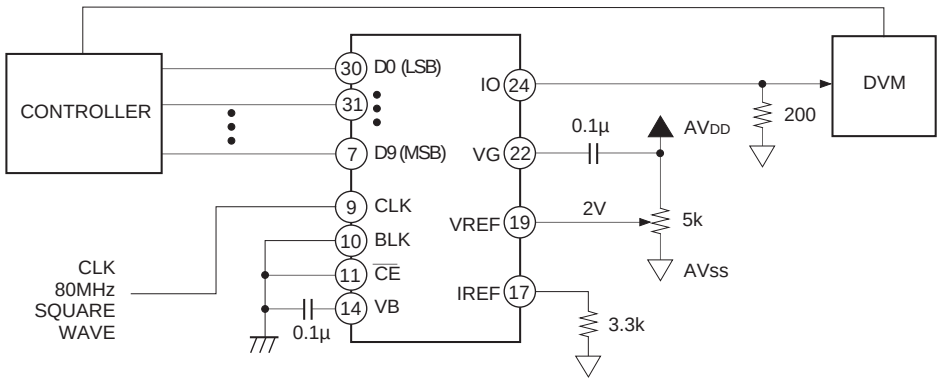
Analog Input Resistance
Digital Input Current
} **Measurement Circuit**



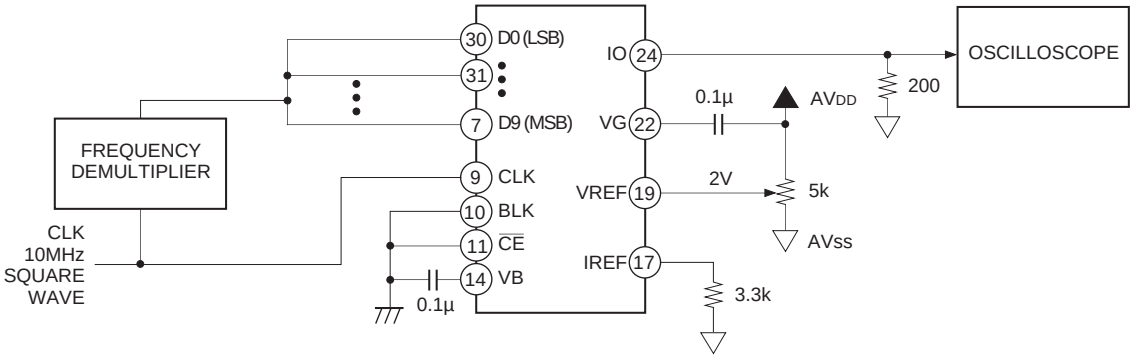
Maximum Conversion Rate Measurement Circuit



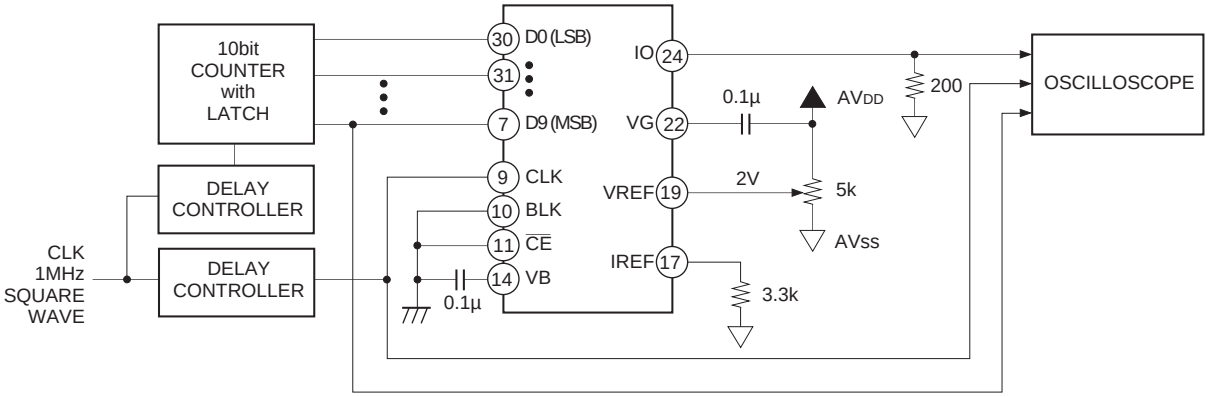
DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit

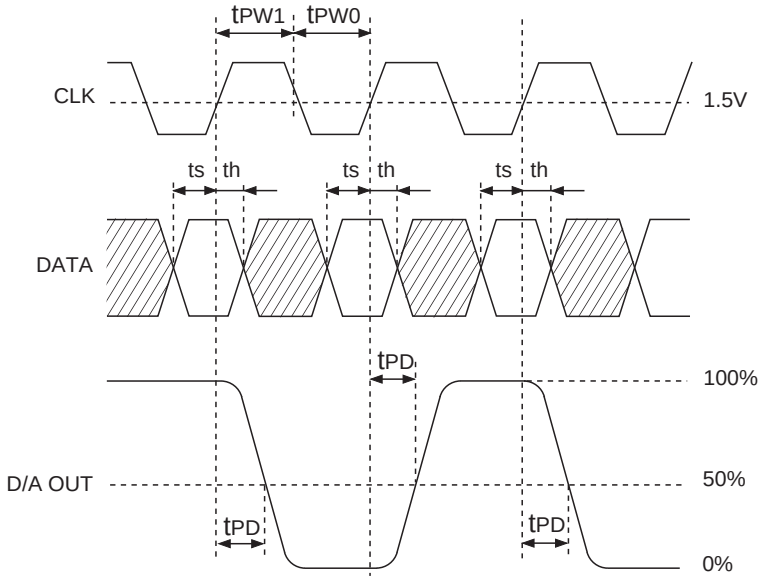


Setup Time / Hold Time / Glitch Energy — Measurement Circuit



Description of Operation

Timing Chart

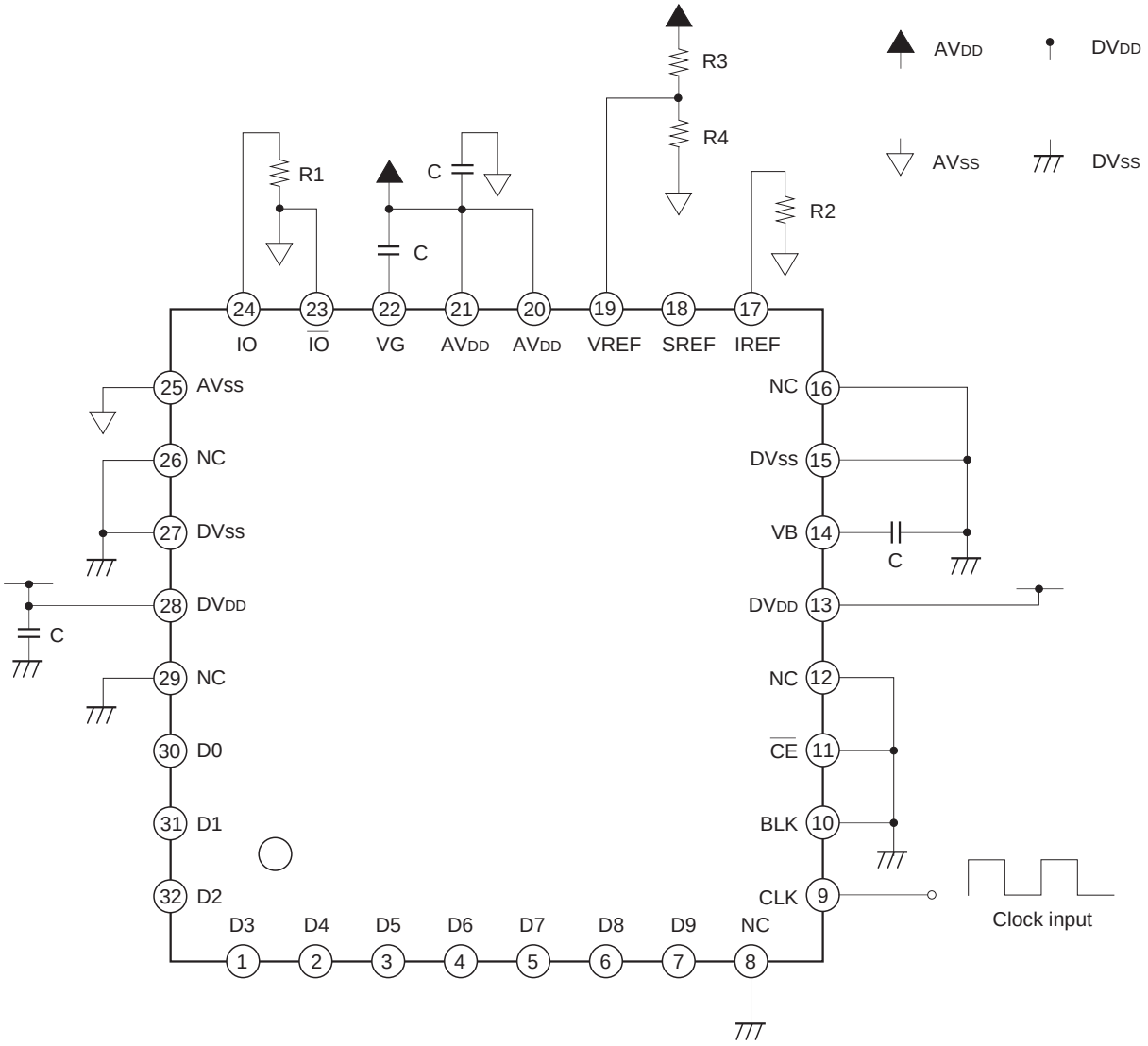


I/O Correspondence Table

(When 2.00 V output full-scale voltage)

Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1 1 1	2.0 V
:	
1 0 0 0 0 0 0 0 0 0	1.0 V
:	
0 0 0 0 0 0 0 0 0 0	0 V

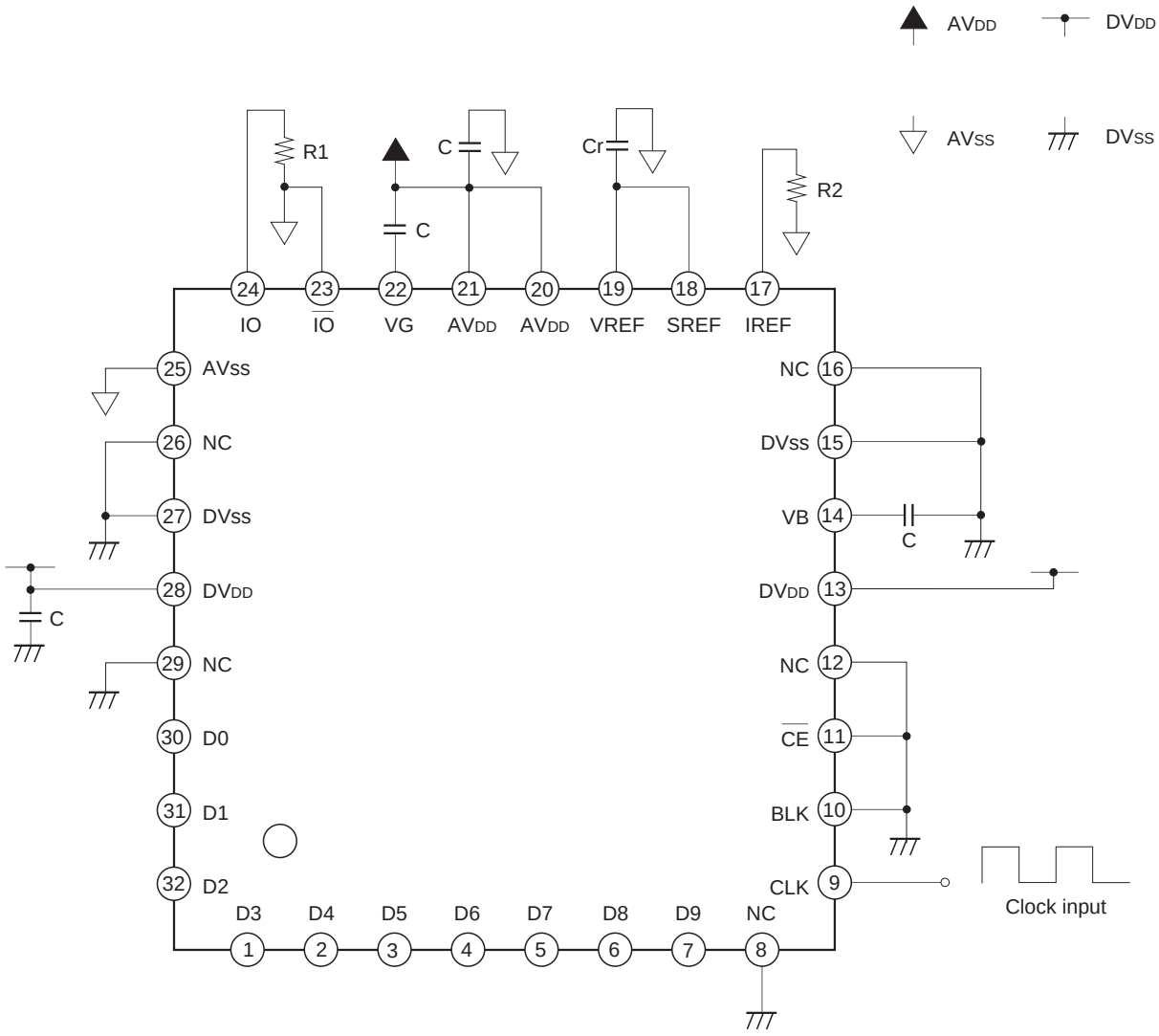
Application Circuit 1



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- Pin 18 is left open when using normally
- R1=200Ω
- R2=3.3kΩ (resistance 16 times R1) (R_{IR})
- R3=3.0kΩ
- R4=2.0kΩ
- C=0.1µF

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2



- When 5.0V supply voltage (DV_{DD} and AV_{DD})
- Digital input from Pins 30 to 32 and Pins 1 to 7
- R1=200Ω
- R2=2.0kΩ
- C =0.1µF
- Cr =4.7µF

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- Selecting the Output Resistance

  CXD2315Q is a current output type D/A converter. To create the output voltage, connect the resistor to the current output pin IO.

  Specifications: Output full-scale voltage V_{FS} = 1.8 to 2.0 [V]
  Output full-scale current I_{FS} = 10 or less [mA]

  Calculate the output resistance from $V_{FS} = I_{FS} \times R_{OUT}$. Connect a resistance sixteen times the output resistance to the reference current pin IREF. In some cases, as this value may not exist, a similar value can be used instead.

  Note that the V_{FS} will be the following. $V_{FS} = V_{REF} \times 16\ R_{OUT}/R$

  V_{REF} is the voltage set at the VREF pin, R_{OUT} is the resistor to be connected to the current output pin IO and R_{IR} is the resistor to be connected to the IREF. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data settling time. Set the best values according to the purpose of use.

- Correlation between Data and Clock

  For the CXD2315Q to display the desired performance as a D/A converter, the data transmitted from outside and the clock must be synchronized properly. Adjust the setup time (ts) and hold time (th) as specified in "Electrical Characteristics".

- Power supply and ground

  Separate the analog and digital power supplies and grounds around the device to reduce noise effects. By-pass the power supply pin to each ground with a 0.1 µF ceramics capacitor as near to the pin as possible for both the digital and analog signals.

- Latch up

  Analog and digital power supply must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on.

- IREF pin

  The IREF pin is very sensitive to improve the AC characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.

- VG pin

  It is recommended to use a 1 µF capacitor to improve the AC characteristics though the typical capacitance value externally connected to the VG pin is 0.1 µF.

- SREF

  SREF is an independent regulated voltage source. By connecting the SREF pin and the VREF pin, stable output amplitudes that do not depend on fluctuations in the power supply can be obtained.

  In this case, as described above, $V_{FS} = V_{SR} \times 16R_{OUT}/R_{IR}$, set the V_{FS} according to R_{IR}. V_{SR} is the output voltage of the SREF pin.

  Do not use this pin as a reference power supply for other ICs because this is dedicated for the VG pin of the CXD2315Q.

• $\overline{IO}$ pin
The $\overline{IO}$ pin is the inverted current output pin described in the Pin Description. The sum of the currents output from the IO pin and the $\overline{IO}$ pin becomes the constant value for any input data.
However, the performances such as the linearity error of the $\overline{IO}$ pin output current is not guaranteed.

GE (Glitch energy)

GE, described in the CXD2315Q, is a spike noise which appears synchronizing with the clock falling edge when the input data (for 1 to 1024 input) changes to 128, 256, 384, 512, 640, 768, 896, and 1024. Fig. 1 shows the change state of GE for the staircase wave output, and Fig. 2 shows the repetitive output waveform where the GE appears. These figures exhibit the difference of this IC from the conventional device.

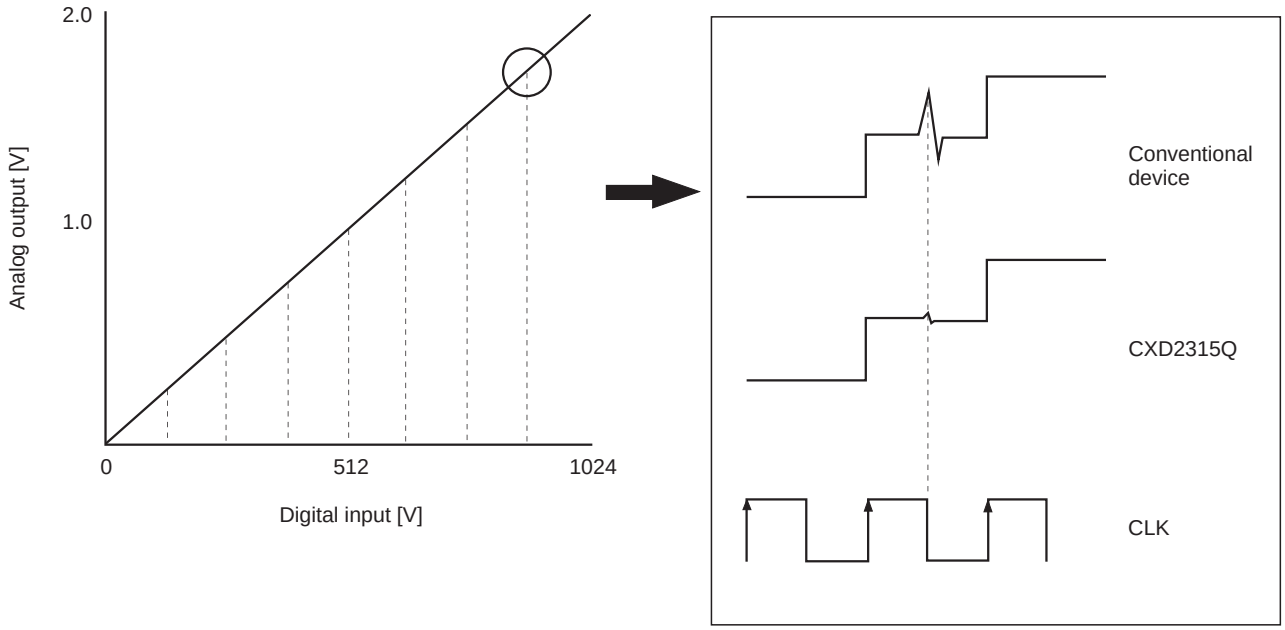


Fig. 1. Change of GE for staircase wave output

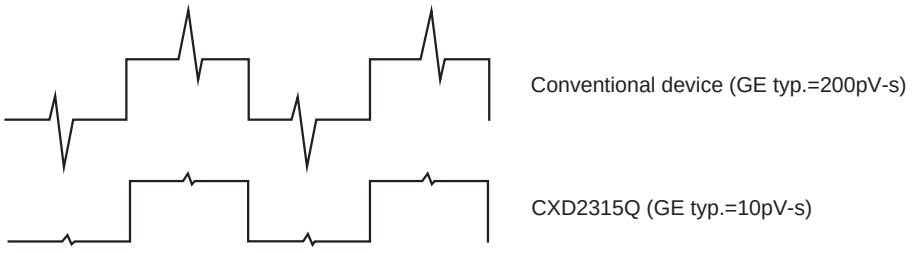


Fig. 2. Repetitive output waveform where GE appears (for 200 Ω, 2 Vp-p output)

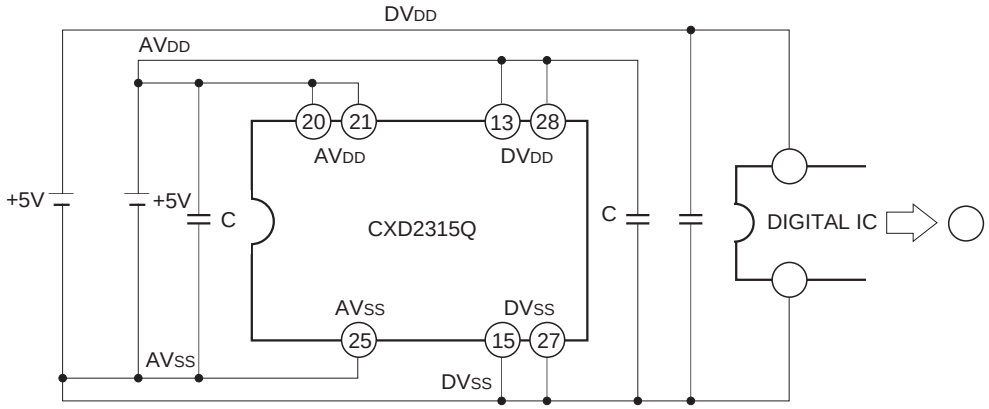
The CXD2315Q reduces the GE much shown in Fig.s 1 and 2.

Latch Up Prevention

The CXD2315Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 20 and 21) and DV_{DD} (Pins 13 and 28), when power supply is ON.

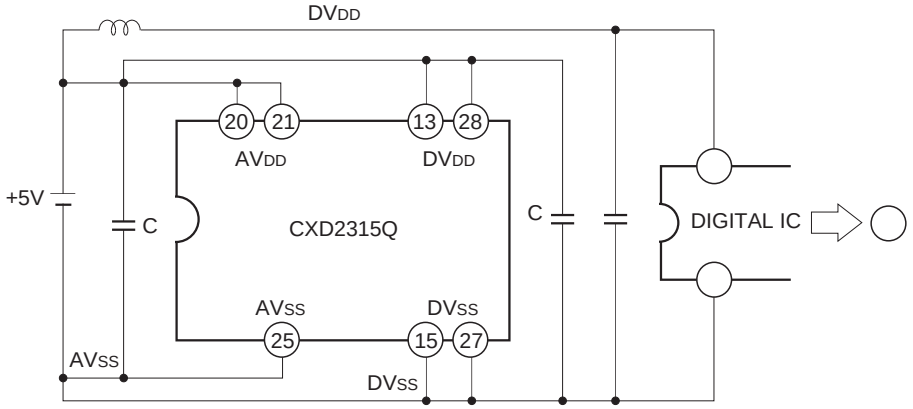
1. Correct usage

a. When analog and digital supplies are from different sources

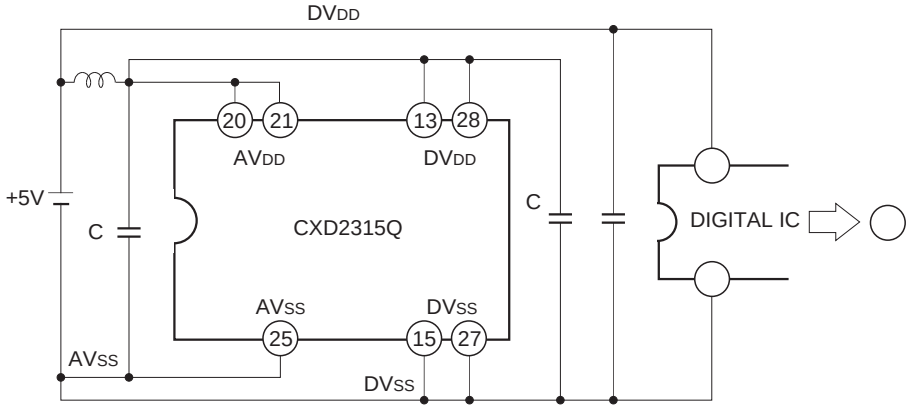


b. When analog and digital supplies are from a common source

(i)

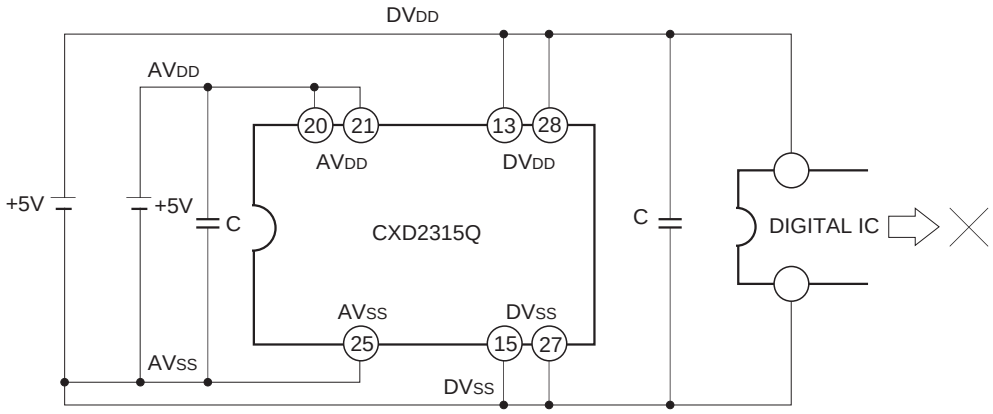


(ii)



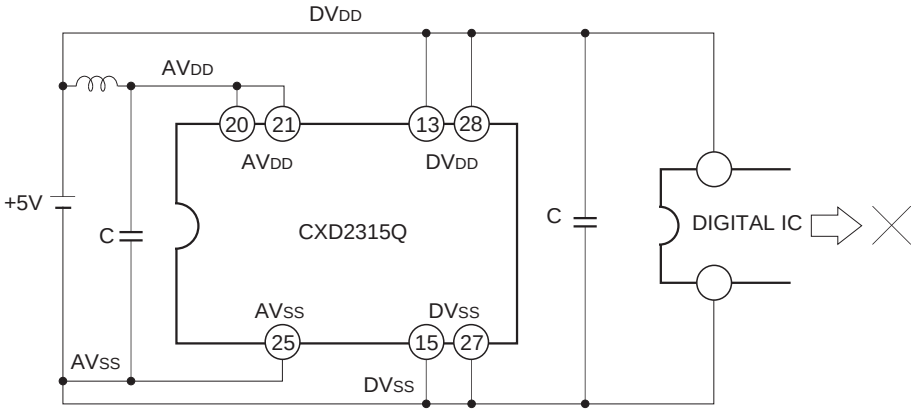
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

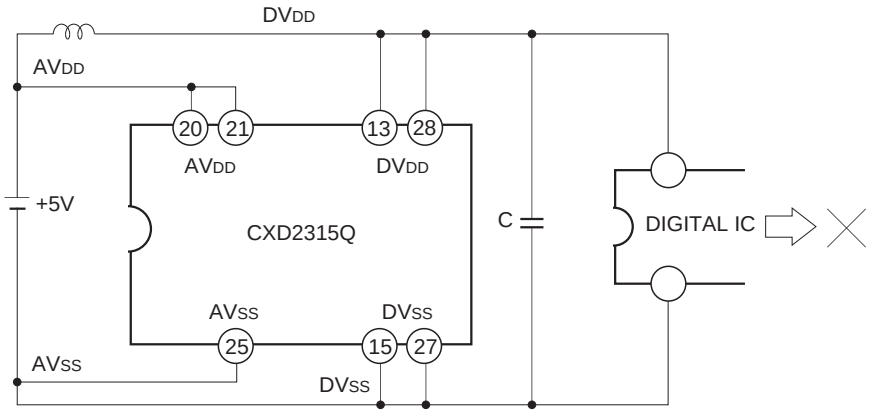


b. When analog and digital supplies are from common source

(i)



(ii)



Example of Representative Characteristics

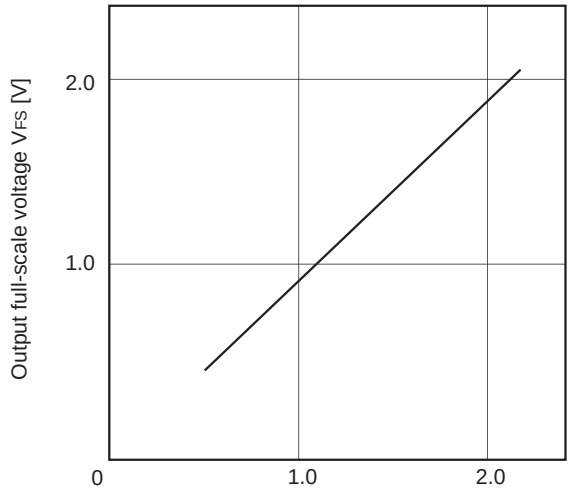


Fig. 3. Reference voltage vs.Output full-scale voltage

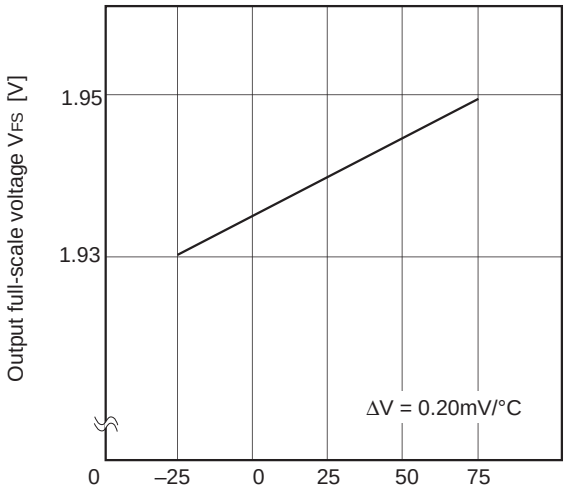


Fig. 4. Ambient temperature vs. Output full-scale voltage

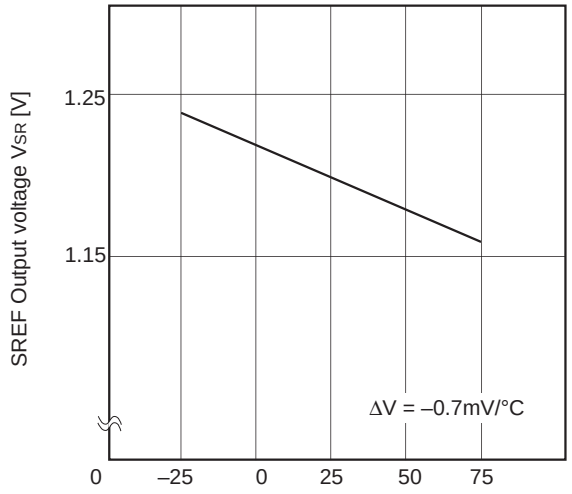


Fig. 5. Ambient temperature vs. SREF output voltage

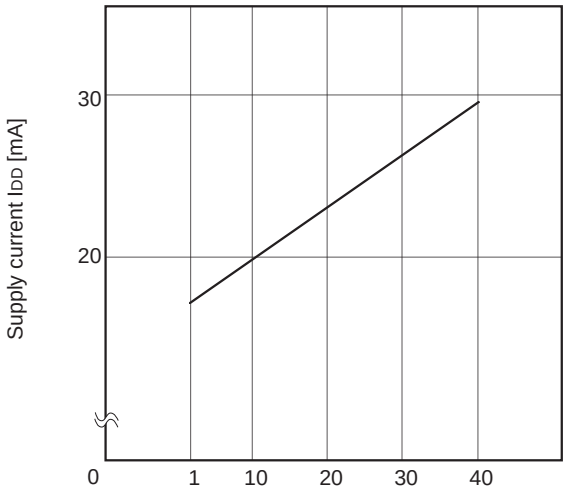
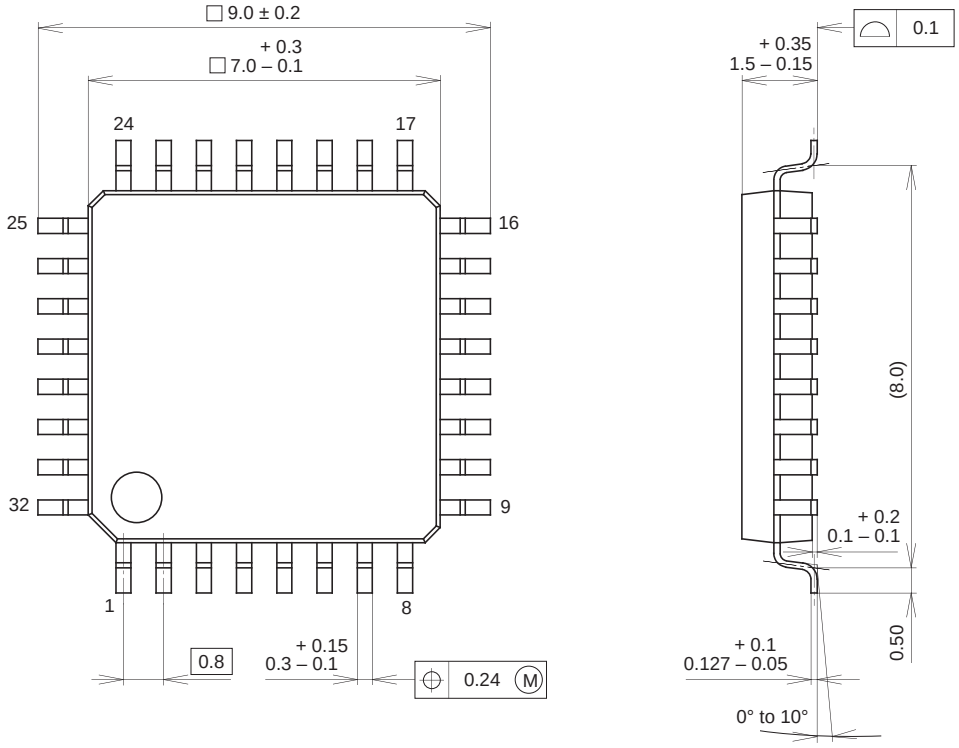


Fig. 6. Output frequency vs. Supply current

Standard Measurement Conditions and Description
- AD_{DD}=DV_{DD}=5V
- V_{REF}=2.0V
- R_{OUT}=200Ω
- R_{IR}=3.3kΩ
- F_{CLK}=80MHz
- Ta=25°C
- Fig. 4 includes the temperature characteristics of external metal film resistor.
- Input data in Fig. 6=all “0” and “1” of rectangular wave; clock frequency=80MHz.

Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g