

CMOS 8-bit Single Chip Microcomputer

Piggy/evaluation chip

Description

The CXP740000 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP740056/740096/740010.

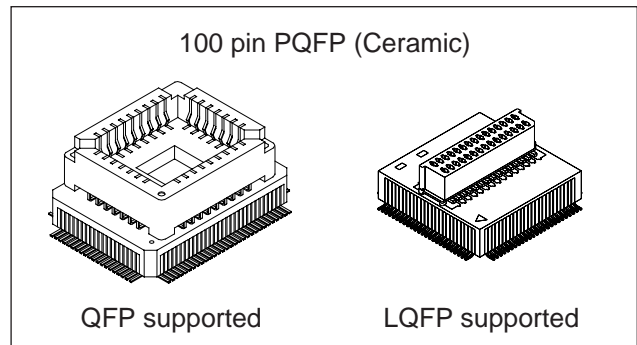
Features

- A wide instruction set (211 instructions) which covers various types of data.
 - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle
 - 167ns at 24MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (2.7 to 5.5V)
 - 122µs at 32kHz operation (2.7 to 5.5V)
- Applicable EPROM CXP27C702K
(Maximum 120K bytes are available.)
- Incorporated RAM capacity 4096 bytes
- Peripheral functions
 - A/D converter 8 bits, 8 channels, successive approximation method
(Conversion time of 10.3µs/24MHz)
 - Serial interface Start-stop sync type (UART), 1 channel
Incorporated buffer RAM
(Auto transfer for 1 to 32 bytes), 2 channels
8-bit clock sync type (MSB/LSB first selectable), 1 channel
 - Timer 8-bit timer, 2 channels
8-bit timer/counter, 2 channels
19-bit time-base timer, 16-bit capture timer/counter
32kHz timer/counter
 - Remote control unit receive circuit Internal noise elimination circuit
Internal 8-bit, 6-stage FIFO for measured data
 - PWM output 12 bits, 12 channels
- Interruption 24 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP740000. Refer to the Products List for details.

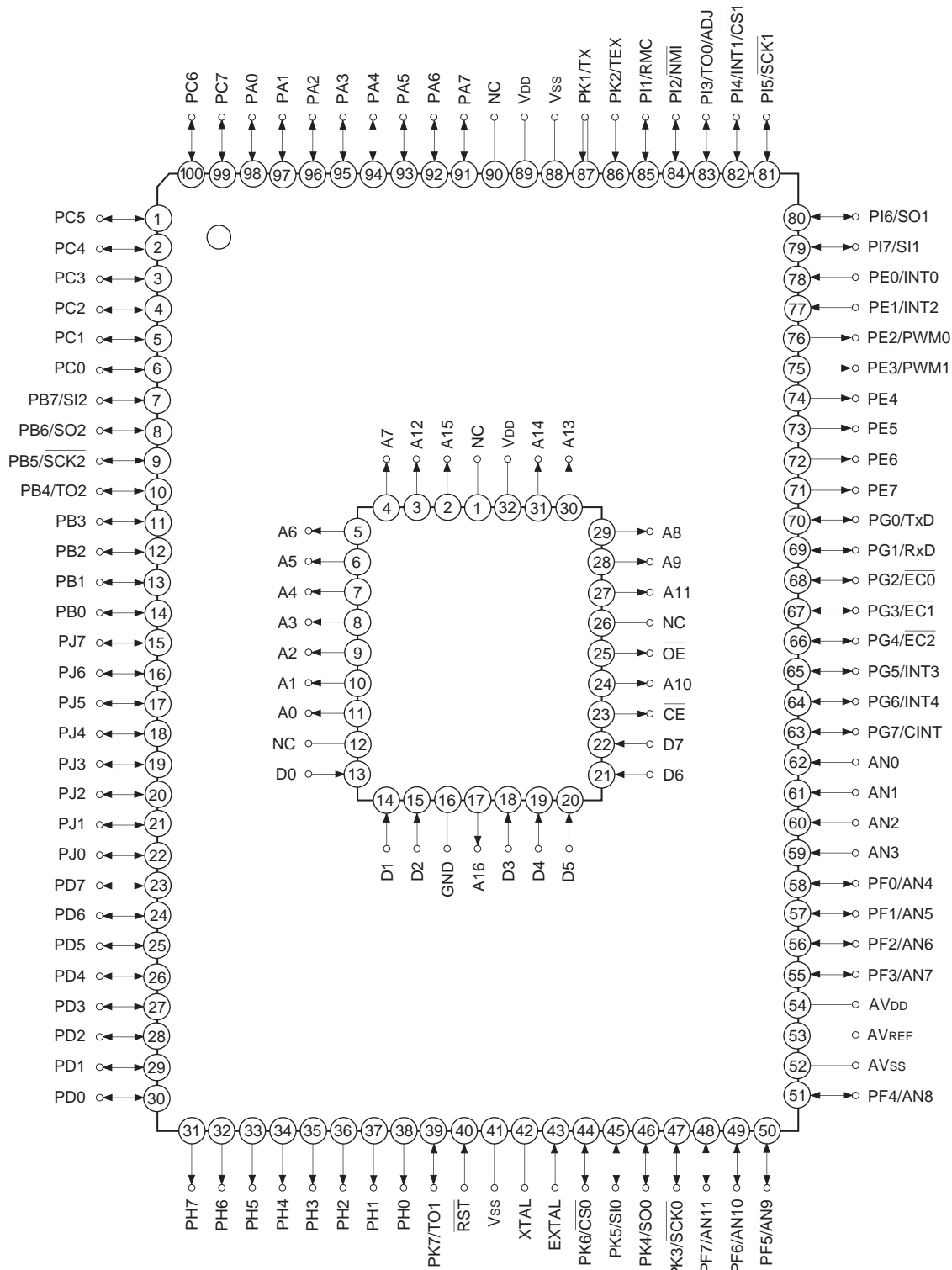
Structure

Silicon gate CMOS IC



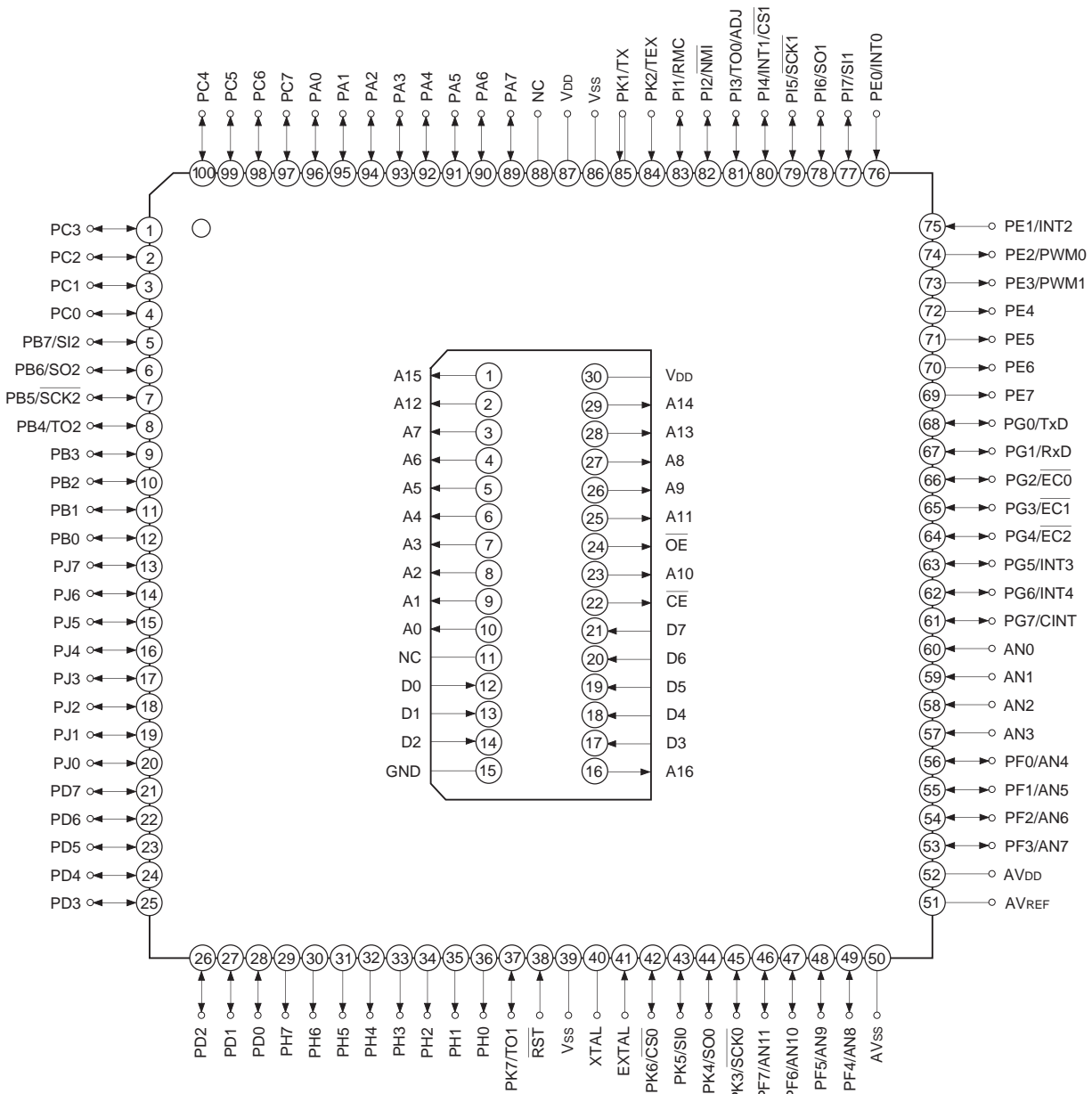
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Pin Assignment in Piggyback Mode (QFP package)



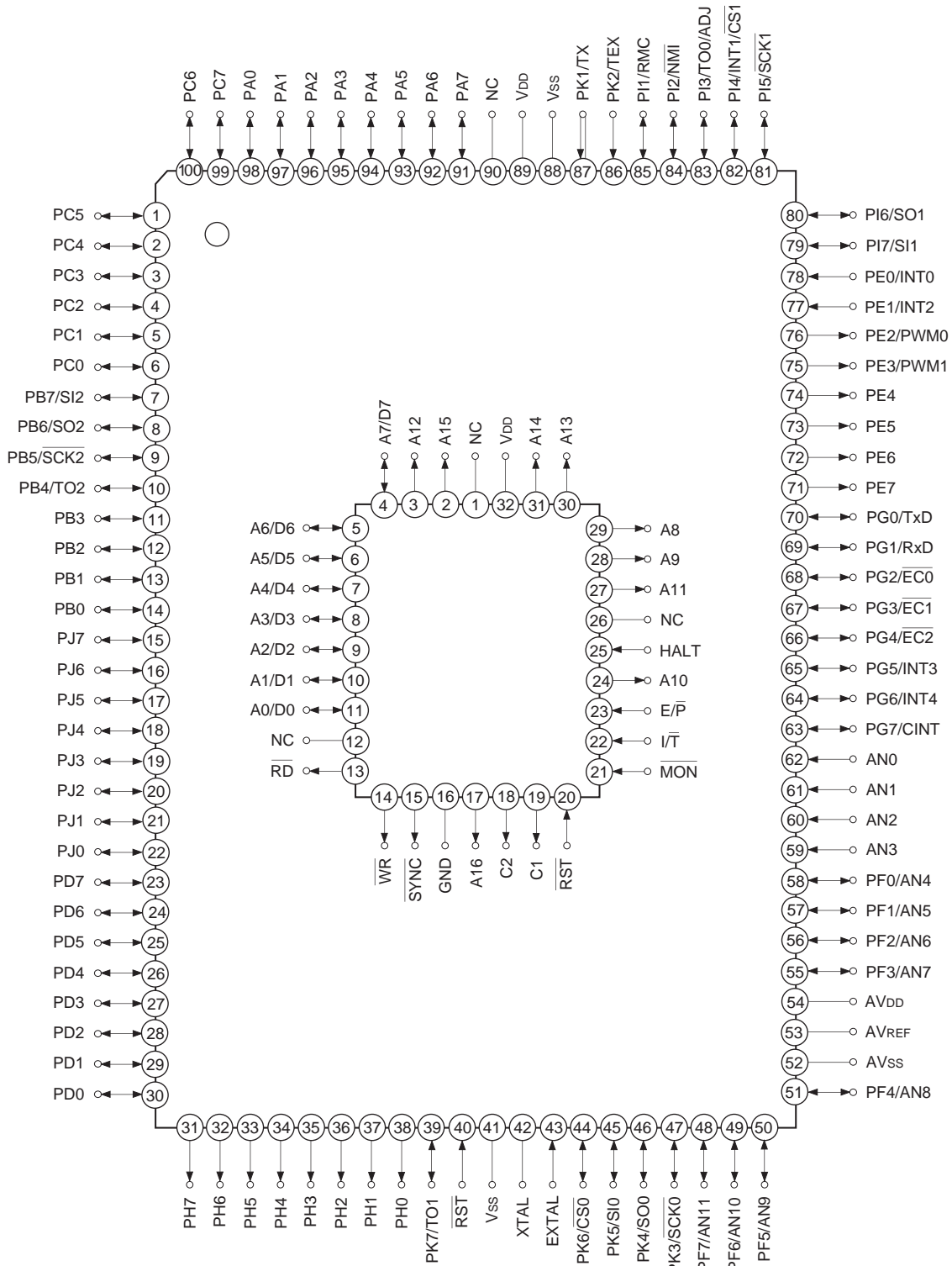
- Note)** 1. NC (Pin 90) is left open.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment in Piggyback Mode (LQFP package)



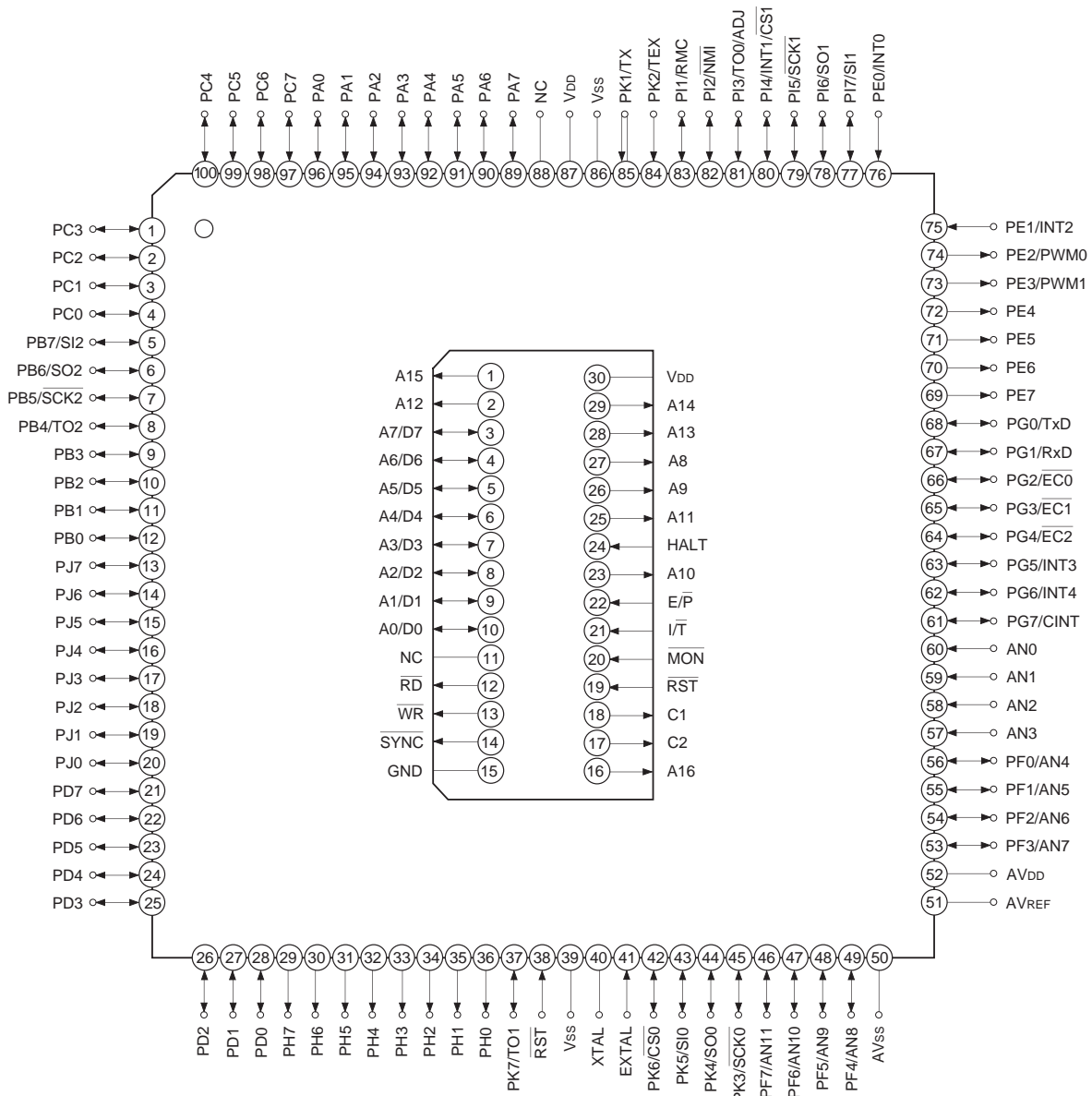
- Note)** 1. NC (Pin 88) is left open.
 2. Vss (Pins 39 and 86) are both connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



- Note)** 1. NC (Pin 90) is left open.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment in Evaluator Mode (LQFP package)



- Note** 1. NC (Pin 88) is left open.
 2. Vss (Pins 39 and 86) are both connected to GND.

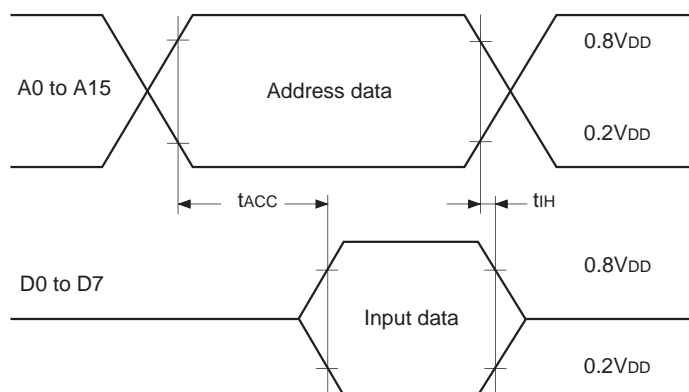
EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 2.7$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1	ns
				50*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

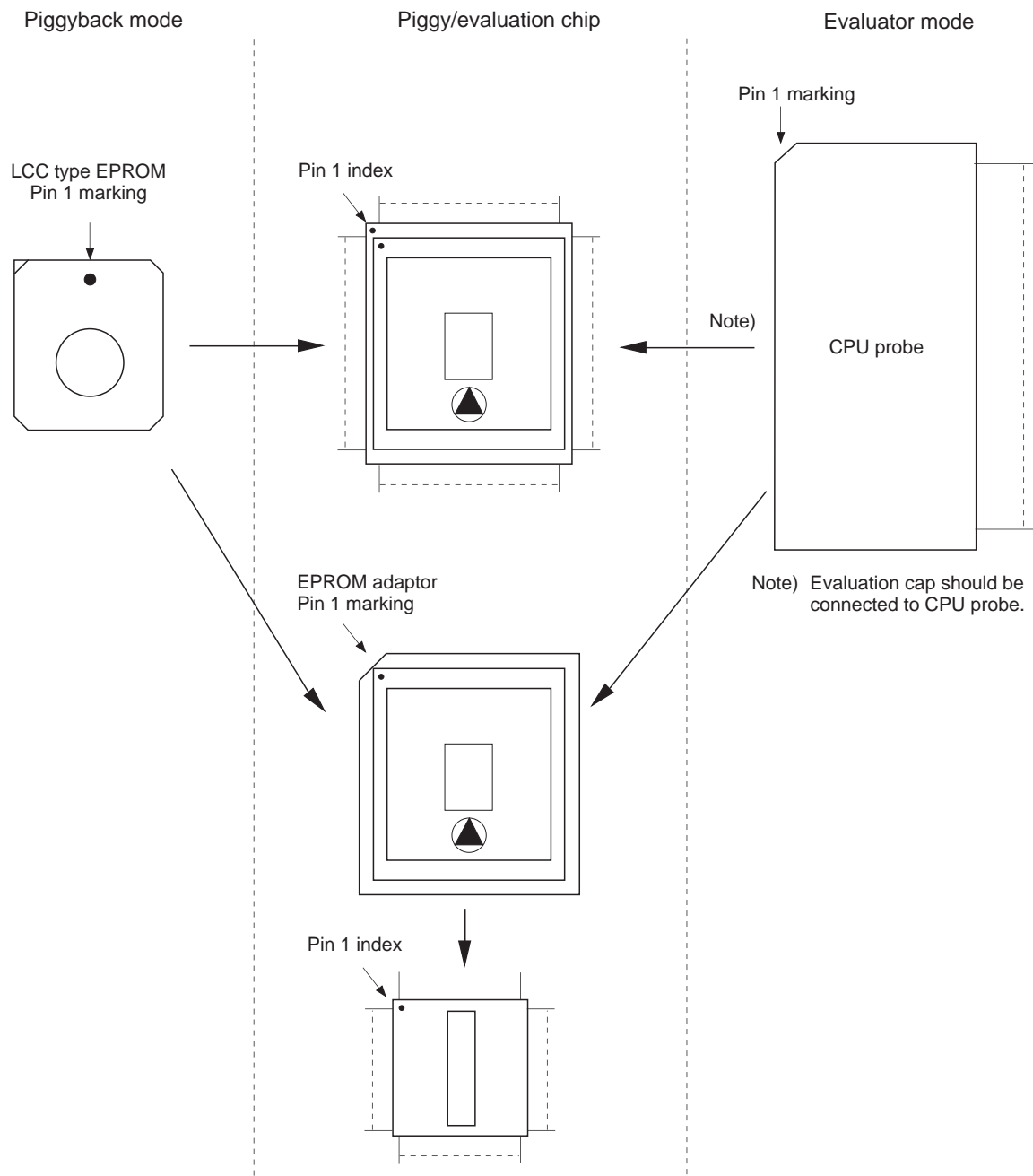
*2 At 12MHz operation ($V_{DD} = 2.7$ to 5.5V), at 24MHz operation ($V_{DD} = 4.5$ to 5.5V)



Products List

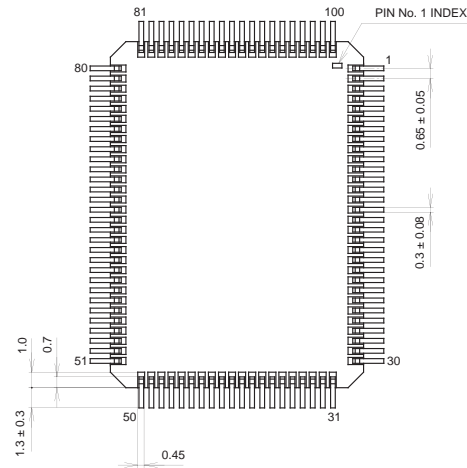
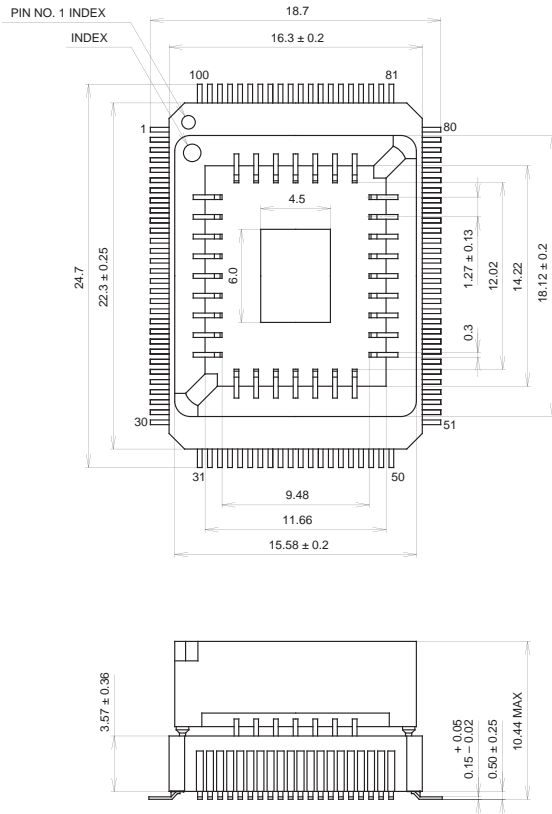
Option item	Products			
	Mask ROM			Piggy/evaluation chip
	CXP740056	CXP740096	CXP740010	CXP740000-U01Q CXP740000-U01R
Package	100-pin plastic QFP/LQFP			100-pin ceramic PQFP
ROM capacity	56K bytes	96K bytes	120K bytes	EPROM 120K bytes
Pull-up resistor for reset pin	Existent/Non-existent			Existent

Piggyback mode/evaluator mode can be switched as shown below.



Package Outline Unit: mm

100PIN PQFP (CERAMIC)

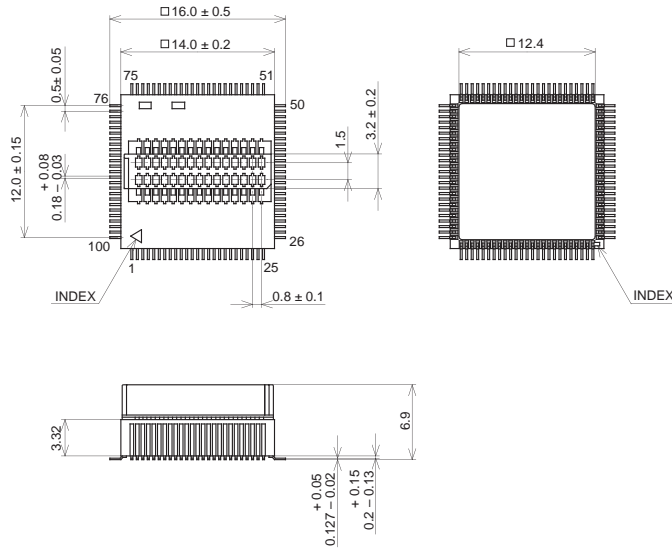


PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	—————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP(CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L05
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	—————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.4g