SONY

CXP824P40A

CMOS 8-bit Single Chip Microcomputer

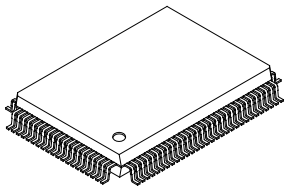
Description

The CXP824P40A is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer counter, fluorescent display tube, controller/driver, remote control reception circuit, CTL duty detection circuit, 14-bit PWM output and high-speed output circuit besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP824P40A also provides sleep/stop function that enables lower power consumption.

CXP824P40A is the PROM-incorporated version of the CXP82440A with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic)



Structure

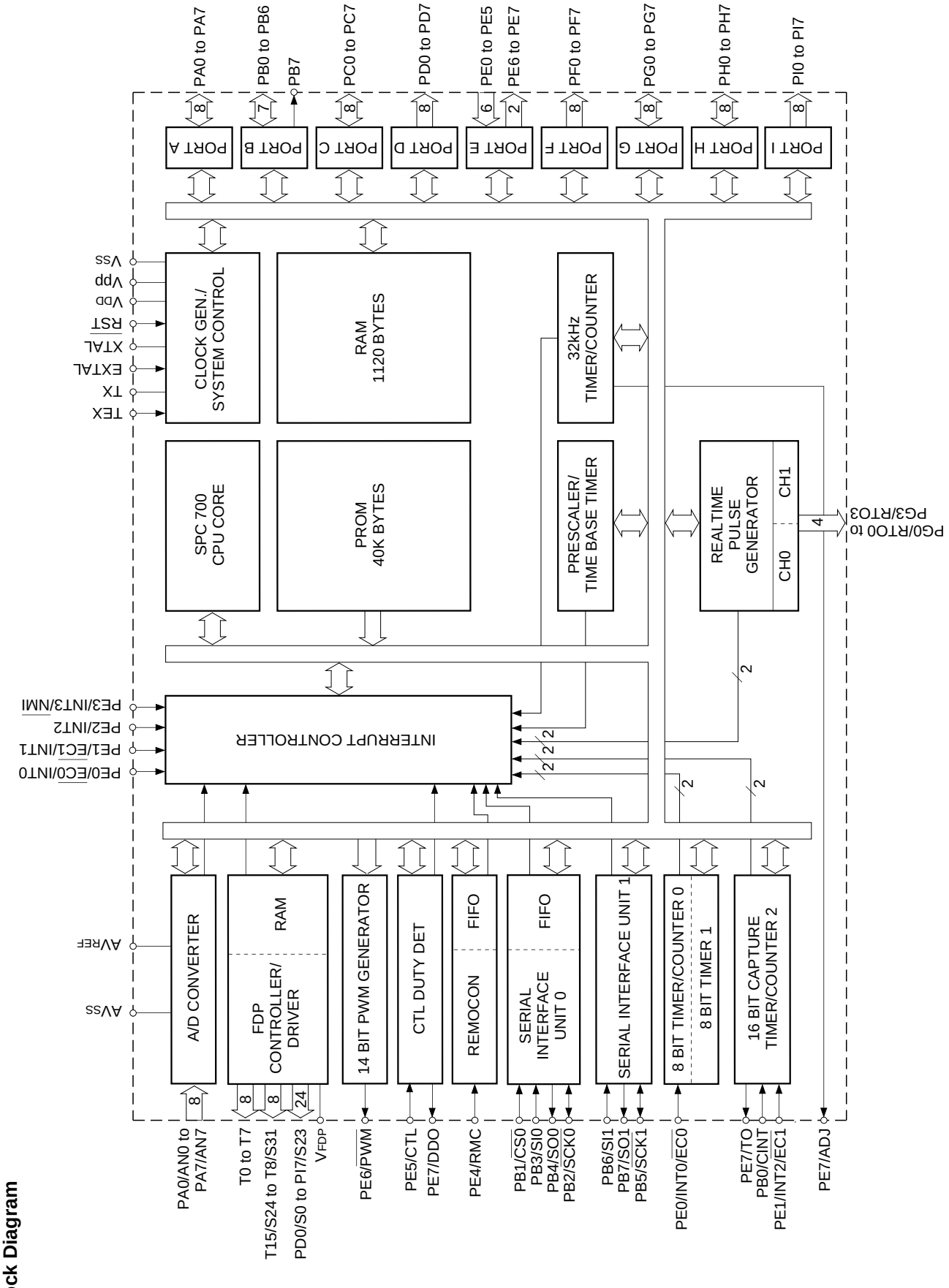
Silicon gate CMOS IC

Features

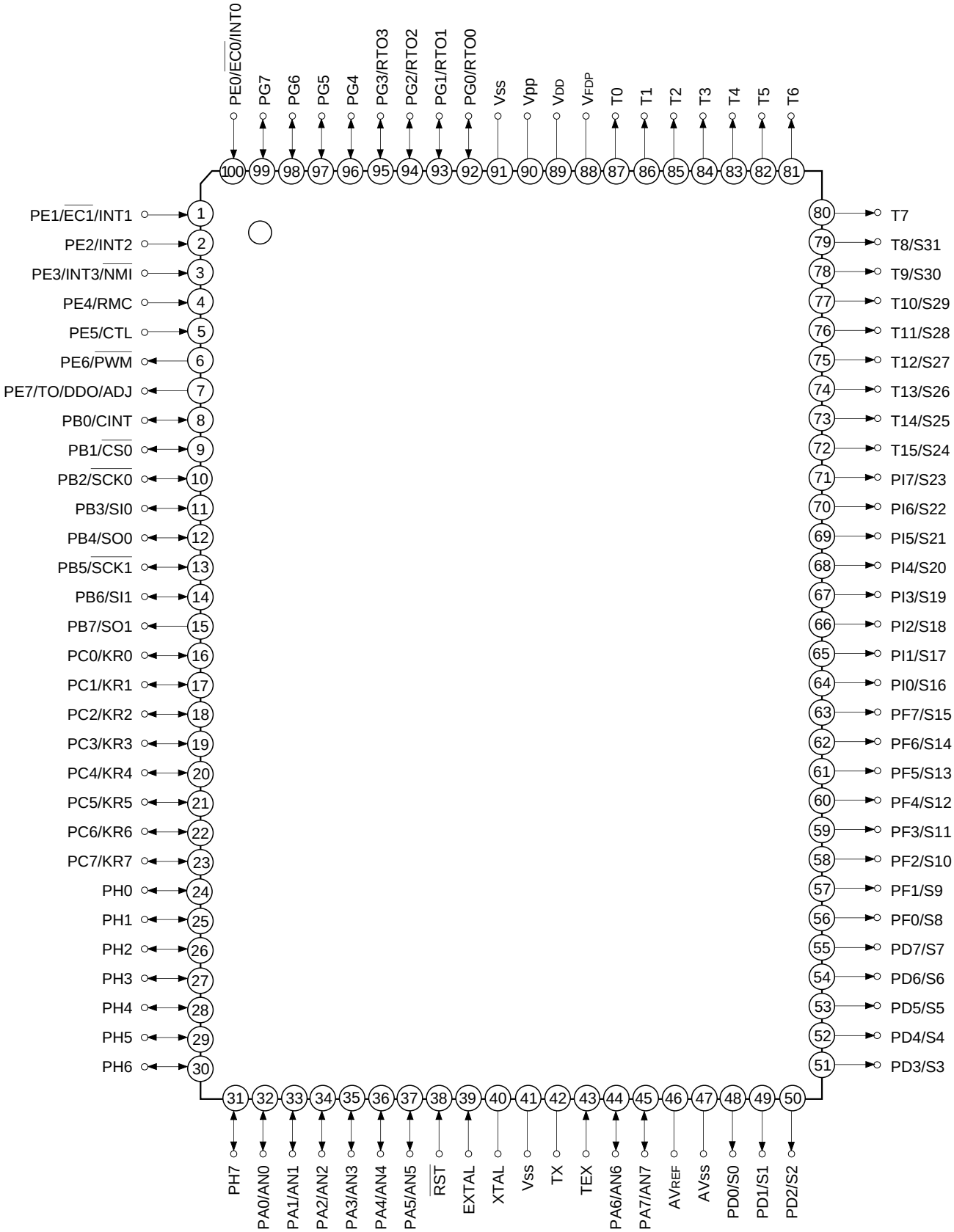
- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 400ns at 10MHz operation; 122µs at 32kHz operation
- Incorporated PROM capacity — 40K bytes
- Incorporated RAM capacity — 1120 bytes (including fluorescent display area)
- Peripheral functions
  - — A/D converter — 8-bit, 8-channel, successive approximation method (Conversion time of 32µs/10MHz)
  - — Serial interface — Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock sync type, 1 channel
  - — Timers — 8-bit timer, 8-bit timer/counter, 19-bit time base timer; 16-bit capture timer/counter, 32kHz timer/counter
  - — Fluorescent display tube controller/driver — Maximum of 384 segments display possible; 1 to 16-digit dynamic display; Dimmer function; High voltage drive output (40V); On-chip pull-down resistor (Mask option); Hardware key scan function (Maximum of 16 × 8 key matrix compatible)
  - — Remote control receiving circuit — Incorporated noise elimination circuit; 8-bit measurement counter with on-chip 6-stage FIFO
  - — PWM output — 14 bits, 1 channel
  - — CTL duty detection circuit
  - — High-speed output circuit — RTG 4 pins
- Interruption — 19 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP

E94Z17-PP

Block Diagram



Pin Assignment (Top View)



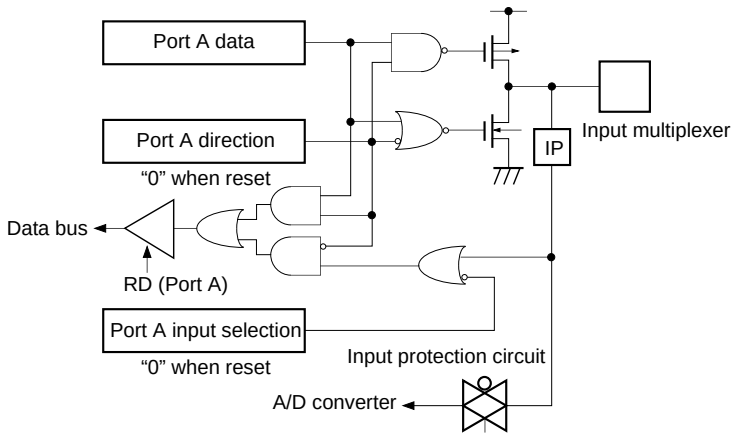
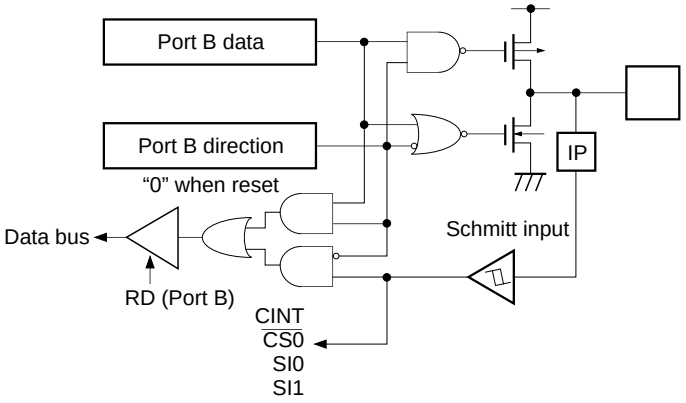
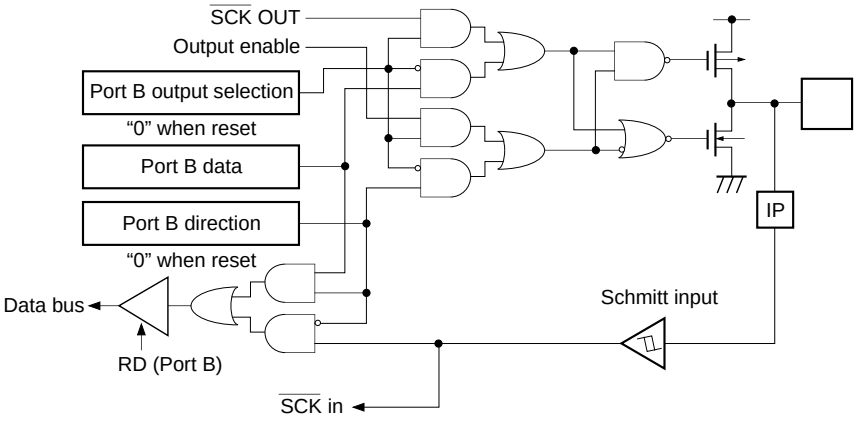
Note) 1. Vpp (Pin 90) must be connected to V_{DD}.
2. Vss (Pins 41 and 91) are both connected to GND.

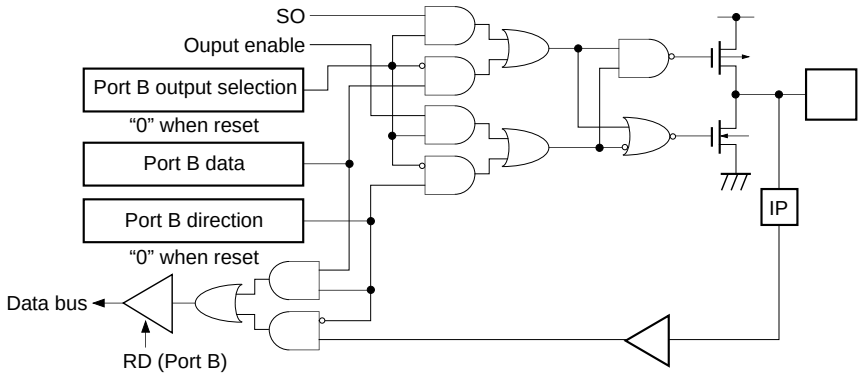
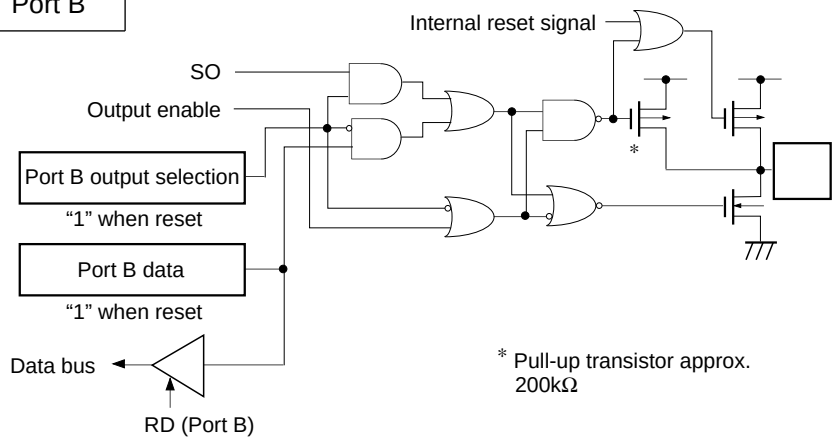
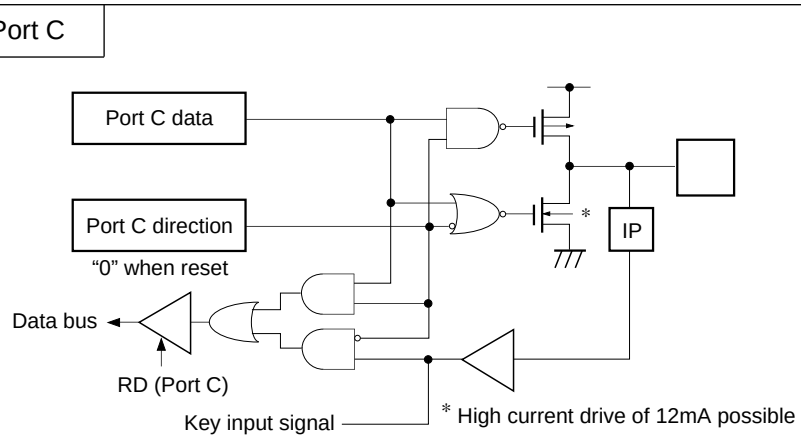
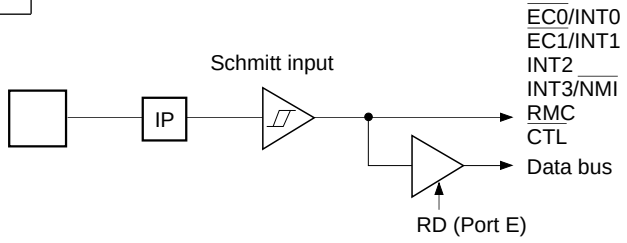
Pin Description

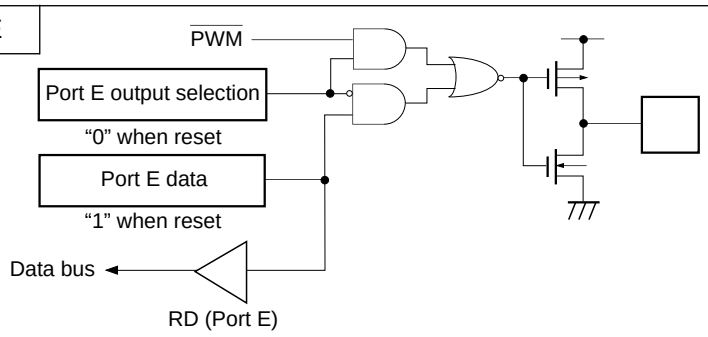
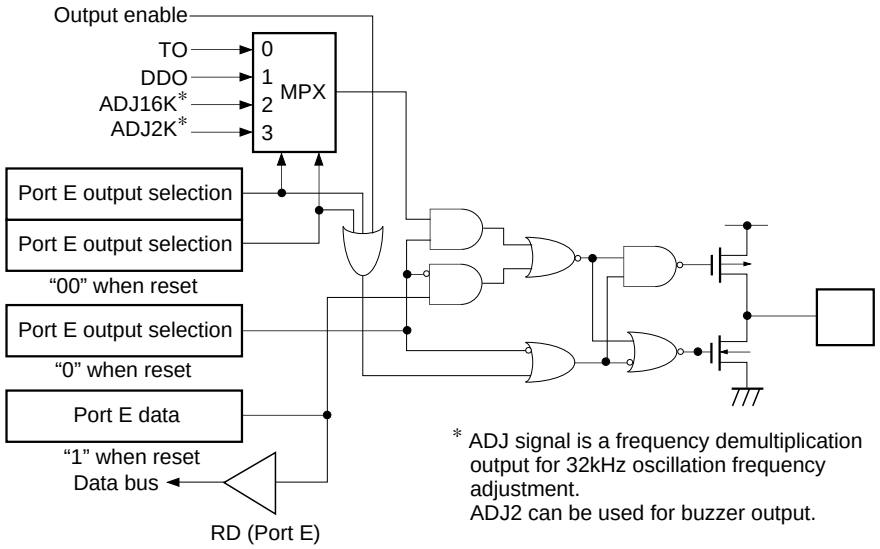
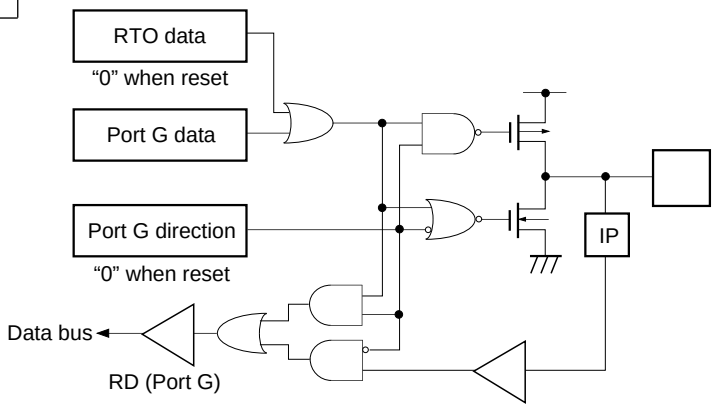
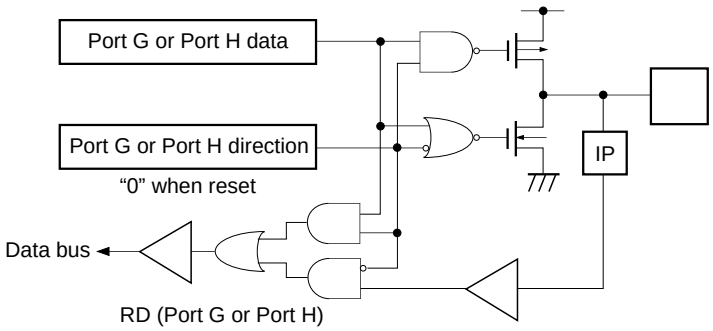
Pin code	I/O		Functions	
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in single bit units. (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O for lower 7 bits can be set in a unit of single bits. Uppermost bit (PB7) is for output only. (8 pins)	Capture input to 16-bit timer/counter.	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	Output/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. (8 pins)	Serves as key return inputs when operating key scan with FDP segment signal.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal outputs.	
$\overline{PE0}$/INT0/ $\overline{EC0}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
$\overline{PE1}$/INT1/ $\overline{EC1}$	Input/Input/Input			
PE2/INT2	Input/Input			Non-maskable interruption request input.
$\overline{PE3}$/INT3/ $\overline{NMI}$	Input/Input/Input			
PE4/RMC	Input/Input		Remote control reception circuit input.	
PE5/CTL	Input/Input		Input for CTL duty direction circuit.	
PE6/$\overline{PWM}$	Output/Output		14-bit PWM output.	
PE7/TO/ DDO/ADJ	Output/Output/ Output/Output		Output for the 16-bit timer/counter rectangular waves, CTU duty detection, and 32kHz oscillation frequency demultiplication.	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PG0/RTO0 to PG3/RTO3	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Data for the lower 4 bits are gated with the contents of RTO or OR-gate output. (8 pins)	Outputs for real-time pulse generator (RTG). Functions as high-precision, real-time pulse output port. (4 pins)	
PG4 to PG7	I/O			

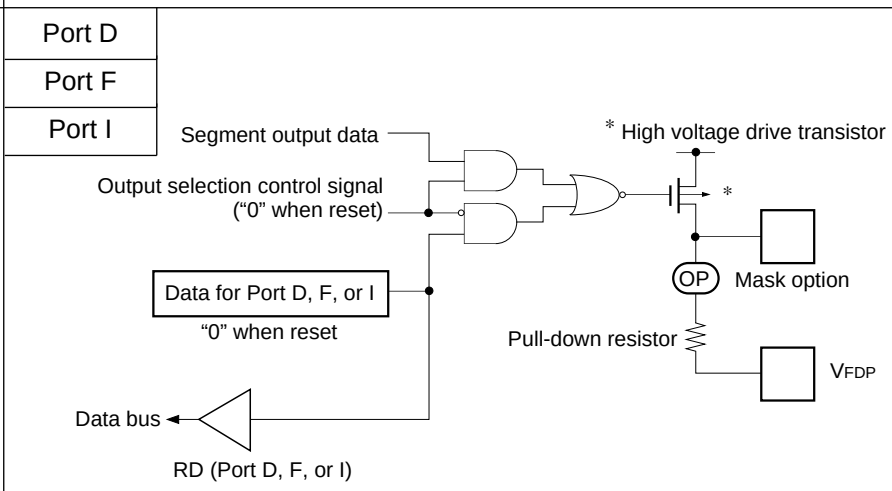
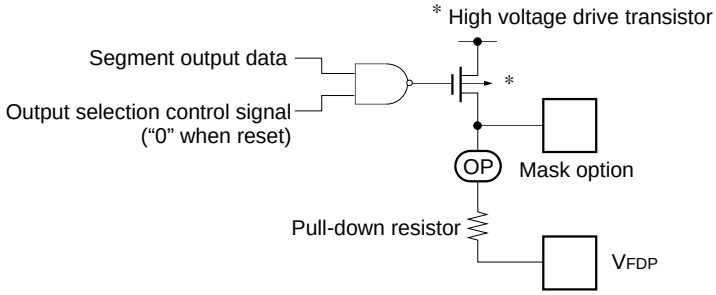
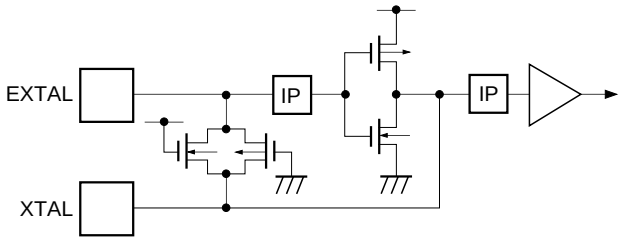
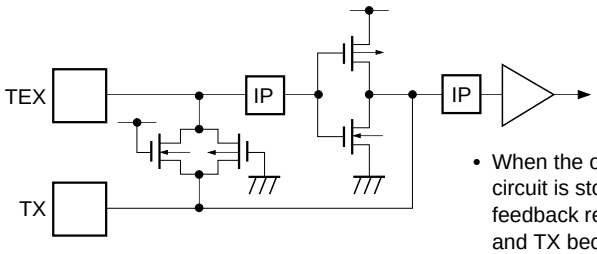
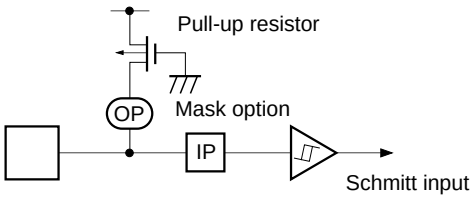
Pin code	I/O	Functions	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PI0/S16 to PI7/S23	Output/Output	(Port I) 8-bit output ports. (8 pins)	FDP segment signal outputs.
T8/S31 to T15/S24	Output/Output	Outputs for FDP timing (digit) signals/segment signals.	
T0 to T7	Output	FDP timing signal outputs.	
V_{FDP}		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		A/D converter GND.	
V_{DD}		Vcc supply.	
Vpp		V_{CC} supply for incorporated PROM writing. Connect to V_{DD} during normal operation.	
V_{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/CINT PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	Port B 	Hi-Z
PB7/SO1 1 pin	Port B 	High level
PC0/KR0 to PC7/KR7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 $\overline{\quad}$ PE3/INT3/$\overline{NMI}$ PE4/$\overline{RMC}$ PE4/$\overline{CTL}$ 6 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE6/$\overline{PWM}$ 1 pin	Port E 	High level
PE7/TO/ DDO/ADJ 1 pin	Port E  * ADJ signal is a frequency demultiplication output for 32kHz oscillation frequency adjustment. ADJ2 can be used for buzzer output.	High level
PG0/RTO0 to PG3/RTO3 4 pins	Port G 	Hi-Z
PG4 to PG7 PH0 to PH7 12 pins	Port G Port H 	Hi-Z

Pin	Circuit format	When reset
PD0/S0 to PD7/S7 PF0/S8 to PF7/S15 PI0/S16 to PI7/S23 24 pins	Port D / Port F / Port I 	Hi-Z or Low level (when PD resistance is added)
T15/S24 to T8/S31 T0 to T7 16 pins		Hi-Z or Low level (when PD resistance is added)
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become “Low” level and “High” level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin		Hi-Z or High level (when pull-up resistance is added)

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AVss	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Display output voltage	V_{OD}	V_{DD} – 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} is reference.
High level output current	I_{OH}	–5	mA	All pins excluding outputs*2 (value per pin)
	I_{ODH1}	–15	mA	Display outputs S0 to S23 (value per pin)
	I_{ODH2}	–35	mA	Display outputs T0 to T7, and T8/S31 to T15/S24 (value per pin)
High level total output current	$\sum I_{OH}$	–40	mA	Total for all pins excluding display outputs
	$\sum I_{ODH}$	–100	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	Port 1
	I_{OLC}	20	mA	High current Port 1*3
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1) V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2) Specifies output current of general-purpose I/O ports.

*3) The high current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High-speed mode Guaranteed operation range
		3.5	5.5	V	Low-speed mode Guaranteed operation range
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
	Vpp	Vpp = V_{DD}		V	*4
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*3
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2
	V_{ILEX}	–0.3	0.4	V	EXTAL*3
Operating temperature	Topr	–10	+75	°C	

*1) Value for each pin of normal input port (PA, PB4, PC, PG, PH).

*2) Value of the following pins: $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, SI0, SI1, $\overline{EC0}$/INT0, $\overline{EC1}$/INT1, INT2, INT3/$\overline{NMI}$, RMC, CTL.

*3) Specifies only during external clock input.

*4) Vpp and V_{DD} should be set a same voltage.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA, PB, PC, PE6, PE7, PG, PH	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
Display output current	I_{OH}	S0 to S23	V_{DD} = 4.5V V_{OH} = V_{DD} – 2.5V	–8			mA
		S24/T15 to S31/T8, T0 to T7		–20			mA
Open drain output leakage current (P-CH Tr off state)	I_{LOL}	S24/T15 to S31/T8, T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} – 35V V_{FDP} = V_{DD} – 35V			–20	µA
Pull-down resistance	R_L	S24/T15 to S31/T8, T0 to T7	V_{DD} = 5V V_{FDP} = V_{DD} – 35V	60	100	270	kΩ
I/O leakage current	I_{IZ}	PA to PC, PE, PG, PH	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*	I_{DD1}	V_{DD}	High speed mode operation (1/2 frequency demultiplier clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		20	40	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		450	1100	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		1.2	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, 10MHz crystal oscillation; and termination of 32kHz oscillation			30	µA
Input capacity	C_{IN}	Pins other than S0 to S31, T0 to T7, PB7, PE6, AV_{REF}, AV_{SS}, V_{FDP}, V_{DD}, V_{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

* When all pins are open.

The leakage carrent is not specified because PB7 is dedicated for output.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3	t_{sys} + 50*			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			µs
Event count input rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

* tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FE$_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

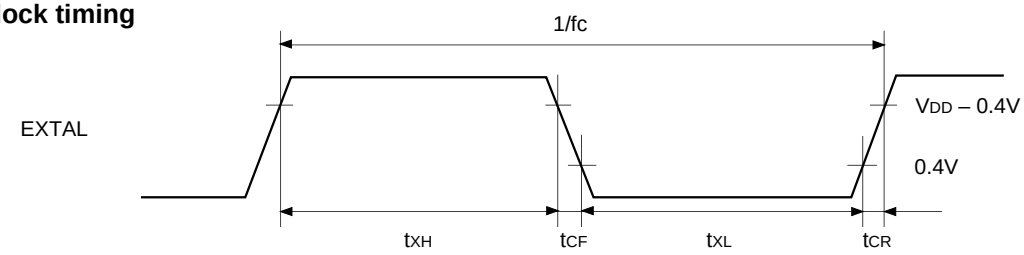


Fig. 2. Clock application conditions

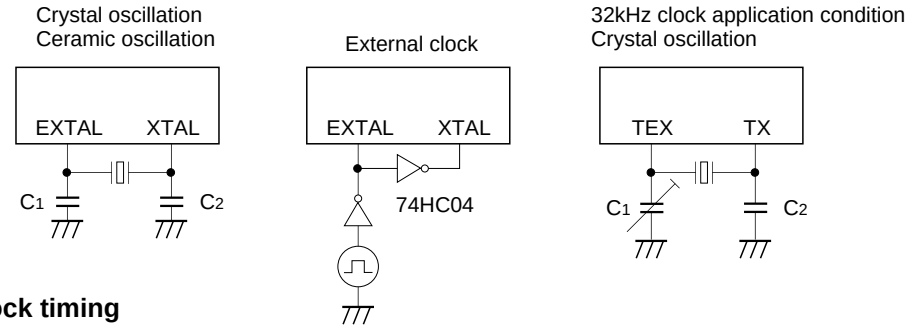
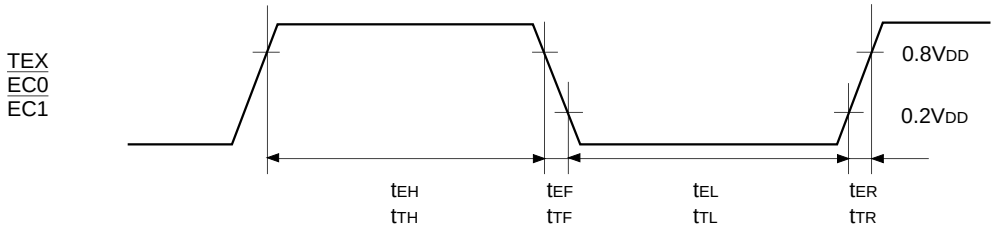


Fig. 3. Event count clock timing



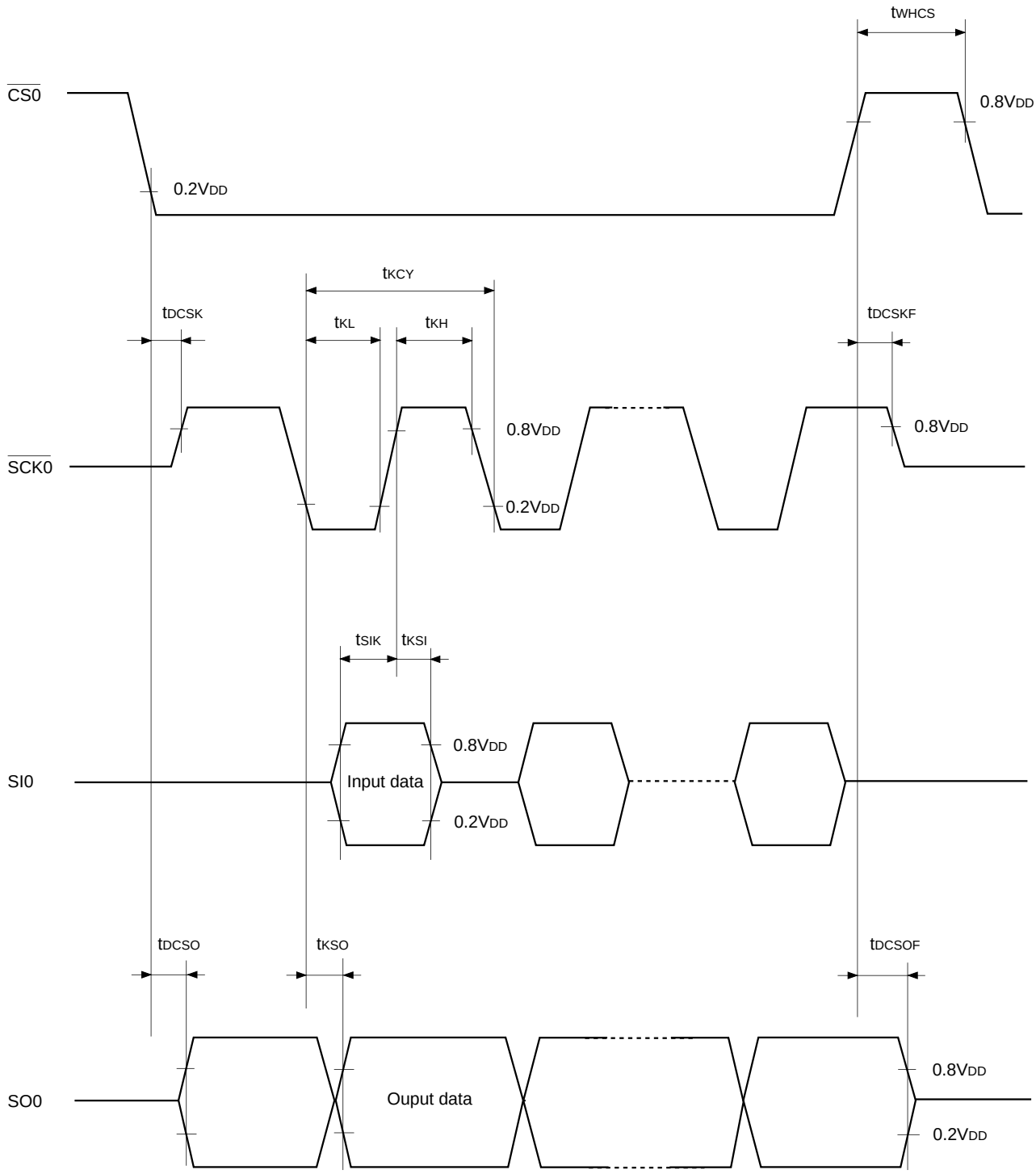
(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \uparrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: $00FE_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

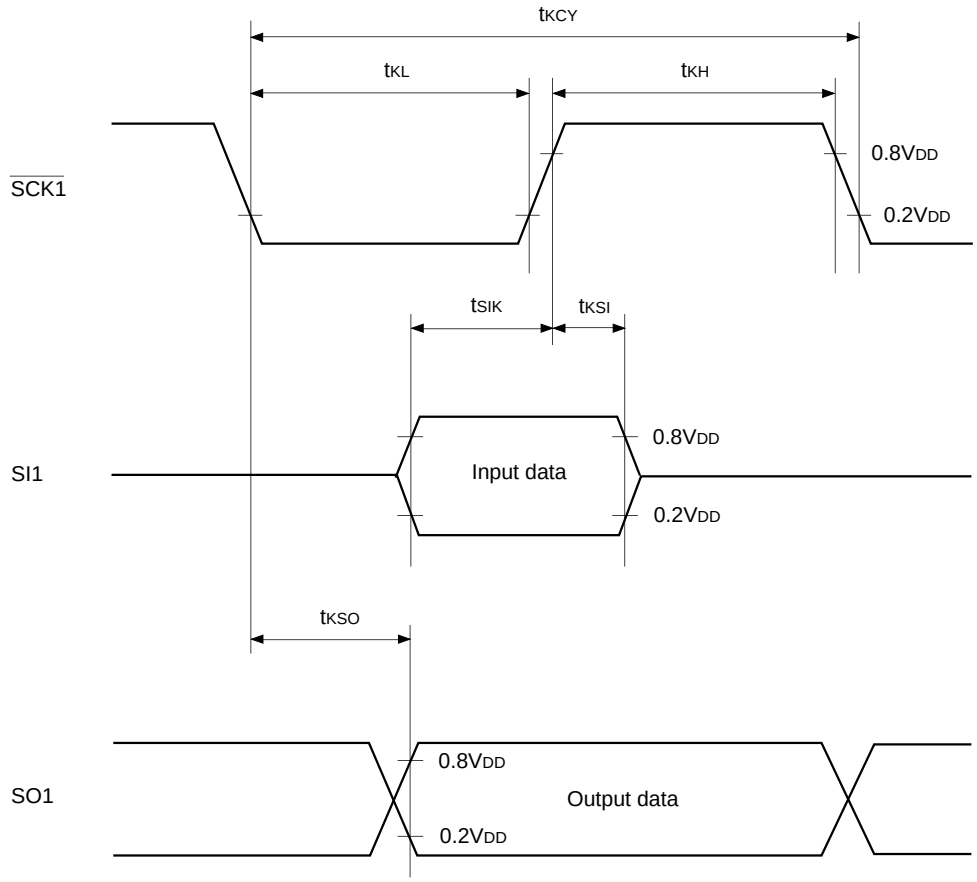


Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Ouput mode	16000/fc		ns
$\overline{SCK1}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Ouput mode	8000/fc – 50		ns
SI1 input set-up time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ ouput mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ ouput mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ ouput mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing

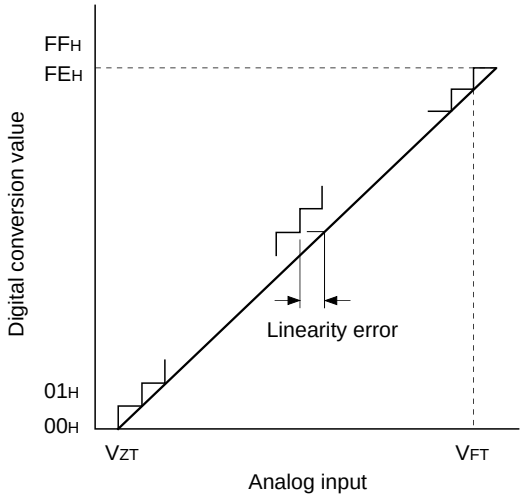


(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definition of A/D converter terms



*1) V_{ZT}: Value at which the digital transfer value changes from 00_H to 01_H and vice versa.

*2) V_{FT}: Value at which the digital transfer value changes from FE_H to FF_H and vice versa.

*3) f_{ADC} indicates the below values due to ADC operation clock selection (ADCS: Bit 6 of address $00F9_H$).

During PS2 selection, f_{ADC} = fc/2

During PS1 selection, f_{ADC} = fc

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 $\overline{NMI}$/INT3		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

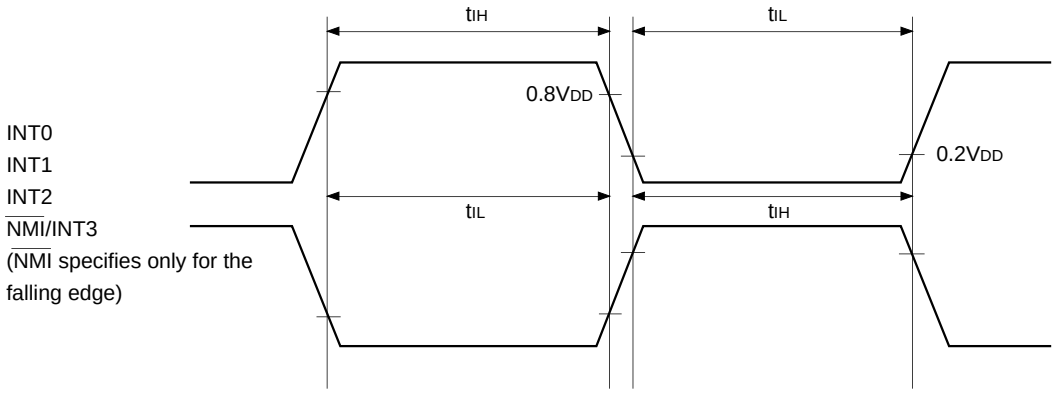
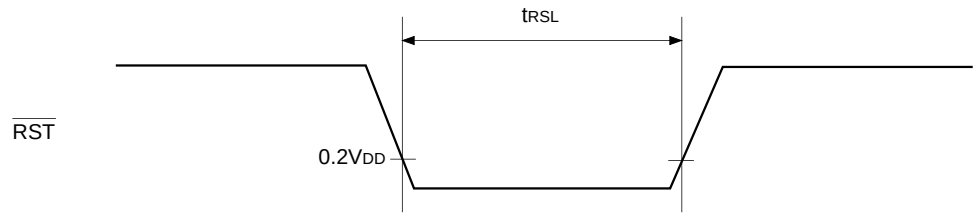


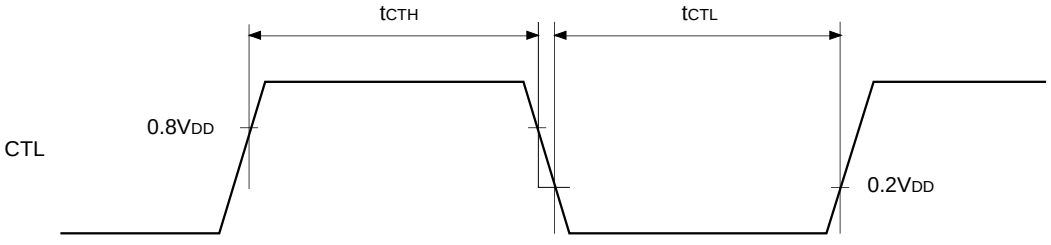
Fig. 8. $\overline{RST}$ input timing



(5) Others (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CLK input High, Low level width	t_{CTH} t_{CTL}	CTL	tsys = 2000/fc	tsys + 200		ns

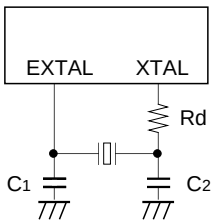
Fig. 9. Other timing



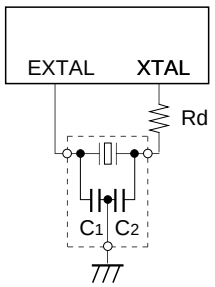
Appendix

Fig. 10. Recommended oscillation circuit

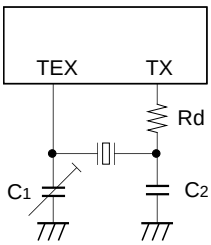
(i) Main clock



(ii) Main clock



(iii) Sub clock



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CO., LTD	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

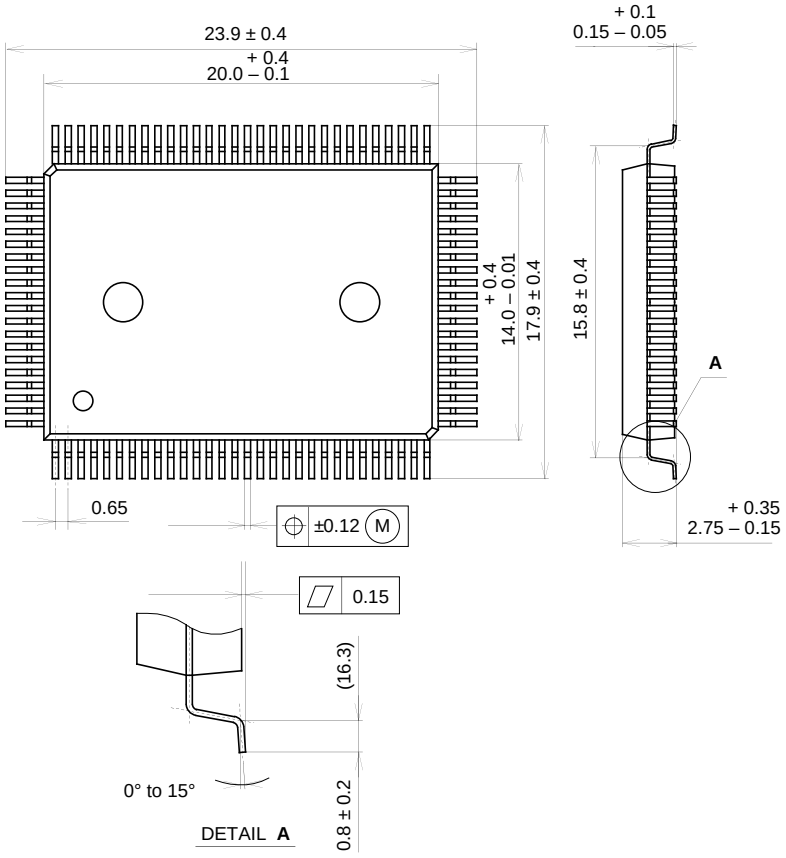
Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

Mask option table

Option	Mask product	CXP824P40Q-1-□□□
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	32K bytes/40K bytes	PROM 40K bytes
Reset pin pull-up resistance	Existent/non-existent	Existent
High voltage drive pin pull-up resistor	Existent/non-existent	Non-existent (S0/PD0 to S23/PI7) Existent (T0 to T15/S24)

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g