

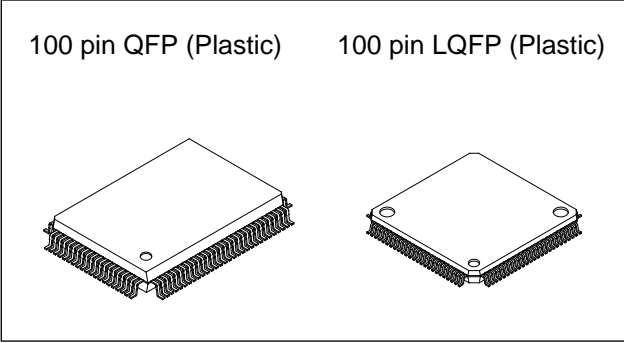
CMOS 8-bit Single Chip Microcomputer

Description

The CXP832P40A is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, capture timer counter, LCD controller/driver, remote control reception circuit and 14-bit PWM output besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

Also the CXP832P40A provides sleep/stop function which enables to lower power consumption.

The CXP832P40A is the PROM-incorporated version of the CXP83240A with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



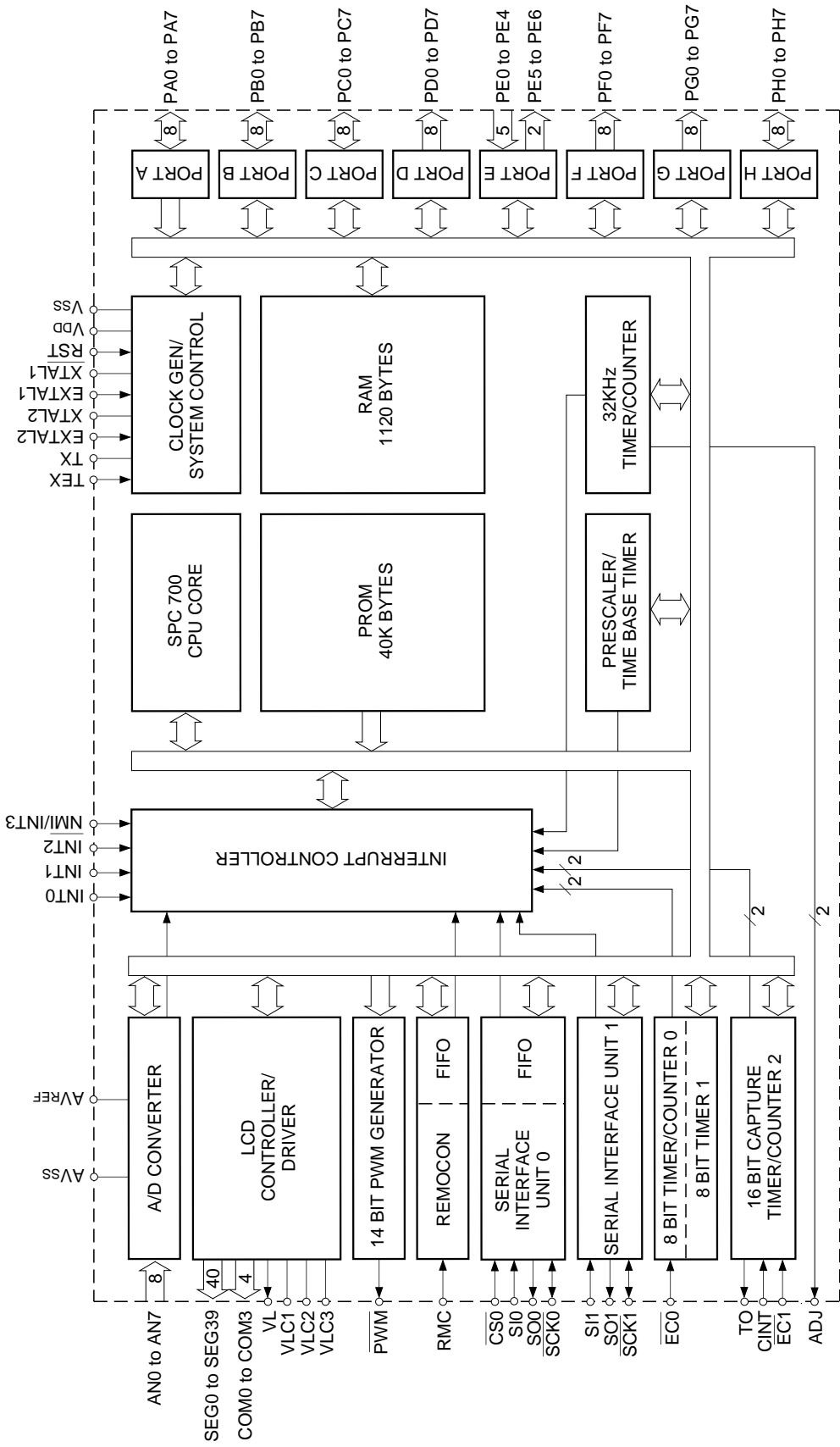
structure

Silicon gate CMOS IC

Features

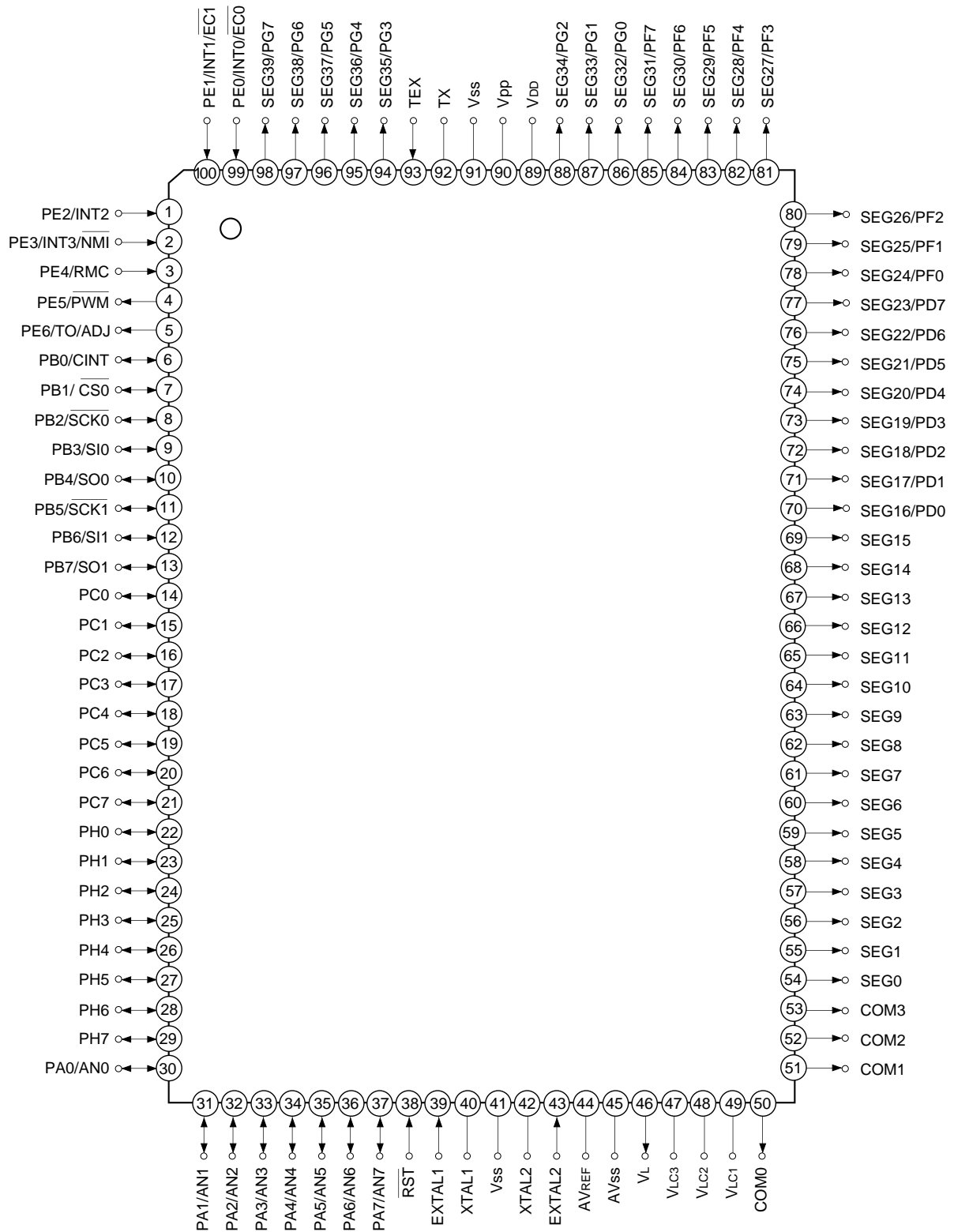
- Wide-range instruction system (213 instructions) to cover various types of data.
 - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
 8μs at 500kHz operation
 122μs at 32kHz operation
- Incorporated PROM capacity 40K bytes
- Incorporated RAM capacity 1120 bytes (includes LCD display data area)
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive approximation method
 (Conversion time of 32μs/10MHz)
 - Serial interface 8-bit, 8-stage FIFO incorporated
 (Auto transfer for 1 to 8 bytes), 1 channel
 - Timer 8-bit clock synchronized type, 1 channel
 8-bit timer, 8-bit timer/counter, 19-bit time base timer,
 16-bit capture timer/counter, 32kHz timer/counter
 - LCD controller/driver Maximum 160 segment display possible (during 1/4 duty)
 4 common output, 40 segment output
 Display method static, 1/2, 1/3, 1/4 duty
 Bias method 1/2, 1/3 bias
 - Remote control reception circuit 8-bit pulse measurement counter with on-chip, 6-stage FIFO
 - PWM output circuit 14 bits, 1 channel
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP/LQFP

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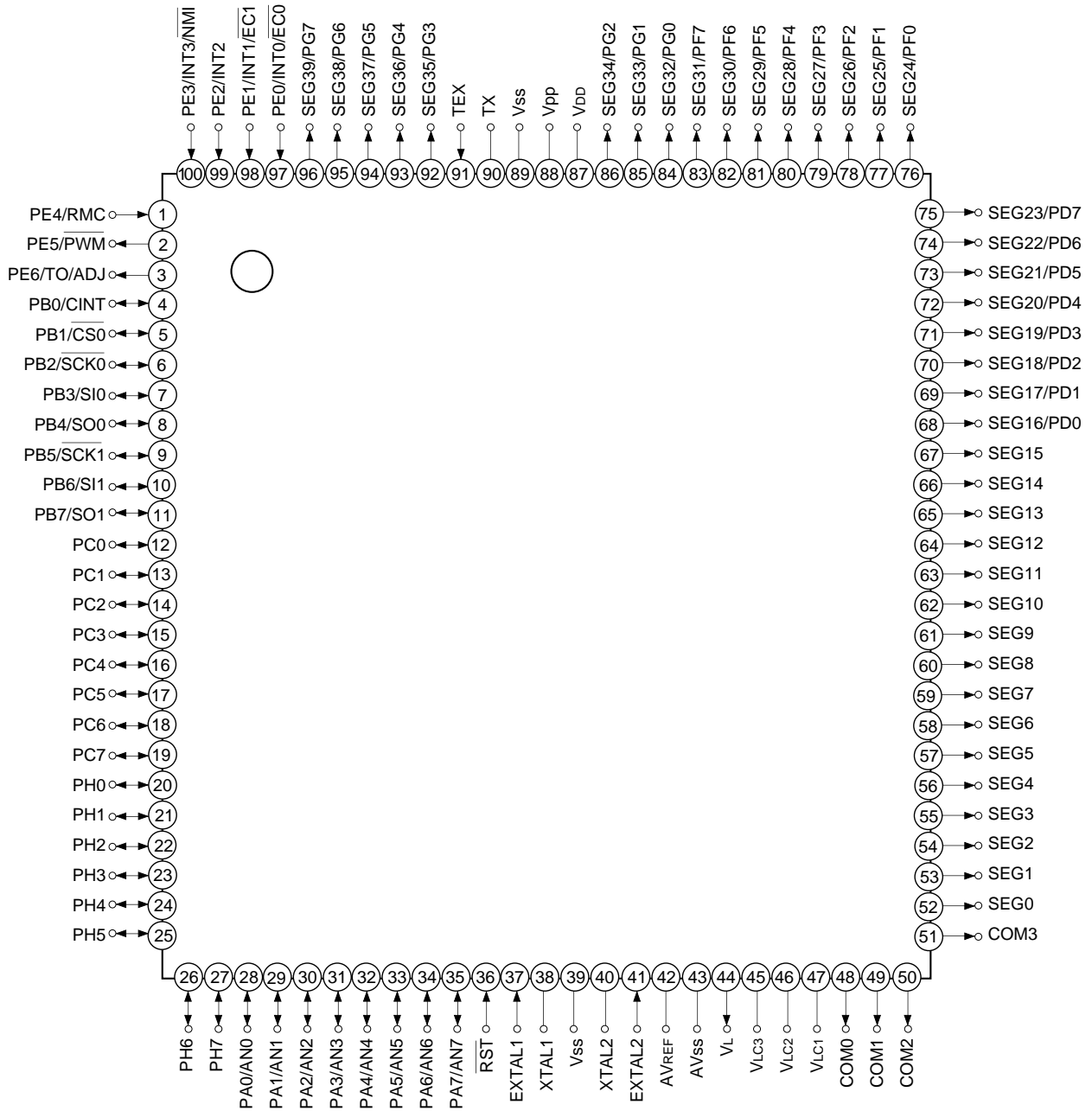
Block Diagram

Pin Assignment (Top View) (QFP package)



- Note)**
1. Vpp (Pin 90) is always connected to VDD.
 2. Vss (Pin 41 and 91) are both connected to GND.

Pin Assignment (Top View) (LQFP package)



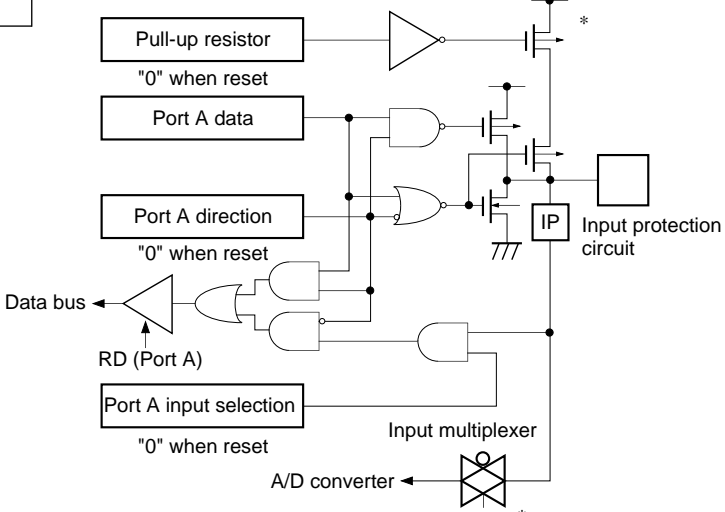
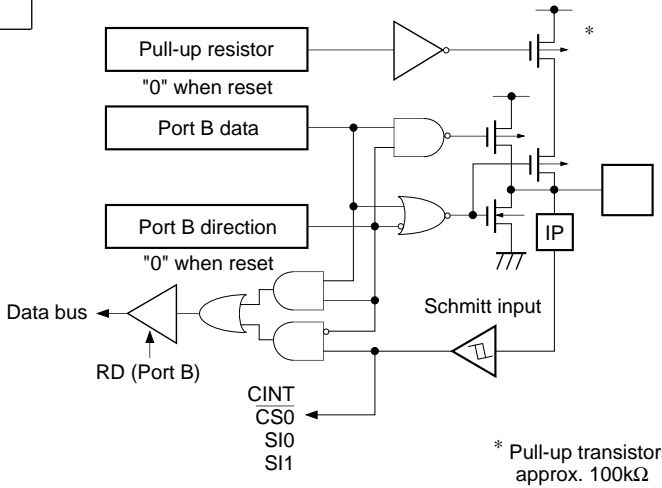
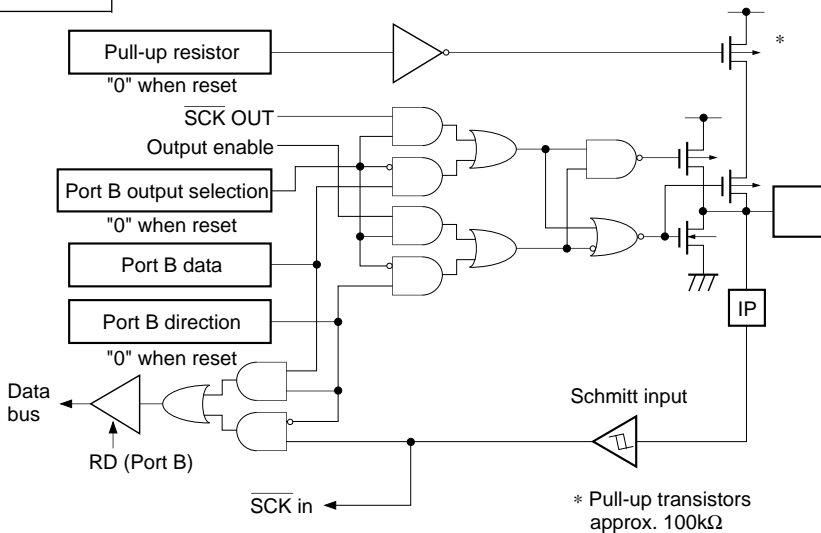
- Note)**
1. Vpp (Pin 88) is always connected to V_{DD}.
 2. Vss (Pin 39 and 89) are both connected to GND.

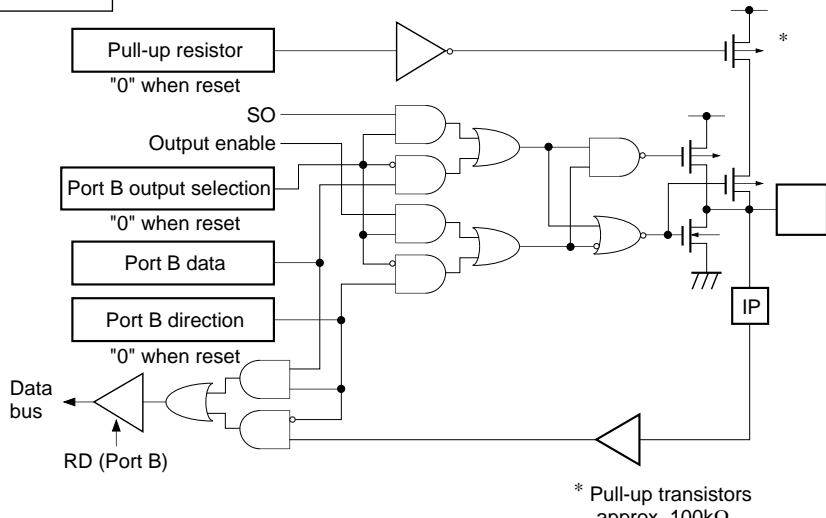
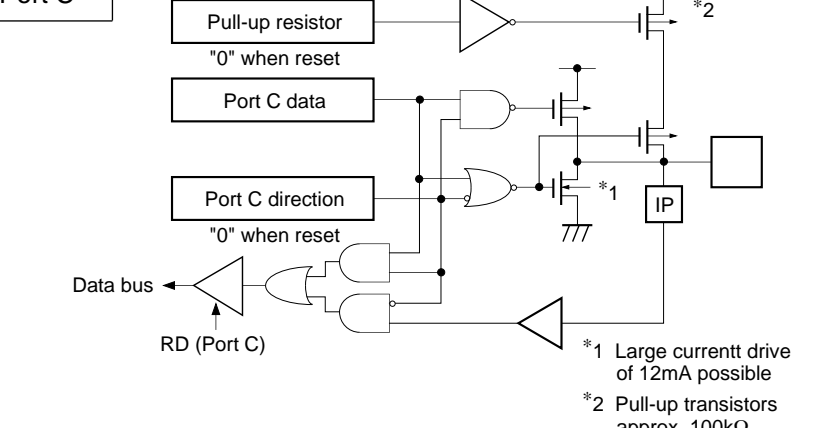
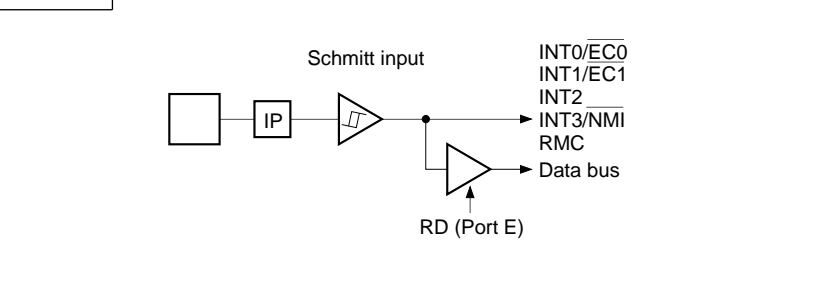
Pin Description

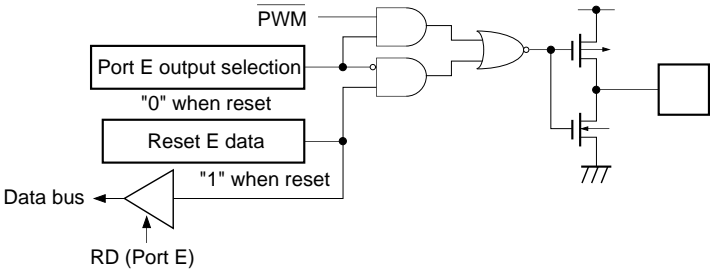
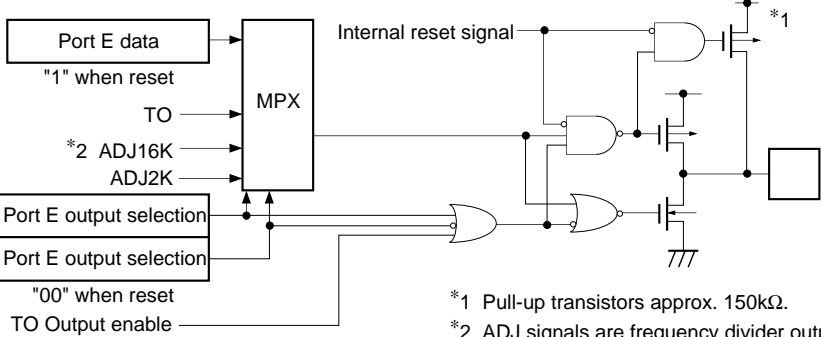
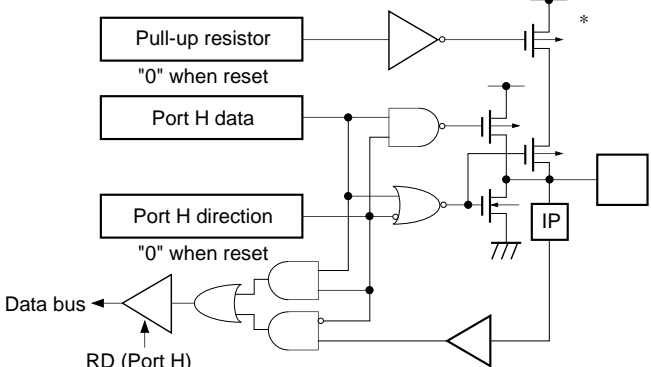
Symbol	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.	
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/input		Serial data input (CH1).	
PB7/SO1	I/O/Output		Serial data output (CH1).	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a single bit unit. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		
$\overline{\text{PE}}_0/\text{INT}_0/\text{EC}_0$	Input/Input/Input	(Port E) 7-bit port. lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for timer/counter. (2 pins)	
$\overline{\text{PE}}_1/\text{INT}_1/\text{EC}_1$	Input/Input/Input		External interruption request inputs. (4 pins)	Non-maskable interruption request input.
PE2/INT2	Input/Input			
$\overline{\text{PE}}_3/\text{INT}_3/\text{NMI}$	Input/Input/Input		Remote control reception circuit input.	
PE4/RMC	Input/Input		14-bit PWM output.	
PE5/ $\overline{\text{PWM}}$	Output/Output		Rectangular wave output for 16-bit timer/counter (duty output 50%).	Output for 32kHz oscillation frequency division.
PE6/TO/ADJ	Output/Output/Output			
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		

Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal output.
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
PG0/SEG32 to PG7/SEG39	Output/Output	(port G) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output.	
COM0 to COM3	Output	LCD common signal output.	
V _{LC1} to V _{LC3}		LCD bias power supply.	
V _L	Output	Control pin to cut off the current flowing to external LCD bias resistor during standby.	
EXTAL1	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL1; opposite phase clock should be input to XTAL1. System clock oscillation of EXTAL1 and XTAL1 is used for normal operation mode (Max. 10MHz).	
XTAL1			
EXTAL2	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL2; opposite phase clock should be input to XTAL2. System clock oscillation of EXTAL2 and XTAL2 is used for sub clock mode (Typ. 500kHz).	
XTAL2			
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32.768kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active system reset.	
V _{pp}		Positive power supply for built-in PROM writing. Under normal operating conditions, connect to V _{DD} .	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		Positive power supply.	
V _{SS}		GND. Two V _{SS} are connected to GND.	

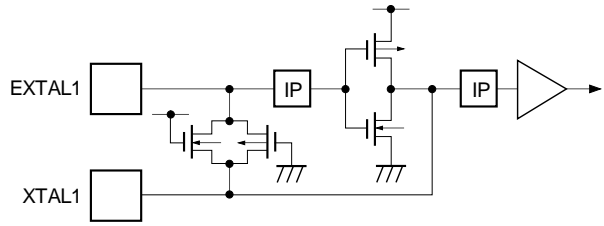
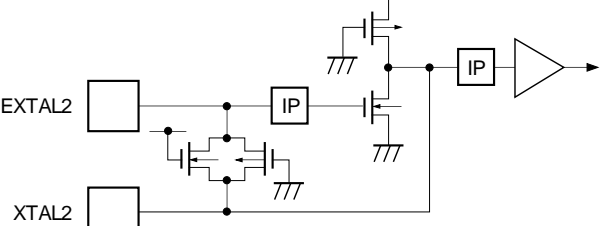
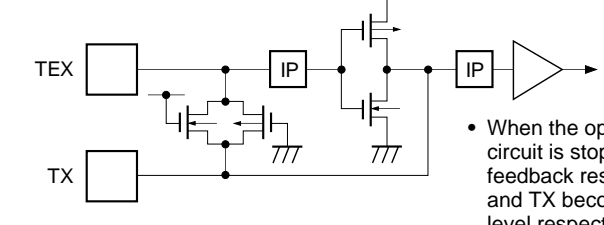
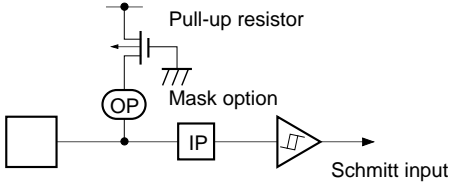
I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 Large current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PE0/INT0/$\overline{EC0}$ PE1/INT1/$\overline{EC1}$ PE2/INT2 PE3/INT3/NMI PE4/RMC</p> <p>5 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>

P in	Circuit format	When reset
<p>PE5/PWM</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE6/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>*1 Pull-up transistors approx. 150kΩ. *2 ADJ signals are frequency divider outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p>	<p>High level (High level with 150kΩ resistor when reset)</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format		When reset
<p>PD0 to PD7 PF0 to PF7 PG0 to PG7</p> <p>24 pins</p>	<p>Port D</p> <p>Port F</p> <p>Port G</p>		<p>Segment output (V_{DD} level)</p>
<p>SEG0 to SEG15</p> <p>16 pins</p>	<p>Segment</p>		<p>V_{DD} level</p>
<p>COM0 to COM3</p> <p>4 pins</p>	<p>Common</p>		<p>V_{DD} level</p>
<p>V_L</p> <p>1 pin</p>			<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL1 XTAL1</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL1 becomes "High" level. 	<p>Oscillation</p>
<p>EXTAL2 XTAL2</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL2 becomes "High" level. 	<p>EXTAL2 Hi-Z XTAL2 High level</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed and TEX and TX become "Low" level and "High" level respectively. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Iem	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	V _{pp}	−0.3 to +13.0	V	Incorporated PROM
	AV _{SS}	−0.3 to +0.3	V	
LCD bias voltage	V _{LC1} , V _{LC2} , V _{LC3}	−0.3 to +7.0*1	V	
Input voltage	V _{IN}	−0.3 to +7.0*1	V	
Output voltage	V _{OUT}	−0.3 to +7.0*1	V	
High level output current	I _{OH}	−5	mA	Output per pin
High level total output current	∑I _{OH}	−50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding large current outputs
	I _{OLC}	20	mA	Value per pin*2 for large current outputs
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	−10 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package
		380		LQFP package

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode guaranteed operation range* ¹
		3.5	5.5		Low-speed mode guaranteed operation range* ¹
		3.0	5.5		Guaranteed operation range during EXTAL2 clock (sub clock mode)
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	V _{pp}	V _{pp} = V _{DD}		V	* ⁶
LCD bias voltage	V _{LC1}	V _{SS}	V _{DD}	V	LCD power supply range* ⁵
	V _{LC2}				
	V _{LC3}				
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ³
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ³
	V _{ILEX}	-0.3	0.4	V	EXTAL* ⁴
Operating temperature	Topr	-10	+75	°C	

*¹ During EXTAL1 clock (main clock mode), high-speed mode is 1/2 frequency division clock selection; low-speed mode is 1/16 frequency division clock selection.

*² Value for each pin of normal input ports (PA, PB4, PB7, PC and PH).

*³ Value of the following pins; $\overline{\text{RST}}$, $\overline{\text{CINT}}$, $\overline{\text{CS0}}$, $\overline{\text{SI0}}$, $\overline{\text{SI1}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{NMI/INT3}}$, and $\overline{\text{RMC}}$.

*⁴ Specifies only during external clock input.

*⁵ Optimal values are determined by LCD used.

*⁶ V_{pp} and V_{DD} should be set to same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA, PB, PC, PD*1, PE5, PE6	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PF to PG*1 VL (VOL only)	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC	VDD = 4.5V, IOL = 12.0mA			1.5	V
Input current	IIHE1	EXTAL1	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IILE1		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IIHE2	EXTAL2	VDD = 5.5V, VIH = 5.5V	0.3		30	μA
	IILE2		VDD = 5.5V, VIL = 0.4V	-0.3		-30	μA
	IIHT	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
	IILT		VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IILR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
	IIH	PA to PC*3, PH*3	VDD = 4.5V, VIH = 4.0V	-3.33			μA
IIL	VDD = 5.5V, VIL = 0.4V				-50	μA	
I/O leakage current	IIZ	PE0 to PE4, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Common output impedance	R _{COM}	COM0 to COM3	VDD = 5V, VLC1 = 3.75V, VLC2 = 2.5V, VLC3 = 1.25V		3	5	kΩ
Segment output impedance	R _{SEG}	SEG0 to SEG15 SEG16 to SEG39*1			5	15	kΩ
Supply current*4	IDD1	VDD	High-speed mode operation (1/2 frequency division clock)		20	45	mA
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)				
			VDD = 3.5V, 500kHz crystal oscillation (C1 = C2 = 22pF)				
	IDD2		VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		0.6	1.3	mA
	IDD3		SLEEP mode				
	IDD1		VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)		1.5	8	mA
	IDD2		VDD = 3.5V, 500kHz crystal oscillation (C1 = C2 = 22pF)		0.5	1.0	mA
IDD3	VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		9	30	μA		
IDDSS	STOP mode VDD = 5.5V, 10MHz, 500kHz crystal oscillation and termination of 32kHz oscillation				30	μA	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C _{IN}	Pins other than PB7, PE5, PE6 V _{LC1} to V _{LC3} COM0 to COM3 SEG0 to SEG15 PD0/SEG16 to PD7/SEG23 PF0/SEG24 to PF7/SEG31 PG0/SEG32 to PG7/SEG39 AV _{REF} , AV _{SS} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PG0/SEG32 to PG7/SEG39, PD, PF and PG are the case when the common pin is selected as port; SEG16 to SEG39 are when the common pin is selected as segment output.

*2 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 PA to PC, and PH specify the input current when a pull-up resistor has been selected; leakage current when no resistor has been selected. (PE0 to PE4 specify the leakage current.)

*4 When all output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL1 EXTAL1	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	tXL, tXH	EXTAL1	Fig. 1, Fig. 2 external clock drive	37.5			ns
System clock input rise and fall time	tCR, tCF	EXTAL1	Fig. 1, Fig. 2 external clock drive			200	ns
System clock frequency	fc	XTAL2 EXTAL2	VDD = 3.0 to 5.5V Fig. 1, Fig. 2	0.3	0.5	0.7	MHz
System clock input pulse width	tXL, tXH	EXTAL2	VDD = 3.0 to 5.5V Fig. 1, Fig. 2 external clock drive	450			ns
System clock input rise and fall time	tCR, tCF	EXTAL2	VDD = 3.0 to 5.5V Fig. 1, Fig. 2 external clock drive			200	ns
Event count input clock pulse width	tEH, tEL	$\overline{EC0}$ $\overline{EC1}$	Fig. 3	t _{sys} + 50*			ns
Event count input clock rise and fall time	tER, tEF	$\overline{EC0}$ $\overline{EC1}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	tTL, tTH	TEX	Fig. 3	10			μs
Event count input clock rise and fall time	tTR, tTF	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11").

Fig. 1. Clock timing

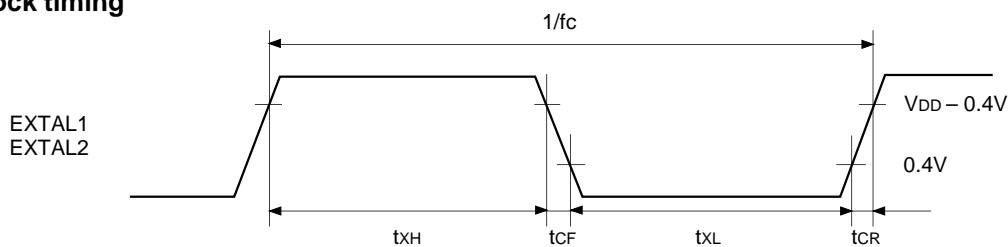


Fig. 2. Clock applied conditions

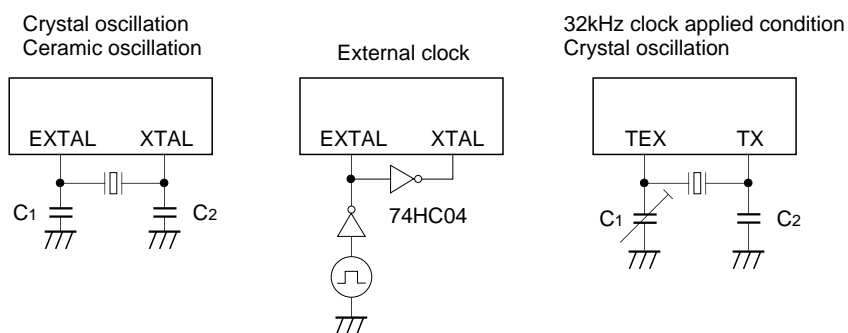
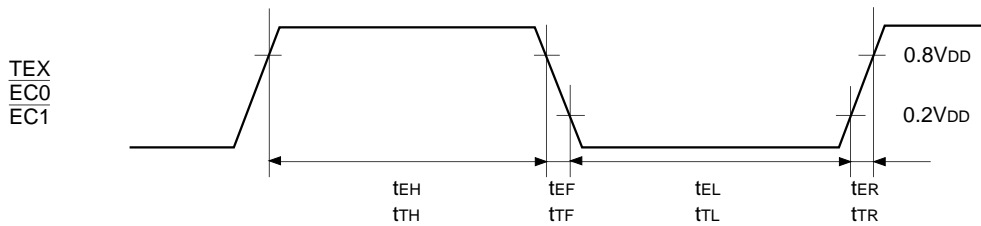


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

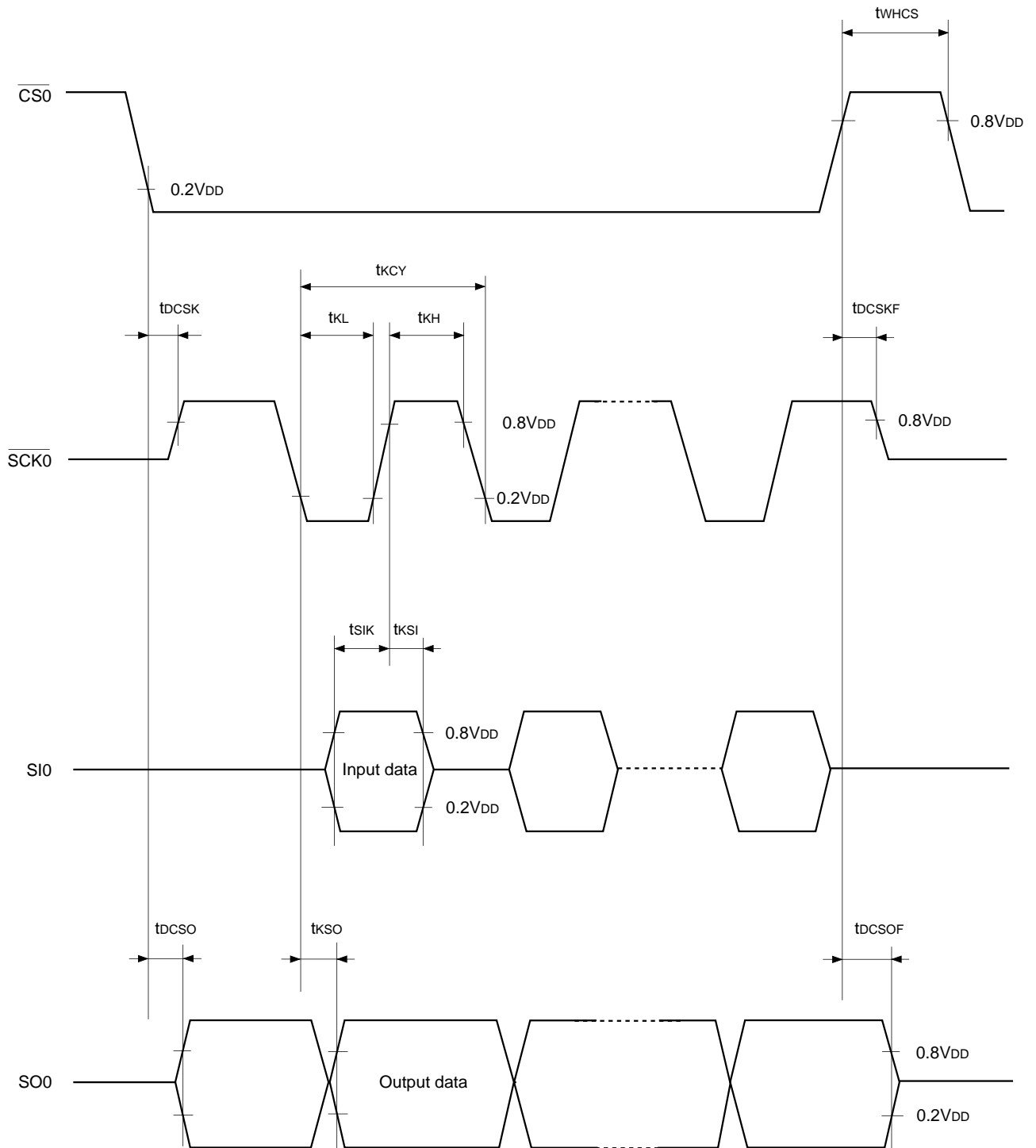
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK0}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/ f_c (upper two bits = "00"), 4000/ f_c (upper two bits = "01"), 16000/ f_c (upper two bits = "11")

Note 2) The load condition for the $\overline{\text{SCK0}}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



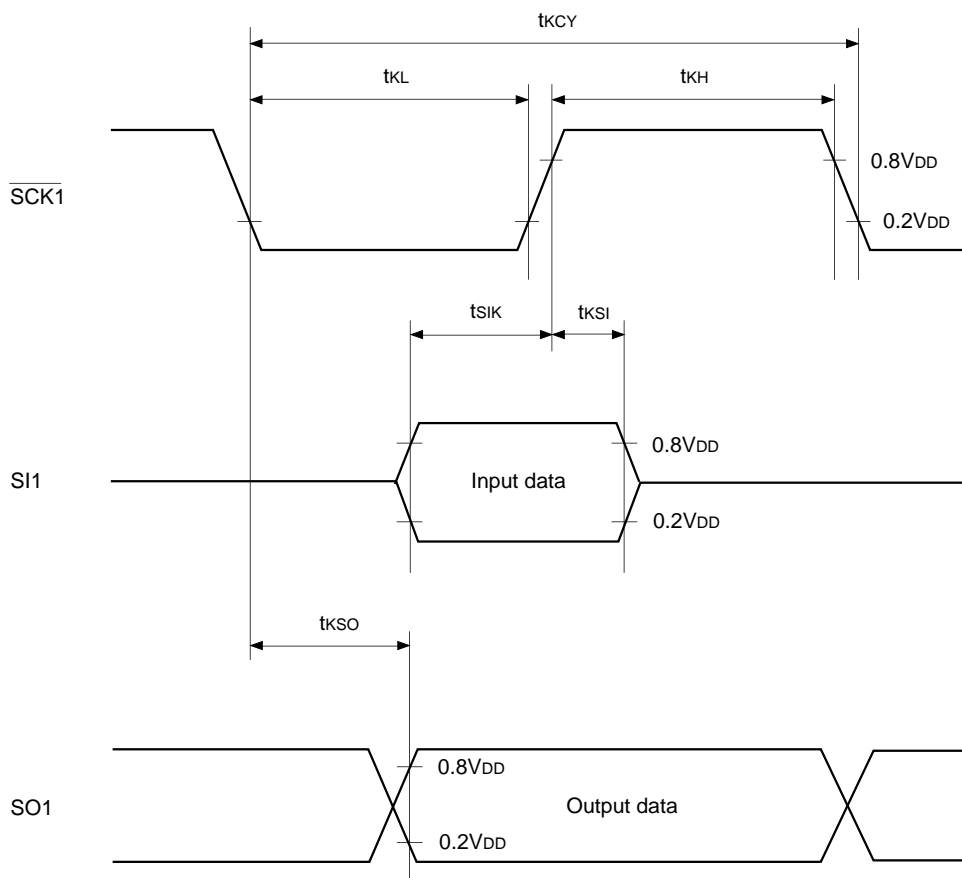
Serial Transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH}	$\overline{\text{SCK1}}$	input mode	400		ns
	t_{KL}		Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ \uparrow)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ \uparrow)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ $\downarrow \rightarrow$ SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer CH1 timing

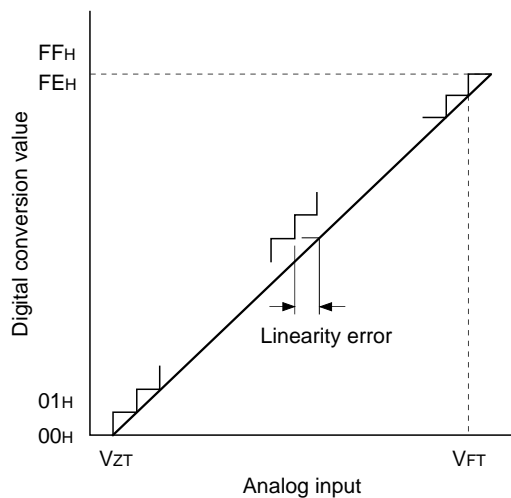


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						± 3	LSB
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-10	10	70	mV
Full-scale transition voltage	V_{FT}^{*2}			4910	4970	5030	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definition of A/D converter terms



- *1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- *2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- *3 f_{ADC} indicates the below values due to the Bit 6 (CKS) of A/D control register (address: 00F9H) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control register (address: 00FFH).

PCK1, PCK0	CKS	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 $\overline{\text{NMI/INT3}}$		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 7. Interruption input timing

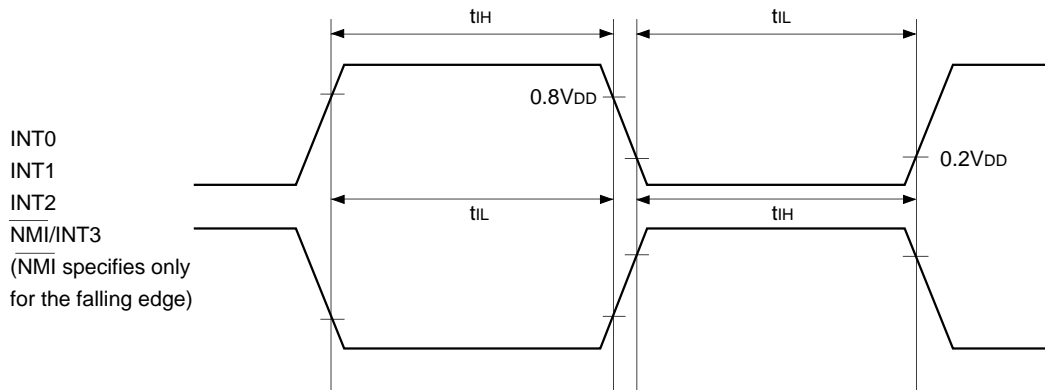
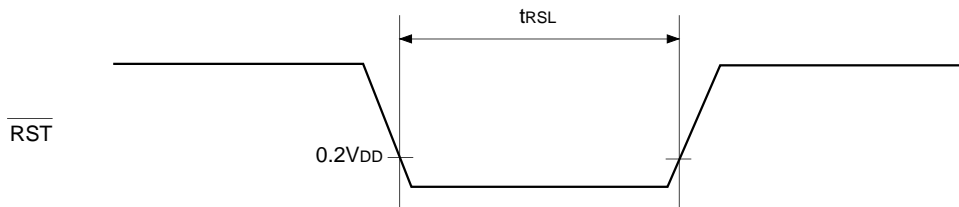
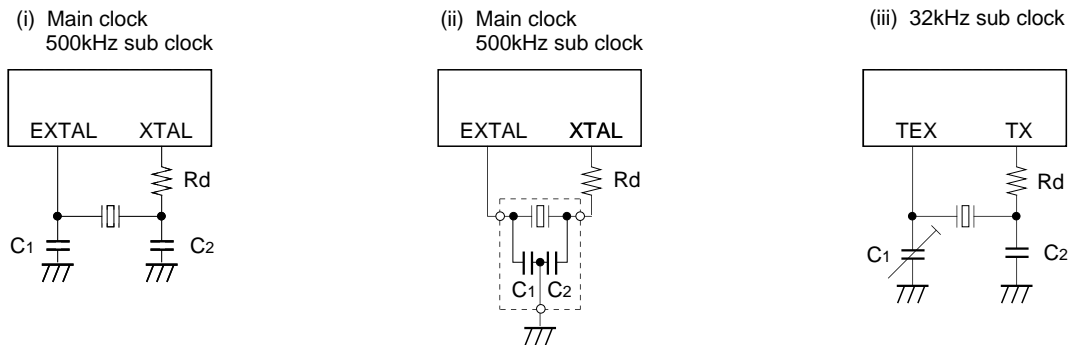


Fig. 8. $\overline{\text{RST}}$ input timing



Appendix

Fig. 9. SPC700 series recommended oscillation circuit



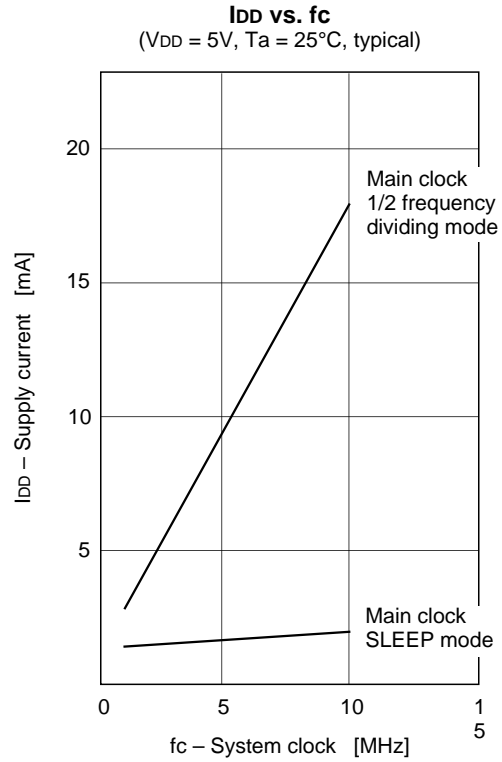
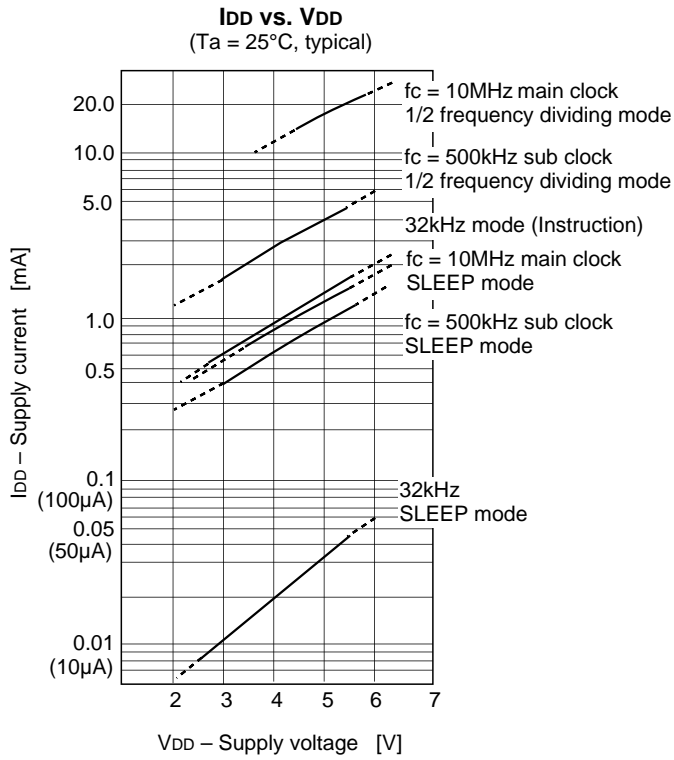
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MG	8.00				
	CSA10.0MT	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	15	15	2.2k	(i)
		8.00				
		10.00			470	
KINSEKI LTD.	HC-49/U (-S)	4.19	22	22	560	
		8.00	18	18	0	
		10.00				

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Selection Guide

Option item	Mask product				Incorporated PROM product	
Product name	CXP83120A	CXP83124A	CXP83232A	CXP83240A	CXP832P40AQ-1-□□□	CXP832P40AR-1-□□□
Package	100-pin plastic QFP/LQFP				100-pin plastic QFP	100-pin plastic LQFP
ROM capacitance	20K bytes	24K bytes	32K bytes	40K bytes	PROM 40K bytes	
Reset pin pull-up resistor	Existent/Non-existent				Existent	Existent

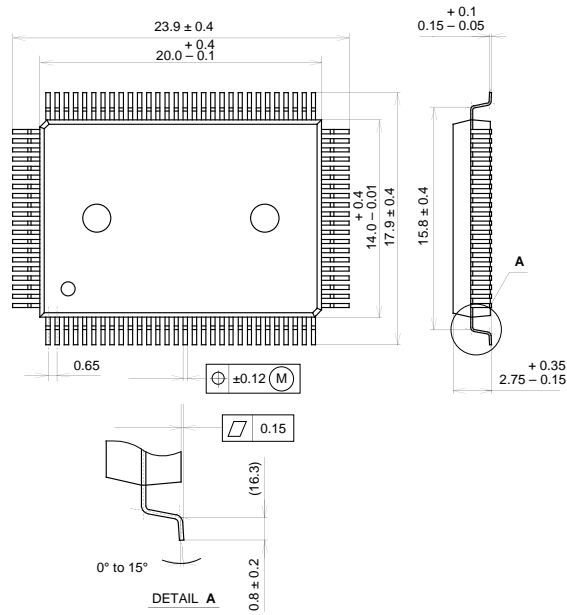
Characteristics Curves



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

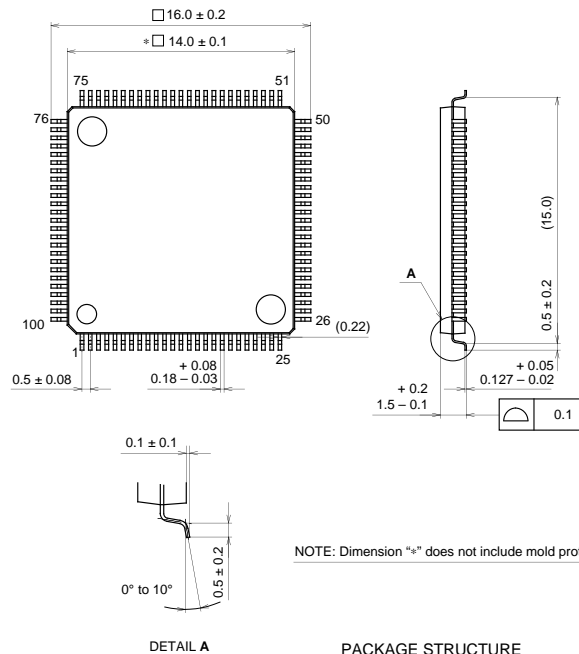


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	+QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	+QFP100-P-1414-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____