SONY

CXP84332M/84340M

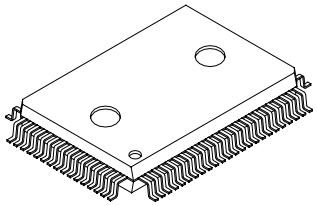
CMOS 8-bit Single Chip Microcomputer

Description

CXP84332M/84340M is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, remote control reception circuit, PWM output, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84332M/84340M also provides a sleep/stop function that enables lower power consumption.

80 pin QFP (Plastic)



Features

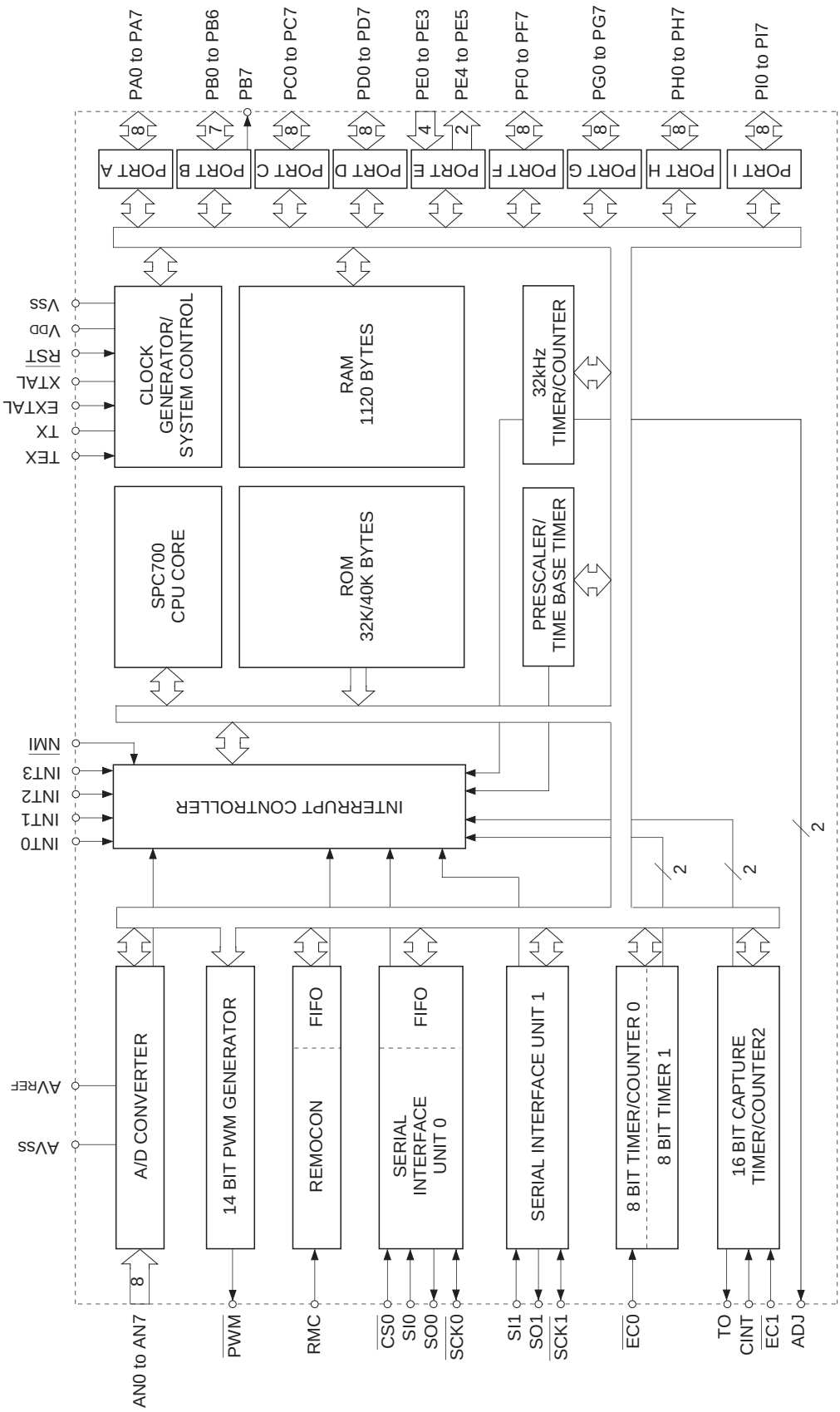
- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 200ns at 20MHz operation; 122µs at 32kHz operation
- Incorporated ROM capacity — 32K bytes (CXP84332M); 40K bytes (CXP84340M)
- Incorporated RAM capacity — 1120 bytes
- Peripheral functions
  - — A/D converter — 8 bits, 8 channels, successive approximation method (Conversion time of 16µs/20MHz)
  - — Serial interface — 8-bit, 8-stage FIFO incorporated (Auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock synchronization, 1 channel
  - — Timers — 8-bit timer; 8-bit timer/counter; 19-bit time base timer; 16-bit capture timer/counter; 32kHz timer/counter
  - — Remote control reception circuit — 8-bit pulse measuring counter, 6-stage FIFO
  - — PWM output — 14 bits, 1 channel
- Interruption — 15 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 80-pin plastic QFP
- Piggyback/evaluation chip — CXP84300 80-pin ceramic QFP

Structure

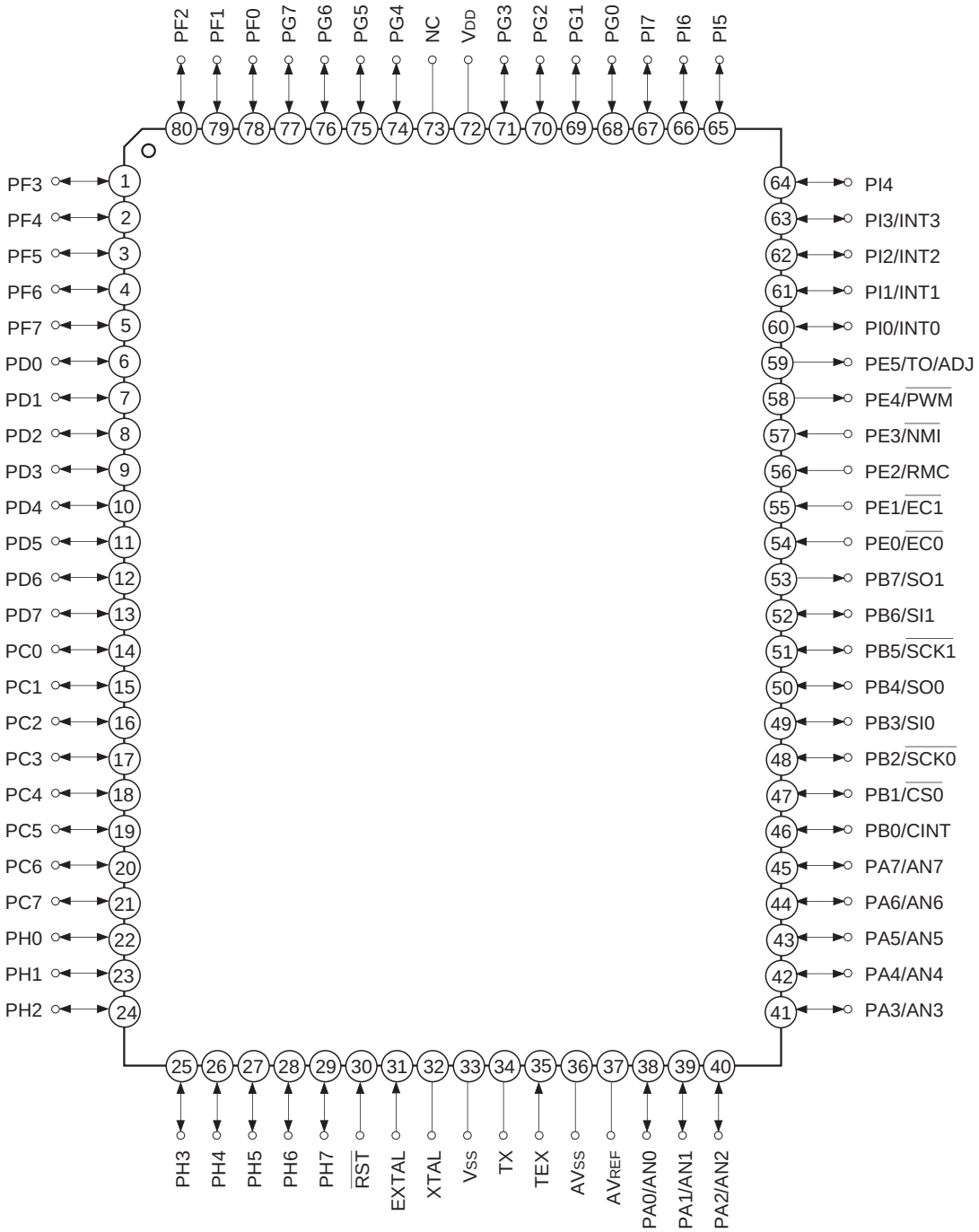
Silicon gate CMOS IC

E95X06-ST

Block Diagram



Pin Assignment (Top View)



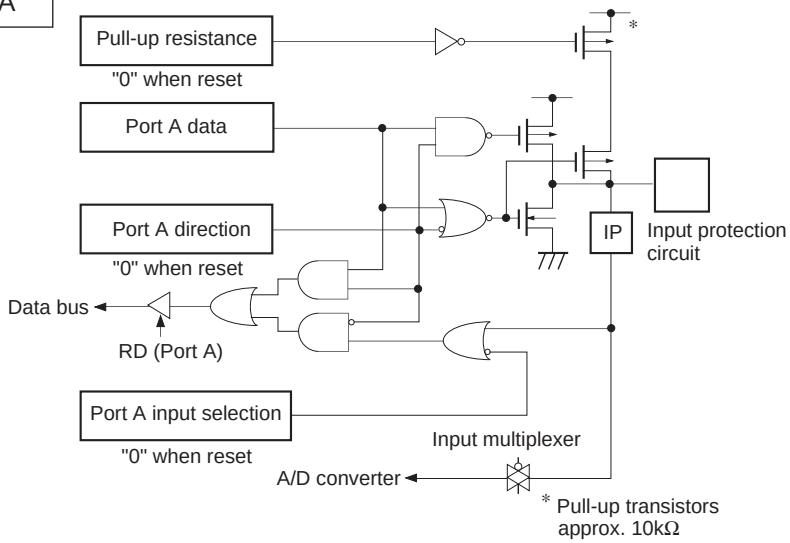
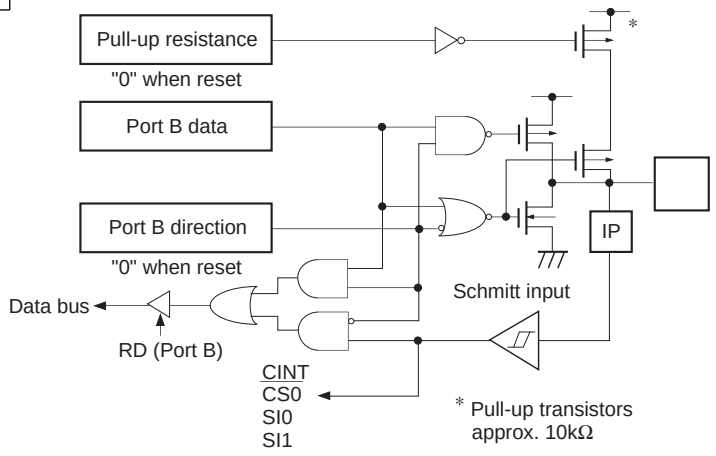
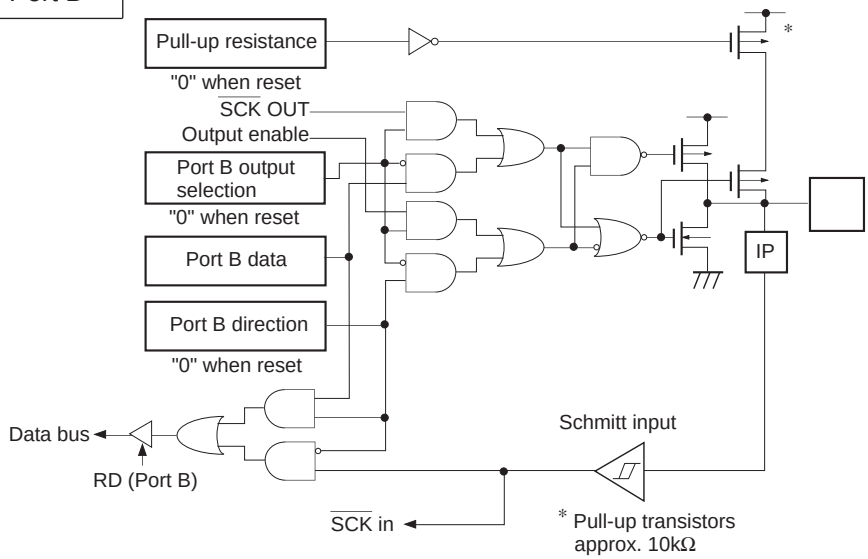
Note) NC (Pin 73) must be connected to V_{DD}.

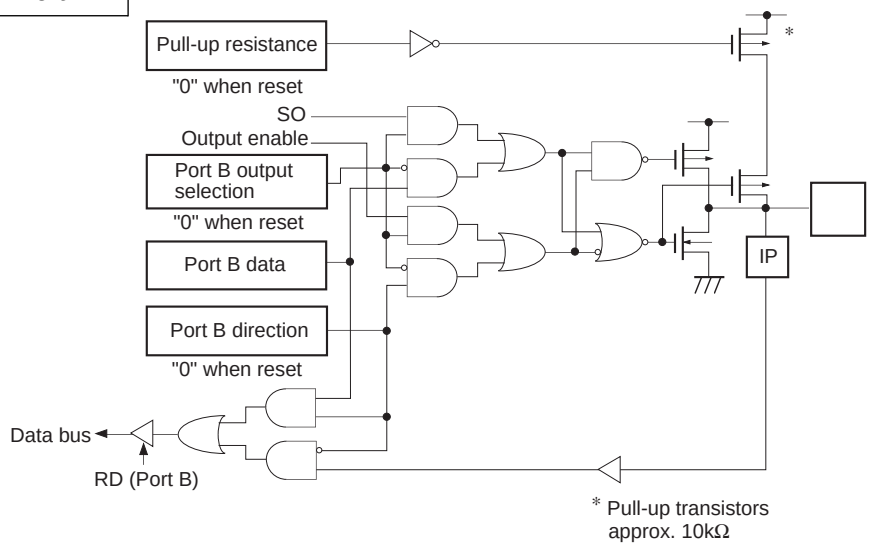
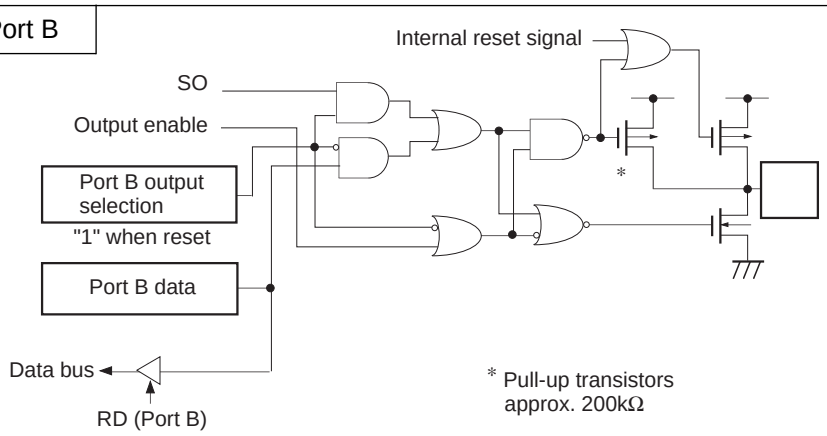
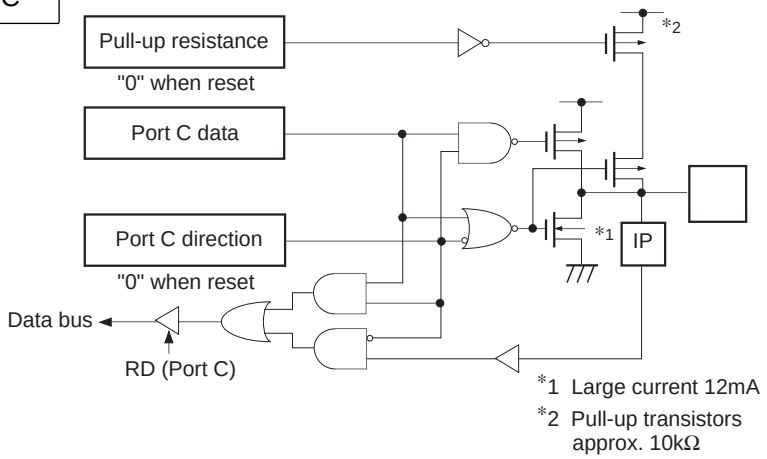
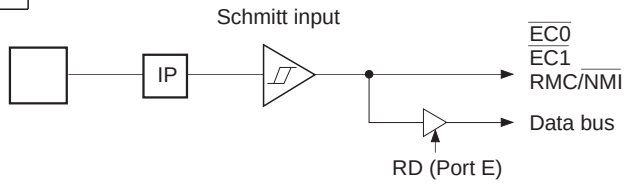
Pin Description

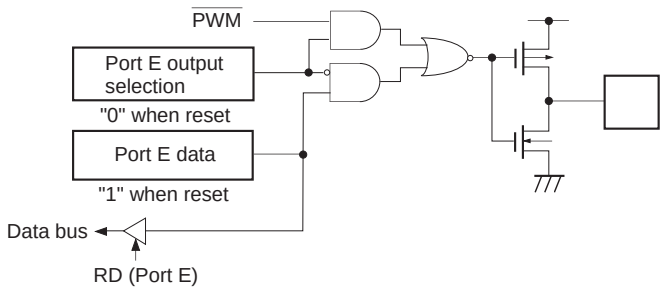
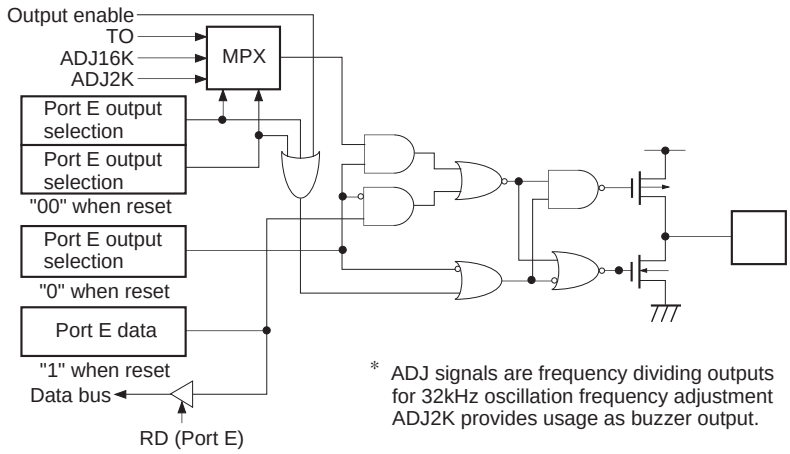
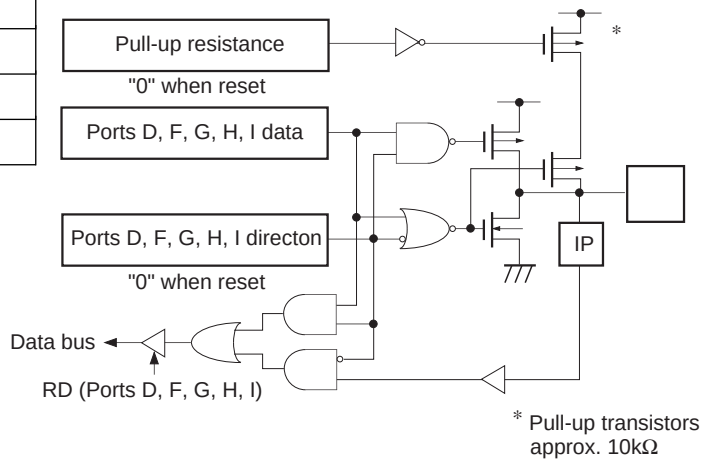
Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Lower 7-bit I/O port in which I/O can be set in a unit of single bits. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/$\overline{EC0}$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/$\overline{EC1}$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/$\overline{NMI}$	Input/Input		Non-maskable interruption request input.
PE4/$\overline{PWM}$	Output/Output		14-bit PWM output.
PE5/TO/ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter and output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

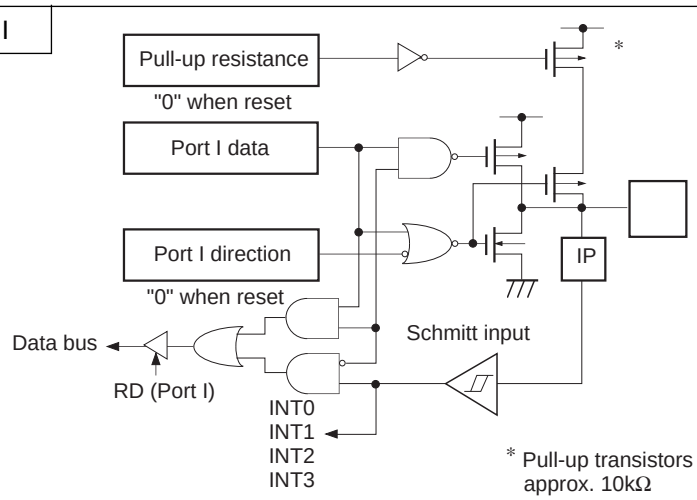
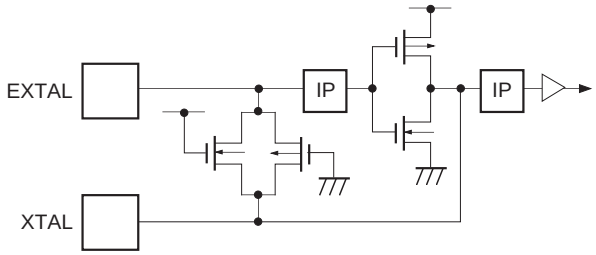
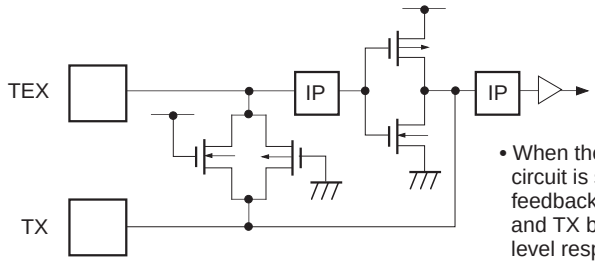
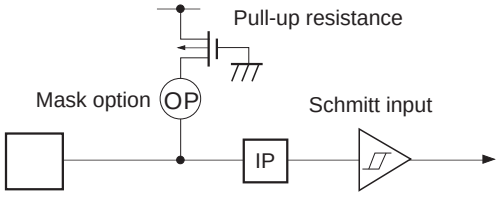
Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (4 pins)
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillaton circuit. For usage as event counter, input to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V_{DD}.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
V_{DD}		Vcc supply.	
Vss		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/$\overline{\text{CINT}}$ PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{\text{SCK0}}$ PB5/SCK1 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	Port B 	Hi-Z
PB7/SO1 1 pin	Port B 	High level with approx. 200kΩ resistor when reset
PC0 to PC7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC0}$ PE1/EC1 PE2/RMC PE3/$\overline{NMI}$ 4 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE4/$\overline{\text{PWM}}$ 1 pin	Port E 	High level
PE5/TO/ADJ 1 pin	Port E 	High level
PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7 36 pins	Port D Port F Port G Port H Port I 	Hi-Z

Pin	Circuit format	When reset
PI0/INT0 to PI3/INT3 4 pins	Port I 	Hi-Z
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become “Low” level and “High” level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output per pin
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Value per pin, excluding large current outputs
	I_{OLC}	20	mA	Value per pin*2 for large current outputs
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1) V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2) The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for high speed mode*1
		3.5	5.5		Guaranteed operation range for low speed mode*1
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*4
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*2
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL*4
Operating temperature	Topr	–20	+75	°C	

*1) High speed mode is 1/2 frequency dividing clock selection; low-speed mode is 1/16 frequency dividing clock selection.

*2) Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF to PH, PI4 to PI7).

*3) Value of the following pins: $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$, $\overline{EC1}$, RMC, $\overline{NMI}$, INT0, INT1, INT2, INT3.

*4) Specifies only during external clock input.

Electrical Characteristics

DC Characteristics (Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA to PD, PE4, PE5, PF to PI	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–1.5		–400	µA
	I_{IL}	PA to PD*2, PF to PI*2				–2.0	mA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–10			µA
I/O leakage current	I_{IZ}	PE0 to PE3, $\overline{RST}$*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Power supply current*3	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency dividing clock) V_{DD} = 5.5V, 20MHz crystal oscillation (C_1 = C_2 = 15pF)		32	52	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		38	100	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 20MHz crystal oscillation (C_1 = C_2 = 15pF)		1.4	10	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, termination of 20MHz and 32kHz crystal oscillation			10	µA
Input capacity	C_{IN}	PA, PB0 to PB6, PC, PD, PE0 to PE3, PF to PI, EXTAL, XTAL, TEX, TX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1) $\overline{RST}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2) PA to PD, and PF to PI pins specifie the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*3) When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		20	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	23.0			ns
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$ EC1	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC0}$ EC1	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise time, fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1) tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FE$_H$).
tsys (ns) = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Fig. 1. Clock timing

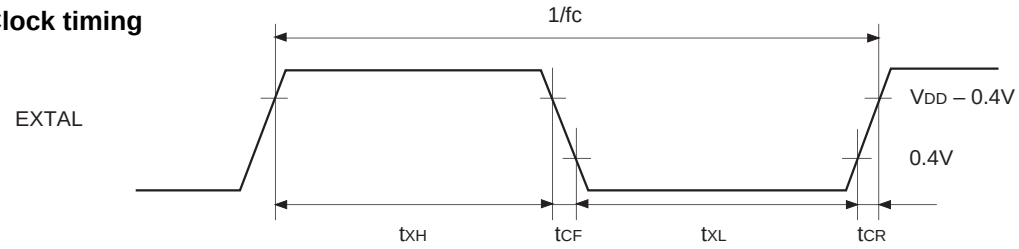


Fig. 2. Clock applied conditions

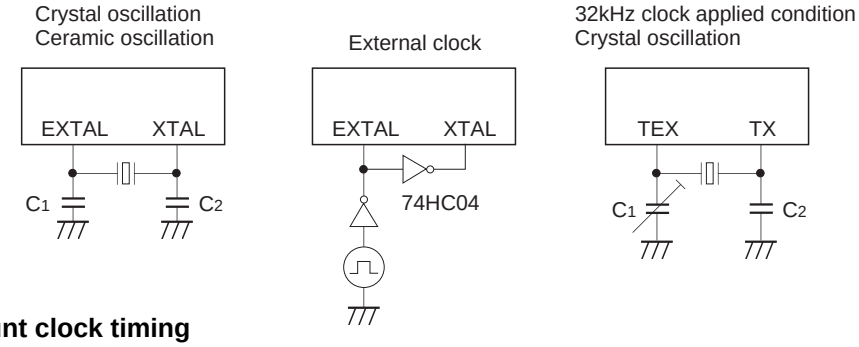
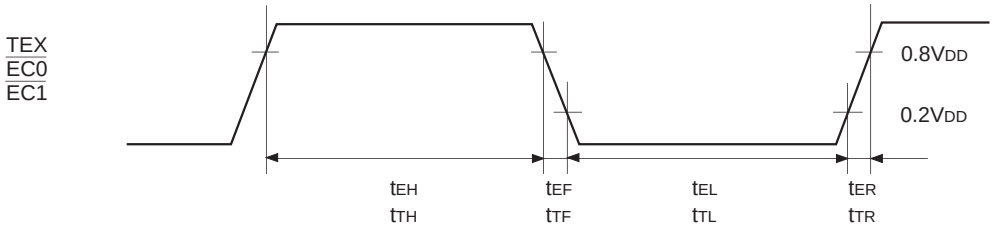


Fig. 3. Event count clock timing



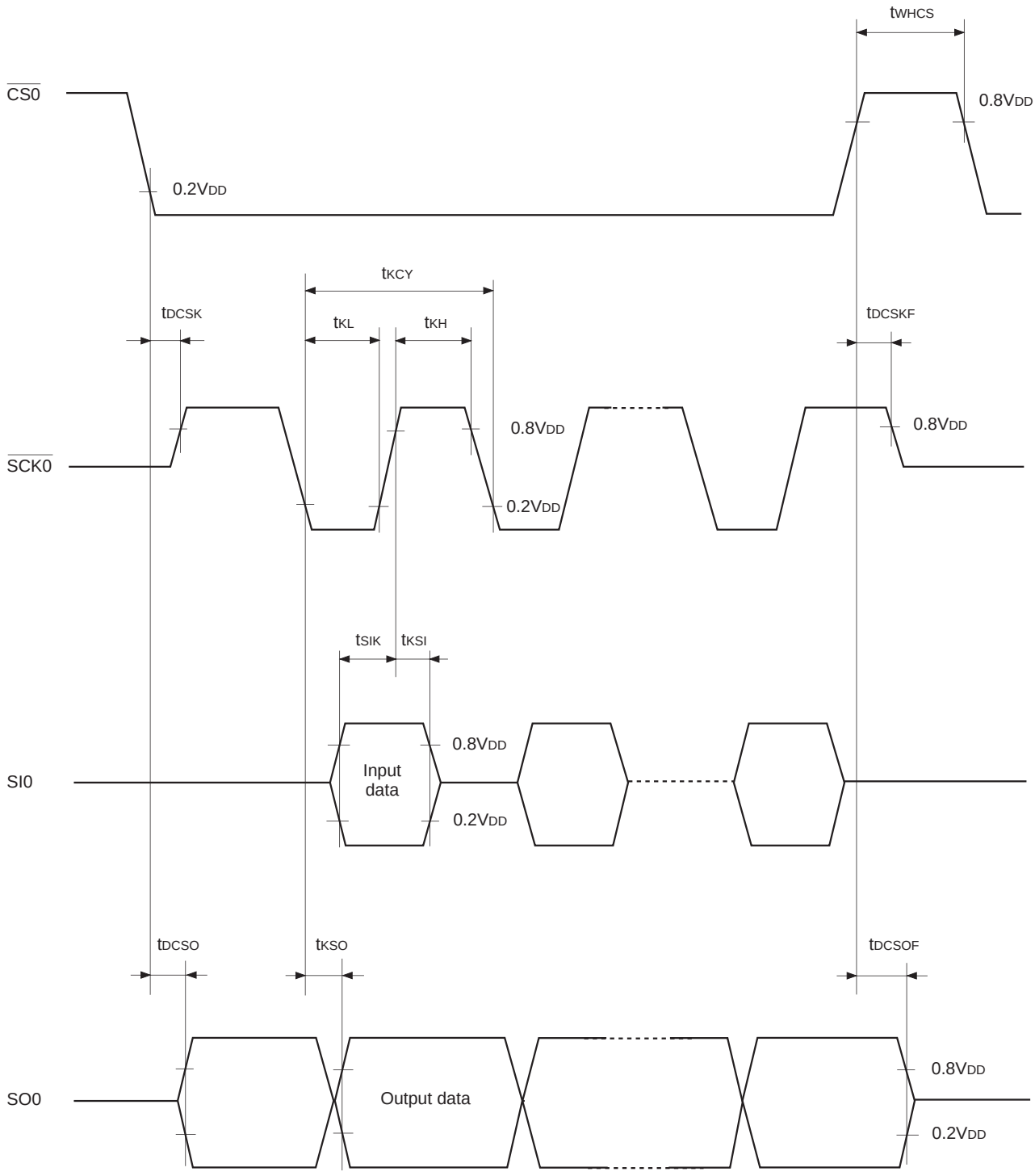
(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys+200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FE$_H$).
tsys (ns) = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

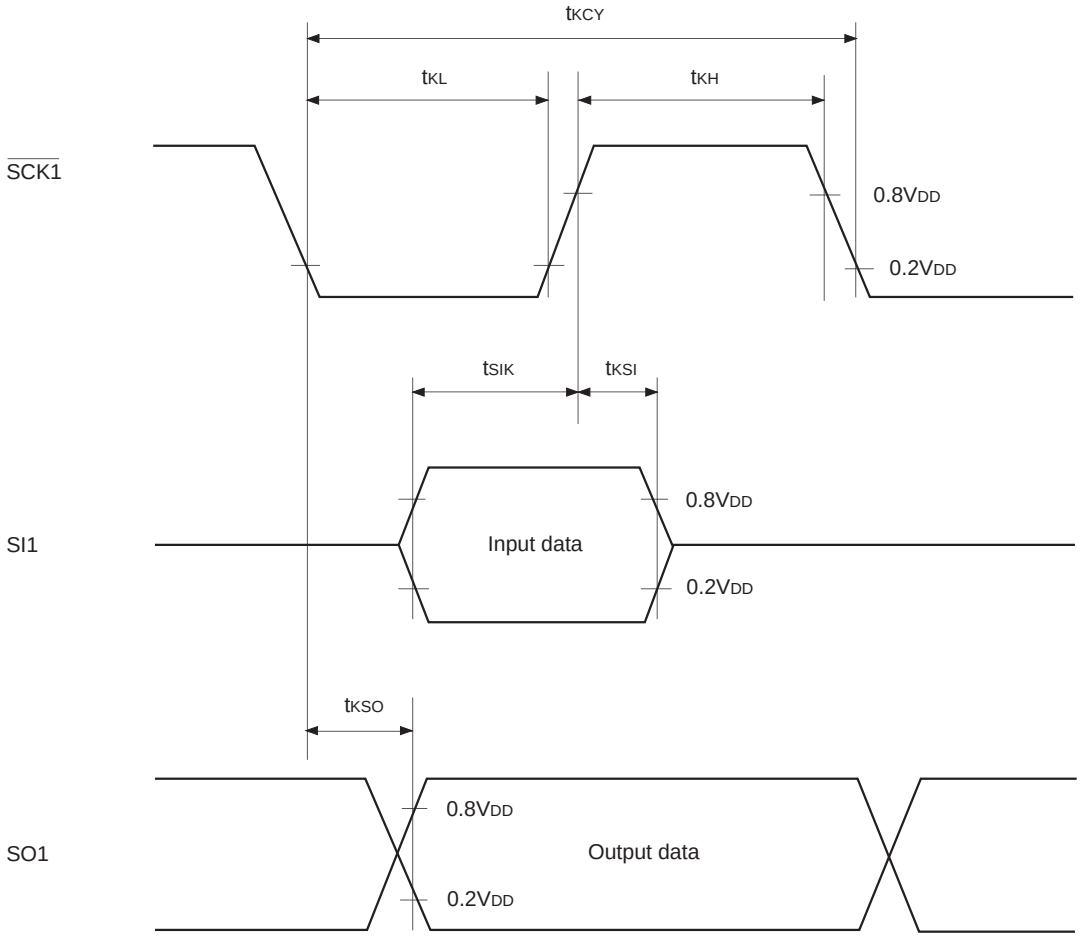


Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input set-up time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing

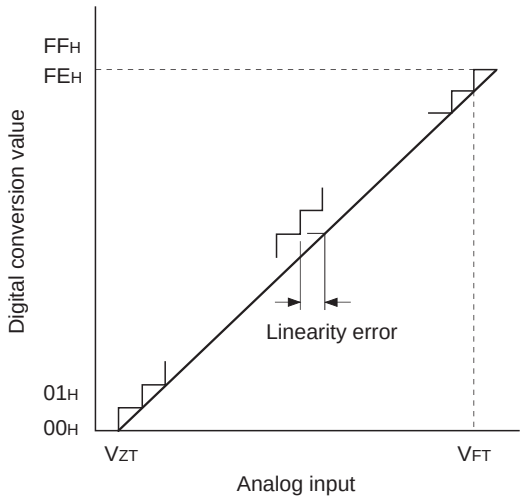


(3) A/D converter characteristics

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to V_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{REF} = 5.0V Vss = AV_{SS} = 0V			±5	LSB
Zero transition voltage	V_{ZT}*1			–10	10	110	mV
Full-scale transition voltage	V_{FT}*2			4870	4970	5070	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definition of A/D converter terms



*1) V_{ZT} : Value at which the digital transfer value changes from 00_H to 01_H and vice versa.

*2) V_{FT} : Value at which the digital transfer value changes from FE_H to FF_H and vice versa.

*3) f_{ADC} indicates the values below due to the contents of bit 6 (CKS) of the A/D control register (ADC: $00F9_H$) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: $00FE_H$).

CKS / PCK1, 0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig 7. Interruption input timing

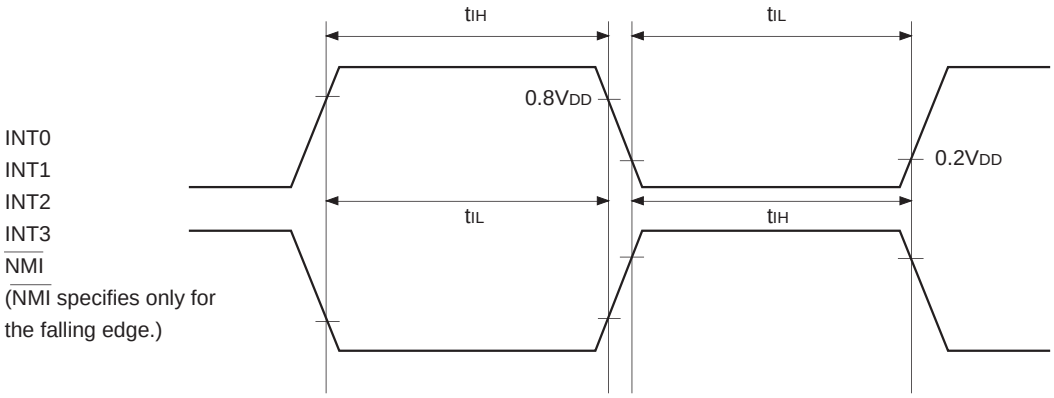
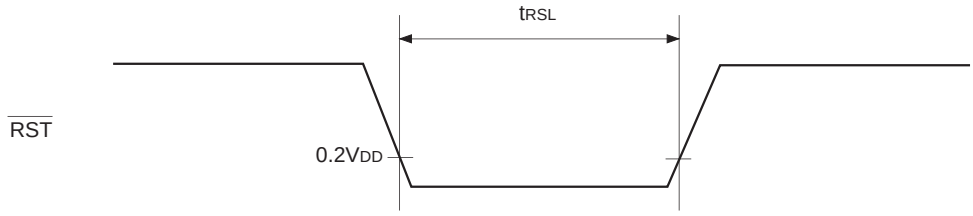


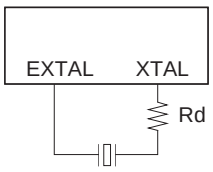
Fig. 8. $\overline{RST}$ input timing



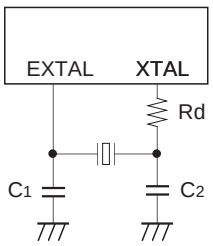
Appendix

Fig. 9. Recommended oscillation circuit

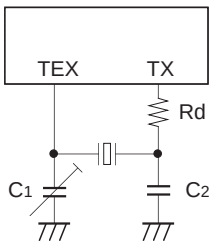
(i) Main clock



(ii) Main clock



(iii) Sub clock



Products List

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA16.00MXZ072	16.00	0	0	0	(i)
	CSA20.00MXZ046	20.00				
RIVER ELETEC CO., LTD.	HC-49/U03	16.00	8	8	0	(ii)
		20.00	6	6		
KINSEKI LTD.	P3	32.768kHz	50	22	1M	(iii)

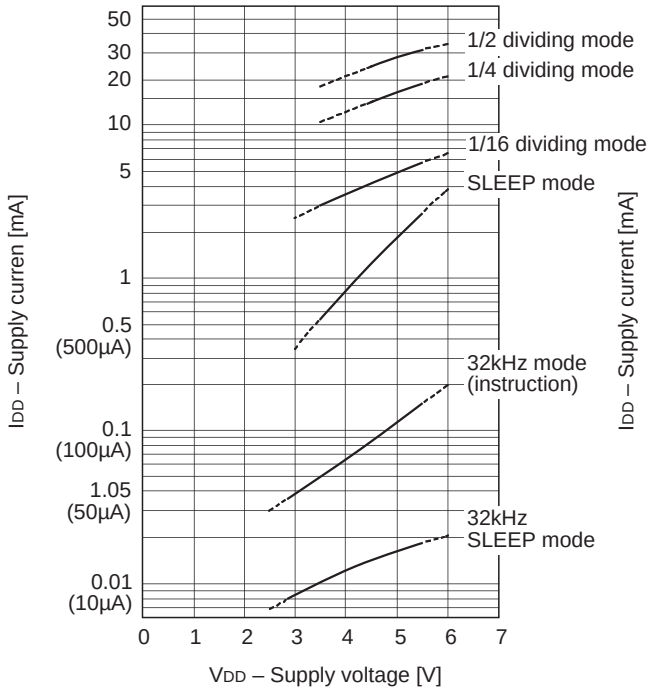
Mask option table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent

Example of Representative Characteristics

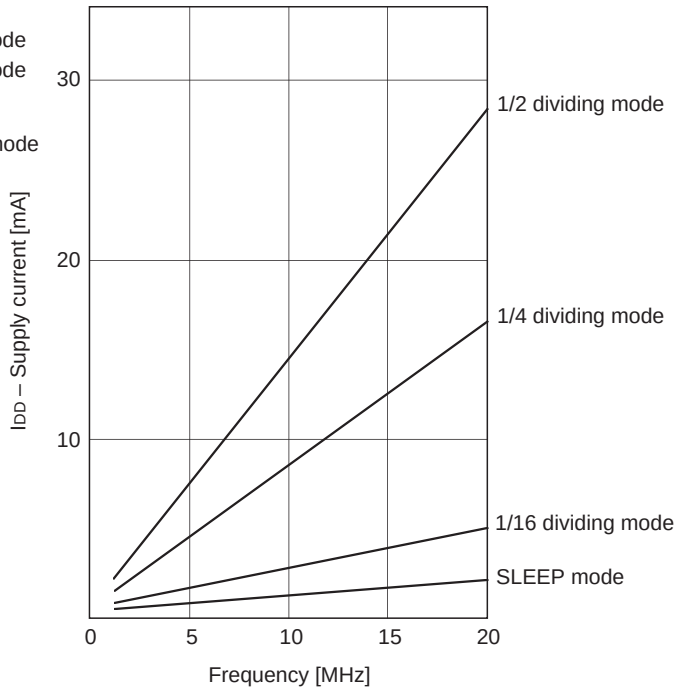
IDD vs. VDD

(fc = 20MHz, Ta = 25°C, Typical)



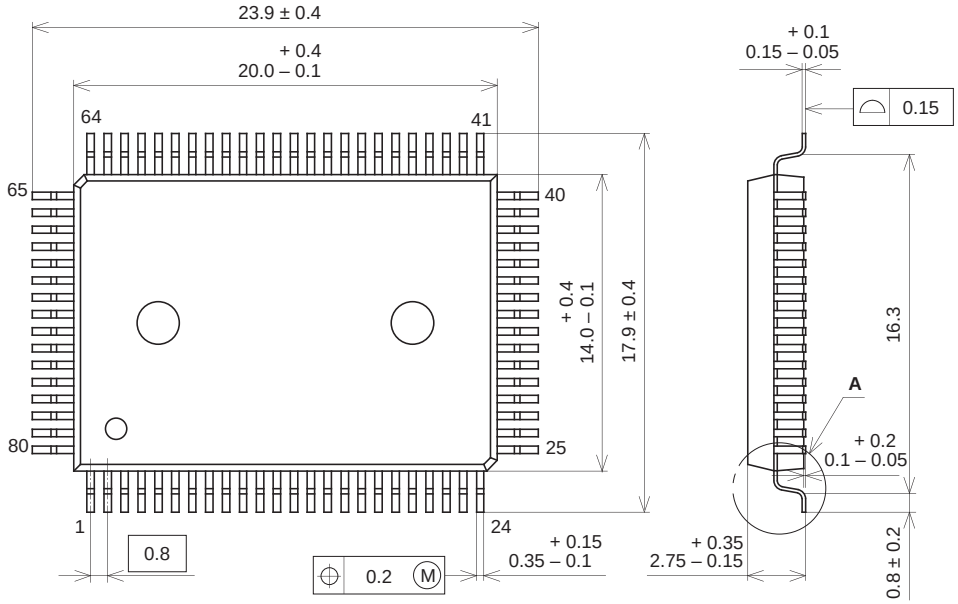
IDD vs. fc

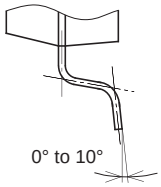
(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g