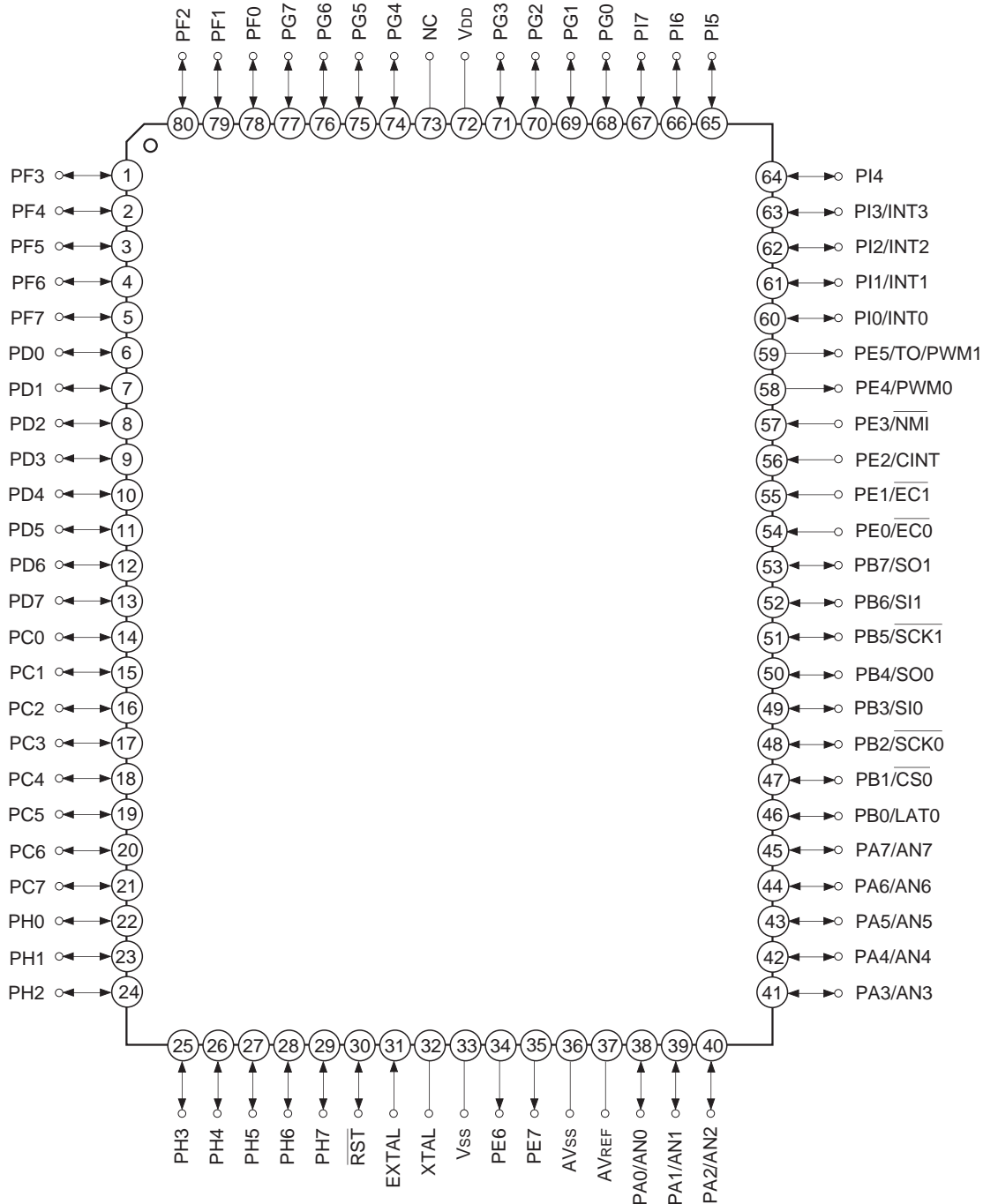


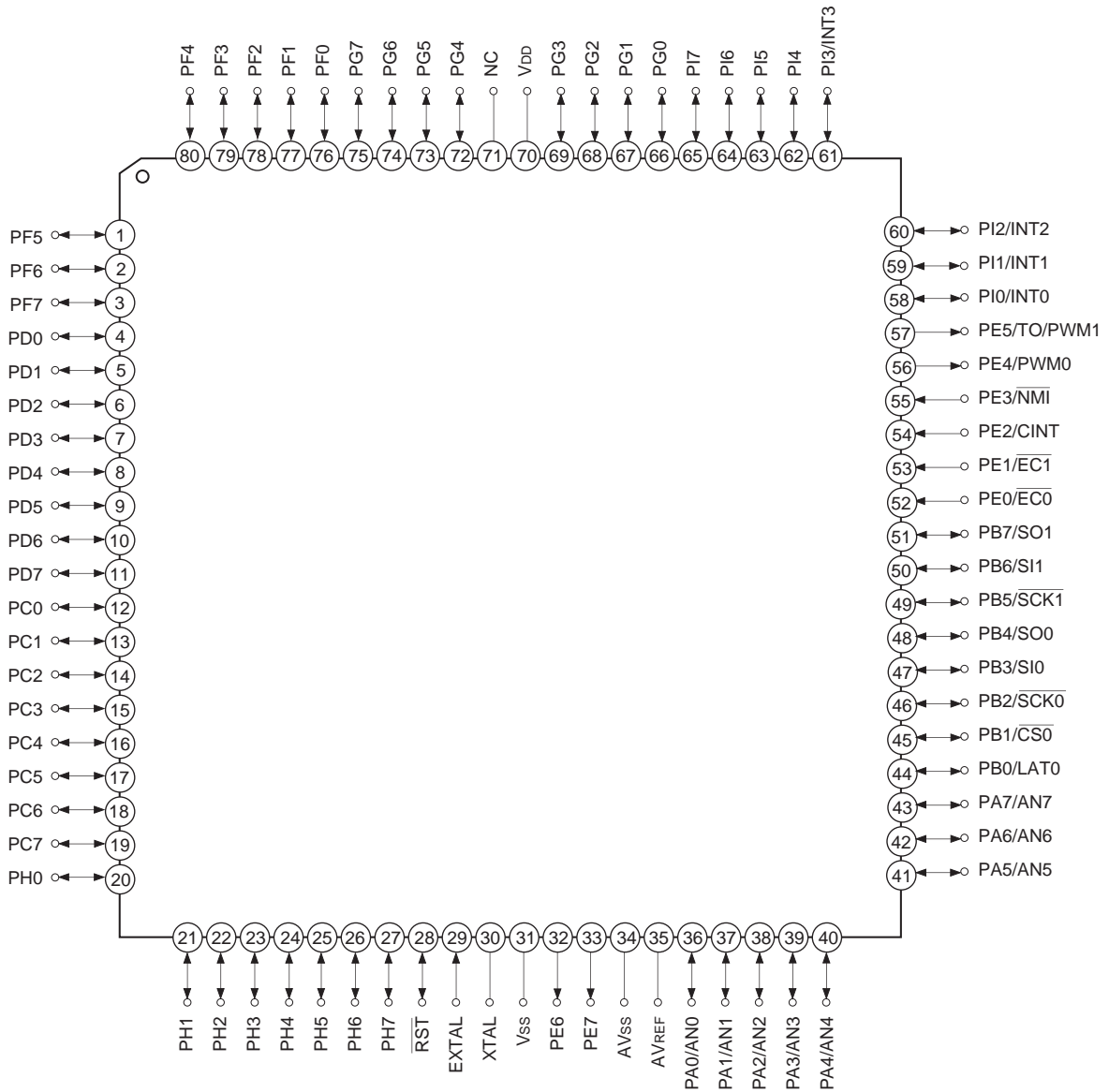
Block Diagram

Pin Assignment (Top View) 80-pin QFP package



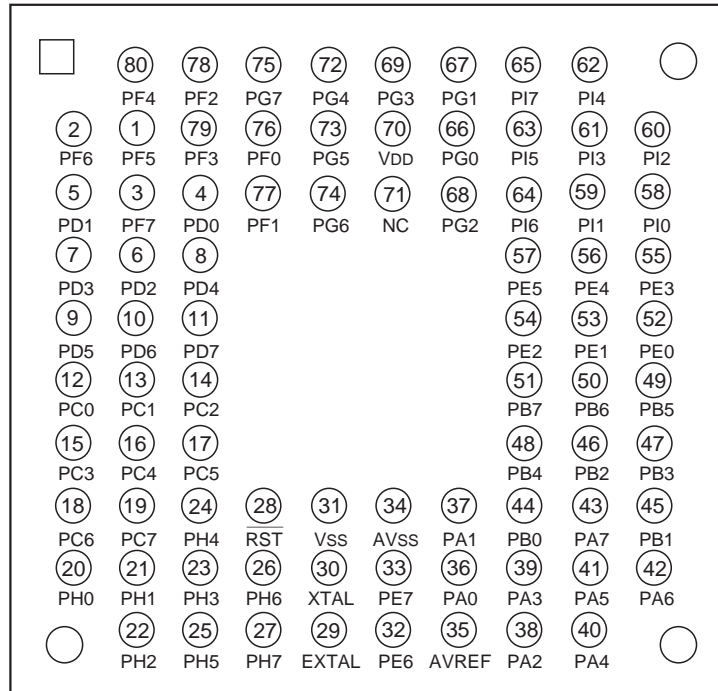
Note) NC (Pin 73) is left open. However, this pin is used for the Flash EEPROM incorporated version (CXP845F60).

Pin Assignment (Top View) 80-pin LQFP package



Note) NC (Pin 73) is left open.

Pin Assignment (Top View) 80-pin LFLGA package



Note) NC (Pin 71) is left open.

Pin Description

Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/LAT0	I/O/Output	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Latch output for serial interface (CH0).
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC0}}$	Input/Input	(Port E) 8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs. (8 pins)	External event inputs for timer/counter. (2 pins)
PE1/ $\overline{\text{EC1}}$	Input/Input		Capture trigger input.
PE2/CINT	Input/Input		Non-maskable interruption request input.
PE3/ $\overline{\text{NMI}}$	Input/Input		8-bit PWM0 output.
PE4/PWM0	Output/Output		Rectangular wave output for 16-bit timer/counter and 8-bit PWM1 output.
PE5/TO/ PWM1	Output/Output/ Output		
PE6	Output		
PE7	Output		
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

Symbol	I/O	Description	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (4 pins)
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input it to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	System reset for active at Low level. This pin is I/O pin, and outputs Low level at the power on with the power-on reset function executed. (Mask option)	
NC		No connected. Leave this pin open. However, this is used for the Flash EEPROM incorporated version (CXP845F60).	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
VDD		Positive power supply.	
Vss		GND	

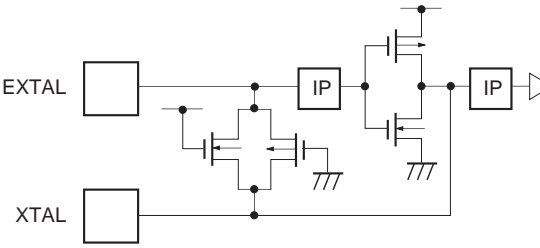
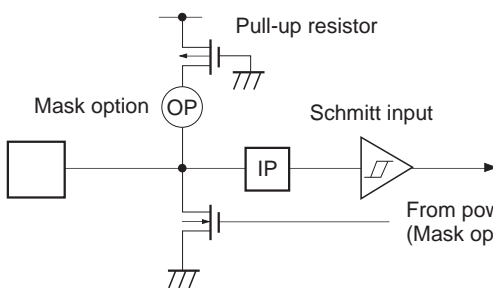
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistor "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PB0/LAT0</p> <p>1 pin</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>LAT0</p> <p>Latch output enable</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>3 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>$\overline{\text{CS0}}$ SI0 SI1</p> <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>SCK OUT</p> <p>Serial clock output enable</p> <p>Port B function selection "0" when reset</p> <p>Port B data "0" when reset</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>SCK0, SCK1 in</p> <p>Schmitt input</p> <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor</p> <p>SO</p> <p>Serial data output enable</p> <p>Port B function selection "0" when reset</p> <p>Port B data "0" when reset</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p> <p>Pull-up resistor "0" when reset</p> <p>Port C data</p> <p>Port C direction "0" when reset</p> <p>Data bus</p> <p>RD (Port C)</p> <p>*1 Large current drive (12mA: V_{DD} = 4.5 to 5.5V) (5mA: V_{DD} = 3.0 to 3.6V)</p> <p>*2 Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{EC0}$ PE1/$\overline{EC1}$ PE2/\overline{CINT} PE3/\overline{NMI}</p> <p>4 pins</p>	<p>Port E</p> <p>Schmitt input</p> <p>IP</p> <p>$\overline{EC0}$, $\overline{EC1}$ \overline{CINT}, \overline{NMI}</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE4/PWM0</p> <p>1 pin</p>	<p>Port E</p> <p>PWM0</p> <p>Port E function selection "0" when reset</p> <p>Port E data "1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>High level</p>
<p>PE5/TO/ PWM1</p> <p>1 pin</p>	<p>Port E</p> <p>Internal reset signal</p> <p>Port E data "1" when reset</p> <p>MPX</p> <p>TO → 01</p> <p>PWM1 → 1x</p> <p>Port E function selection (upper)</p> <p>Port E function selection (lower) "00" when reset</p> <p>TO output enable</p> <p>* Pull-up transistor approx. 150kΩ ($V_{DD} = 4.5$ to $5.5V$) approx. 400kΩ ($V_{DD} = 3.0$ to $3.6V$)</p>	<p>High level (with resistor of pull-up transistor ON for reset)</p>
<p>PE6, PE7</p> <p>2 pins</p>	<p>Port E</p> <p>Port E data "0" when reset</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Low level</p>

Pin	Circuit format	When reset
PD0 to PD7 PF0 to PF7 PG0 to PG7 PI4 to PI7 28 pins	<p> Pull-up resistor "0" when reset Ports D, F, G, I data Ports D, F, G, I direction "0" when reset Data bus RD * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V) </p>	Hi-Z
PH0 to PH7 8 pins	<p> Pull-up resistor "0" when reset Port H data Port H direction "0" when reset Data bus RD (Port H) Edge detection Standby release * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V) </p>	Hi-Z
PI0/INT0 to PI3/INT3 4 pins	<p> Pull-up resistor "0" when reset Port I data Port I direction "0" when reset Data bus RD Schmitt input INT0 INT1 INT2 INT3 * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V) </p>	Hi-Z

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode and XTAL becomes High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p> <p>From power-on reset circuit (Mask option)</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	Output (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total of all output pins
Low level output current	I _{OL}	15	mA	Pins excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current outputs (value per pin*2)
Low level total output current	∑I _{OL}	100	mA	Total of all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		500	mW	LFLGA-80P-02

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC)

Note Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage*1	V _{DD}	4.5 (3.0)	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5 (2.7)	5.5		Guaranteed operation range for 1/16 frequency dividing clock and sleep mode
		2.0	5.5		Guaranteed data hold range during stop mode
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*3
	V _{IHEX}	0.9V _{DD}	V _{DD} + 0.3	V	EXTAL*4
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*3
	V _{ILEX}	-0.3	0.1V _{DD}	V	EXTAL*4
Operating temperature	T _{opr}	-20	+75	°C	

*1 Specifies values in parenthesis for 1 to 20MHz system clock operation.

*2 Normal input ports (PA, PB0, PB4, PB7, PC, PE0 to PE3, PD, PF to PH, PI4 to PI7)

*3 RST, CINT, CS0, SCK0, SCK1, EC0, EC1, SI0, SI1, NMI, INT0, INT1, INT2, INT3

*4 Specifies only during external clock input.

Electrical Characteristics

DC Characteristics (V_{DD} 4.5 to 5.5V)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4 to PE7, PF to PI, $\overline{\text{RST}}$ (only V_{OL})*1	$V_{DD} = 4.5\text{V}$, $I_{OH} = -0.5\text{mA}$	4.0			V
			$V_{DD} = 4.5\text{V}$, $I_{OH} = -1.2\text{mA}$	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE4 to PE7, PF to PI, $\overline{\text{RST}}$ (only V_{OL})*1	$V_{DD} = 4.5\text{V}$, $I_{OL} = 1.8\text{mA}$			0.4	V
			$V_{DD} = 4.5\text{V}$, $I_{OL} = 3.6\text{mA}$			0.6	V
		PC	$V_{DD} = 4.5\text{V}$, $I_{OL} = 12.0\text{mA}$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5\text{V}$, $V_{IH} = 5.5\text{V}$	0.1		25	μA
	I_{ILE}		$V_{DD} = 5.5\text{V}$, $V_{IL} = 0.4\text{V}$	-0.1		-25	μA
	I_{ILR}	$\overline{\text{RST}}$ *2	$V_{DD} = 5.5\text{V}$, $V_{IL} = 4.0\text{V}$	-1.5		-400	μA
	I_{IL}	PA to PD*3 PF to PI*3	$V_{DD} = 4.5\text{V}$, $V_{IL} = 4.0\text{V}$	-2.78		-50	μA
I/O leakage current	I_{IZ}	PA to PD*3 PF to PI*3 PE0 to PE3, $\overline{\text{RST}}$ *2	$V_{DD} = 5.5\text{V}$, $V_I = 0, 5.5\text{V}$			± 10	μA
Supply current *4	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation $V_{DD} = 5.5\text{V}$, 28MHz crystal oscillation ($C_1 = C_2 = 5\text{pF}$)		28	58	mA
	I_{DD2}						
	I_{DDS1}		Sleep mode		4.0	10	mA
	I_{DDS2}		$V_{DD} = 5.5\text{V}$, 28MHz crystal oscillation ($C_1 = C_2 = 5\text{pF}$)				
	I_{DDS3}		Stop mode $V_{DD} = 5.5\text{V}$, termination of 28MHz crystal oscillation			10	μA
Input capacity	C_{IN}	PA to PD, PE0 to PE3, PF to PI, EXTAL, $\overline{\text{RST}}$	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 Specifies $\overline{\text{RST}}$ pin when the power-on reset circuit is selected with mask option.

*2 For $\overline{\text{RST}}$ pin, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*3 For PA to PD and PF to PI pins, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*4 When all pins are open.

DC Characteristics (V_{DD} = 3.0 to 3.6V)

(T_a = -20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE4 to PE7, PF to PI, $\overline{\text{RST}}$ (only V _{OL})*1	V _{DD} = 3.0V, I _{OH} = -0.15mA	2.7			V
			V _{DD} = 3.0V, I _{OH} = -0.5mA	2.3			V
V _{DD} = 3.0V, I _{OL} = 1.2mA				0.3		V	
V _{DD} = 3.0V, I _{OL} = 1.6mA				0.5		V	
Low level output voltage	V _{OL}	PC	V _{DD} = 3.0V, I _{OL} = 5mA			1.0	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.6V, V _{IH} = 3.6V	0.05		15	μA
	I _{ILE}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.05		-15	μA
	I _{ILR}	$\overline{\text{RST}}$ *2	V _{DD} = 3.6V, V _{IL} = 2.7V	-0.7		-200	μA
	I _{IL}	PA to PD*3 PF to PI*3	V _{DD} = 3.6V, V _{IL} = 2.7V			-30	μA
V _{DD} = 3.0V, V _{IL} = 2.7V			-1.0			μA	
I/O leakage current	I _{Iz}	PA to PD*3 PF to PI*3 PE0 to PE3, $\overline{\text{RST}}$ *2	V _{DD} = 3.6V, V _I = 0, 3.6V			±5	μA
Supply current*4	I _{DD1}	V _{DD}	1/2 frequency dividing clock operation		13.5	30	mA
	I _{DD2}		V _{DD} = 3.6V, 20MHz crystal oscillation (C ₁ = C ₂ = 10pF)				
	I _{DDS1}		Sleep mode		1.2	4.0	mA
	I _{DDS2}		V _{DD} = 3.6V, 20MHz crystal oscillation (C ₁ = C ₂ = 10pF)				
	I _{DDS3}		Stop mode			5	μA
	V _{DD} = 3.6V, termination of 20MHz crystal oscillation						

*1 Specifies $\overline{\text{RST}}$ pin when the power-on reset circuit is selected with mask option.

*2 For $\overline{\text{RST}}$ pin, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*3 For PA to PD and PF to PI pins, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*4 When all pins are open.

AC Characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	$V_{DD} = 4.5$ to 5.5V	1	28	MHz
					1	20	
System clock input pulse width	t_{XL} , t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	$V_{DD} = 4.5$ to 5.5V	15.6		ns
					23		
System clock input rise time, fall time	t_{CR} , t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			100	ns
Event count input clock pulse width	t_{EH} , t_{EL}	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3			$t_{\text{sys}} + 50^{*1}$	ns
Event count input clock rise time, fall time	t_{ER} , t_{EF}	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3			20	ns

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

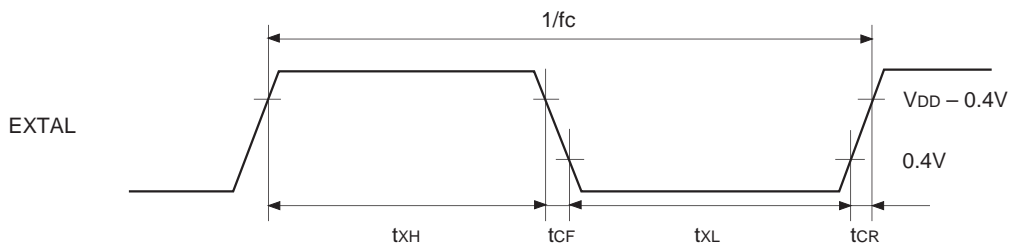


Fig. 1. Clock timing

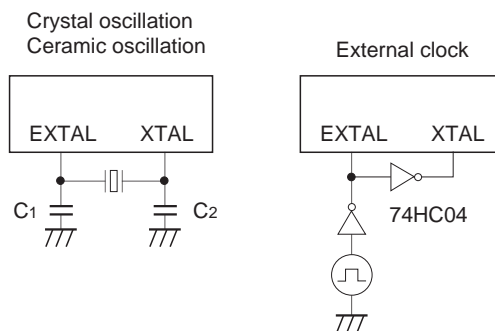


Fig. 2. Clock applied conditions

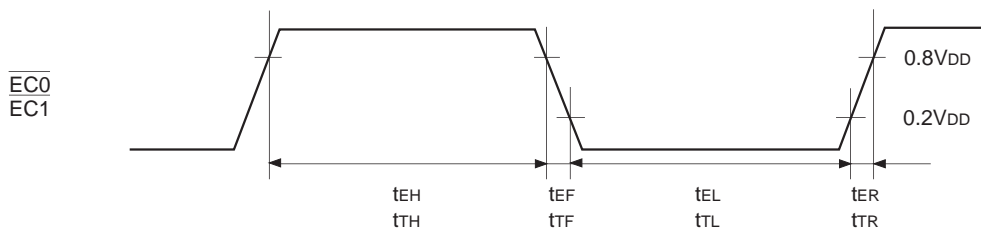


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5t _{sys} + 100	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5t _{sys} + 100	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		1.5t _{sys} + 100	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		1.5t _{sys} + 100	ns
$\overline{CS0}$ High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 150		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK0}$ High, Low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 90		ns
			Output mode	4000/fc - 25		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	50		ns
			$\overline{SCK0}$ output mode	100		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{KSI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 100		ns
			$\overline{SCK0}$ output mode	50		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 100	ns
			$\overline{SCK0}$ output mode		50	ns
$\overline{SCK0} \downarrow \rightarrow LAT0$ output delay time	t _{LADLY}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t _{KCY}	t _{KCY} + 50	ns
LAT0 data pulse width	t _{LAPLS}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t _{KCY} - 10	t _{KCY} + 50	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK0 = output mode)		1.5t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK0 = output mode)		1.5t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		1.5t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		1.5t _{sys} + 200	ns
$\overline{\text{CS0}}$ High level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK0}}$ High, Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 80		ns
			Output mode	4000/fc - 50		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	80		ns
			$\overline{\text{SCK0}}$ output mode	150		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	t _{sys} + 120		ns
			$\overline{\text{SCK0}}$ output mode	70		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK0}}$ output mode		80	ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{LAT0}$ output delay time	t _{LADLY}	LAT0	Latch output mode (SCK0 = output mode)	t _{KCY}	t _{KCY} + 100	ns
LAT0 data pulse width	t _{LAPLS}	LAT0	Latch output mode (SCK0 = output mode)	t _{KCY} - 10	t _{KCY} + 100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load condition for the $\overline{\text{SCK0}}$ output mode, SO0 output delay time is 50pF + 1TTL.

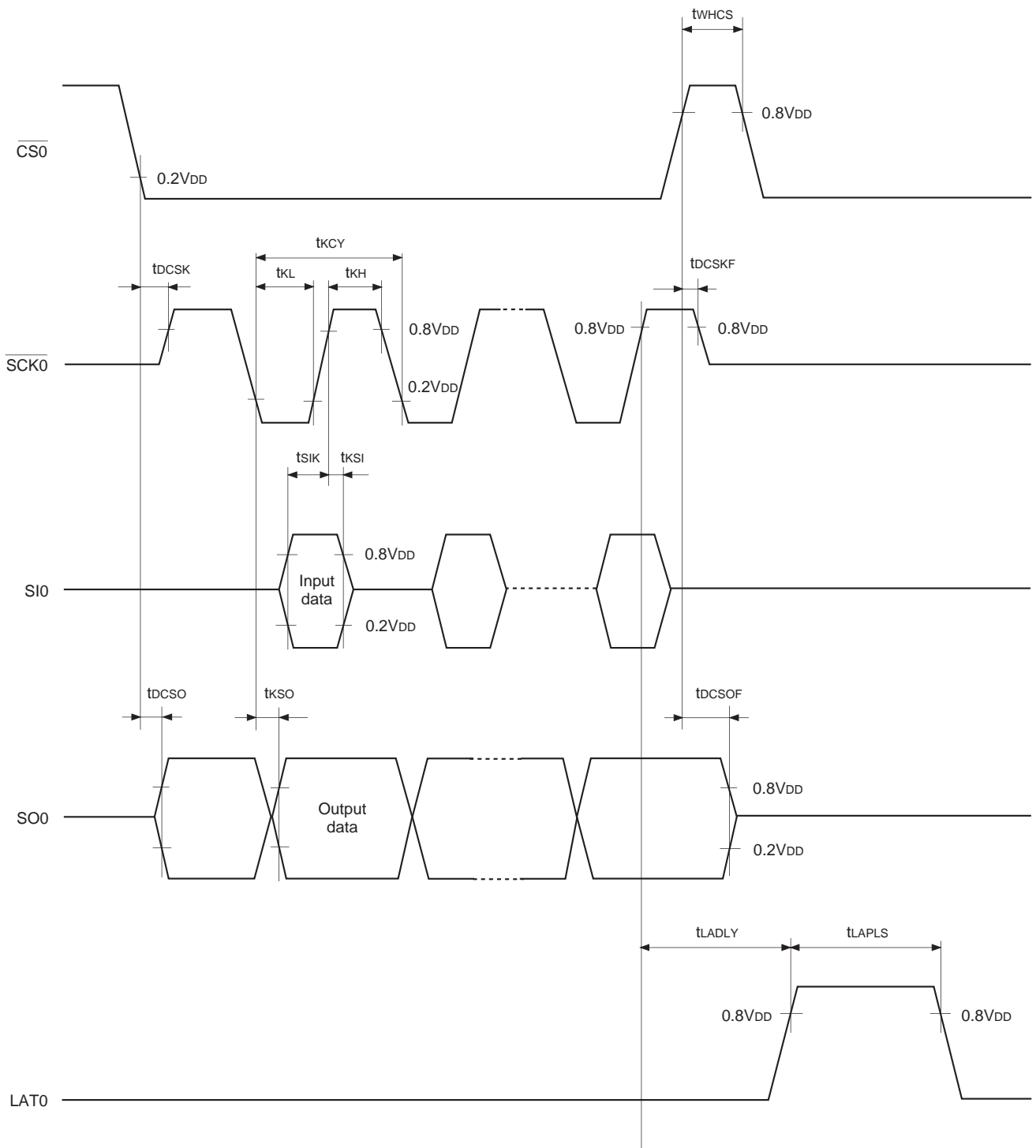


Fig. 4. Serial transfer CH0 timing

(3) Serial transfer (CH1)(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	$\overline{\text{SCK1}}$	Input mode	500		ns
			Output mode	8000/fc		ns
SCK1 High, Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK1}}$	Input mode	200		ns
			Output mode	4000/fc - 25		ns
SI1 input set-up time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	50		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	50		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		100	ns
			$\overline{\text{SCK1}}$ output mode		50	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is 50pF + 1TTL.(Ta = -20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	$\overline{\text{SCK1}}$	Input mode	700		ns
			Output mode	8000/fc		ns
SCK1 High, Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK1}}$	Input mode	300		ns
			Output mode	4000/fc - 50		ns
SI1 input set-up time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	70		ns
			$\overline{\text{SCK1}}$ output mode	150		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	150		ns
			$\overline{\text{SCK1}}$ output mode	70		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		150	ns
			$\overline{\text{SCK1}}$ output mode		80	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is 50pF.

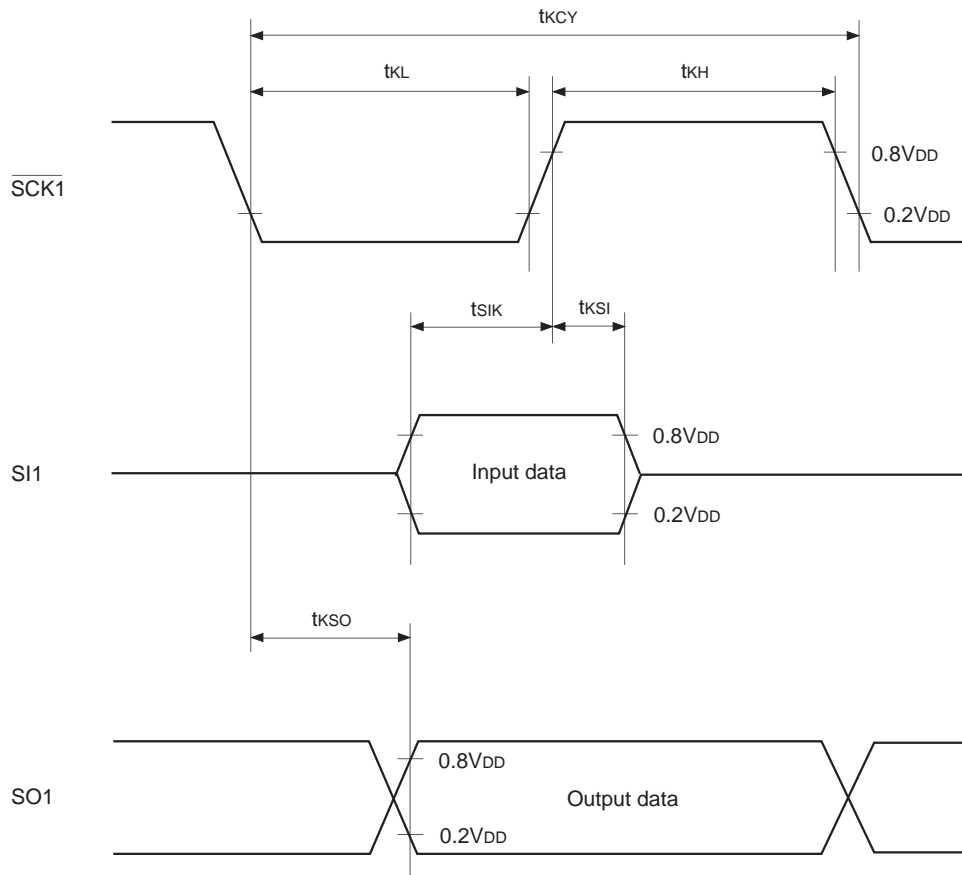


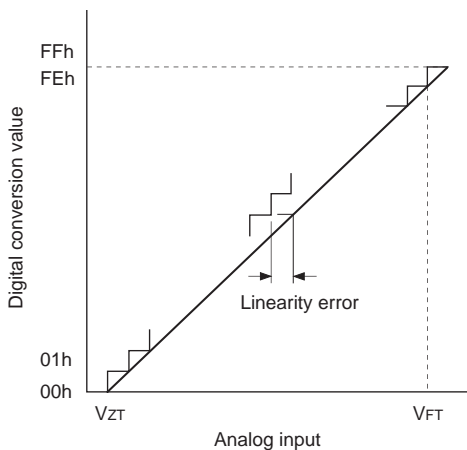
Fig. 5. Serial transfer CH1 timing

(4) A/D converter characteristics (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, AVREF = 4.0 to VDD, VSS = AVSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVREF = 5.0V VSS = AVSS = 0V			±4	LSB
Zero transition voltage	VZT*1			-10	10	70	mV
Full-scale transition voltage	VFT*2			4910	4970	5030	mV
Conversion time	tCONV			27/fADC*3			µs
Sampling time	tSAMP			6/fADC*3			µs
Reference input voltage	VREF	AVREF		VDD - 0.5		VDD	V
Analog input voltage	VIAN	AN0 to AN7		0		AVREF	V
AVREF current	IREF	AVREF	Operation mode		0.6	1.0	mA
	IREFS		Sleep mode Stop mode			10	µA

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, AVREF = 2.7 to VDD, VSS = AVSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVREF = 3.3V VSS = AVSS = 0V			±5	LSB
Zero transition voltage	VZT*1			-10	6.5	70	mV
Full-scale transition voltage	VFT*2			3216	3280.5	3345	mV
Conversion time	tCONV			27/fADC*3			µs
Sampling time	tSAMP			6/fADC*3			µs
Reference input voltage	VREF	AVREF		VDD - 0.3		VDD	V
Analog input voltage	VIAN	AN0 to AN7		0		AVREF	V
AVREF current	IREF	AVREF	Operation mode		0.4	0.7	mA
	IREFS		Sleep mode Stop mode			5	µA



*1 VZT: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 VFT: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 fADC indicates the values below due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h).

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

However, the selection for fADC = fc (CKS = "0") is limited in the clock range of fc = 1 to 14MHz (VDD 4.5 to 5.5V) and fc = 1 to 10MHz (VDD = 3.0 to 4.5V).

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level widths	t _{IH}	INT0 INT1 INT2 INT3		1		μs
	t _{IL}	$\overline{\text{NMI}}$				
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

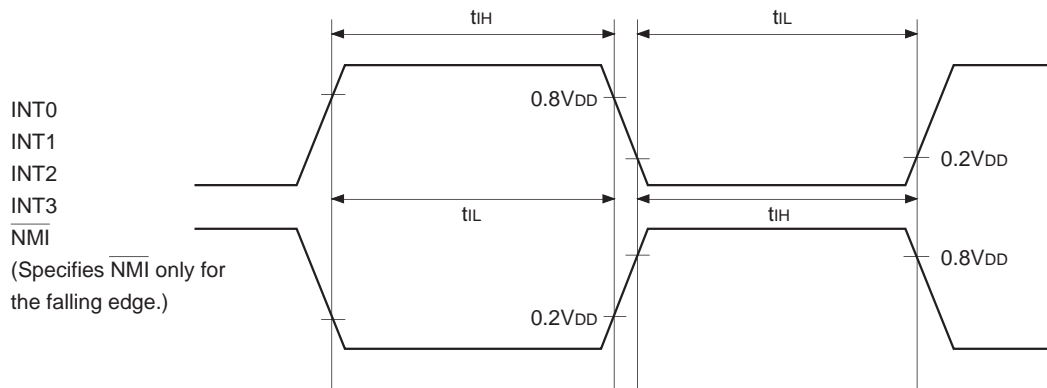


Fig 7. Interruption input timing

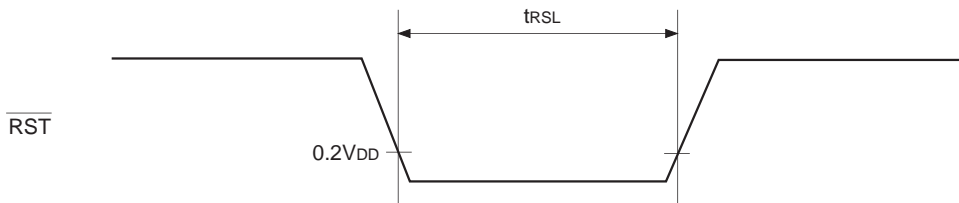


Fig. 8. $\overline{\text{RST}}$ input timing

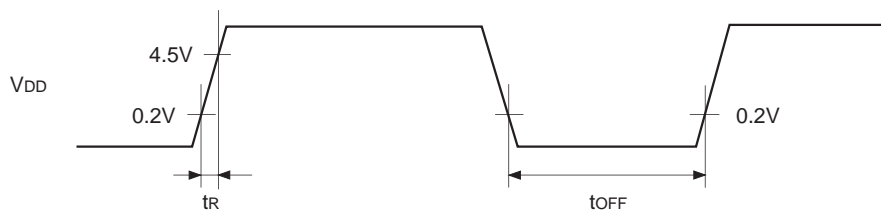
(5) Power-on reset*1

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t _R	VDD	Power-on reset	0.05	50	ms
Power supply cut-off time	t _{OFF}		Repetitive power-on reset	1		ms

*1 Specifies only when the power-on reset function is selected.

Power-on reset function can be selected only for the supply voltage range of 4.5 to 5.5V.



Take care when turning the power on.

Fig. 9. Power-on reset

Appendix

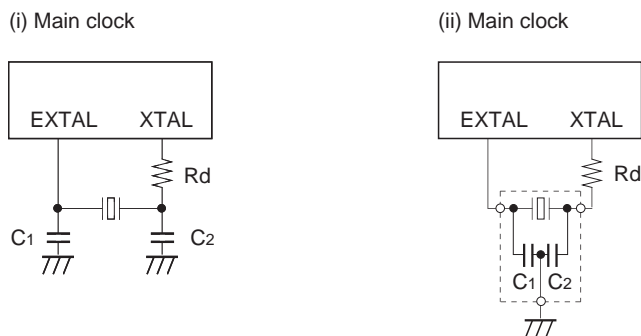


Fig. 10. SPC700 Series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CSA10.0MTZ	10.00				
	CSA12.00MTZ	12.00				
	CST8.00MTW*	8.00				(ii)
	CST10.0MT*	10.00				
	CST12.0MTW*	12.00				
	CSA16.00MXZ040	16.00	5	5	0	(i)
	CST16.00MXZ0C1*	16.00	5	5	0	(ii)
	CSA20.00MXZ040	20.00	OPEN	OPEN	0	(i)
	CSA24.00MXZ040	24.00	3	3	0	
CSA28.00MXZ040	28.00	3	3	0		
TDK CORPORATION.	CCR20.0MC6*	20.00	16	16	0	(ii)
	CCR24.0MC6*	24.00	16	16	0	
KINSEKI LTD.	HC49/U-S	28.00	1	1	220	(i)
	CX-11F	28.00	1	1	220	

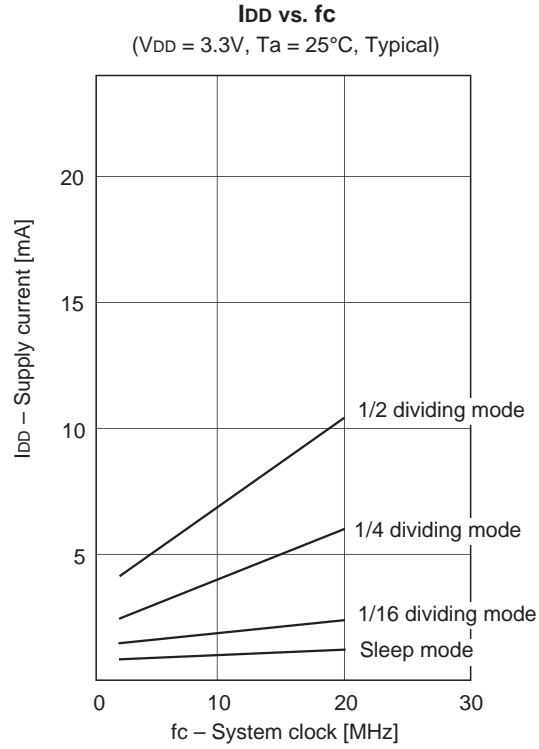
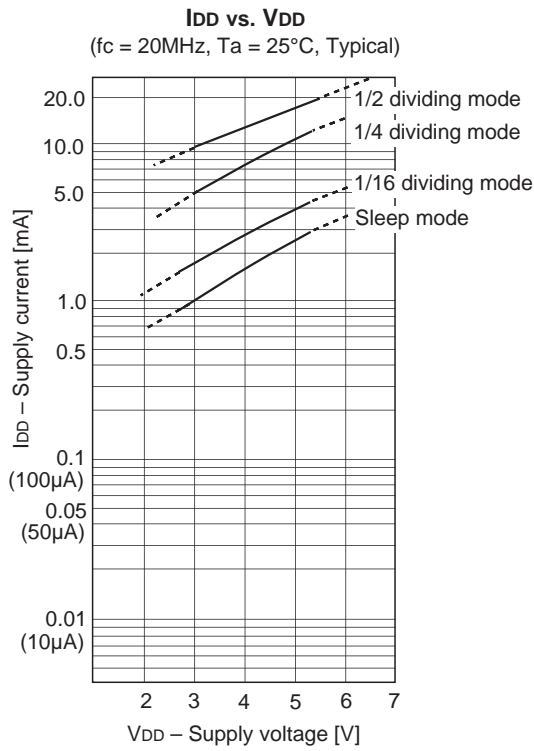
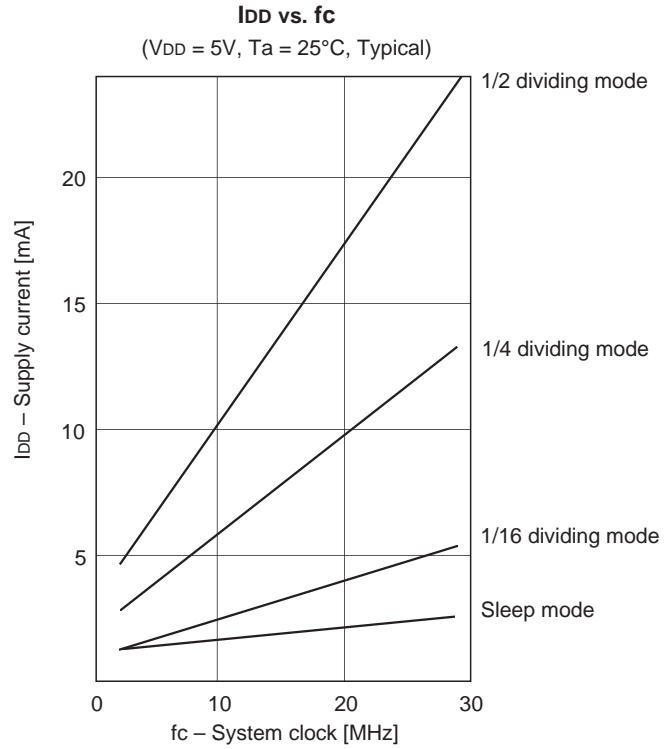
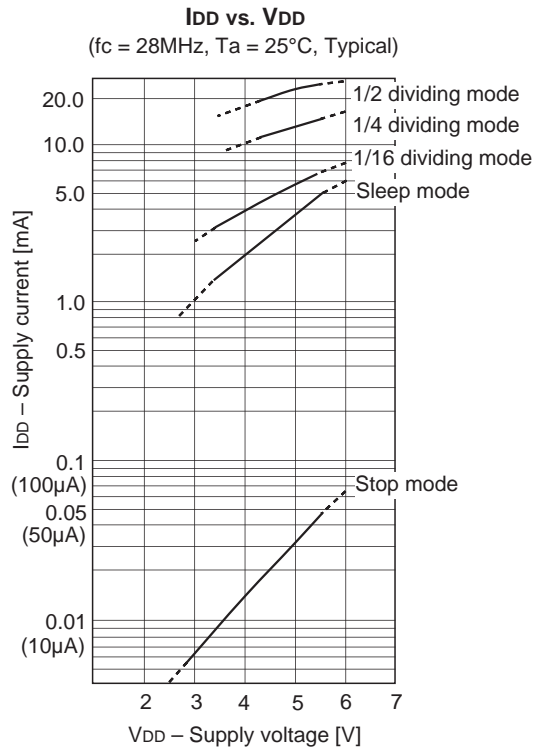
Models with an asterisk (*) have the built-in ground capacitance (C1, C2).

Mask option table

Item	Contents	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit *1	Non-existent	Existent

*1 "Existent" for power-on reset circuit cannot be selected when the supply voltage VDD of 3.0 to 4.5V.

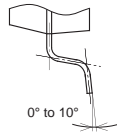
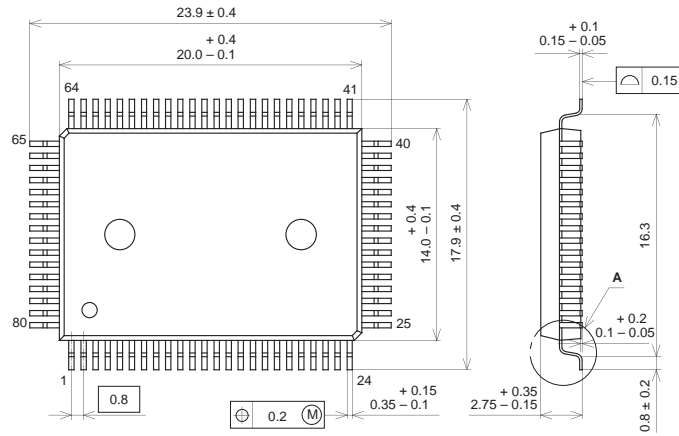
Characteristics Curves



Package Outline

Unit: mm

80PIN QFP (PLASTIC)



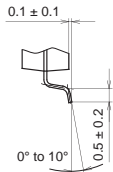
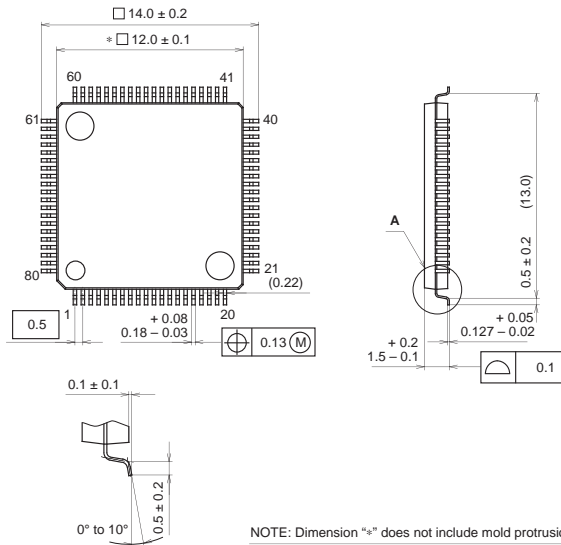
DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN LQFP (PLASTIC)



DETAIL A

NOTE: Dimension "*" does not include mold protrusion.

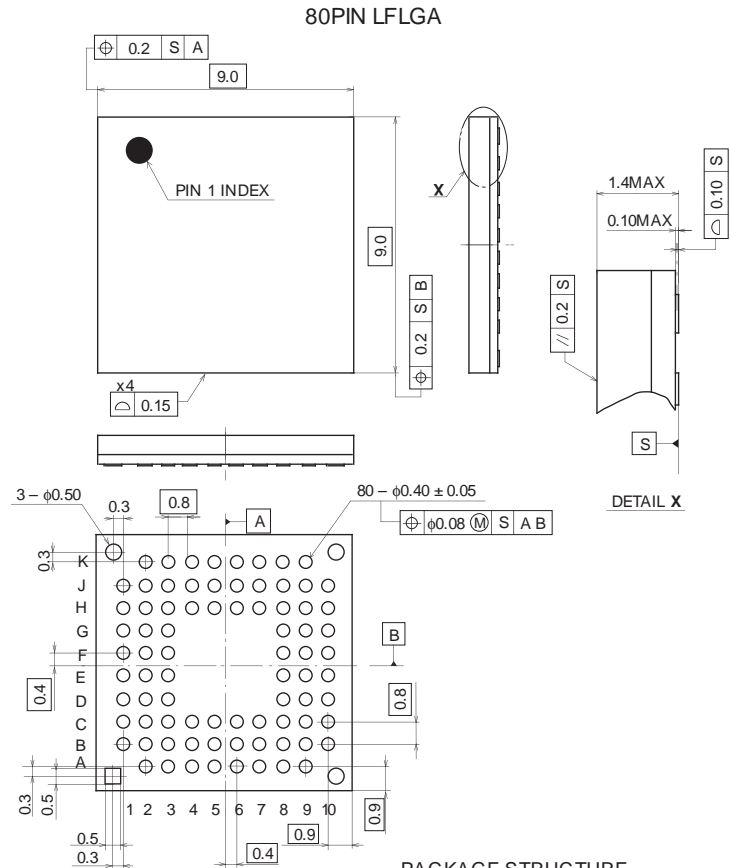
PACKAGE STRUCTURE

SONY CODE	LQFP-80P-L01
EIAJ CODE	LQFP080-P-1212
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5g

Package Outline

Unit: mm



PACKAGE STRUCTURE

SONY CODE	LFLGA-80P-02
EIAJ CODE	P-LFLGA80-9x9-0.8
JEDEC CODE	

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.3g