

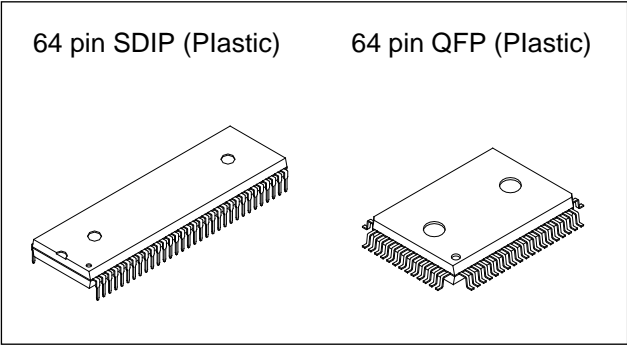
CMOS 8-bit Single Chip Microcomputer

Description

The CXP858P56A is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time-base timer, closed caption decoder, data slicer, on-screen display function, I²C bus interface, PWM output, remote control reception circuit, HSYNC counter and watchdog timer as well as basic configuration like 8-bit CPU, PROM, RAM and I/O port.

Also this IC provides a power-on reset function and sleep function that enables to lower power consumption.

The CXP858P56A is the PROM-incorporated version of the CXP85856A with built-in mask ROM. This provides the additional feature of being able to write directly into the program (also into the OSD character ROM or caption character ROM possible). Thus, it is most suitable for evaluation use during system development and for small-quantity production.



Structure

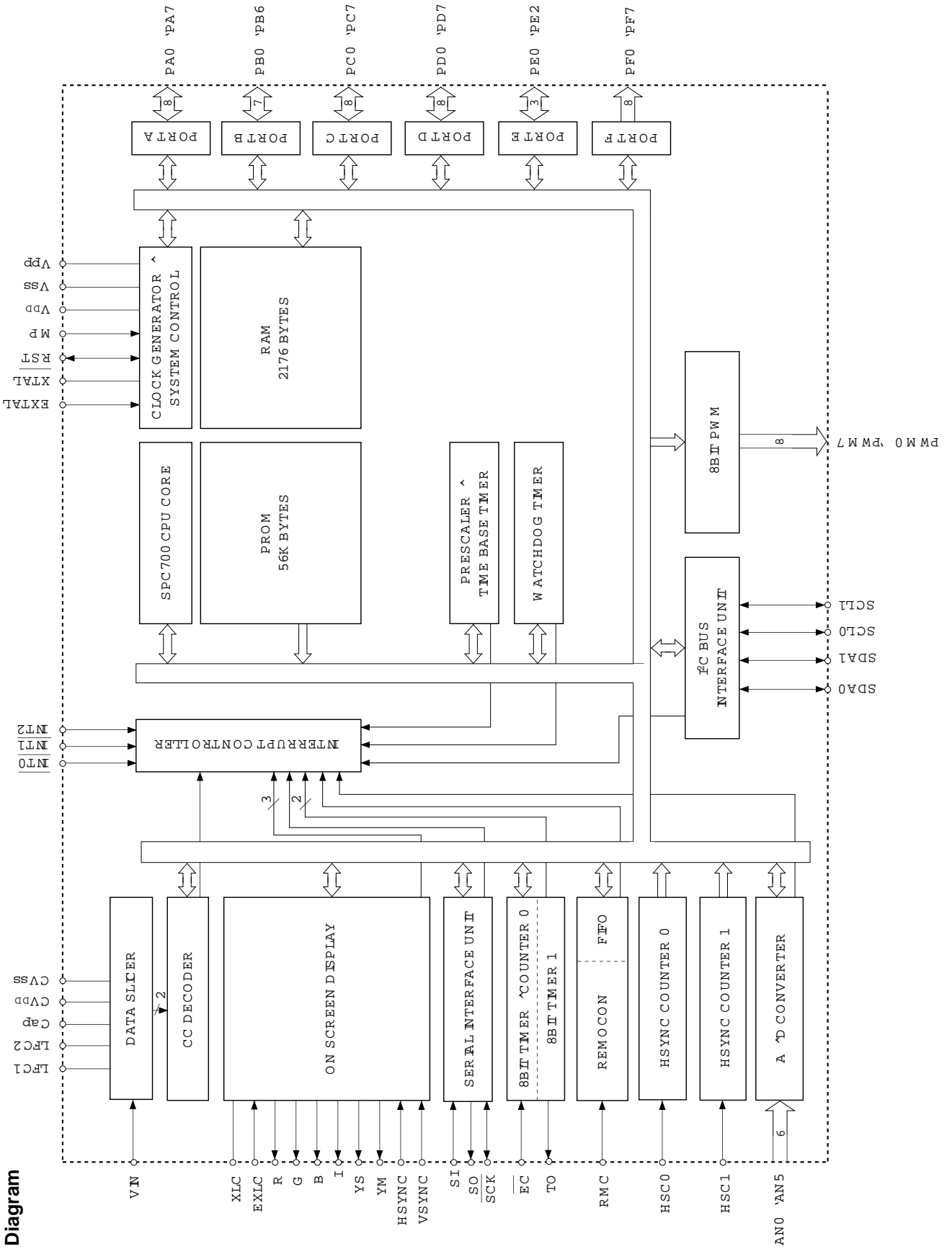
Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 333ns at 12MHz operation
- Incorporated PROM 56K bytes (Programming)
 4.5K bytes (OSD)
 3K bytes (Caption)
- Incorporated RAM 2176 bytes (Excludes the closed caption decoder and on-screen display VRAM)
- Peripheral functions
 - A/D converter 8-bit 6-channel successive approximation method
 (Conversion time of 26.7µs at 12MHz)
 - Serial interface 8-bit clock sync type, 1 channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
 - Closed caption decoder
- On-screen display (OSD) function
 - Incorporated data slicer,
 conforming to FCC (EDS supported), 8 × 13 dots, 192 character types,
 15 character colors, 4 lines × 34 characters, italic, underline, vertical scrolling,
 15 frame background colors/half blanking
 - 12 × 16 dots, 192 character types, 15 character colors, 2 lines × 24 characters,
 8 frame background colors/half blanking,
 15 background colors on full screen/half blanking,
 edging and vertical scrolling for every line,
 jitter elimination circuit,
 sprite OSD, 12 × 16 dots, 1 screen, 8 colors for every dot
- I²C bus interface
- PWM output 8 bits, 8 channels
- Remote control reception circuit 8-bit pulse measurement counter, 6-stage FIFO
- HSYNC counter 2 channels
- Watchdog timer
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep
- Package 64-pin plastic SDIP/QFP

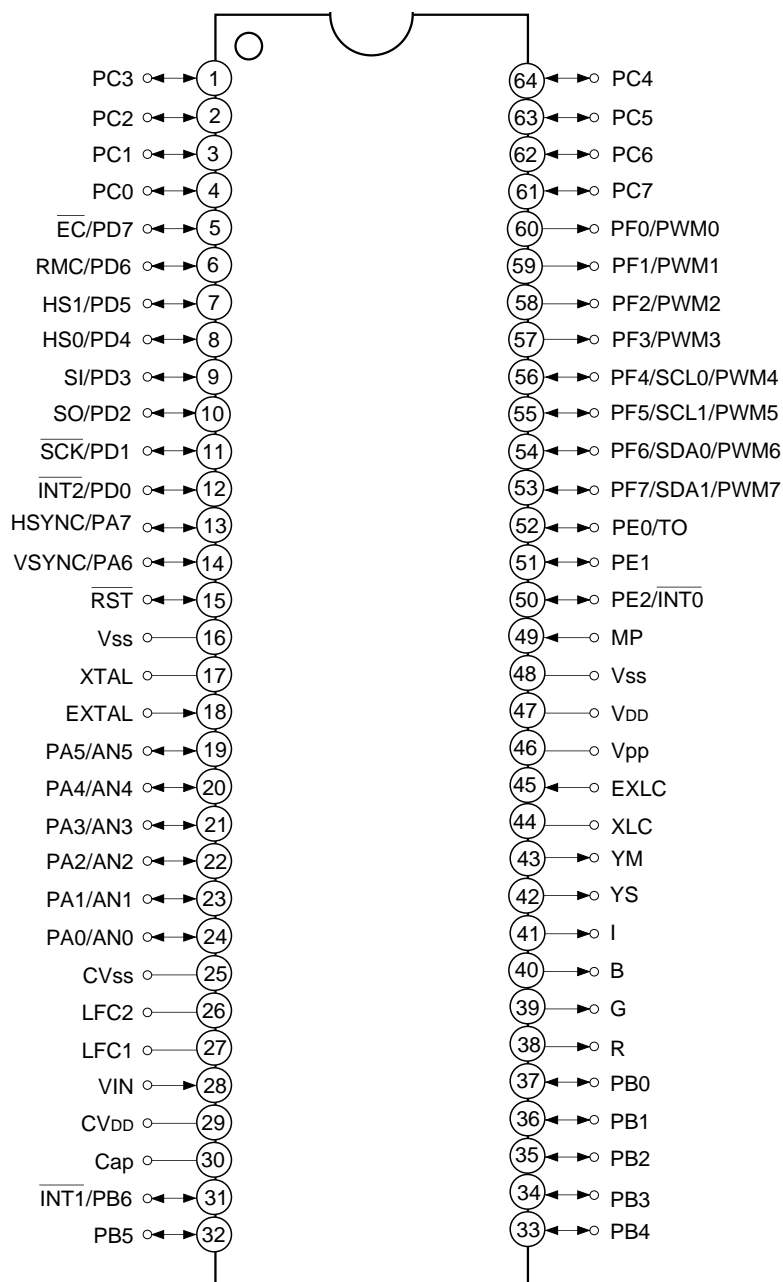
Purchase of Sony's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conform to the I²C Standard Specifications as defined by Philips.

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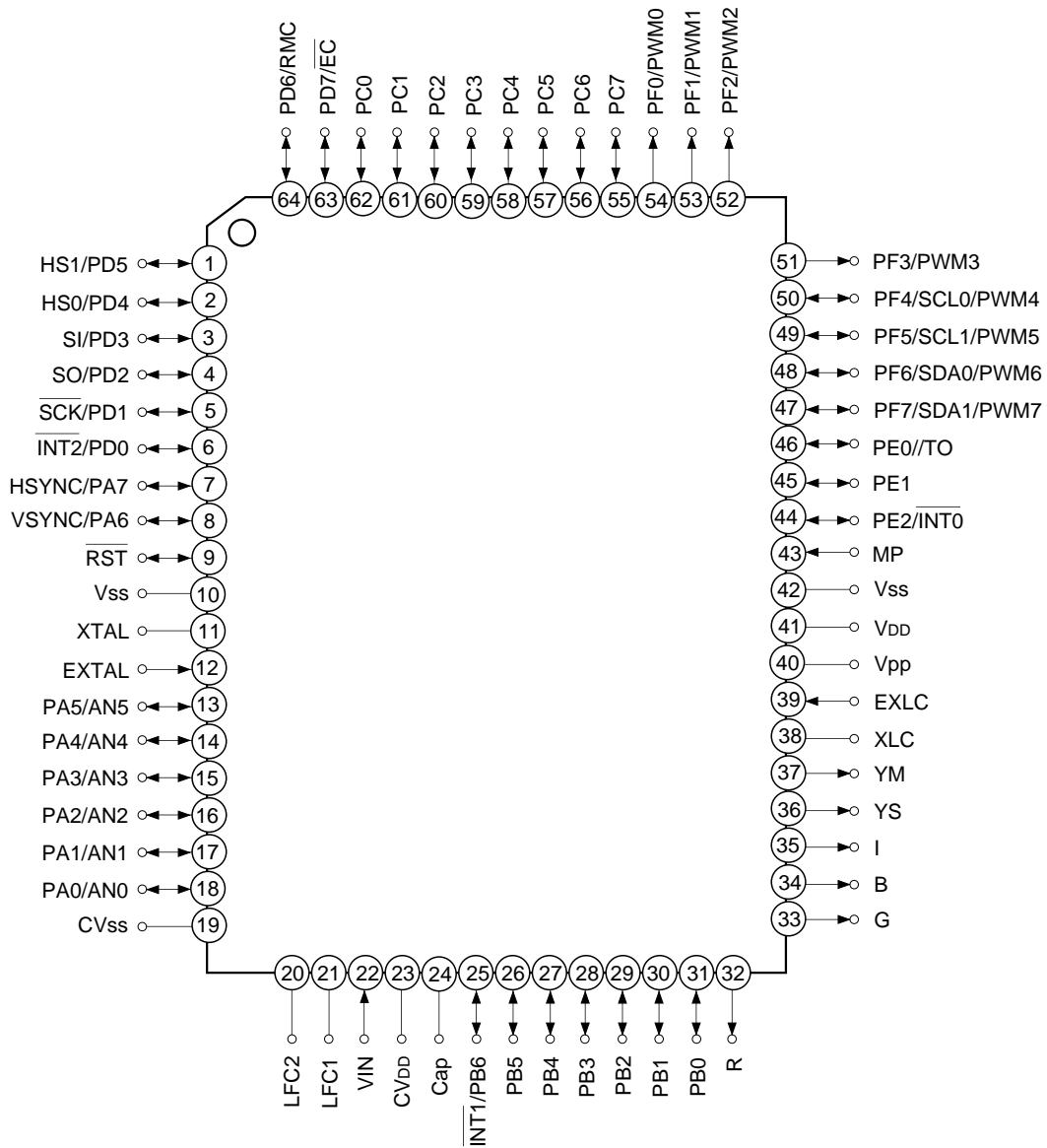
Block Diagram

Pin Assignment (Top View) 64-pin SDIP



- Note)** 1. Vpp (Pin 46) must be connected to VDD.
 2. Vss (Pins 16 and 48) must be connected to GND.
 3. MP (Pin 49) must be connected to GND.

Pin Assignment (Top View) 64-pin QFP



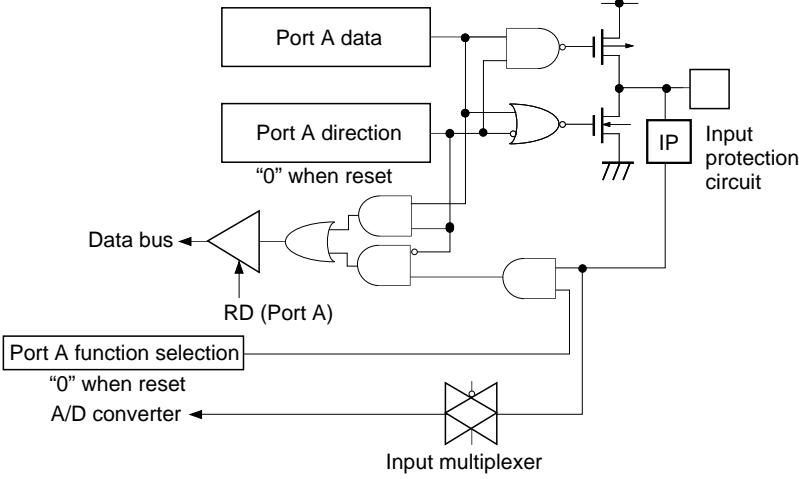
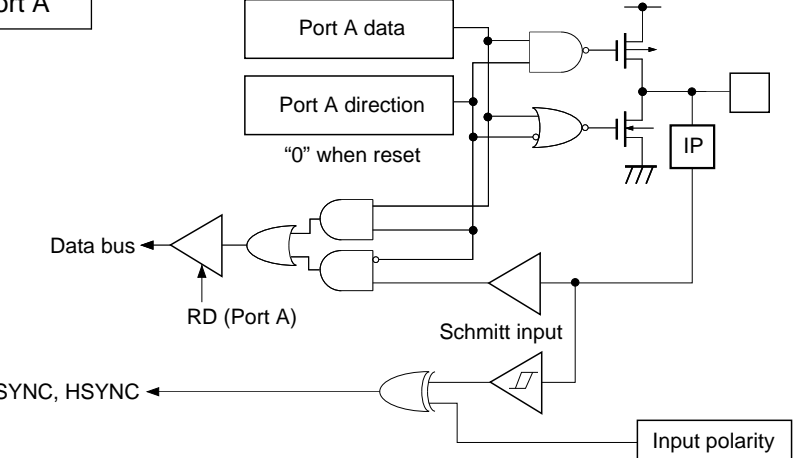
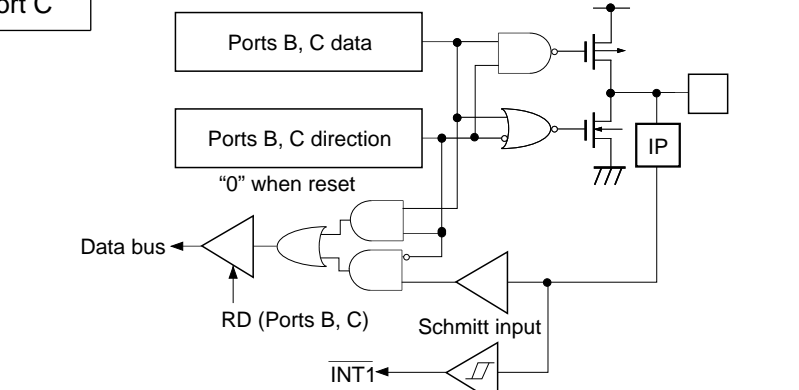
- Note**
1. Vpp (Pin 40) must be connected to VDD.
 2. Vss (Pins 10 and 42) must be connected to GND.
 3. MP (Pin 43) must be connected to GND.

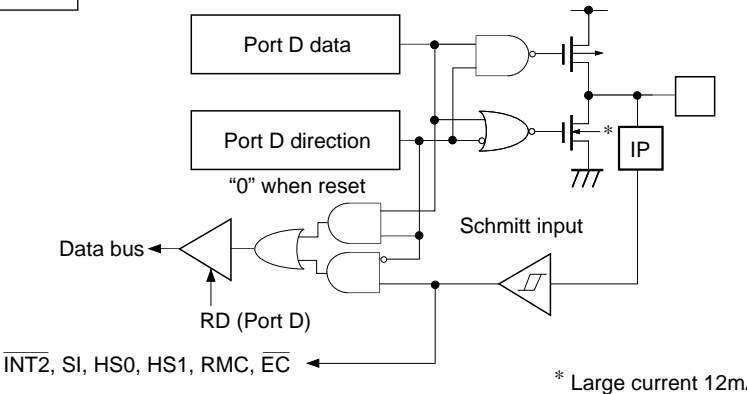
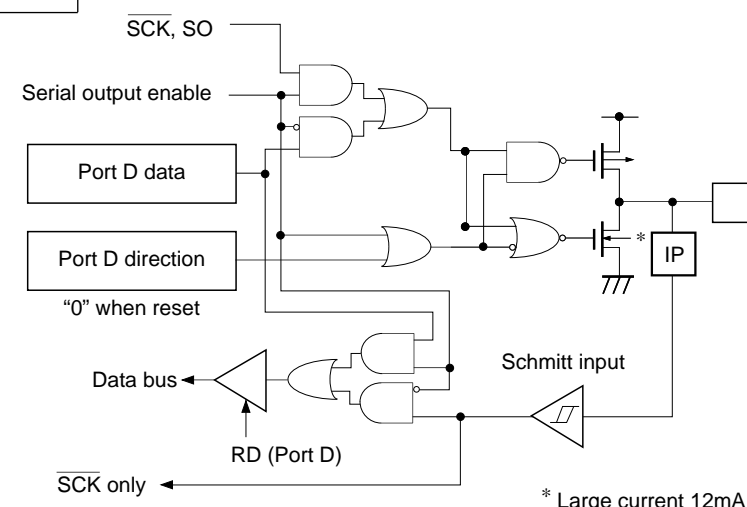
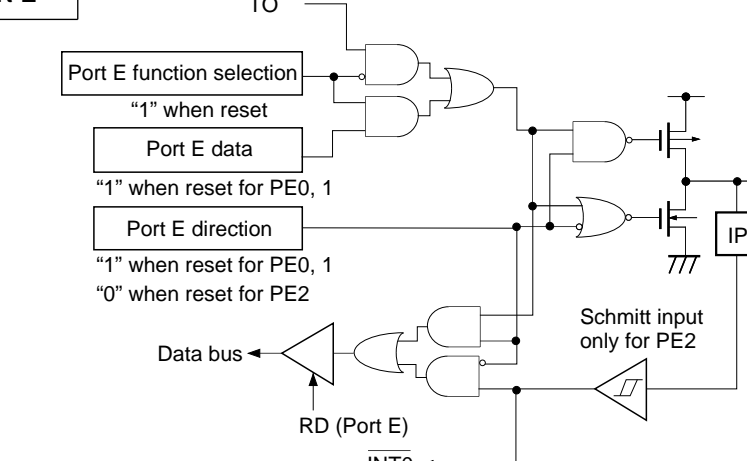
Pin Description

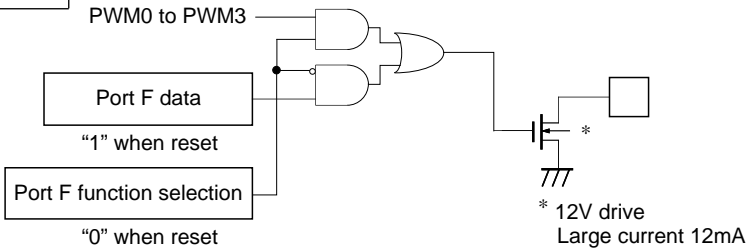
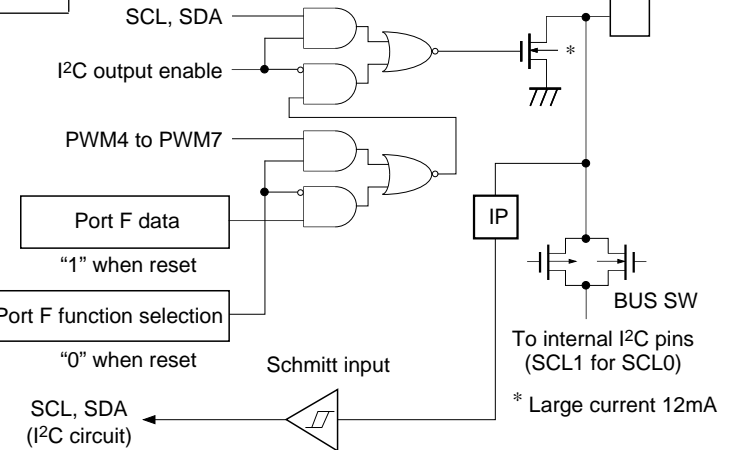
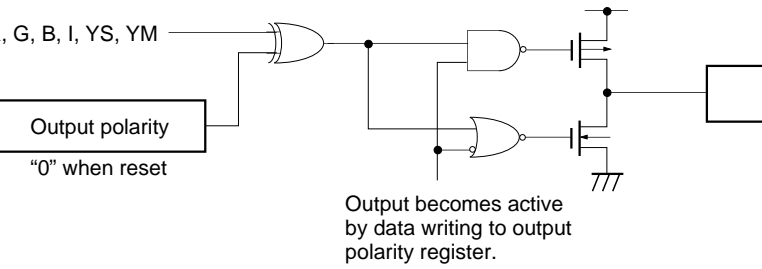
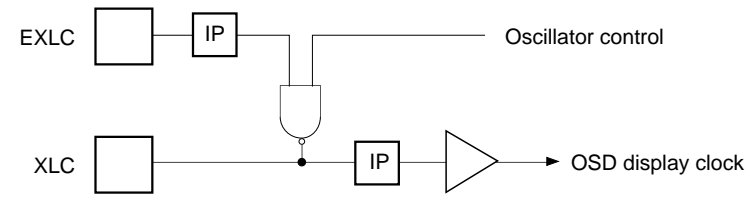
Symbol	I/O	Description	
PA0/AN0 to PA5/AN5	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.
PB0 to PB5	I/O	(Port B) 7-bit I/O port. I/O can be set in a unit of single bits. (7 pins)	
PB6/ $\overline{\text{INT1}}$	I/O/Input		External interruption request input. Active at the falling edge.
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA synk current. (8 pins)	External interruption request input. Active at the falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.
PD6/RMC	I/O/Input		Remote control reception circuit input.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.
PE0/TO	I/O/Output	(Port E) 3-bit I/O port. I/O can be set in a unit of single bits. (3 pins)	Rectangular wave output for timer/counter.
PE1	I/O		
PE2/ $\overline{\text{INT0}}$	I/O/Input		Input for external interruption request. Active at the falling edge.
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-ch open drain output. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM outputs. (8 pins)
PF4/SCL0/PWM4 PF5/SCL1/PWM5	Output/I/O		Transfer clock I/O for I ² C bus interface. (2 pins)
PF6/SDA0/PWM6 PF7/SDA1/PWM7	Output/I/O		Transfer data I/O for I ² C bus interface. (2 pins)
R, G, B, I, YS, YM	Output	6-bit OSD display outputs. (6 pins)	

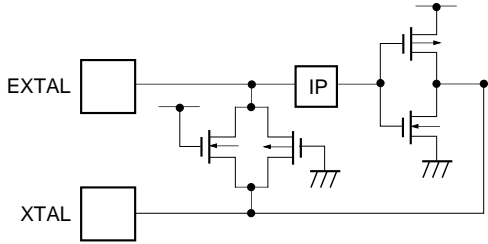
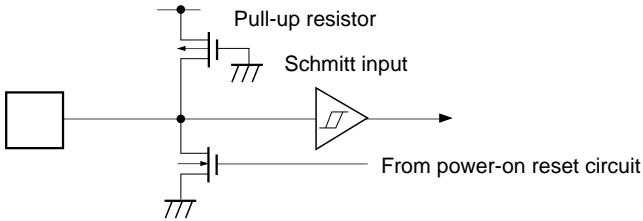
Symbol	I/O	Description
EXLC	Input	OSD display clock oscillation I/O. Oscillator frequency is determined by the external L and C.
XLC	Output	
VIN	Input	External composite video signal input. Input a 2Vp-p signal via a capacitor.
Cap	—	Connects a capacitor for the data slicer between Cap and CVss.
LFC1, LFC2	—	Connects a capacitor for the PLL circuit LPF between LFC1 and LFC2.
CVDD		Positive power supply for data slicer.
CVss		GND for data slicer.
EXTAL	Input	Connects a crystal for system clock oscillation. When an external clock is supplied, input it to EXTAL and leave XTAL open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset; active at Low level. I/O pin. Outputs a Low level when the power is turned on and the power-on reset function operates.
MP	Input	Test mode input. Must be connected to GND.
Vpp		Positive power supply for internal PROM writing. Under normal conditions, connect to VDD.
VDD		Positive power supply.
Vss		GND. Connect two Vss pins to GND.

Input/Output Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p>	<p>Port A</p>  <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" when reset A/D converter</p> <p>Input multiplexer</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>
<p>PA6/VSYNC PA7/HSYNC</p> <p>2 pins</p>	<p>Port A</p>  <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>VSYNC, HSYNC</p> <p>Schmitt input</p> <p>Input polarity "0" when reset</p>	<p>Hi-Z</p>
<p>PB0 to PB5 PB6/INT1 PC0 to PC7</p> <p>15 pins</p>	<p>Port B</p> <p>Port C</p>  <p>Ports B, C data</p> <p>Ports B, C direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports B, C)</p> <p>INT1</p> <p>Schmitt input</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0/$\overline{\text{INT2}}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{\text{EC}}$</p> <p>6 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD1/$\overline{\text{SCK}}$ PD2/SO</p> <p>2 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/TO PE1 PE2/$\overline{\text{INT0}}$</p> <p>3 pins</p>	<p>Port E</p>  <p>Schmitt input only for PE2</p>	<p>PE0, PE1: High level PE2: Hi-Z</p>

Pin	Circuit format	When reset
<p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p>	<p>Port F</p>  <p>* 12V drive Large current 12mA</p>	<p>Hi-Z</p>
<p>PF4/SCL0/PWM4 PF5/SCL1/PWM5 PF6/SDA0/PWM6 PF7/SDA1/PWM7</p> <p>4 pins</p>	<p>Port F</p>  <p>* Large current 12mA</p> <p>To internal I2C pins (SCL1 for SCL0)</p>	<p>Hi-Z</p>
<p>R G B I YS YM</p> <p>6 pins</p>	 <p>Output becomes active by data writing to output polarity register.</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>	 <p>Oscillator control</p> <p>OSD display clock</p>	<p>Oscillation halted</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. (This device does not enter the stop mode.) 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p> <p>From power-on reset circuit</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Medium drive output voltage	V _{OUTP}	-0.3 to +15.0	V	PF0 to PF3 pins
High level output current	I _{OH}	-5	mA	
High level total output current	ΣI _{OH}	-50	mA	Total of all output pins
Low level output current	I _{OL}	15	mA	Ports excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current output port (value per pin)* ²
Low level total output current	ΣI _{OL}	100	mA	Total of all output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	1000	mW	SDIP-64P-01
		600	mW	QFP-64P-L01

*¹ V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*² The large current output port is Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.5	5.5	V	Guaranteed data hold range for stop mode* ¹
	V _{pp}	V _{pp} = V _{DD}		V	* ⁶
Data slicer supply voltage	CV _{DD}	4.5	5.5	V	* ⁵
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	* ³
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	* ³
	V _{ILEX}	-0.3	0.4	V	EXTAL pin* ⁴
Operating temperature	T _{opr}	-10	+75	°C	

*¹ This device does not enter the stop mode.

*² PA, PB, PC, PE0 to PE1, SCL0 to SCL1, SDA0 to SDA1 pins.

*³ INT2, SCK, SO, SI, HS0, HS1, RMC, EC, INT1, HSYNC, VSYNC, RST pins.

*⁴ Specifies only during external clock input.

*⁵ CV_{DD} and V_{DD} should be set to the same voltage.

*⁶ V_{pp} and V_{DD} should be set to the same voltage.

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PD, PE, R, G, B, I, YS, YM	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA to PD, PE, R, G, B, I, YS, YM, PF0 to PF3, RST*1	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PD, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V
			VDD = 4.5V, IOL = 4.0mA			0.6	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiHL		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiLR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
I/O leakage current	IIZ	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Open drain output leakage current (in N-ch Tr OFF state)	ILOH	PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA
I ² C bus switch connection impedance (in output Tr OFF state)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω
Supply current	IDD	VDD*3	1/2 frequency dividing clock operation VDD = 5.5V 12MHz crystal oscillation (C1 = C2 = 15pF)		43	55	mA
	IDDSL		Sleep mode VDD = 5.5V 12MHz crystal oscillation (C1 = C2 = 15pF)		2.5	5.5	mA
	IDDST		Stop mode*4 VDD = 5.5V Termination of 12MHz crystal oscillation	—	—	—	μA
	ICVDD		CVDD	VDD = 5.5V	—	5.0	10.0
Input capacitance	CIN	PA to PE, SCL, SDA, EXLC, EXTAL, VIN, RST	1MHz clock 0V for no-measured pins		10	20	pF

*1 Specifies RST pin only when the power-on reset circuit is selected with mask option.

*2 For RST pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistance is selected.

*3 When all output pins are left open. Specifies only when the OSD oscillation is halted.

*4 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2		12.0		MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall times	t _{CR} , t _{CF}	EXTAL	Fig 1, Fig 2 External clock drive			200	ns
Event counter input clock pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	t _{sys} *1 + 50			ns
Event counter input clock rise and fall times	t _{ER} , t _{EF}	\overline{EC}	Fig. 3			20	ms

*1 Indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

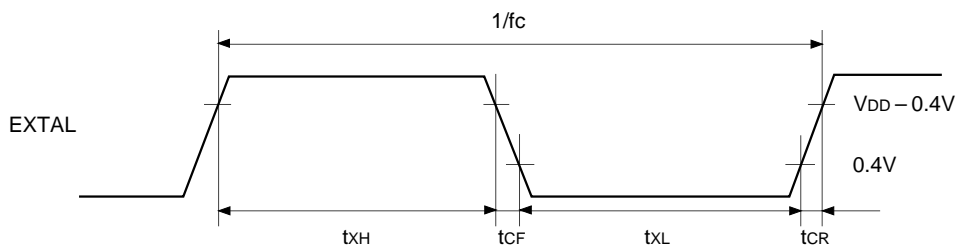


Fig. 2. Clock applied condition

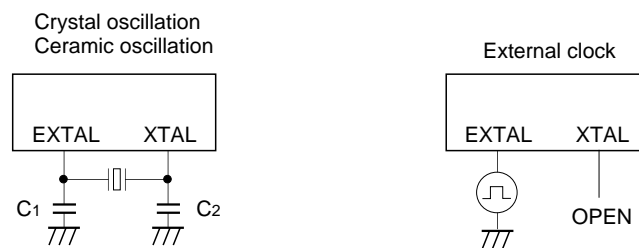
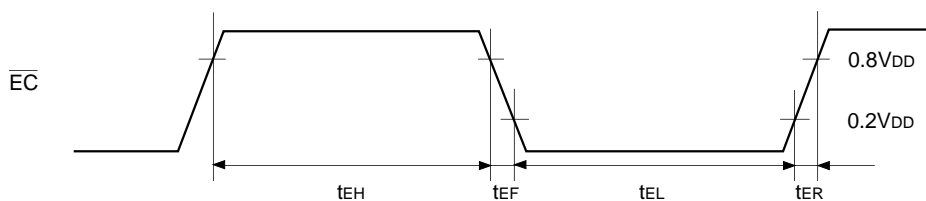


Fig. 3. Event count clock timing



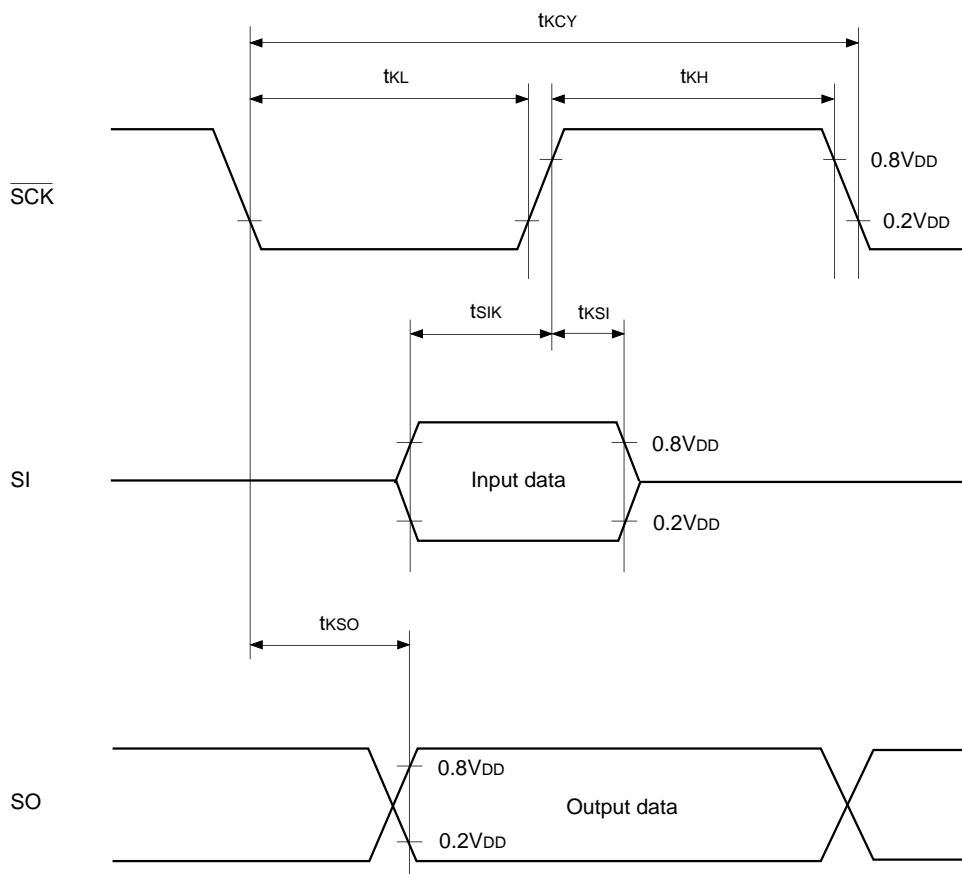
(2) Serial transfer

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH}	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	t_{KL}		$\overline{\text{SCK}}$ output mode	$4000/f_c - 50$		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 4. Serial transfer timing

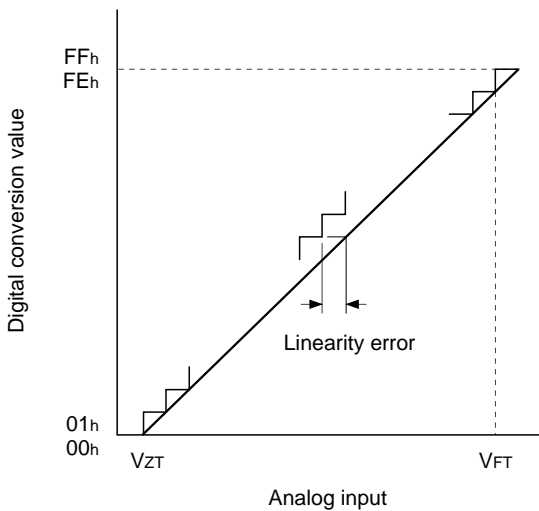


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			± 3	LSB
Zero transition voltage	V_{ZT}^{*1}			-10	10	70	mV
Full-scale transition voltage	V_{FT}^{*2}			4910	4970	5030	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Analog input voltage	V_{IAN}	AN0 to AN5		0		V_{DD}	V

Fig. 5. Definitions of A/D converter terms



- *1 Value at which the digital conversion value changes from 00h to 01h and vice versa.
- *2 Value at which the digital conversion value changes from FEh to FFh and vice versa.
- *3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEh).

PCK1, 0	CKS	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH}	$\overline{\text{INT0}}$		1		μs
	t_{IL}	$\overline{\text{INT1}}$ $\overline{\text{INT2}}$				
Reset input Low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 6. Interruption input timing

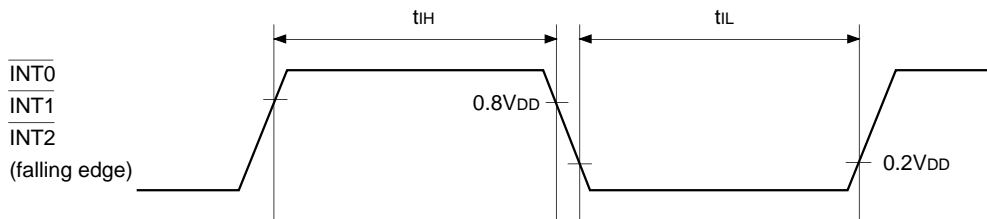
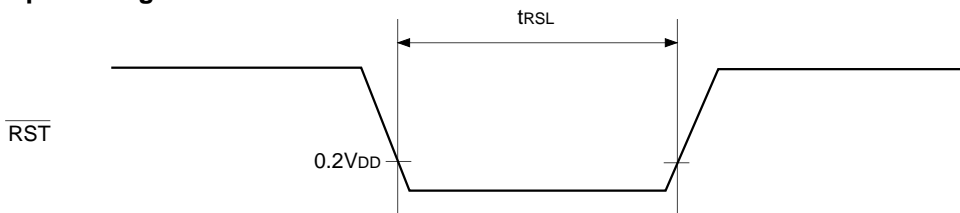


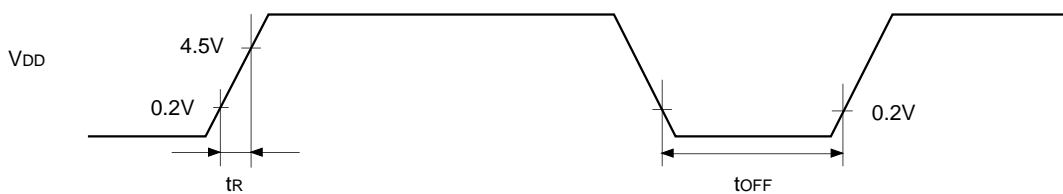
Fig. 7. $\overline{\text{RST}}$ input timing



(5) Power-on reset ($T_a = -10$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cutt-off time	t_{OFF}		Repeated power-on reset	1		ms

Fig. 8. Power-on reset



Take care when turning the power on.

(6) I²C bus timing

(T_a = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	SCL		0	100	kHz
Bus-free time before starting transfer	t _{BUF}	SDA, SCL		4.7		μs
Hold time for starting transfer	t _{HD; STA}	SDA, SCL		4.0		μs
Clock Low level width	t _{LOW}	SCL		4.7		μs
Clock High level width	t _{HIGH}	SCL		4.0		μs
Setup time for repeated transfers	t _{SU; STA}	SDA, SCL		4.7		μs
Data hold time	t _{HD; DAT}	SDA, SCL		0*1		μs
Data setup time	t _{SU; DAT}	SDA, SCL		250		ns
SDA, SCL rise time	t _R	SDA, SCL			1	μs
SDA, SCL fall time	t _F	SDA, SCL			300	ns
Setup time for transfer completion	t _{SU; STO}	SDA, SCL		4.7		μs

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

Fig. 9. I²C bus transfer timing

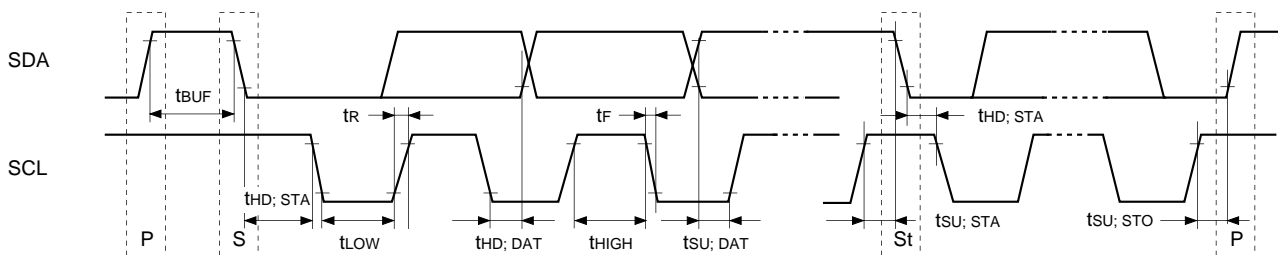
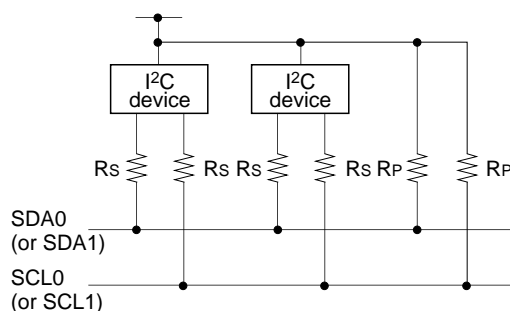


Fig. 10. I²C device recommended circuit



- A pull-up resistor (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (R_s = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD timing

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
OSD clock frequency	f _{OSC}	EXLC XLC	Fig. 12	4	16.5	MHz
HSYNC pulse width	t _{HWD}	HSYNC	Fig. 11	1.2		μs
HSYNC after-write rise and fall times	t _{HCG}	HSYNC	Fig. 11		200	ns
VSYNC before-write rise and fall times	t _{VCG}	VSYNC	Fig. 11		1.0	μs

Fig. 11. OSD timing

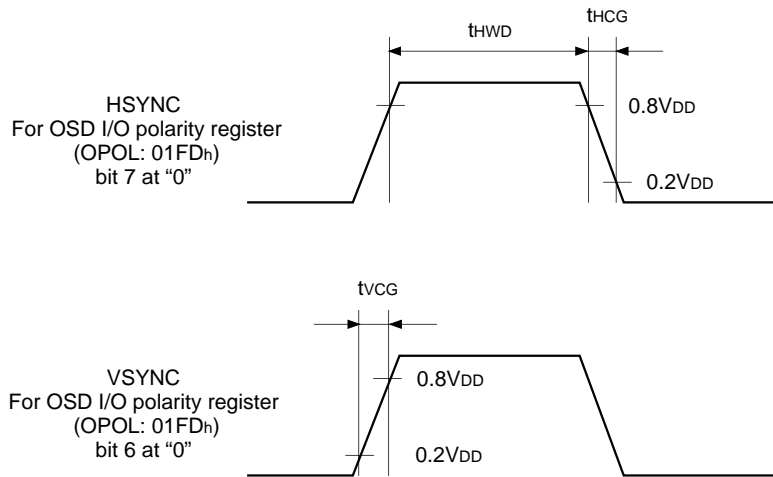
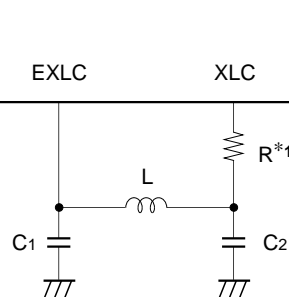


Fig. 12. LC oscillation circuit connection



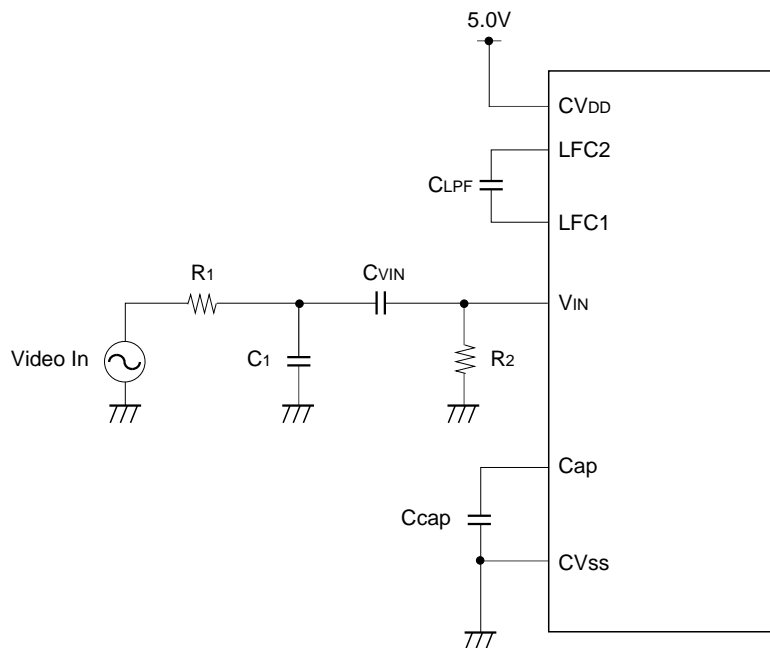
*1 The XLC series resistor can reduce the frequency of occurrence of the undersired radiation.

(8) Data slicer external circuit

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Remarks
VIN pin coupling capacitance	C_{VIN}	VIN		0.1		μF	The B characteristic or more of temperature characteristics is recommended.
Cap pin capacitance	Ccap	Cap		4700		pF	The B characteristic or more of temperature characteristics is recommended.
PLL low-pass filter capacitance	C_{LPF}	LFC1, LFC2		0.47		μF	The B characteristic or more of temperature characteristics is recommended.
Composite video signal input	Video In	VIN		2.0		Vp-p	

Fig. 13. Data slicer external recommended circuit



[Recommended Constant]

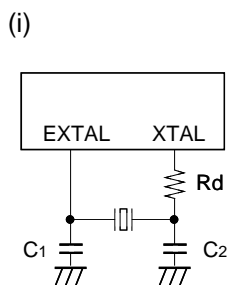
$R_1 = 220\Omega$ (error: 5%; allowable power dissipation: 1/8W or more)

$R_2 = 1\text{M}\Omega$ (error: 5%; allowable power dissipation: 1/8W or more)

$C_1 = 1200\text{pF}$ (ceramic), the B characteristic or more of temperature characteristics is recommended.

Appendix

Fig. 14. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	R _d (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	12.0	5	5	0*1	(i)
KINSEKI LTD.	HC-19/U (-S)	12.0	15	15	0*1	(i)

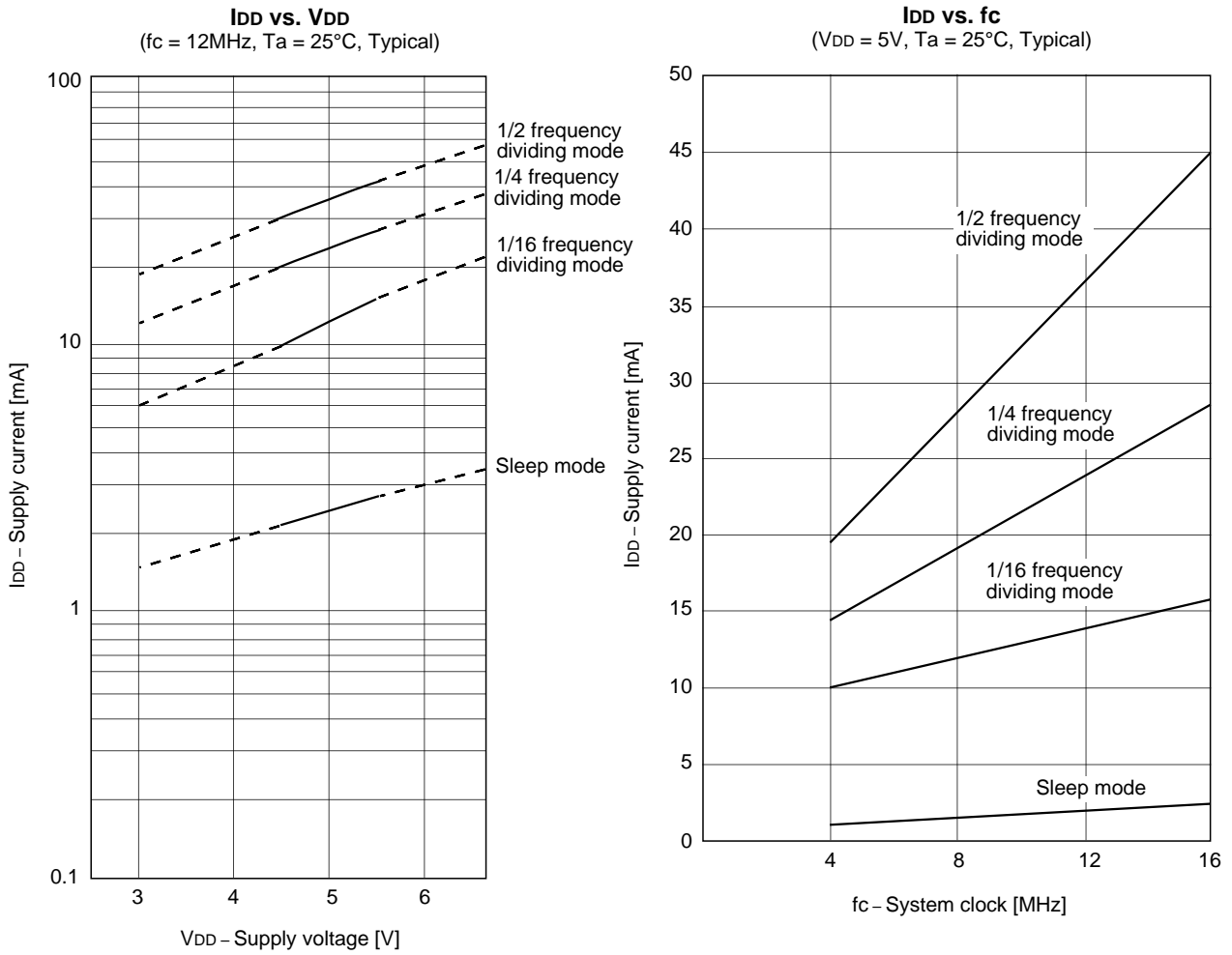
*1 The XTAL series resistor can reduce the effect of electrostatic discharge noise.

Products List

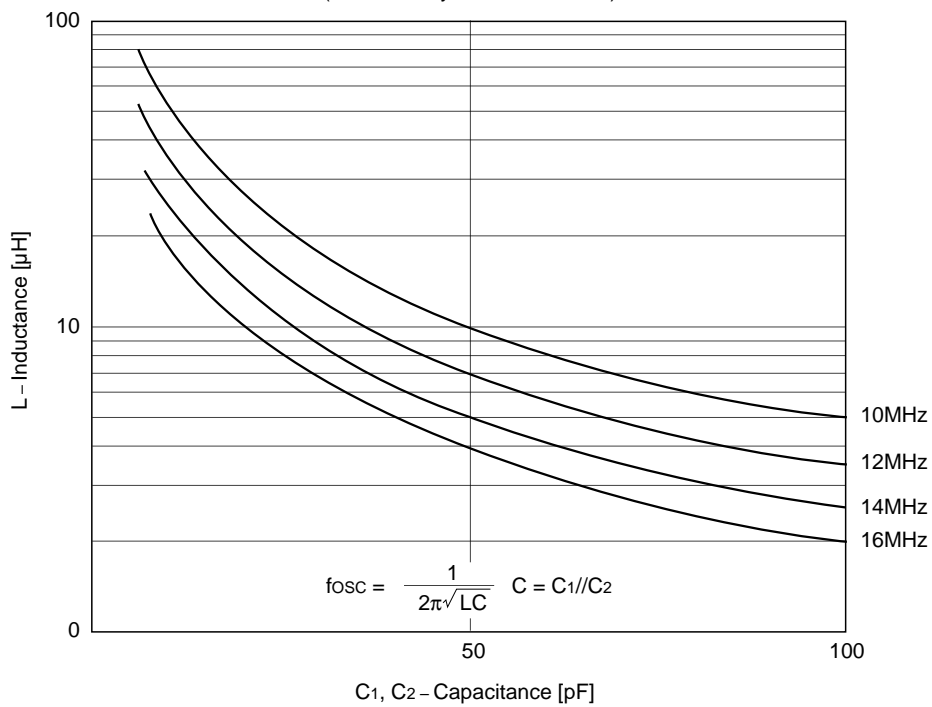
Option item	Mask	CXP858P56AS-1-□□□ CXP858P56AQ-1-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP
Program ROM capacity	40/48/56K bytes	PROM 56K bytes
Reset-pin pull-up resistor	Existent/Non-existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent
Font data	User specified	User specified (PROM)*2

*2 The font data for the one-time PROM version can be written in the same way as for the program.

Fig. 15. Characteristics curves



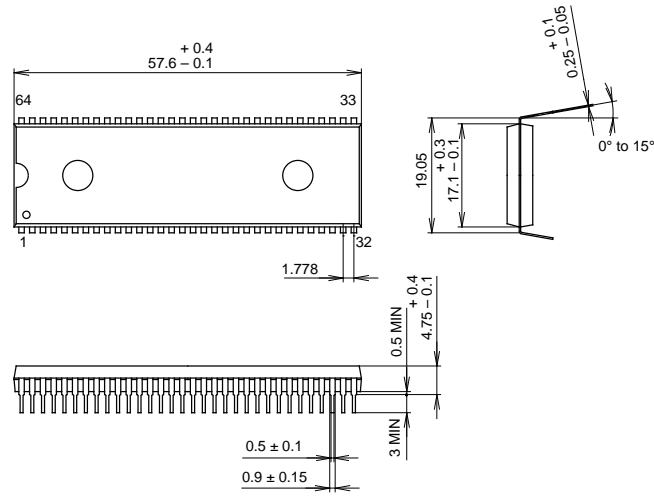
Parameter curve for OSD oscillation L vs. C
(Theoretically calculated value)



Package Outline

Unit: mm

64PIN SDIP (PLASTIC) 750mil

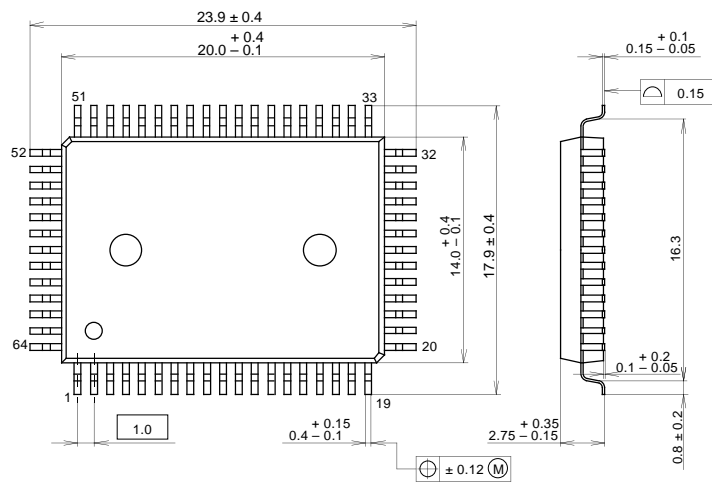


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750-A
JEDEC CODE	

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g