# SONY

CXP864P61

CMOS 8-bit Single Chip Microcomputer

Description

The CXP864P61 is the CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I2C bus interface, PWM output, remote control reception circuit, HSYNC counter, watchdog timer, 32kHz timer/counter besides the basic configurations of 8-bit CPU, PROM, RAM, I/O ports.

The CXP864P61 also provides a sleep function that enables to lower the power consumption.

The CXP864P61 is the PROM-incorporated version of the CXP86461 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.
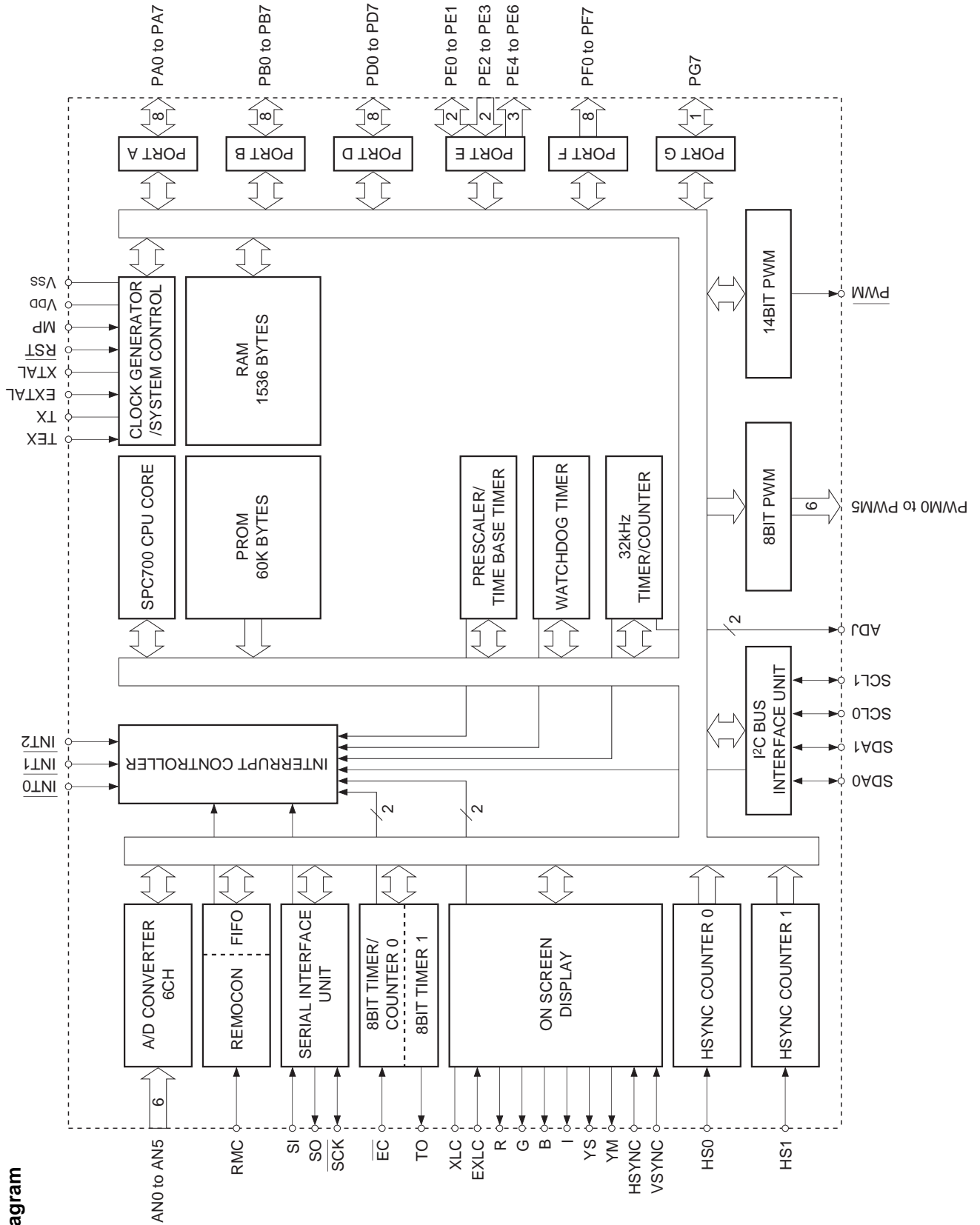
52 pin SDIP (Plastic)
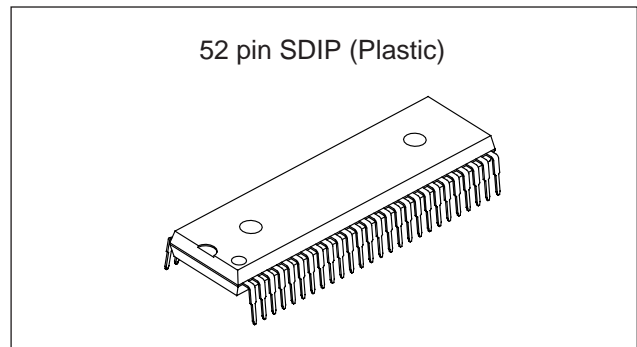
Structure
Silicon gate CMOS IC

Features
- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle   250ns at 16MHz operation (4.5 to 5.5V)
  - 122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated PROM   60K bytes
- Incorporated RAM   1536 bytes (Excludes VRAM for on-screen display and sprite RAM)
- Peripheral functions
  - — A/D converter   8 bits, 6 channels, successive approximation method
    (Conversion time of 3.25µs at 16 MHz)
  - — Serial interface   8-bit clock sync type, 1 channel
  - — Timer   8-bit timer
    - 8-bit timer/counter
    - 19-bit time-base timer
    - 32kHz timer/counter
  - — On-screen display (OSD) function 12×16 dots, 52 character types
    - 15 character colors, 2 lines $\times$ 24 characters,
    - frame background 8 colors/ half blanking,
    - background on full screen 15 colors/ half blanking
    - edging/ shadowing/ rounding for every line,
    - background with shadow for every character, double scanning,
    - sprite OSD, 12×16 dots, 1 screen, 8 colors for every dot
  - — I2C bus interface
  - — PWM output   8 bits, 8 channels
    - 14 bits, 1 channel
  - — Remote control reception circuit   8-bit pulse measurement counter, 6-stage FIFO
  - — HSYNC counter   2 channels
  - — Watchdog timer
- Interruption   13 factors, 13 vectors, multi-interruption possible
- Standby mode   Sleep
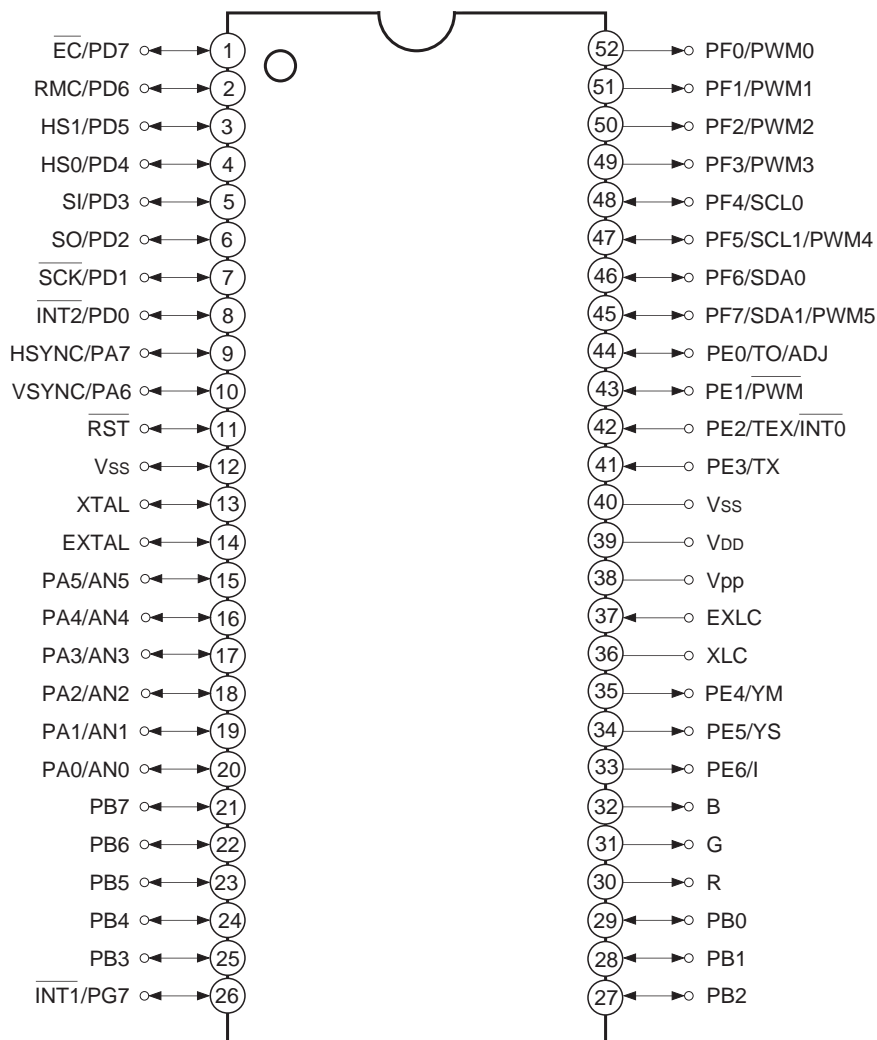- Package   52-pin plastic SDIP

E97740A84

Block Diagram

Pin Assignment (Top View)

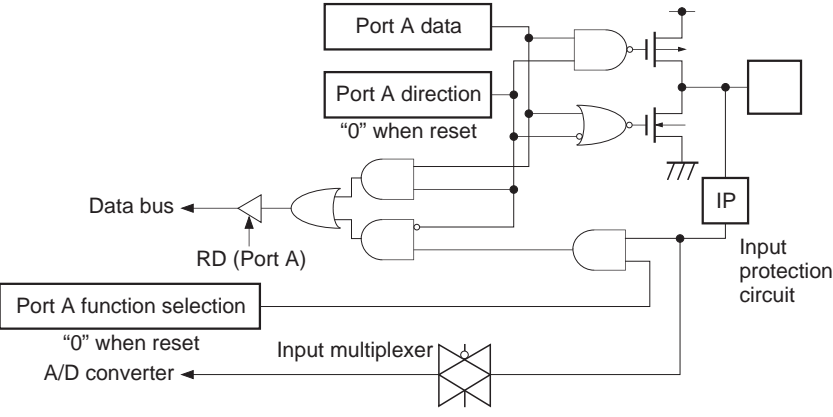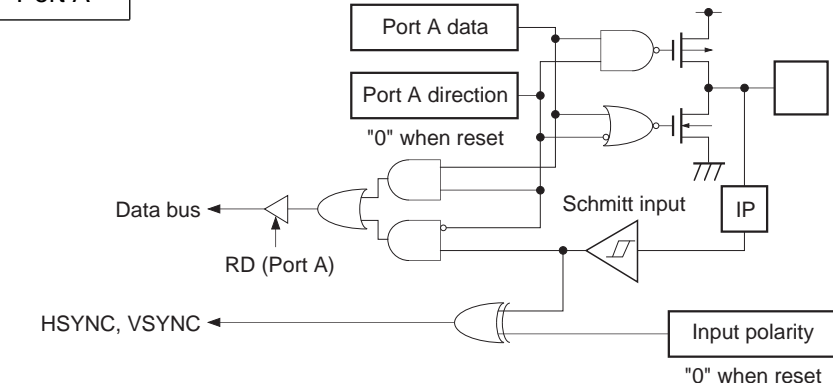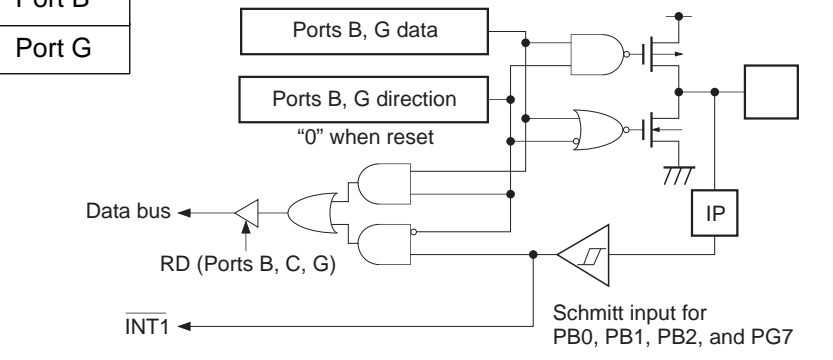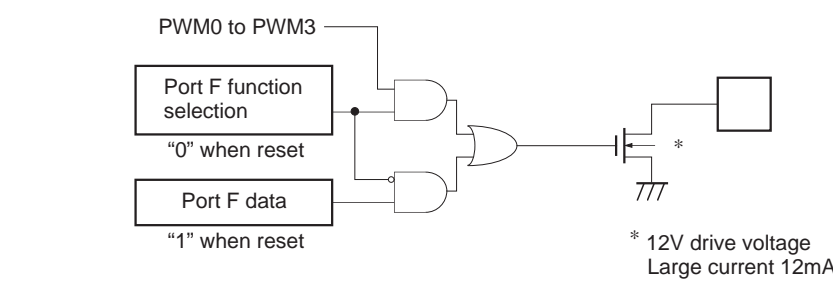| Left pin	No.		No.	Right pin
$\overline{EC}$/PD7	1		52	PF0/PWM0
RMC/PD6	2		51	PF1/PWM1
HS1/PD5	3		50	PF2/PWM2
HS0/PD4	4		49	PF3/PWM3
SI/PD3	5		48	PF4/SCL0
SO/PD2	6		47	PF5/SCL1/PWM4
$\overline{SCK}$/PD1	7		46	PF6/SDA0
$\overline{INT2}$/PD0	8		45	PF7/SDA1/PWM5
HSYNC/PA7	9		44	PE0/TO/ADJ
VSYNC/PA6	10		43	PE1/$\overline{PWM}$
$\overline{RST}$	11		42	PE2/TEX/$\overline{INT0}$
Vss	12		41	PE3/TX
XTAL	13		40	Vss
EXTAL	14		39	VDD
PA5/AN5	15		38	Vpp
PA4/AN4	16		37	EXLC
PA3/AN3	17		36	XLC
PA2/AN2	18		35	PE4/YM
PA1/AN1	19		34	PE5/YS
PA0/AN0	20		33	PE6/I
PB7	21		32	B
PB6	22		31	G
PB5	23		30	R
PB4	24		29	PB0
PB3	25		28	PB1
$\overline{INT1}$/PG7	26		27	PB2

Note)

1. Vpp (Pin 38) is left open.
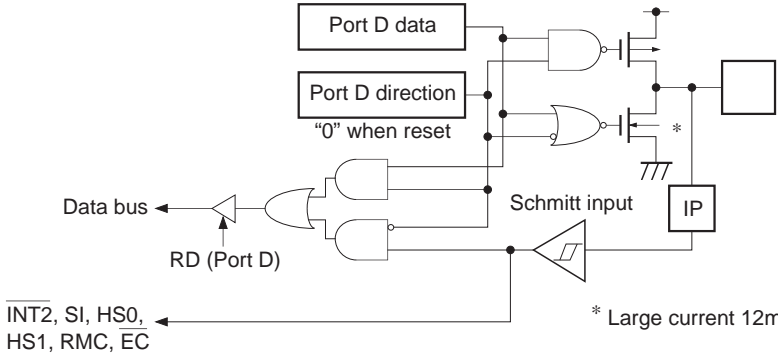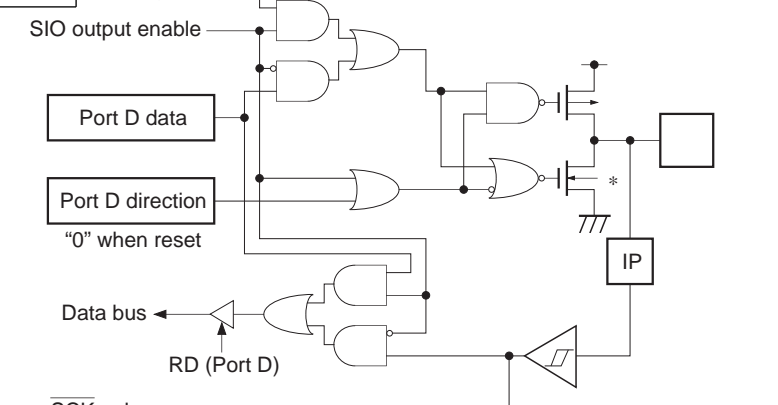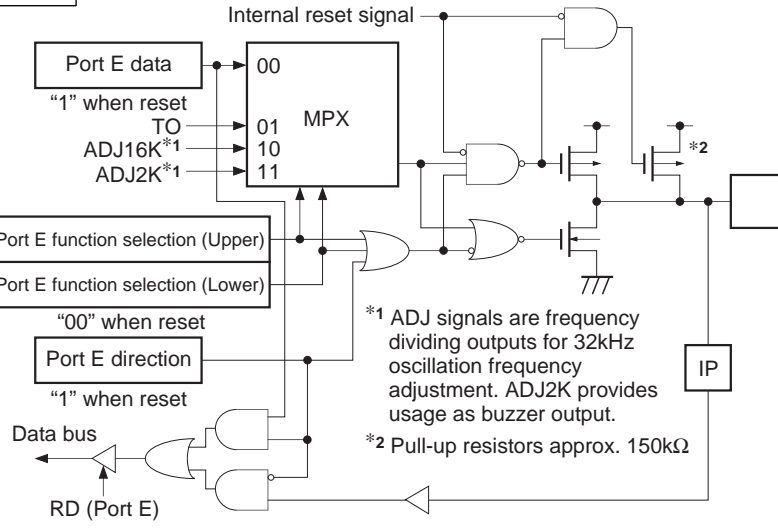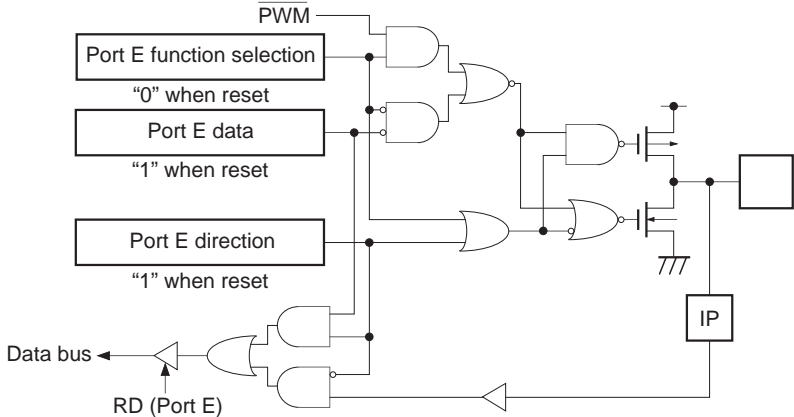2. Vss (Pins 12 and 40) are both connected to GND.

Pin Description

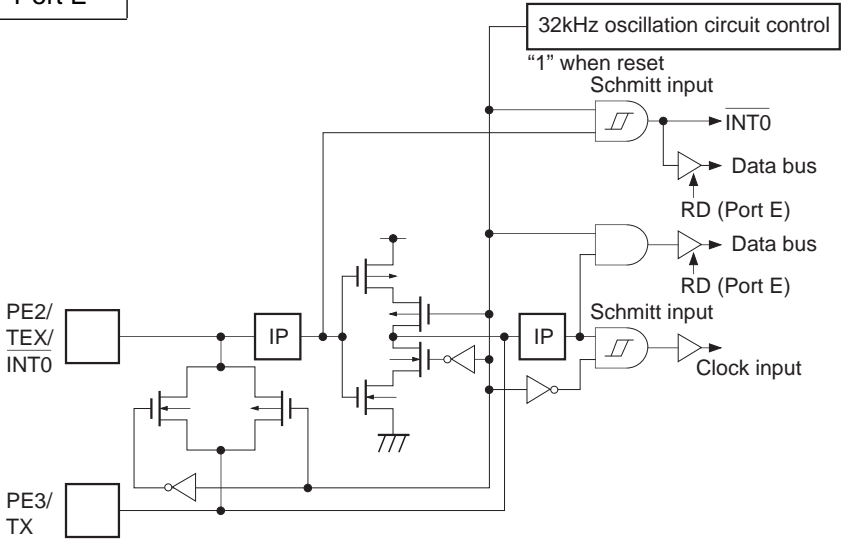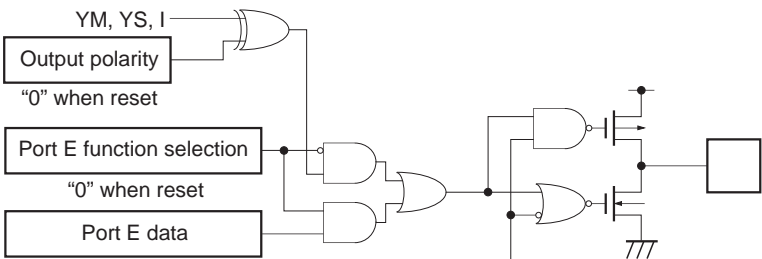| Symbol	I/O	Description		
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)	
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.	
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.	
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PD0/$\overline{INT2}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA synk current. (8 pins)	External interruption request input. Active at the falling edge.	
PD1/$\overline{SCK}$	I/O/I/O		Serial clock I/O.	
PD2/SO	I/O/Output		Serial data output.	
PD3/SI	I/O/Input		Serial data input.	
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.	
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.	
PD6/RMC	I/O/Input		Remote control reception circuit input.	
PD7/$\overline{EC}$	I/O/Input		External event input for timer/counter.	
PE0/TO/ADJ	I/O/Output/ Output	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single bit. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)	Rectangular wave output for 8-bit timer/counter.	32kHz oscillation frequency dividing output.
PE1/$\overline{PWM}$	I/O/Output		14-bit PWM output.	
PE2/TEX/$\overline{INT0}$	Input/Input/ Input		Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.	External interruption request input. Active at the falling edge.
PE3/TX	Input/Output			
PE4/YM	Output/Output		OSD display 6-bit output. (6 pins)	
PE5/YS	Output/Output			
PE6/I	Output/Output			
B	Output			
G	Output			
R	Output			
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port. Open drain output of large current (12mA) and N channel. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (4 pins)	
PF4/SCL0	Output/I/O		I^2C bus interface transfer clock I/O. (2 pins)	
PF5/SCL1/ PWM4	Output/I/O/ Output			8-bit PWM output.
PF6/SDA0	Output/I/O		I^2C bus interface transfer data I/O. (2 pins)	
PF7/SDA1/ PWM5	Output/I/O/ Output			8-bit PWM output.

Symbol	I/O	Description	
PG7/$\overline{INT1}$	I/O/Input	(Port G) 1-bit I/O port. I/O can be set in a unit of single bits. (1 pin)	External interruption request input. Active at the falling edge.
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.	
XTAL	Output		
$\overline{RST}$	Input	System reset; active at Low level.	
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.	
XLC	Output		
V$_{DD}$		Positive power supply.	
Vss		GND. Connect two Vss pins to GND.	
Vpp		Positive power supply for incorporated-PROM writing. No connected for normal operation.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA5/AN5 6 pins		Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins		Hi-Z
PB0 to PB7 PG7/INT1 9 pins		Hi-Z
PF0/PWM0 to PF3/PWM3 4 pins		Hi-Z

Pin	Circuit format	When reset
PD0/$\overline{\text{INT2}}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{\text{EC}}$ 6 pins	**Port D** Port D data Port D direction — "0" when reset Data bus ← RD (Port D) $\overline{\text{INT2}}$, SI, HS0, HS1, RMC, $\overline{\text{EC}}$ Schmitt input — IP * Large current 12mA	Hi-Z
PD1/$\overline{\text{SCK}}$ PD2/SO 2 pins	**Port D** $\overline{\text{SCK}}$, SO SIO output enable Port D data Port D direction — "0" when reset Data bus ← RD (Port D) $\overline{\text{SCK}}$ only IP * Large current 12mA PD2 is not Schmitt input.	Hi-Z
PE0/TO/ADJ 1 pin	**Port E** Internal reset signal Port E data — "1" when reset — 00 TO — 01 MPX ADJ16K*1 — 10 ADJ2K*1 — 11 Port E function selection (Upper) Port E function selection (Lower) — "00" when reset Port E direction — "1" when reset Data bus ← RD (Port E) *2 IP *1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output. *2 Pull-up resistors approx. 150kΩ	High level (with the resistor of pull-up transister ON when reset)

Pin	Circuit format	When reset
PE1/$\overline{\text{PWM}}$ 1 pin	**Port E** $\overline{\text{PWM}}$ Port E function selection "0" when reset Port E data "1" when reset Port E direction "1" when reset IP Data bus ◄ RD (Port E)	High level
PE2/TEX/$\overline{\text{INT0}}$ PE3/TX 2 pins	**Port E** 32kHz oscillation circuit control "1" when reset Schmitt input $\overline{\text{INT0}}$ Data bus RD (Port E) Data bus RD (Port E) PE2/ $\overline{\text{TEX}}$/ $\overline{\text{INT0}}$ IP IP Schmitt input Clock input PE3/ TX	Oscillation halted Port input
PE4/YM PE5/YS PE6/I 3 pins	**Port E** YM, YS, I Output polarity "0" when reset Port E function selection "0" when reset Port E data Writing data to output polarity register and port data register brings output to active.	Hi-Z

Pin	Circuit format	When reset
PF4/SCL0 PF5/SCL1/PWM4 PF6/SDA0 PF7/SDA1/PWM5 4 pins	**Port F** SCL, SDA I²C bus enable PWM4, PWM5 Port F function selection "0" when reset Port F data "1" when reset Schmitt input SCL, SDA (I²C bus circuit) IP * Large current 12mA BUS SW To internal I²C pins (SCL1 for SCL0)	Hi-Z
R G B 3 pins	R, G, B Output polarity "0" when reset Writing data to output polarity register brings output to active.	Hi-Z
EXLC XLC 2 pins	Oscillation control EXLC IP IP → OSD display clock XLC	Oscillation halted
EXTAL XTAL 2 pins	EXTAL IP XTAL • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. (This device does not enter the stop mode.)	Oscillation
$\overline{\text{RST}}$ 1 pin	Pull-up resistor Schmitt input	Low level

Absolute Maximum Ratings

(Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
	V_{PP}	−0.3 to +13.0	V	Incorporated PROM
Input voltage	V_{IN}	−0.3 to +7.0[*1]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*1]	V	
Medium drive output voltage	V_{OUTP}	−0.3 to +15.0	V	
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Ports excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current output ports (value per pin[*2])
Low level total output current	ΣI_{OL}	130	mA	Total of all output pins
Operating temperature	T_{opr}	−10 to +75	°C	
Storage temperature	T_{stg}	−55 to +150	°C	
Allowable power dissipation	P_D	400	mW	SDIP-52P-01

[*1] V_{IN} and V_{OUT} should not exceed $V_{DD} + 0.3$ V.
[*2] The large current output port is Port D (PD) and Port F (PF).
Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.7	5.5	V	Guaranteed operation range by TEX clock
		—	—	V	Guaranteed data hold operation range during stop[*5]
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[*1]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	[*2]
	V_{IHEX}	$V_{DD} − 0.4$	$V_{DD} + 0.3$	V	EXTAL pin[*3], TEX pin[*4]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[*1]
	V_{ILS}	0	$0.2V_{DD}$	V	[*2]
	V_{ILEX}	−0.3	0.4	V	EXTAL pin[*3], TEX pin[*4]
Operating temperature	T_{opr}	−10	+75	°C	

[*1] PA1 to 5, PB3 to 7, PD2, PE0, PE1, PE3, SCL0 to 1, SDA0 to 1 pins
[*2] VSYNC, HSYNC, INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, RST, PB0, PB1, PB2 pins
[*3] Specifies only during external clock input.
[*4] Specifies only during external event count input.
[*5] This device does not enter the stop mode.

Electrical Characteristics

DC characteristics
(Ta = −10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PD, PE0 to PE1, PE4 to PE6, PG7, R, G, B	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}	PA, PB, PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG7, R, G, B	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	μA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$[1]		−1.5		−400	μA
I/O leakage current	I_{IZ}	PA, PB, PD, PE, PG7, R, G, B, $\overline{RST}$[1]	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	μA
Open drain I/O leakage current (in N-ch Tr off state)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	μA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	μA
I²C bus switch connection impedance (in output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current[2]	I_{DD1}	V_{DD}	1/2 frequency dividing clock V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		25	38	mA
	I_{DD2}		V_{DD} = 3.3V, 32MHz crystal oscillation (C_1 = C_2 = 47pF)		30	90	μA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		1.2	2.1	mA
	I_{DDS2}		V_{DD} = 3.3V, 32MHz crystal oscillation (C_1 = C_2 = 47pF)		15	38	μA
	I_{DDS3}		Stop mode[3] V_{DD} = 5.5V, termination of 16MHz and 32MHz oscillation	—	—	—	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	PA, PB, PD, PE0 to PE3, R, G, B, PF,PG7, EXTAL, TEX, EXLC, $\overline{RST}$	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 For $\overline{RST}$ pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

*2 When all output pins are left open. Specifies only when the OSD oscillation is halted.

*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing
(Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig.2	8		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig.2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig.2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	4tsys[*1]			ns
Event count input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5 V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

[*1] tsys Indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

tsys (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
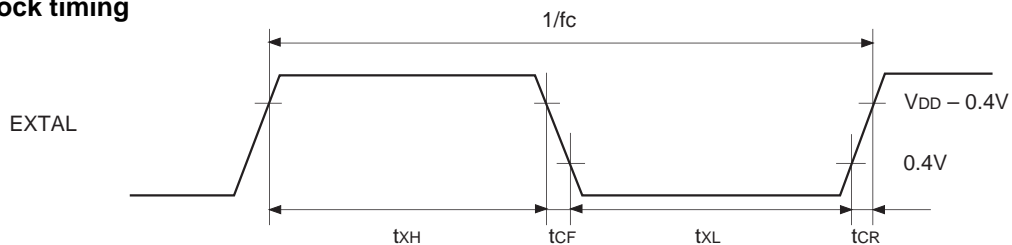
Fig. 1. Clock timing
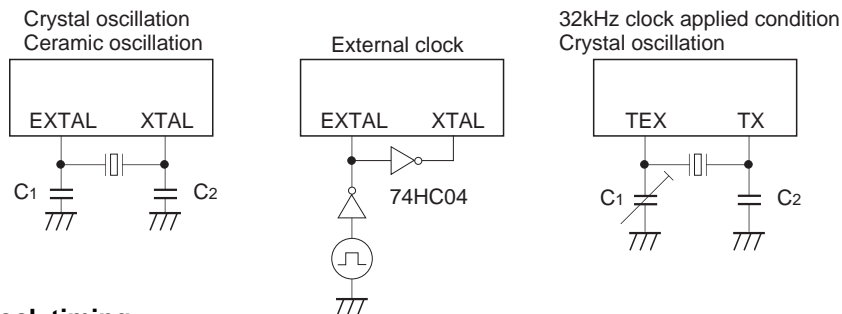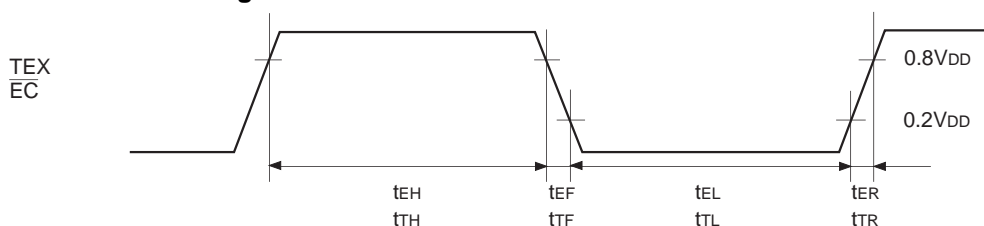

### Fig.2. Clock applied conditions

Fig. 3. Event count clock timing

(2) Serial transfer   (Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc − 50		ns
SI input setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing
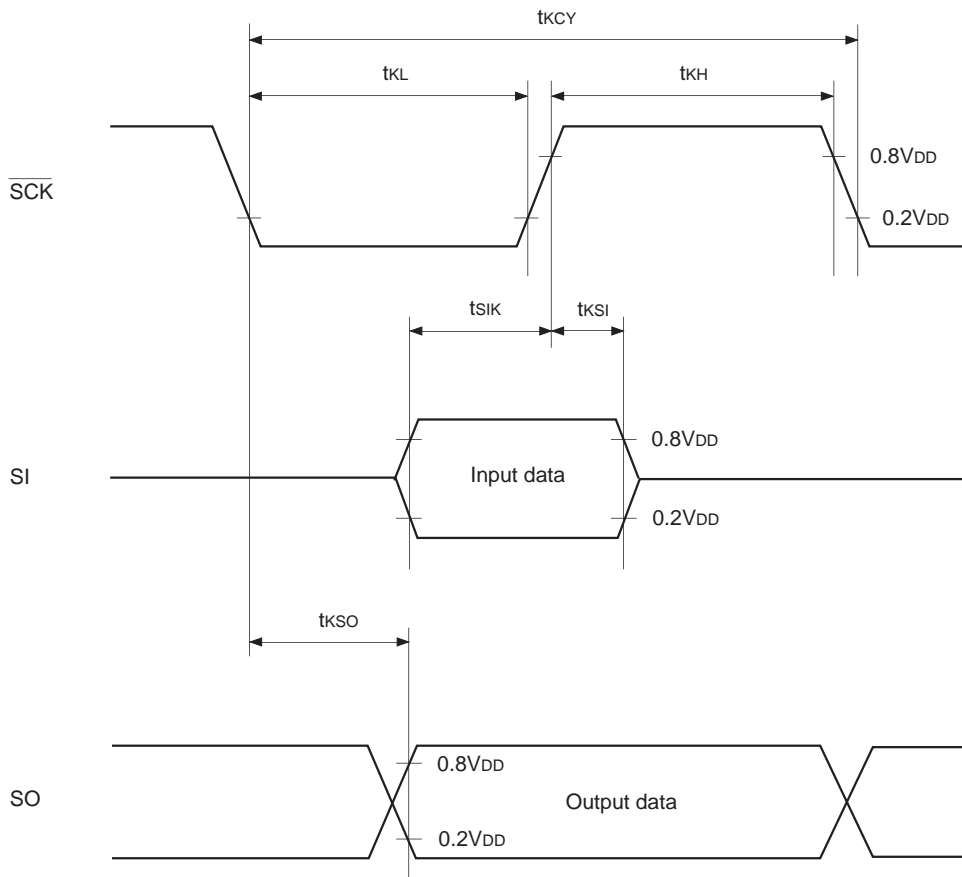
**(3) A/D converter** (Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{ss} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V_{ZT}[*1]		Ta = 25°C V_{DD} = 5.0V V_{ss} = 0V	−10	10	70	mV
Full-scale transition voltage	V_{FT}[*2]			4910	4970	5030	mV
Conversion time	t_{CONV}			$26/f_{ADC}$[*3]			μs
Sampling time	t_{SAMP}			$6/f_{ADC}$[*3]			μs
Analog input voltage	V_{IAN}	AN0 to AN5		0		V_{DD}	V

Fig. 5. Definitions for A/D converter terms
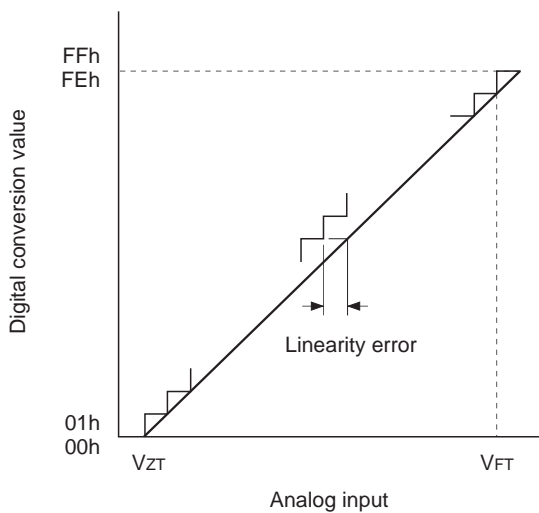
[*1] V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

[*2] V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

[*3] f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

f_{ADC} = fc (CKS = "0"), fc/2 (CKS = "1")

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

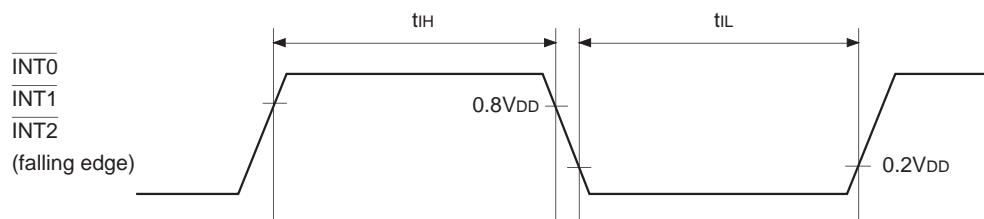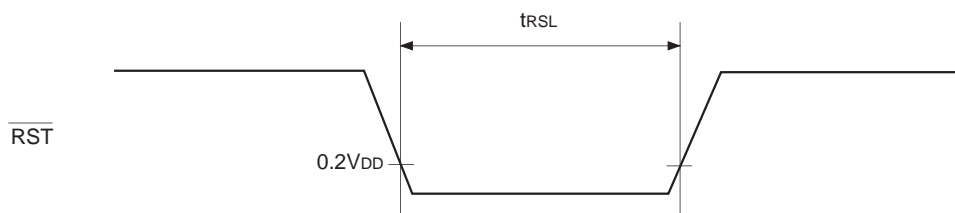**Fig. 6. Interruption input timing**

Fig. 7. $\overline{RST}$ input timing

(5) I²C bus timing (Ta = −10 to +75°C, V_DD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f_SLC	SCL		0	100	kHz
Bus-free time before starting transfer	t_BUF	SDA, SCL		4.7		μs
Hold time for starting transfer	t_HD; STA	SDA, SCL		4.0		μs
Clock Low level width	t_LOW	SCL		4.7		μs
Clock High level width	t_HIGH	SCL		4.0		μs
Setup time for repeated transfers	t_SU; STA	SDA, SCL		4.7		μs
Data hold time	t_HD; DAT	SDA, SCL		0*1		μs
Data setup time	t_SU; DAT	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	μs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	t_SU; STO	SDA, SCL		4.7		μs

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

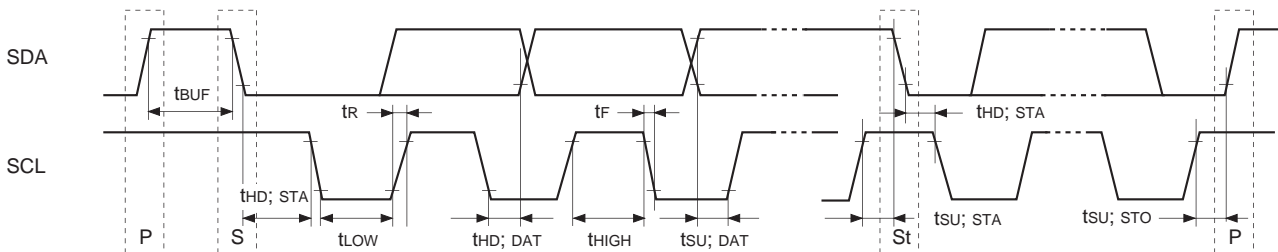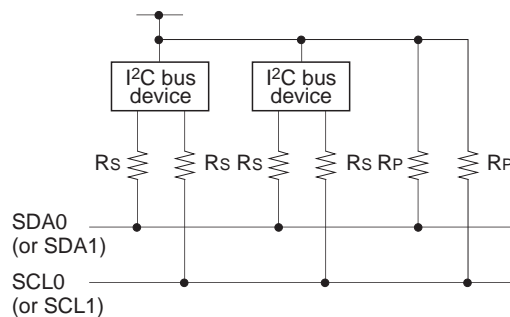**Fig. 8. I²C bus transfer timing**

Fig. 9. I²C bus device recommended circuit

• A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).

• The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be reduce the spike noise caused by CRT flashover.

(6) OSD timing (Ta = −10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 11	4	30.4[*1]	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 10	2		μs
HSYNC after-write rise and fall times	t_{HCG}	HSYNC	Fig. 10		200	ns
VSYNC before-write rise and fall times	t_{VCG}	VSYNC	Fig. 10		1.0	μs

[*1] The maximum value of fosc is specified with the following equation.

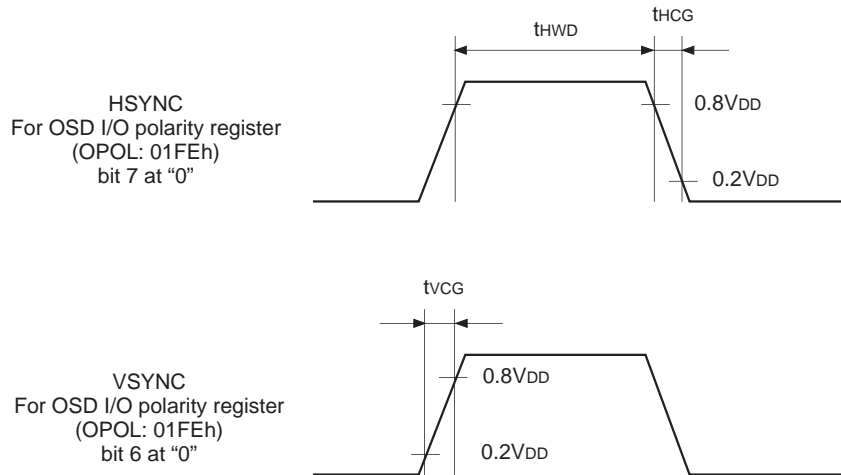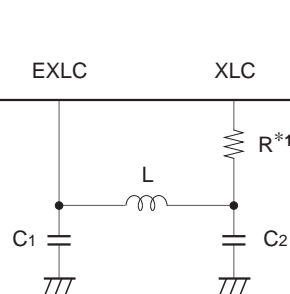$$f_{osc} [max] \leq f_c \times 1.9$$

Fig. 10. OSD timing

HSYNC
For OSD I/O polarity register
(OPOL: 01FEh)
bit 7 at "0"

t_{HWD} t_{HCG}
$0.8V_{DD}$
$0.2V_{DD}$

VSYNC
For OSD I/O polarity register
(OPOL: 01FEh)
bit 6 at "0"

t_{VCG}
$0.8V_{DD}$
$0.2V_{DD}$

Fig. 11. LC oscillation circuit connection

EXLC   XLC
R[*1]
L
C_1 C_2

[*1] The series resistor for XLC can reduce the frequency of occurrence of the undesired radiation.

Appendix

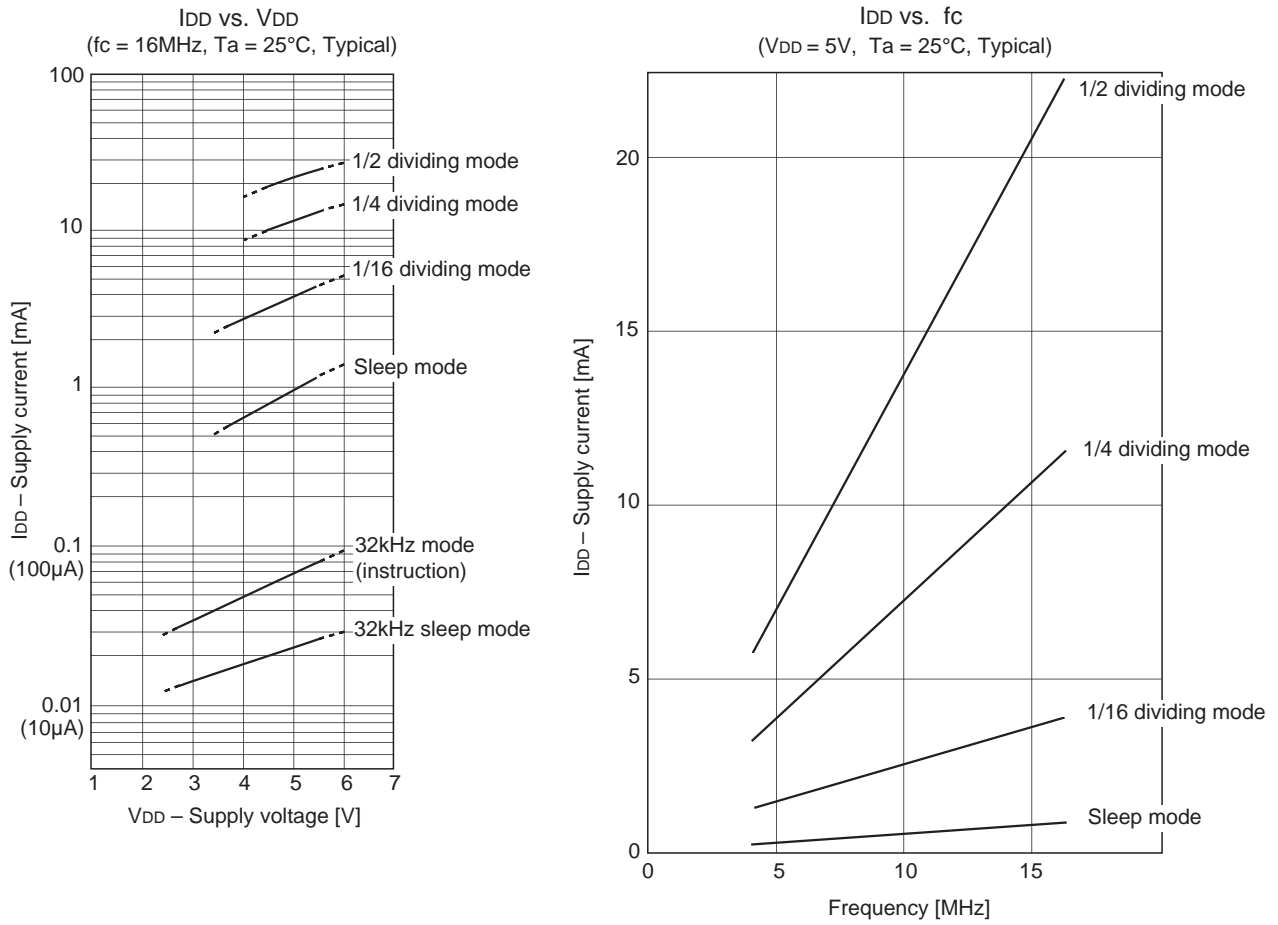**Fig. 12. Recommended oscillation circuit**

(i) Main clock   (ii) Main clock   (iii) Sub clock
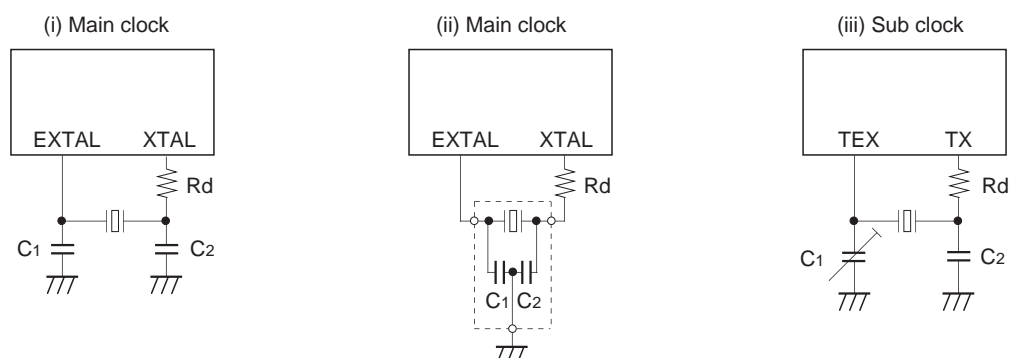
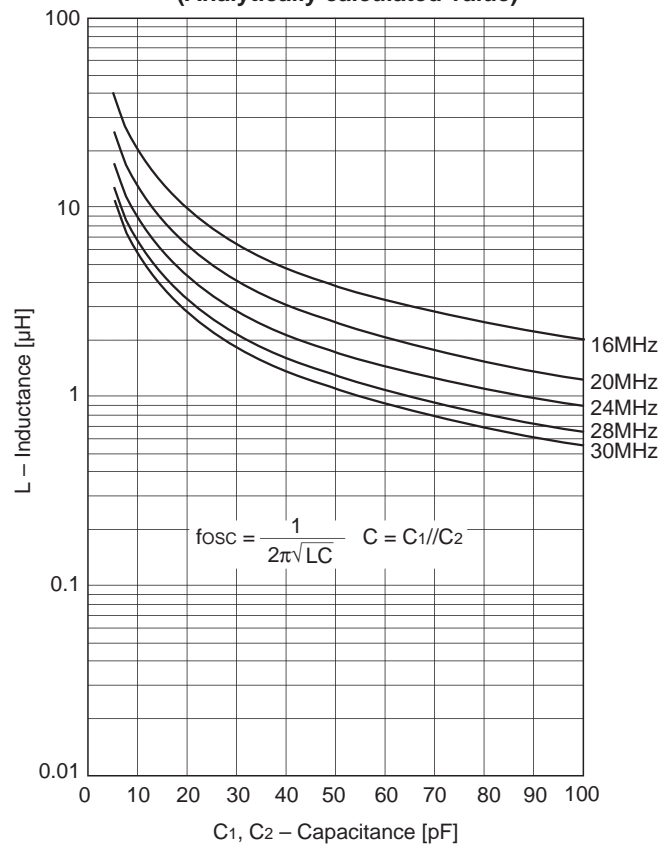| Manufacture	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0 [1]	(i)
	CSA12.0MTZ	12.0				
	CSA16.00MXZ040	16.0	5	5		
	CST10.0MTW*	10.0	30	30		(ii)
	CST12.0MTW*	12.0				
	CST16.00MXW0C1*	16.0	5	5		
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330 [1]	(i)
		12.0	12	12		
		16.0	10	10		
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0 [1]	
		12.0	5	5		
		16.0	OPEN	OPEN		
	P3	32.768kHz	30	33	120k	(iii)

* Models with an asterisk have the bull-in ground capacitance (C_1, C_2).

[1] The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.
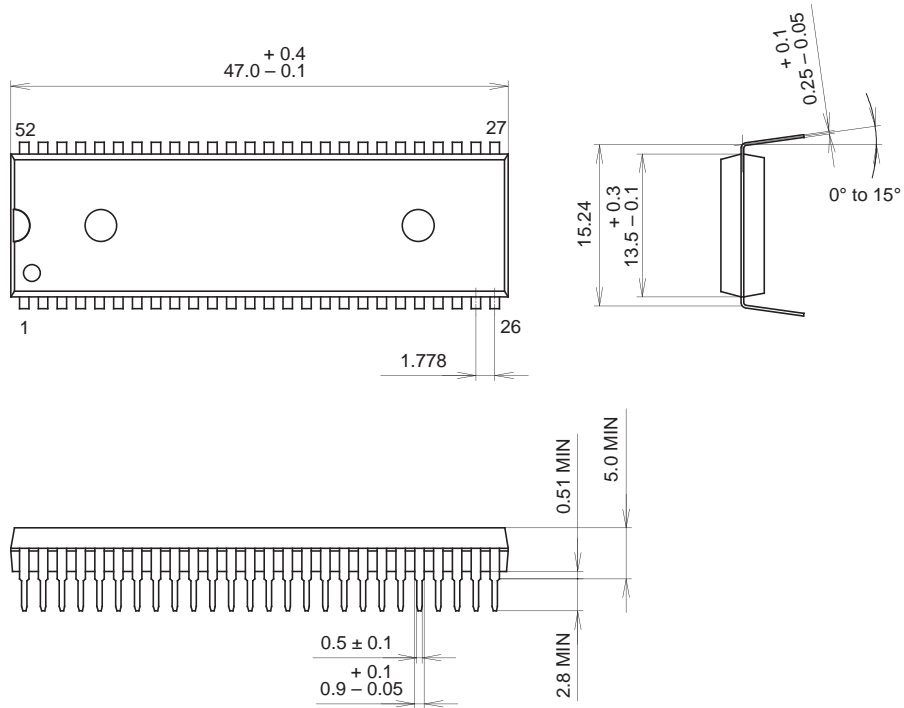
Fig. 13. Characteristic curves

I_{DD} vs. V_{DD}
(fc = 16MHz, Ta = 25°C, Typical)

1/2 dividing mode
1/4 dividing mode
1/16 dividing mode
Sleep mode
32kHz mode (instruction)
32kHz sleep mode

I_{DD} – Supply current [mA]
V_{DD} – Supply voltage [V]

I_{DD} vs. fc
(V_{DD} = 5V, Ta = 25°C, Typical)

1/2 dividing mode
1/4 dividing mode
1/16 dividing mode
Sleep mode

I_{DD} – Supply current [mA]
Frequency [MHz]

Parameter Curve for OSD Oscillator L vs. C
(Analytically calculated value)

16MHz
20MHz
24MHz
28MHz
30MHz

L – Inductance [μH]

$$f_{OSC} = \frac{1}{2\pi\sqrt{LC}} \qquad C = C_1 /\!/ C_2$$

C_1, C_2 – Capacitance [pF]

– 20 –

Package Outline   Unit: mm

52PIN SDIP (PLASTIC) 600mil

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER
PACKAGE WEIGHT	————

SONY CODE	SDIP-52P-01
EIAJ CODE	SDIP052-P-0600-A
JEDEC CODE	————

NOTE : PALLADIUM PLATING
       This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).