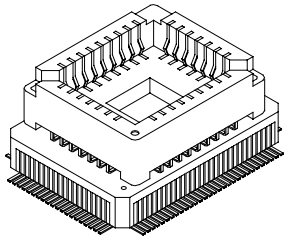
SONY

CXP88100A

CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

100 pin PQFP (Ceramic)



Description

The CXP88100 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP88132/88140/88152/88160/88216/88220/88224.

Features

- A wide instruction set (213 instructions) which cover various types of data.
  - — 16-bit operation/multiplication and division/ boolean bit operation instructions
- Minimum instruction cycle — 250ns at 16MHz operation; 122µs at 32kHz operation
- Applicable EPROM — LCC type 27C512 (Maximum 60Kbytes are available.)
- Incorporated RAM capacity — 1296 bytes
- Peripheral functions
  - — A/D converter — 8-bit, 8-channel, successive approximation method (Conversion time of 20.0µs/16MHz)
  - — Serial interface — Incorporated 8-bit and 8-stage FIFO (auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock synchronous type, 1 channel
  - — Timer — 8-bit timer, 8-bit timer/counter; 19-bit time base timer, 32kHz timer/counter
  - — High precision timing pattern generator — PPG 8-pin, 21-stage programmable, RTG 5 pins, 2 channels
  - — PWM/DA gate output — PWM output 12 bits 2 channels (Repetitive frequency 62.5kHz/16MHz); DA gate pulse output 13 bits, 4 channels
  - — Servo input control — Capstan FG, drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - — PWM output — 14 bits, 1 channel
  - — VISS/VASS circuit — Pulse duty auto detection circuit
  - — Remote control receiving circuit — 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - — Fluorescent display panel controller/driver — Maximum 144 segments display possible; Hardwave key scan function (Maximum 16 x 3 key matrix compatible.)
  - — Tri-state output — PPG output 1 pin, RTG output 1 pin, output 8 pins
  - — Psendo HSYNC output function
  - — High-speed head switching circuit
- Interruption — 22 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin ceramic QFP

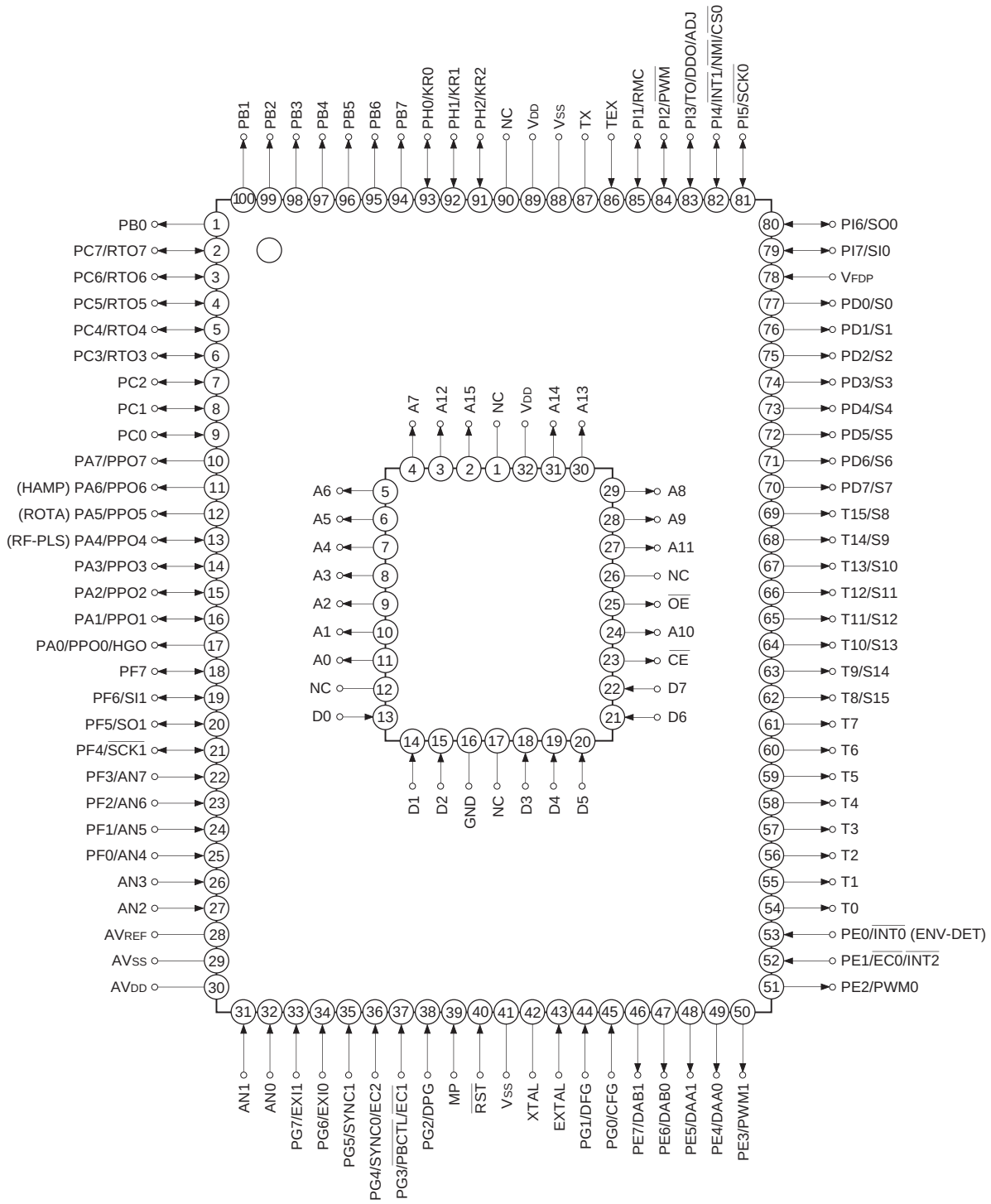
Note) Mask option depends on the type of the CXP88100A. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

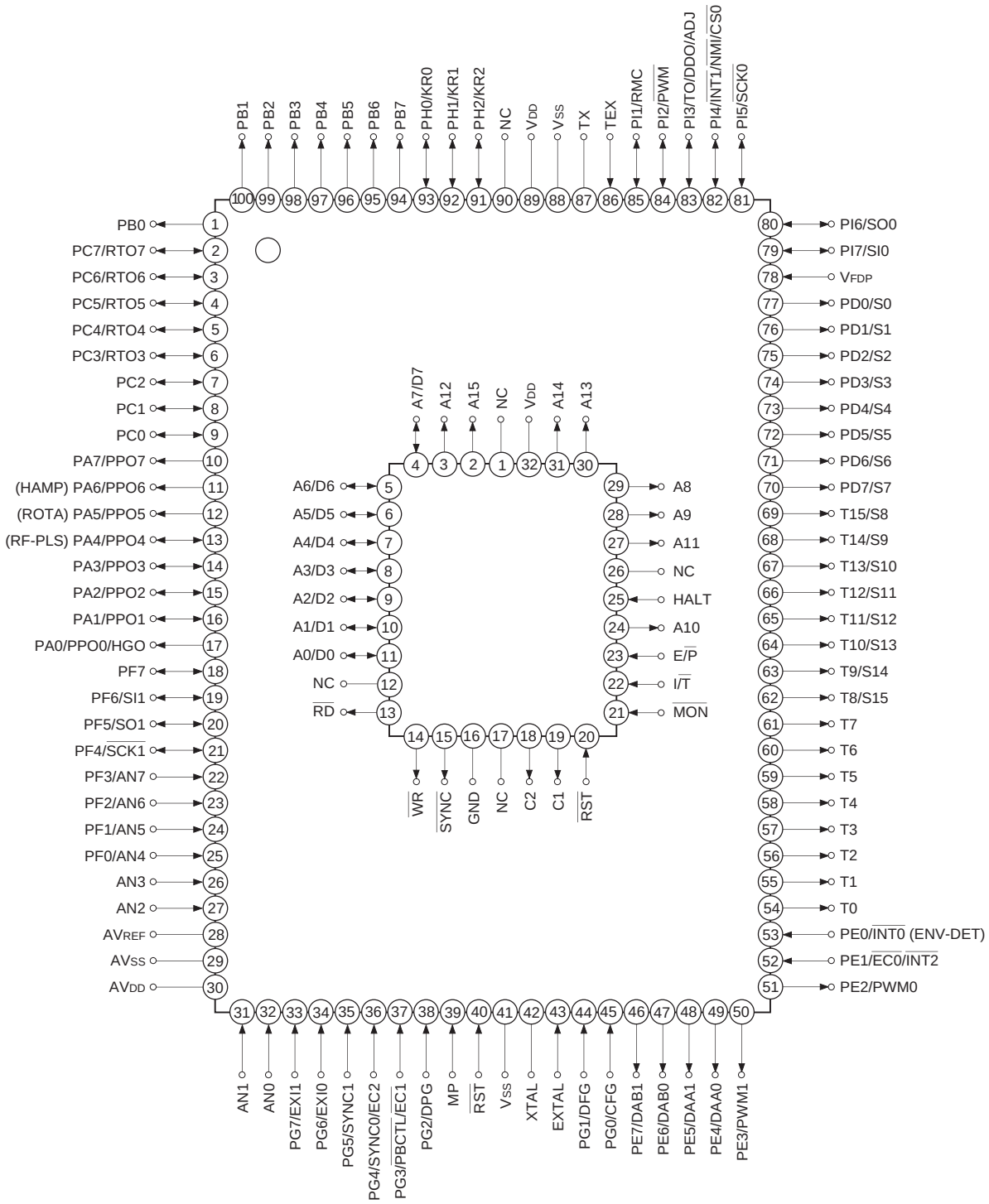
E95626-ST

Pin Assignment in Piggyback Mode



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

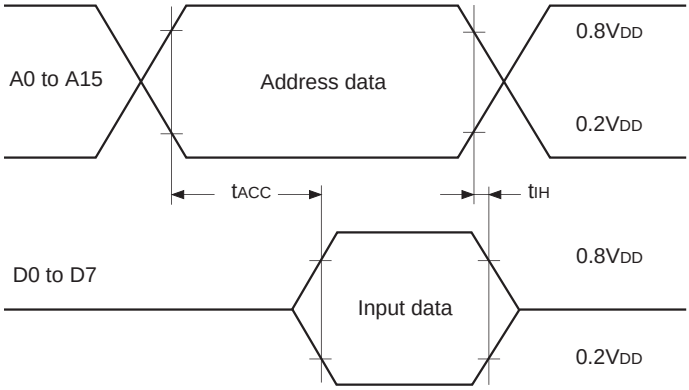
Pin Assignment in Evaluator Mode



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

EPROM Read Timing (Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		75	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



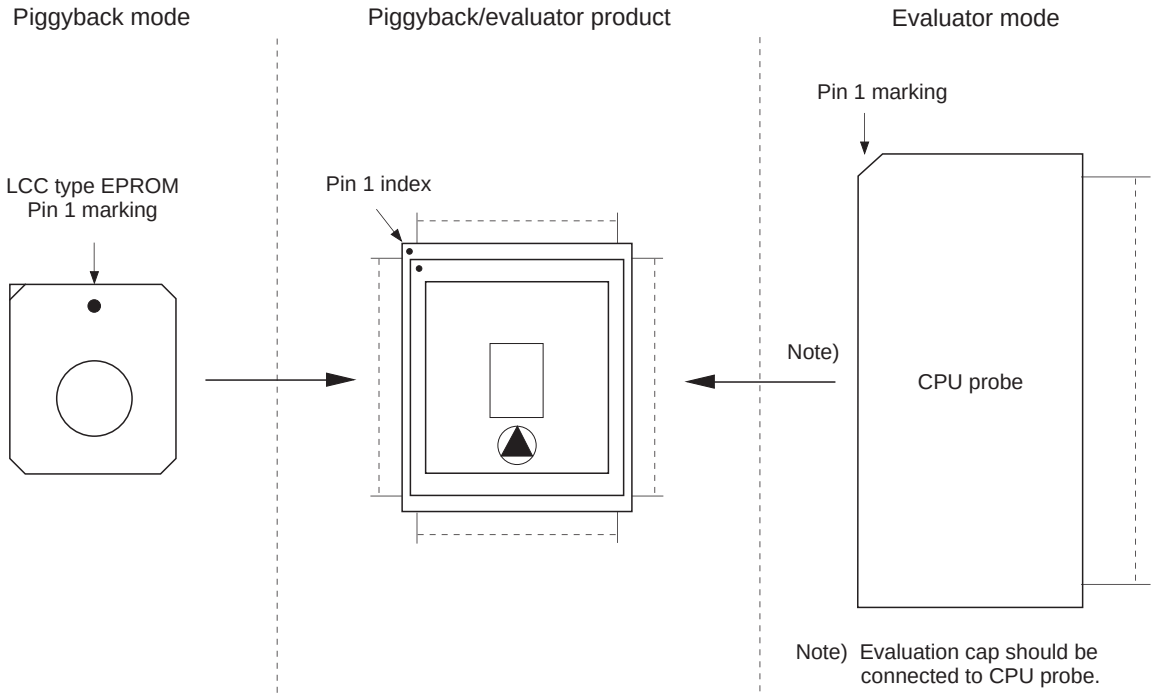
Products List

Option item	Products							
	Mask product							Piggyback/evaluator product
	CXP 88132	CXP 88140	CXP 88152	CXP 88160	CXP 88216	CXP 88220	CXP 88224	CXP88100A-U01Q
Package	100-pin plastic QFP							100-pin ceramic PQFP
ROM capacity	32K bytes	40K bytes	52K bytes	60K bytes	16K bytes	20K bytes	24K bytes	EPROM 60Kbytes
Pull-up resistor for reset pin	Existent/Non-existent							Existent
Input circuit format*1	CMOS schmitt/TTL schmitt							TTL schmitt
Pull-down resistor for high voltage drive pin	Existent/Non-existent							Existent*2

*1 On PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

*2 Not exist on PD0/S0 to PD7/S7.

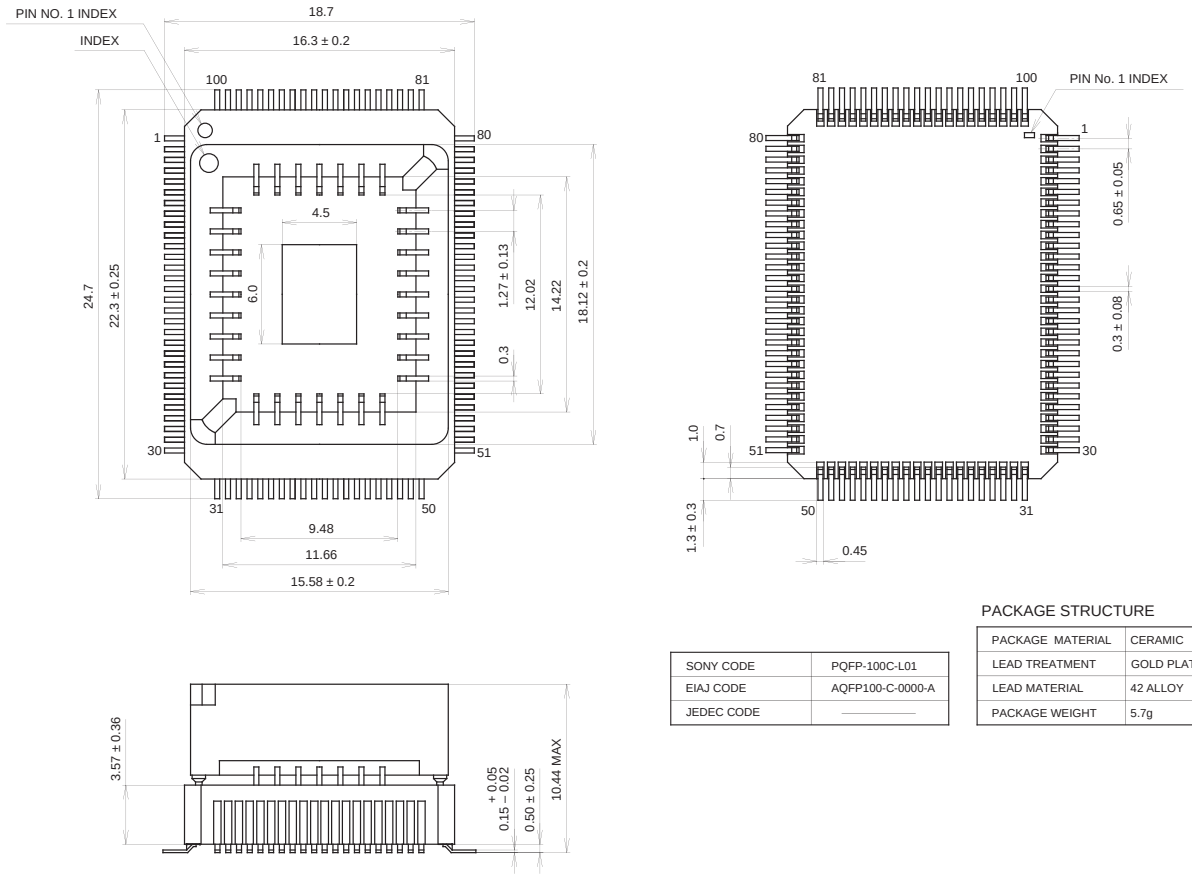
Piggyback mode/evaluator mode can be switched as shown below.



Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g