SONY

CXP88340/88348

CMOS 8-bit Single Chip Microcomputer

Description

The CXP88340/88348 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time-base timer, high precision timing pattern generation circuit, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also, the CXP88340/88348 provides sleep/stop functions which enable to lower power consumption.

100 pin QFP (Plastic)

Structure
Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle   250ns at 16MHz operation
                                                  122µs at 32kHz operation
- Incorporated ROM capacity   40K bytes (CXP88340)
                                                  48K bytes (CXP88348)
- Incorporated RAM capacity   1376 bytes
- Peripheral functions
  — A/D converter   8 bits, 12 channels, successive approximation system
                                                        (Conversion time of 20µs/16MHz)
  — Serial interface   Incorporated 8-bit, 8-stage FIFO
                                                        (Auto transfer for 1 to 8 bytes), 1 channel
                                                        Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channnel
                                                        Incorporated two-wire 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
  — Timer   8-bit timer/counter, 2 channels
                                                        19-bit time-base timer
                                                        32kHz timer/counter
  — High precision timing pattern generation   PPG: Maximum of 19 pins 32 stages programmable
     circuit   RTG: 5 pins, 1 channel
                                                              7-bit, 10-satge FIFO (RECCTL control/ATC control), 1 channel
  — PWM/DA gate output   PWM: 12 bits, 2 channels (Repetitive frequency 62.5kHz at 16MHz)
                                                        DA gate pulse output: 13 bits, 2 channels
  — Analog signal input circuit   PBCTL amplifier circuit
                                                        Reel FG comparator
  — CTL write/rewrite circuit   Recording current control circuit
  — Servo input control   Capstan FG, Drum FG/PG, CTL, Reel FG input
  — VSYNC separator
  — FRC capture unit   Incorporated 26-bit and 8-stage FIFO
  — PWM output   14 bits, 1 channel
  — VISS/VASS circuit   Pulse duty auto detection circuit
  — Remote control receiving circuit   8-bit pulse measurement counter, 6-stage FIFO
  — Tri-state output   PPG output 2 pins
  — High speed head switching circuit
- Interruption   22 factors, 15 vectors, multi-interruption possible
- Standby mode   Sleep/stop
- Package   100-pin plastic QFP
- Piggy/evaluation chip   CXP88400 100-pin ceramic PQFP

E98835-PS

Block Diagram

PA0 to PA7 — PORT A — 8
PB0 to PB7 — PORT B — 8
PC0 to PC7 — PORT C — 8
PD0 to PD7 — PORT D — 8
PE0, 1, 6, 7 — PORT E — 2
PE2 to PE5 — 6
PF0 to PF3 — PORT F — 4
PF4 to PF7 — 4
PG0 to PG3 — PORT G — 4
PH0 to PH3 — PORT H — 4
PH4 to PH7 — 4
PI0 to PI7 — PORT I — 8

CLOCK GENERATOR/ SYSTEM CONTROL

RAM 1376 BYTES

SPC700 CPU CORE

ROM 40K/48K BYTES

PRESCALER/ TIME-BASE TIMER

32kHz TIMER/COUNTER

REALTIME PULSE GENERATOR — CH0 — CH1 — FIFO

FRC CAPTURE UNIT — FIFO

PROGRAMMABLE PATTERN GENERATOR — RAM

INTERRUPT CONTROLLER

NMI

VSS
VDD
MP
RST
TX
TEX
XTAL
EXTAL

INT2
INT1/NMI
INT0

RTO3 to RTO7 — 5
PPO0 to PPO18 — 19

A/D CONVERTER

SERIAL INTERFACE UNIT (CH2) — FIFO

SERIAL INTERFACE UNIT (CH0) — RAM

SERIAL INTERFACE UNIT (CH1) — FIFO

8-BIT TIMER/COUNTER 0
8-BIT TIMER1

V SYNC SEPARATOR

SERVO INPUT CONTROL
CAPSTAIN
DRUM
PBCTL AMP
REEL COMPARATOR

REMOCON INPUT — FIFO
VISS/VASS

14-BIT PWM GENERATOR

12-BIT PWM GENERATOR CH0

12-BIT PWM GENERATOR CH1

CTL R/W CONTROL

AVSS
AVREF
AVDD

AN0 to AN11 — 12
SCL0
SCL1
SDA0
SDA1
CS0
SI0
SO0
SCK0
SI1
SO1
SCK1
EC
TO/DDO
SYNC
EXI0
EXI1
CFG
DFG
DPG
CTLFAMPI
RFG0
RFG1
RMC
PWM
PWM0
DAA0
PWM1
DAA1
ADJ
CTLHEAD
HEADL

Pin Assignment (Top View)

Top pins (100–81): PB6/PPO14, PB7/PPO15, PA0/PPO0, PA1/PPO1, PA2/PPO2, PA3/PPO3, PA4/PPO4, PA5/PPO5, PA6/PPO6, PA7/PPO7, NC, VDD, VSS, TX, TEX, PE0/SCK1, PE1/SO1, PE2/SI1, PE3/SYNC, PE4/EXI0

Left pins (1–30):
1 PB5/PPO13
2 PB4/PPO12
3 PB3/PPO11
4 PB2/PPO10
5 PB1/PPO9
6 PB0/PPO8
7 PC7/RTO7
8 PC6/RTO6
9 PC5/RTO5
10 PC4/RTO4
11 PC3/RTO3
12 PC2/PPO18
13 PC1/PPO17
14 PC0/PPO16
15 PI7
16 PI6
17 PI5
18 PI4
19 PI3
20 PI2
21 PI1
22 PI0/INT0
23 PD7/SI0
24 PD6/SO0
25 PD5/SCK0
26 PD4/CS0
27 PD3/SRVO/TO/DDO/ADJ
28 PD2/PWM
29 PD1/RMC
30 PD0/INT1/NMI

Right pins (80–51):
80 PE5/EXI1
79 PE6/PWM0/DAA0
78 PE7/PWM1/DAA1
77 RFG0
76 RFG1
75 ANOUT
74 AMPVDD
73 CTLFAMPO
72 CTLSAMPI
71 CTLAGND
70 CTLFAMPI (−)
69 CTLFAMPI (+)
68 HEADL (−)
67 HEADL (+)
66 CTLHEAD (+)
65 CTLHEAD (−)
64 AMPVSS
63 VDD
62 AN0
61 AN1
60 AN2
59 AN3
58 PF0/AN4
57 PF1/AN5
56 PF2/AN6
55 PF3/AN7
54 AVDD
53 AVREF
52 AVSS
51 PF4/AN8

Bottom pins (31–50): PH7, PH6, PH5, PH4, PH3/SDA1, PH2/SDA0, PH1/SCL1, PH0/SCL0, MP, RST, VSS, XTAL, EXTAL, PG3/EC/INT2, PG2/DPG, PG1/DFG, PG0/CFG, PF7/AN11, PF6/AN10, PF5/AN9

Note)
1. NC (Pin 90) is always connected to VDD.
2. VDD (Pins 63 and 89) are both connected to VDD
3. Vss (Pins 41 and 88) are both connected to GND.
4. MP (Pin 39) is always connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Head switching output.	
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins) PB0 and PB2 can be tri-state controlled with PPG.	
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. PC3 can be tri-state controlled with RTG. (5 pins)	
PD0/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Input pin to request external interruption and non-maskable interruption.	
PD1/RMC	I/O/Input		Remote control receiving circuit input pin.	
PD2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.	
PD3/TO DDO/ADJ SRVO	I/O/Output/Output/ Output/Output		Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.	
PD4/$\overline{\text{CS0}}$	I/O/Input		Serial chip select (CH0) input pin.	
PD5/$\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O pin.	
PD6/SO0	I/O/Output		Serial data (CH0) output pin.	
PD7/SI0	I/O/Input		Serial data (CH0) input pin.	
PE0/$\overline{\text{SCK1}}$	Output/I/O	(Port E) 8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs. (8 pins)	Serial clock (CH1) I/O pin.	
PE1/SO1	Output/Output		Serial data (CH1) output pin.	
PE2/SI1	Input/Input		Serial data (CH1) input pin.	
PE3/SYNC	Input/Input		Composite sync signal input pin.	
PE4/EXI0	Input/Input		External input pin for FRC capture unit. (2 pins)	
PE5/EXI1	Input/Input			
PE6/PWM0/ DAA0	Output/Output		PWM output pin. (2 pins)	DA gate pulse output pin. (2 pins)
PE7/PWM1/ DAA1	Output/Output			

Description	I/O	Description		
AN0 to AN3	Input			Analog input pin to A/D converter. (12 pins)
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits also serve as standby release input pins. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
PG0/CFG	Input/Input	(Port G) 4-bit input port. (4 pins)	Capstan FG input pin.	
PG1/DFG			Drum FG input pin.	
PG2/DPG			Drum PG input pin.	
PG3/$\overline{EC}$/ $\overline{INT2}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PH0/SCL0 PH1/SCL1	I/O/I/O	(Port H) 8-bit I/O port. Upper four bits are for outputs. I/O can be set in a unit of single bits for lower four bits. Lower four bits are N-ch open drain outputs and which can drive 12mA sink current. Upper four bits are for outputs; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	Serial clock (CH2) I/O pin.	
PH2/SDA0 PH3/SDA1			Serial data (CH2) I/O pin.	
PH4 to PH7	Output			
PI0/$\overline{INT0}$	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PI1 to PI7	I/O			
RFG0, RFG1	Input	Input ports. (2 pins)	Reel FG input pin.	
ANOUT	Output	Output port. (1 pin)	Internal waveform output pin of analog circuit.	
CTLFAMPO	Output	Output port. (1 pin)	PBCTL signal 1st amplifier output pin.	
CTLSAMPI	Input	Input port. (1 pin)	PBCTL signal 2nd amplifier input pin.	
CTLAGND	Output	Output port. (1 pin)	Smoothing capacitor connecting pin.	
CTLFAMPI (−) CTLFAMPI (+)	Input	Input ports. (2 pins)	Input PBCTL signal with capacitor coupled.	
HEADL (−) HEADL (+)	Output	Output ports. (2 pins)	During playback, connect to CTLHEAD (−) and CTLHEAD (+) with internal switch.	
CTLHEAD (−) CTLHEAD (+)	I/O	I/O ports. (2 pins)	During playback, input pin of PBCTL signal; during recording, output pin of PBCTL signal.	
AMPV$_{SS}$		Analog signal input circuit GND pin.		
AMPV$_{DD}$		Analog signal input circuit power supply pin.		

Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)
TX	Output	
$\overline{RST}$	Input	System reset pin; active at low level.
NC		NC pin. Connect this pin to V$_{DD}$ for normal operation.
MP	Input	Test mode input pin. Always connect to GND.
AV$_{DD}$		Positive power supply pin of A/D converter.
AV$_{REF}$	Input	Reference voltage input pin of A/D converter.
AV$_{SS}$		GND pin of A/D converter.
V$_{DD}$		Positive power supply pin.
V$_{SS}$		GND pin. Connect both Vss pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	After a reset
PA0/PPO0 to PA7/PPO7 PB4/PPO12 to PB7/PPO15 12 pins	Port A Port B PPO data Ports A and B data Internal data bus RD (Port A or Port B) Output becomes active from high impedance by data writing to port data register.	Hi-Z
PB0/PPO8 PB2/PPO10 2 pins	Port B PPO8, PPO10 data PB0, PB2 data Internal data bus RD (Port B) PPO9, PPO11 data Output becomes active from high impedance by data writing to port data register.	Hi-Z
PB1/PPO9 PB3/PPO11 2 pins	PPG control/status register bit 0 Tri-state control selection "0" after a reset PPO9, PPO11 data PB1, PB3 data Internal data bus RD (Port B) Output becomes active from high impedance by data writing to port data register.	Hi-Z
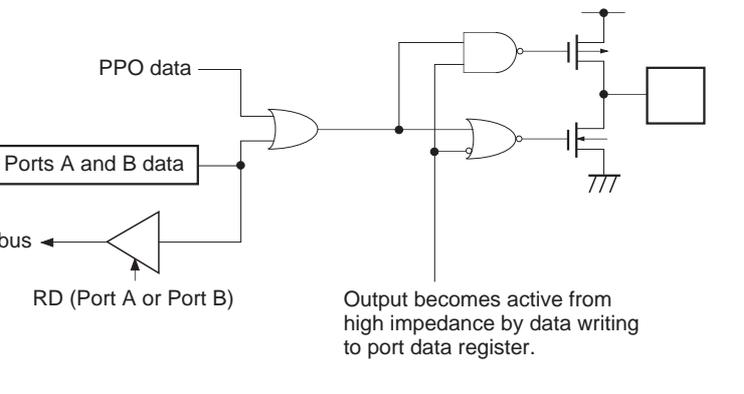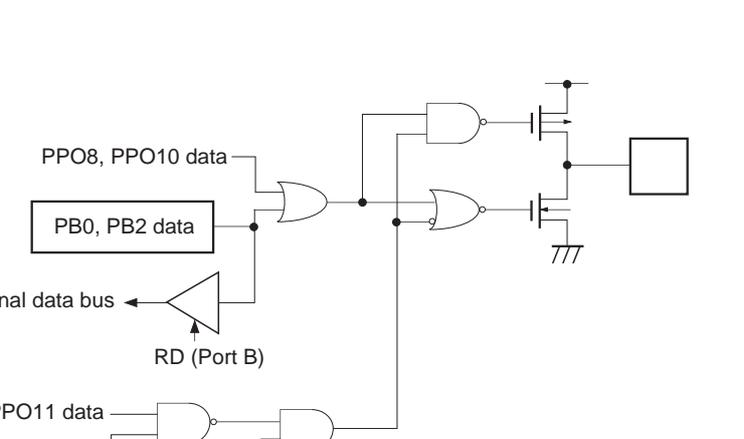
Pin	Circuit format	After a reset
PC0/PPO16 to PC2/PPO18 PC5/RTO5 to PC7/RTO7 6 pins	**Port C** PPO, RTO data Port C data Port C direction "0" after a reset Internal data bus RD (Port C) Internal data bus RD (Port C direction) Input protection circuit IP	Hi-Z
PC3/RTO3 1 pin	**Port C** RTO3 data PC3 data PC3 direction "0" after a reset Internal data bus RD (Port C) Internal data bus RD (Port C direction) RTO4 data RTG interruption control register bit 7 Tri-state control selection "0" after a reset IP	Hi-Z
PC4/RTO4 1 pin	RTO4 data PC4 data PC4 direction "0" after a reset Internal data bus RD (Port C) Internal data bus RD (Port C direction) IP	Hi-Z

Pin	Circuit format	After a reset
PD0/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ PD1/$\overline{\text{RMC}}$ PD4/$\overline{\text{CS0}}$ PD7/SI0 4 pins	**Port D** Port D data Port D direction "0" after a reset Internal data bus ← RD (Port D) Internal data bus ← RD (Port D direction) IP Schmitt input PD1: Remote control circuit PD0: Interruption circuit PD4, PD7: Serial CH0	Hi-Z
PD2/$\overline{\text{PWM}}$ PD3/SRVO/ TO/DDO/ ADJ 2 pins	**Port D** Port D function select "0" after a reset PD2: 14-bit PWM Timer/counter, CTL duty detection circuit, PD3: 32kHz timer, amplifier circuit MPX Port D data Port D direction "0" after a reset Internal data bus ← RD (Port D) Internal data bus ← RD (Port D direction) IP	Hi-Z
PD5/$\overline{\text{SCK0}}$ PD6/SO0 2 pins	**Port D** Port D function select "0" after a reset SIO CH0 MPX Port D data Port D direction "0" after a reset MPX Internal data bus ← RD (Port D) Note) PD5 is schmitt input PD6 is inverter input IP SIO CH0 ←	Hi-Z
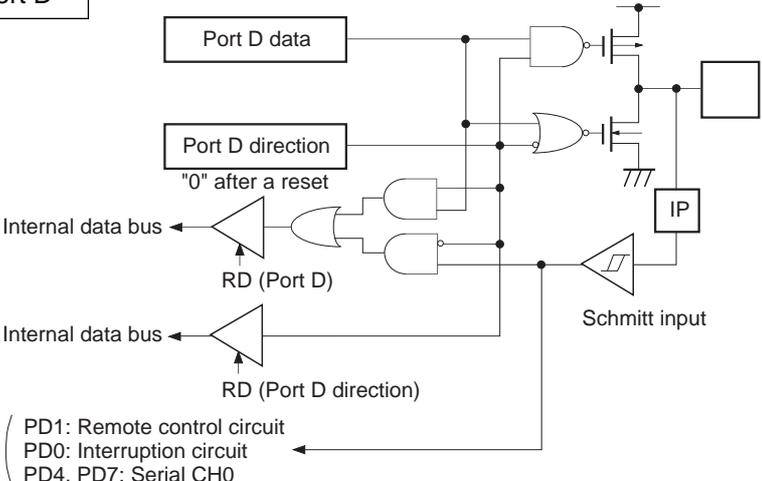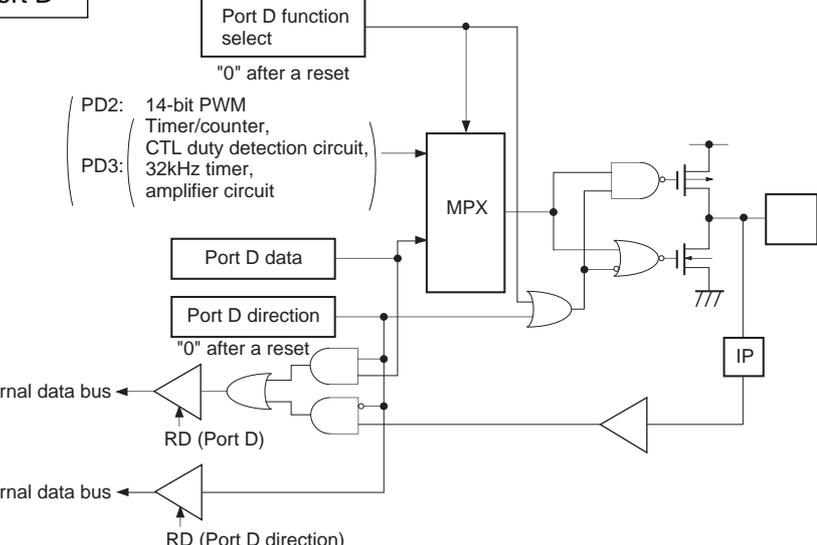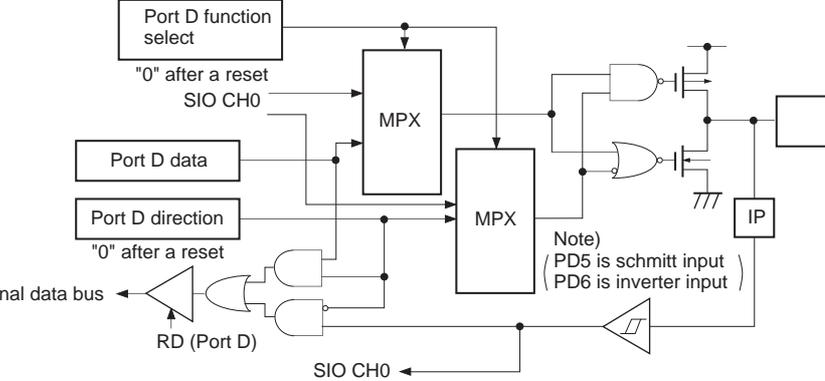
Pin	Circuit format	After a reset
PE0/$\overline{\text{SCK1}}$ 1 pin	**Port E** Port/SCK output select "1" after a reset SIO CH1 → MPX Port E data Hi-Z control IP Internal data bus ← RD (Port E) SIO CH1 ←	Hi-Z
PE1/SO1 1 pin	**Port E** Port E function select "1" after a reset SIO CH1 → MPX Port E data Hi-Z control Internal data bus ← RD (Port E)	Hi-Z
PE2/SI1 PE3/SYNC PE4/EXI0 PE5/EXI1 4 pins	**Port E** Schmitt input IP PE2: SIO CH1 PE3, PE4, PE5: Servo input Internal data bus RD (Port E) Note) For PE3/SYNC, CMOS schmitt input or TTL schmitt input can be selected with the mask option.	Hi-Z
PE6/PWM0/ DAA0 PE7/PWM1/ DAA1 2 pins	**Port E** Port/DA/PWM select "1" after a reset DA gate output or PWM output → MPX Port E data Hi-Z control Internal data bus ← RD (Port E)	High level
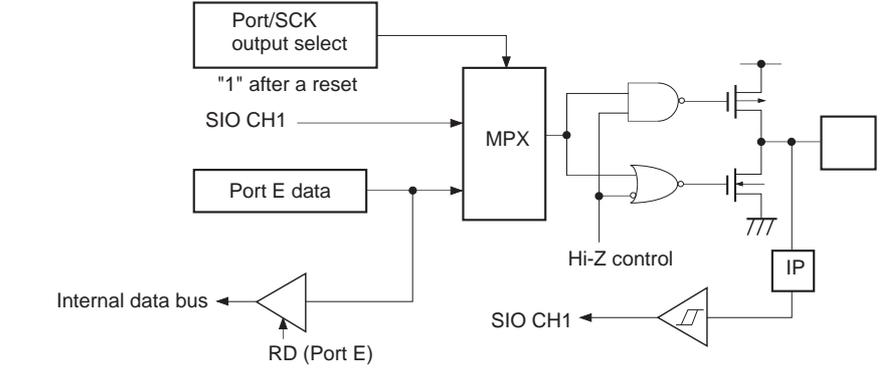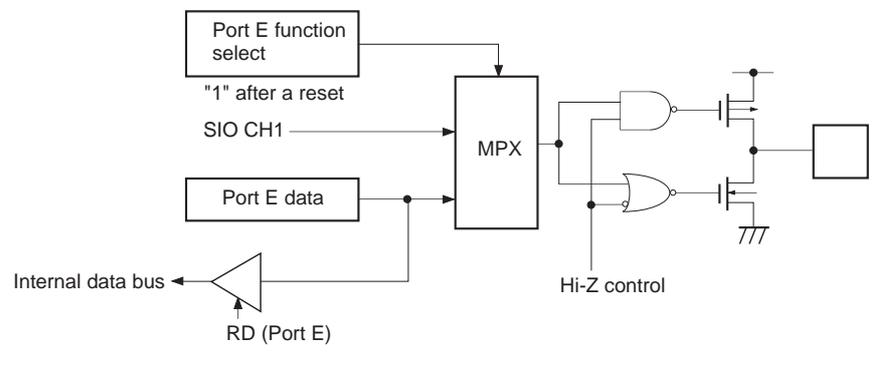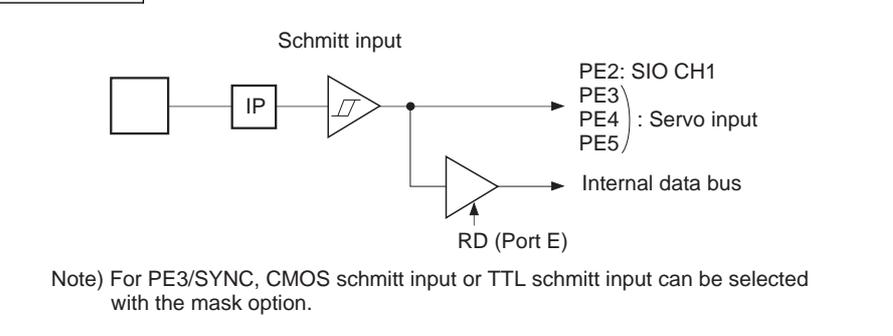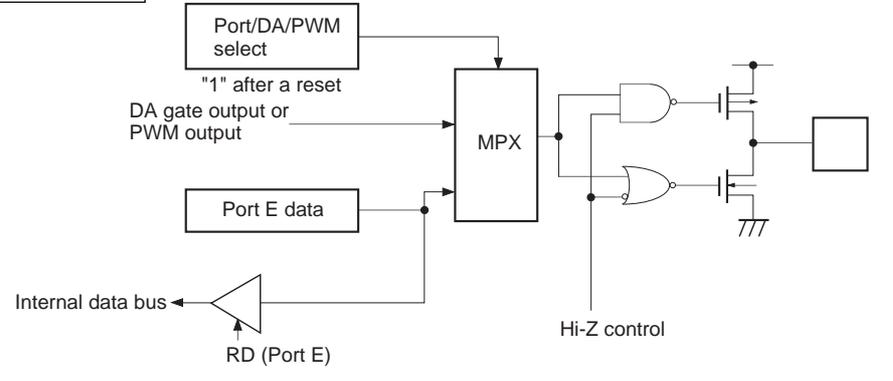
Pin	Circuit format	After a reset
AN0 to AN3 4 pins	Input multiplexer IP → A/D converter	Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F Input multiplexer IP → A/D converter Internal data bus RD (Port F)	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F Port F data Internal data bus RD (Port F) Port/AD select "1" after a reset IP Input multiplexer → A/D converter	Hi-Z
PG0/CFG PG1/DFG PG2/DPG 3 pins	Port G Power ON/OFF control Schmitt input IP → Servo input Internal data bus RD (Port G) Schmitt width selection	Hi-Z
PG3/$\overline{EC}$/$\overline{INT2}$ 1 pin	Port G Schmitt input IP Internal data bus RD (Port G)	Hi-Z
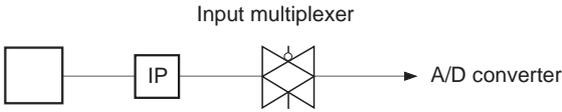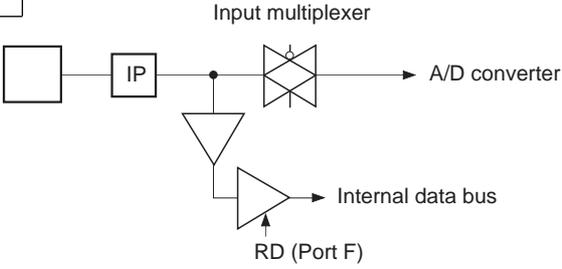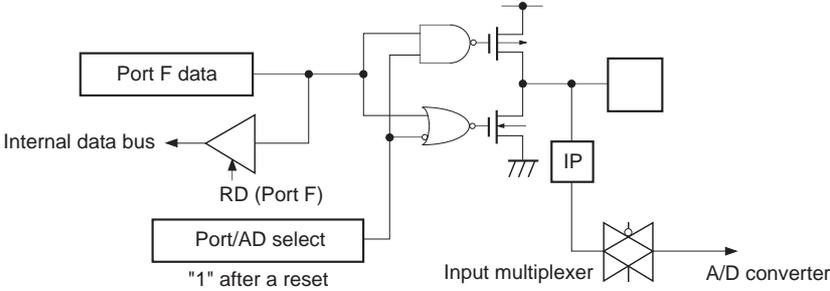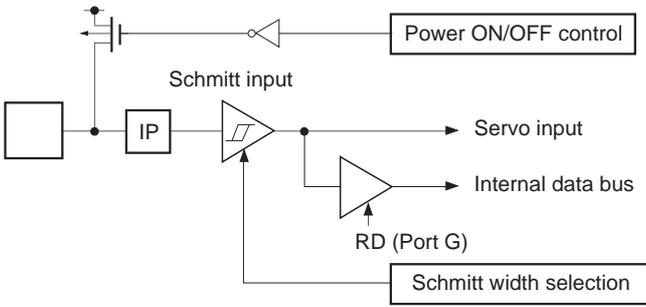
Pin	Circuit format	After a reset
PH0/SCL0 PH1/SCL1 PH2/SDA0 PH3/SDA1 4 pins	Port H SCL, SDA I²C output enable Port H data Port H direction "0" after a reset Internal data bus RD (Port H) Internal data bus RD (Port H direction) Schmitt input IP SCL, SDA (Serial interface (CH2) circuit) Other serial interface (CH2) pin	Hi-Z
PH4 to PH7 4 pins	Port H Port H data Internal data bus RD (Port H) * * 12V drive voltage, large current 12mA	Hi-Z
PI0/INT0 1 pin	Port I Pull-up resistor "0" after a reset PI0 data PI0 direction "0" after a reset Internal data bus RD (Port I) Internal data bus RD (Port I direction) Internal data bus RD (pull-up resistor) IP * Edge detection Standby release Interruption circuit * Pull-up transistors approx. 100kΩ	Hi-Z

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Pin	Circuit format	After a reset
PI1 to PI7 7 pins	Port I Pull-up resistor "0" after a reset Port I data Port I direction "0" after a reset Internal data bus ◄ RD (Port I) Internal data bus ◄ RD (Port I direction) Internal data bus ◄ RD (pull-up resistor) Edge detection Standby release ◄ IP * Pull-up transistors approx. 100kΩ	Hi-Z
CTLFAMPI (+) CTLFAMPI (−) CTLFAMPO 3 pins	CTLAGND CTLFAMPI (+) IP IP CTLFAMPI (−) CTLFAMPO Input pin charge control	1/2AMPV$_{DD}$
CTLSAMPI 1 pin	Input pin charge control IP CTLAGND LPF circuit	1/2AMPV$_{DD}$

Pin	Circuit format	After a reset
CTLAGND 1 pin		1/2AMPV$_{DD}$
CTLHEAD (+) 1 pin		Hi-Z
CTLHEAD (−) 1 pin		Hi-Z
HEADL (+) 1 pin		Hi-Z
HEADL (−) 1 pin		Hi-Z
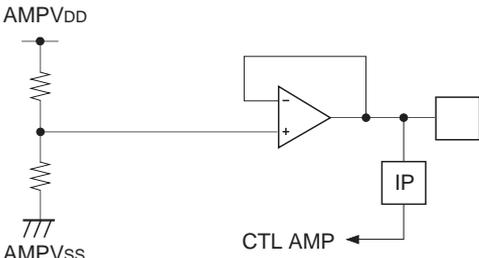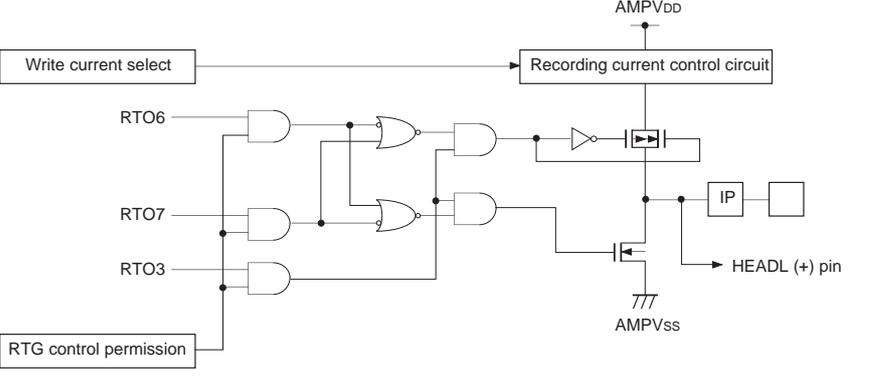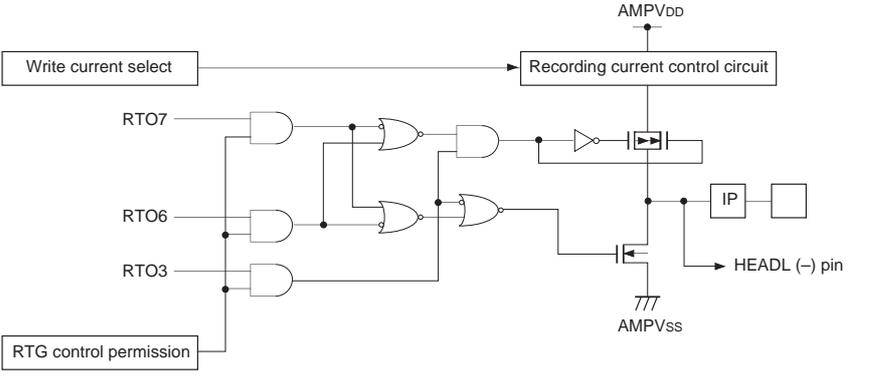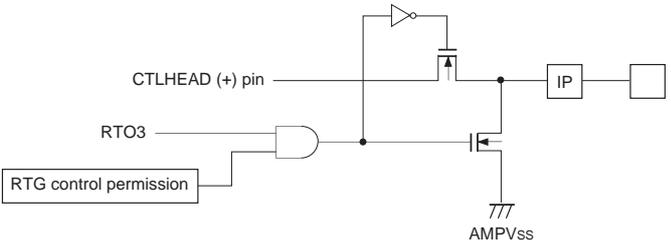
Pin	Circuit format	After a reset
RFG0 RFG1 2 pins	Comparator → Servo output (IP)	Hi-Z
EXTAL XTAL 2 pins	EXTAL, XTAL, IP	• Shows the circuit composition during oscillation. • Feedback resistor is removed and XTAL outputs High level during stop.	Oscillation
TEX TX 2 pins	TEX, TX, IP, 32kHz timer/counter	• Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At that time, TEX outputs Low level and TX outputs High level.	Oscillation
$\overline{RST}$ 1 pin	Mask option, Pull-up resistor, Schmitt input, OP, IP	Low level (during a reset)
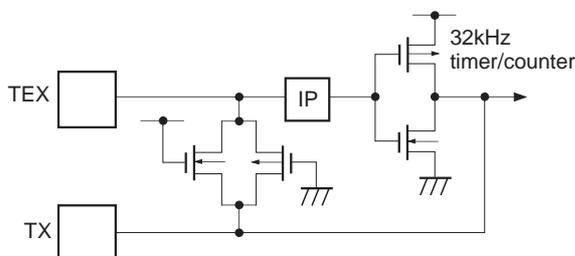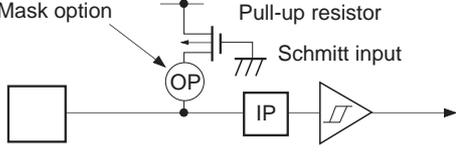
Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0[*1]	V	
	AV_{SS}	−0.3 to +0.3	V	
	$AMPV_{DD}$	$AMPV_{SS}$ to +7.0[*2]	V	
	$AMPV_{SS}$	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0[*3]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*3]	V	
Medium drive output voltage	V_{OUTP}	−0.3 to +15.0	V	Port H (PH7 to PH4) pin
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output ports (value per pin)
	I_{OLC}	20	mA	Large current output port[*4] (value per pin)
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type

[*1] AV_{DD} should not exceed V_{DD} + 0.3V.

[*2] $AMPV_{DD}$ should not exceed V_{DD} + 0.3V.

[*3] V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

[*4] The large current output port is port H (PH7 to PH4).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions   (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during sleep mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during stop
Analog supply voltage	AV_{DD}	4.5	5.5	V	[*1]
	$AMPV_{DD}$	4.5	5.5	V	[*2]
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[*3]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input[*4]
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input[*5]
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin[*6] TEX pin[*7]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[*3]
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input[*4]
	V_{ILTS}	0	0.8	V	TTL schmitt input[*5]
	V_{ILEX}	−0.3	0.4	V	EXTAL pin[*6] TEX pin[*7]
Operating temperature	$Topr$	−20	+75	°C	

[*1] AV_{DD} and V_{DD} should be set to the same voltage.

[*2] $AMPV_{DD}$ and V_{DD} should be set to the same voltage.

[*3] Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PI1 to PI7 and PH0 to PH3), MP pin

[*4] Each pin of $\overline{RST}$, PD0/$\overline{INT1}$/$\overline{NMI}$, PD1/RMC, PD4/$\overline{CS0}$, PD5/$\overline{SCK0}$, PD7/SI0, PE0/$\overline{SCK1}$, PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/$\overline{INT0}$, PG3/$\overline{EC}$/$\overline{INT2}$ (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

[*5] PE3/SYNC (when TTL schmitt input is selected with mask option.)

[*6] Specifies only during external clock input.

[*7] Specifies only during external event input.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V)   (Ta = −20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (V_{OL} only) PI	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	μA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$[1]		−1.5		−400	μA
I/O leakage current	I_{IZ}	PA to PF, PG3, PI, MP, AN0 to AN3, $\overline{RST}$[1]	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	μA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH4 to PH7	V_{DD} = 5.5V, V_{OH} = 12V			50	μA
		PH0 to PH3	V_{DD} = 5.5V, V_{OH} = 5.5V			10	μA
Supply current[2]	I_{DD1}	V_{DD}, V_{SS}	16MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 5.5V[3]		37	50	mA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V		2.1	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF) V_{DD} = 3.3V		58	100	μA
	I_{DDS2}		Sleep mode V_{DD} = 3V ± 0.3V		9	35	μA
	I_{DDS3}		Stop mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V ± 0.5V			10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	PC, PD, PE0, PE2 to PE5, PF, PG, PI, CTLHEAD (+), CTLHEAD (−), CTLFAMPI (+), CTLFAMPI (−), CTLSAMPI, RFG, XTAL, TEX	Clock 1MHz 0V other than the measured pins		10	20	pF

[*1] $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistor is selected.

[*2] When entire output pins are left open.

[*3] When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEh) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 200[1]			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

[1] t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/f_C (Upper 2 bits = "00"), 4000/f_C (Upper 2 bits = "01"), 16000/f_C (Upper 2 bits = "11")
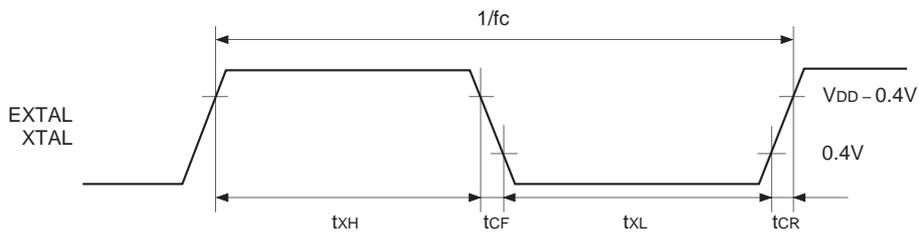
Fig. 1. Clock timing
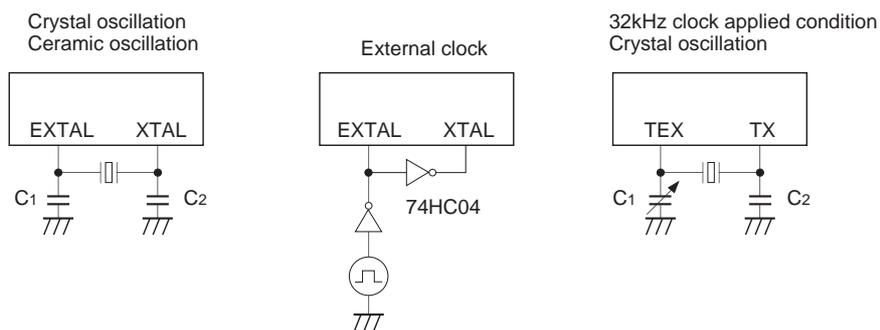
Fig. 2. Clock applied condition
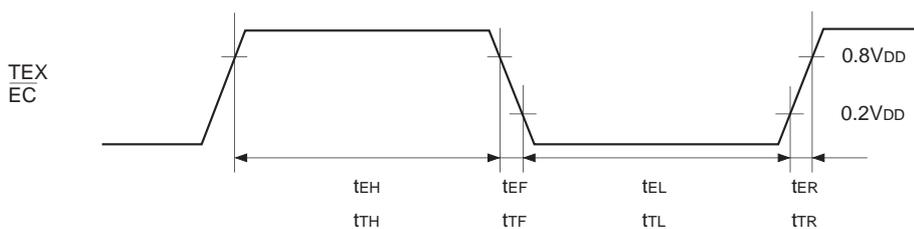
Fig. 3. Event count clock timing

(2) Serial transfer (CH0)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t_{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t_{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t_{DCSO}	SO0	Chip select transfer mode		t_{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		t_{sys} + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	t_{sys} + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2t_{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	t_{sys} + 100		ns
			Output mode	8000/fc − 100		ns
SI0 input set-up time (against $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	−t_{sys} + 100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	2t_{sys} + 100		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		2t_{sys} + 100	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.
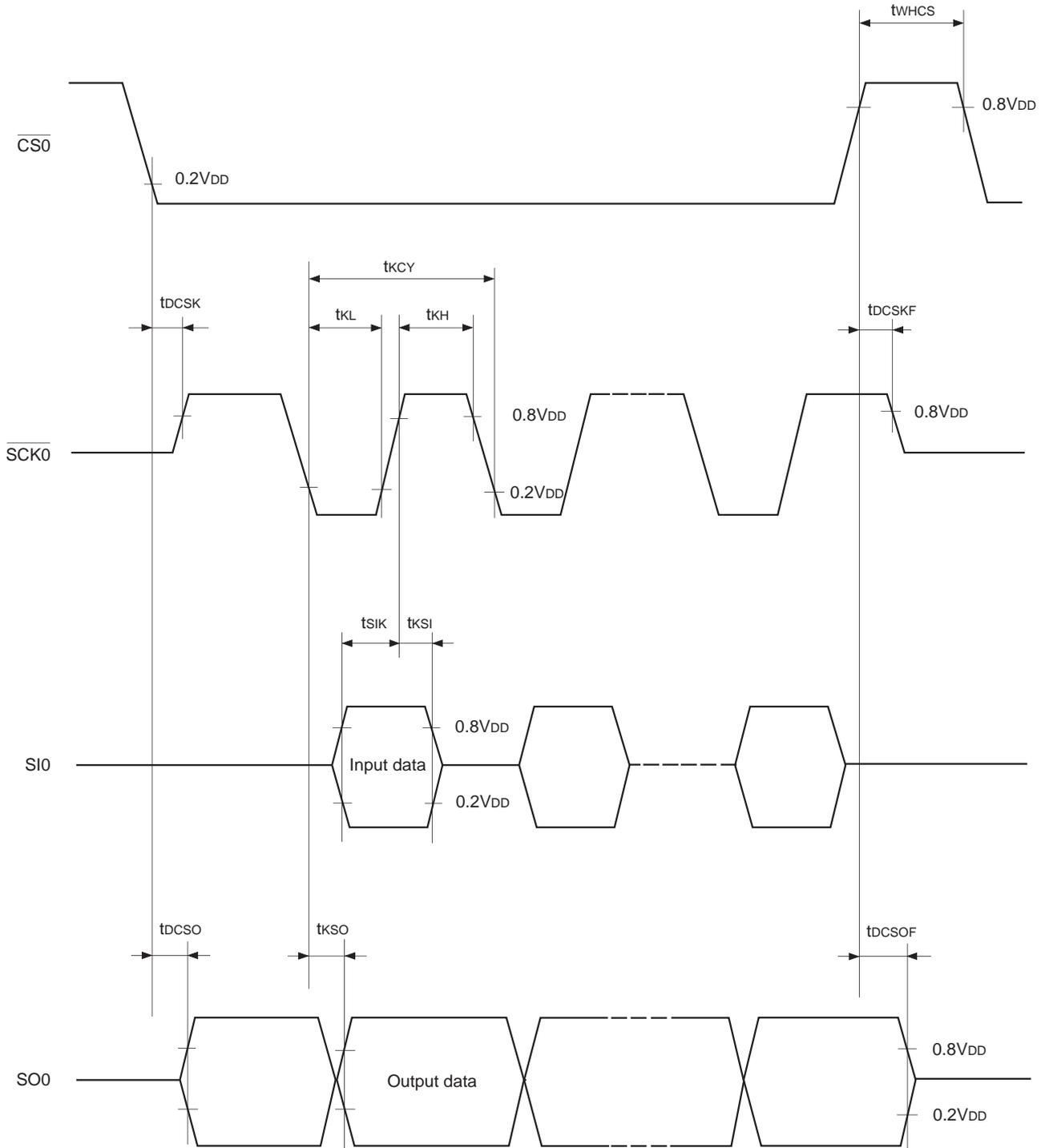
**Fig. 4. Serial transfer timing (CH0)**

Serial transfer (CH1) (SIO mode)   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	$2t_{sys}$ + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	t_{sys} +100		ns
			Output mode	8000/fc − 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	t_{sys} + 200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		t_{sys} + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.
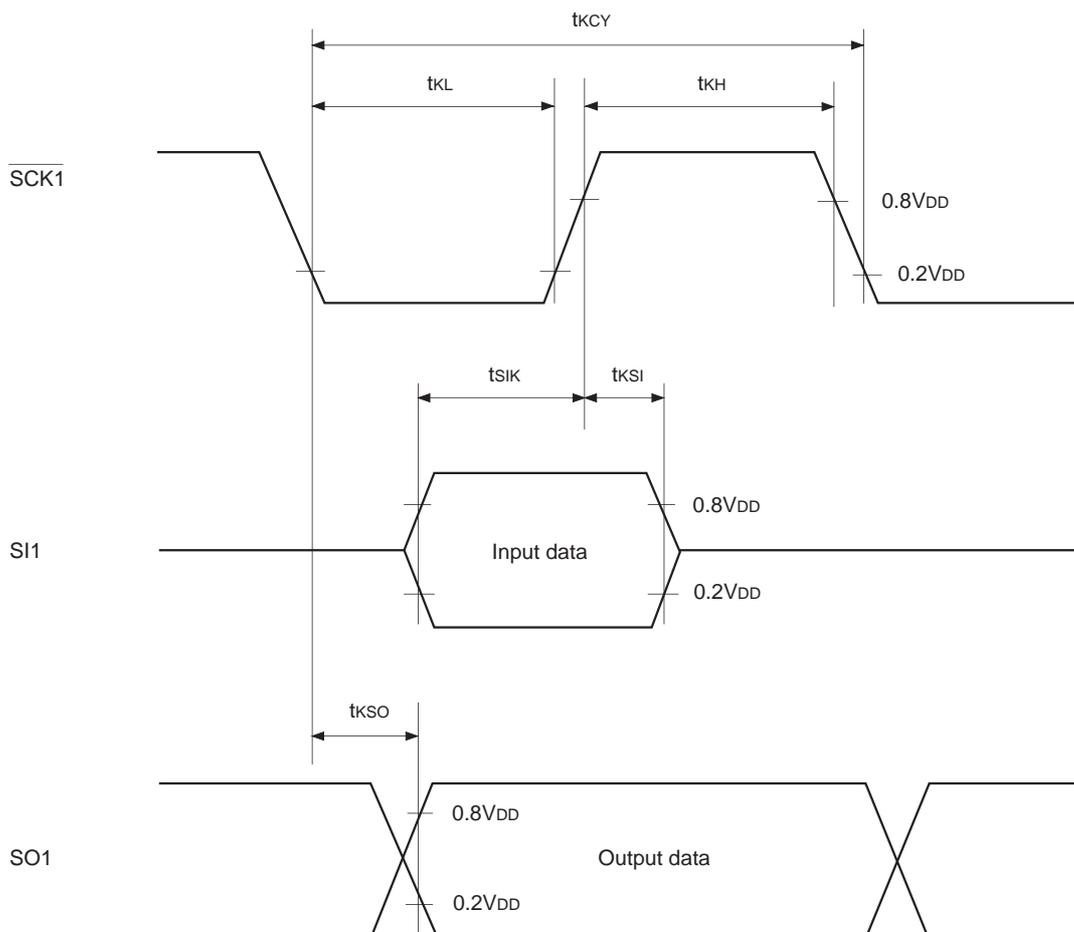
Fig. 5. Serial transfer CH1 timing (SIO mode)

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Serial transfer (CH1) (Special mode) (Ta = –20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO1 cycle time	t$_{LCY}$	SO1 SI1	*1		104		µs
SI1 data setup time	t$_{LSU}$	SI1		2			µs
SI1 data hold time	t$_{LHD}$	SI1		2			µs

*1 t$_{LCY}$ is specified only when serial mode register (CH1) (SIOM1: 05F2h) lower 2 bits (SO1 clock selection) are set at 104µs.

Note) The load of SO1 pin is 50pF + 1TTL.
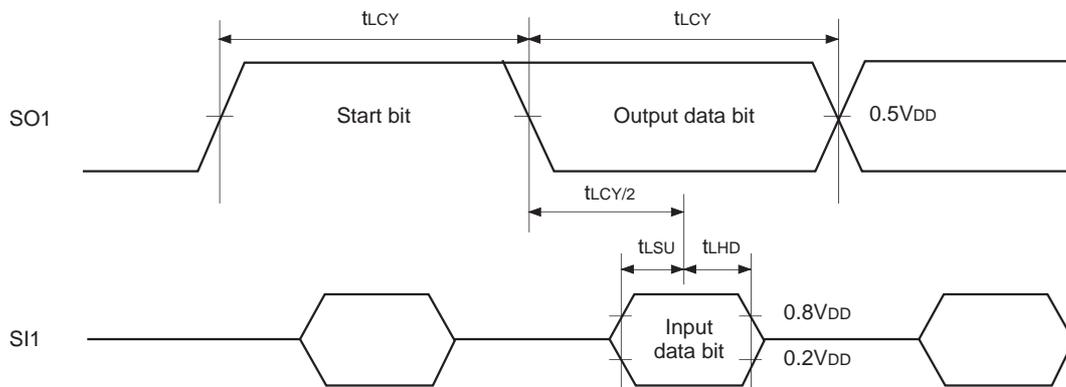
Fig. 6. Serial transfer CH1 timing (Special mode)

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Serial transfer (CH2) (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL			400	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		2.6		μs
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		1.0		μs
Clock low level width	t_{LOW}	SCL		1.0		μs
Clock high level width	t_{HIGH}	SCL		1.0		μs
Setup time for repeated transfers	$t_{SU; STA}$	SDA, SCL		1.0		μs
Data hold time	$t_{HD; DAT}$	SDA, SCL		0[*1]		μs
Data set-up time	$t_{SU; DAT}$	SDA, SCL		100		ns
SDA, SCL rise time	t_R	SDA, SCL			300	ns
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU; STO}$	SDA, SCL		1.6		μs

[*1] The SCL fall time (300ns Max.) is not included in the data hold time.
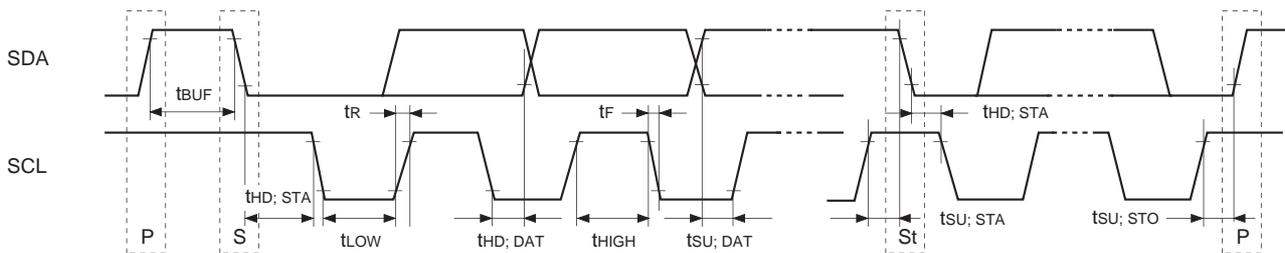
Fig. 7. Serial transfer timing (CH2)
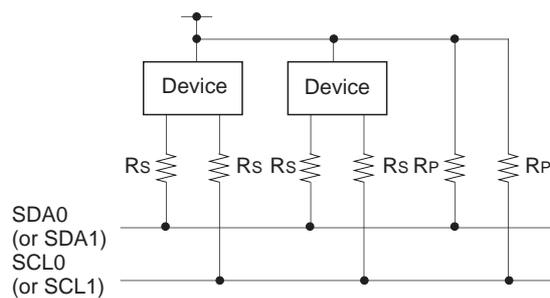
Fig. 8. Device recommended circuit

• A pull-up resistor (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
• The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (R_S = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(4) A/D converter characteristics

(Ta = −20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}[*1]			µs
Sampling time	t_{SAMP}			12/f_{ADC}[*1]			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} − 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
			Sleep mode Stop mode 32kHz operating mode			10	µA
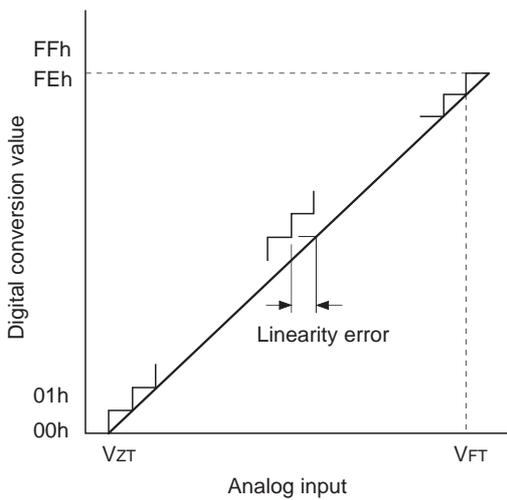
[*1] f_{ADC} indicates the below values due to the peripheral clock control register (PCC: 05F8h) bit 3 and clock control register (CLC: 00FEh) upper 2 bits.

ADCCK / PCK1, PCK0	0 (φ/2 selection)	1 (φ selection)
00 (φ = f_{EX}/2)	f_{ADC} = fc/2	f_{ADC} = fc
01 (φ = f_{EX}/4)	f_{ADC} = fc/4	f_{ADC} = fc/2
11 (φ = f_{EX}/16)	f_{ADC} = fc/16	f_{ADC} = fc/8

Fig. 9. Definitions of A/D converter terms

(4) Interruption, reset input   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PI0 to PI7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

$\overline{INT0}$
$\overline{INT1}$
$\overline{INT2}$
$\overline{NMI}$
PI0 to PI7
(During standby release input)
(Falling edge)
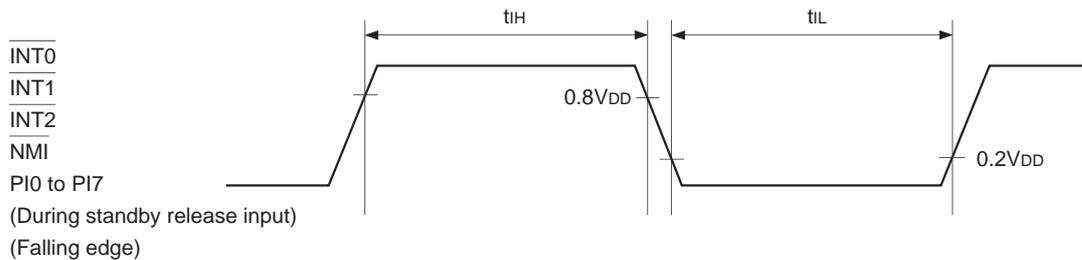
Fig. 10. Interruption input timing

$\overline{RST}$
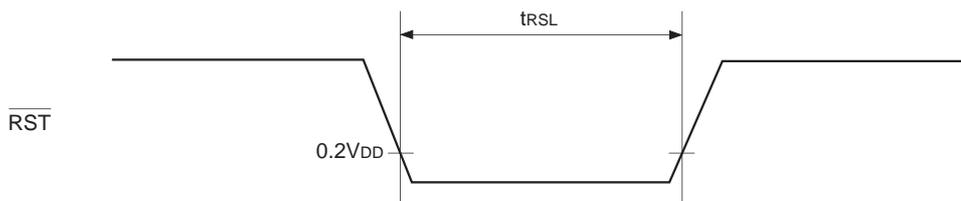
Fig. 11. Reset input timing

(5) Others   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$24t_{FRC} + 200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$16t_{FRC} + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		$8t_{FRC} + 200$		ns
DPG minimum removal time	t_{rem}	DPG		$16t_{FRC} + 200$		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	$t_{sys} = 2000/fc$	$8t_{FRC} + 200 + t_{sys}$		ns

Note 1) $t_{FRC} = 1000/fc$ [ns]

Note 2) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
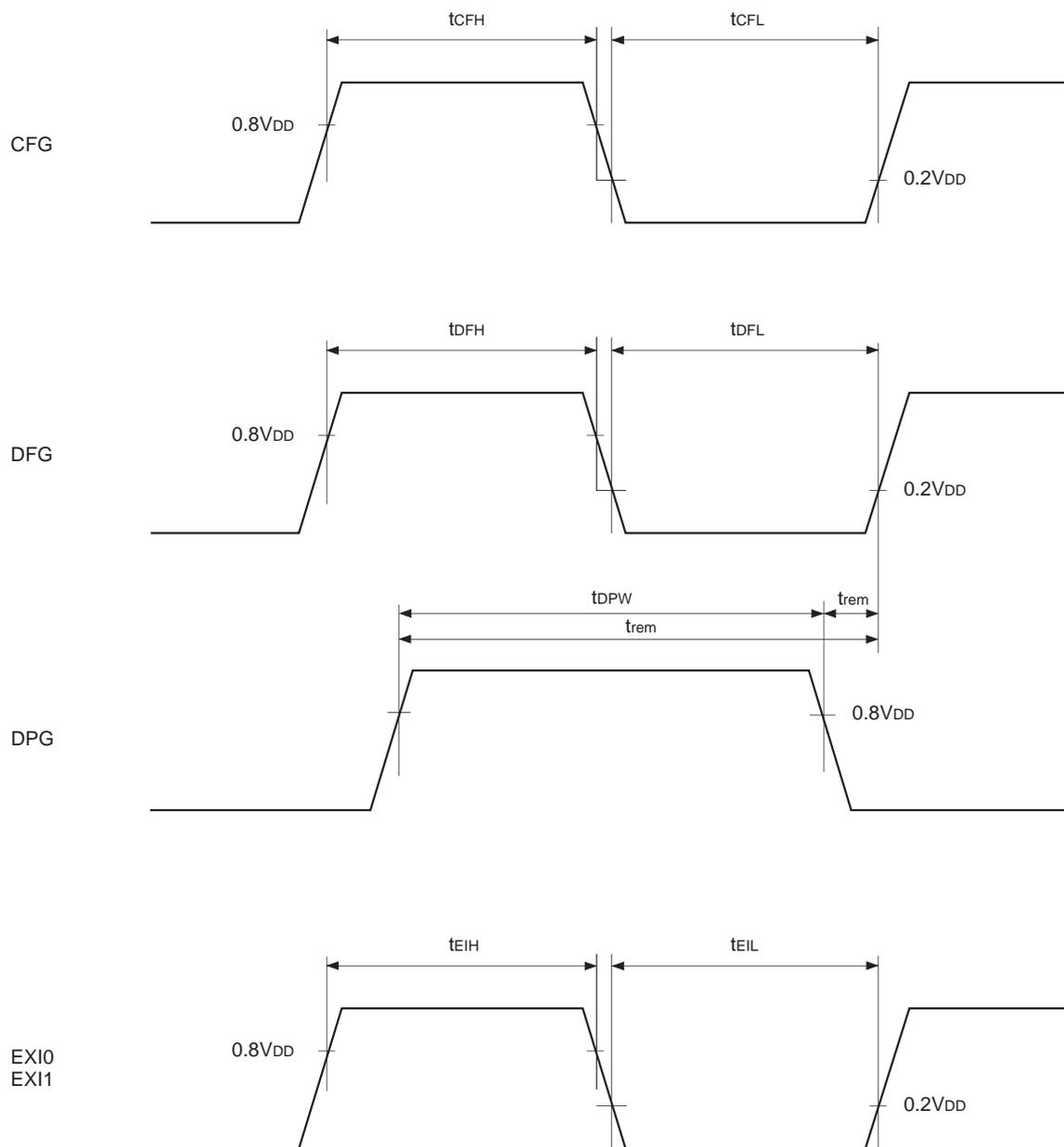
Fig. 12. Other timings

Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics   (AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V$_{OR}$	CTLAGND		2.20	2.45	2.75	V

(2) CTL 1st amplifier characteristics   (AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A$_{VCTL1}$	CTLFAMPI (−) CTLFAMPI (+)	CTLFAMPI (−) = 0V, Gain = 16dB	13.5	15.5	17.5	dB
			CTLFAMPI (−) = 0V, Gain = 34dB	31.8	33.8	35.8	
			CTLFAMPI (−) = 0V, Gain = 49dB	46.5	48.5	50.5	
			CTLFAMPI (−) = 0V, Gain = 55dB	52.5	54.5	56.5	
Output offset voltage	V$_{OSCTL1}$	CTLFAMPI (−) CTLFAMPI (+)	CTLFAMPI (−), CTLFAMPI (+) = open, Gain = 16dB	−25	0	+25	mV

*1 The result after monitoring CTLFAMPO pin when the electrolytic capacitor (10μF) is connected to CTLFAMP (−) and CTLFAMP (+).

(3) CTL 2nd amplifier characteristics   (AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A$_{VCTL2}$	CTLSAMPI	Gain = 5dB	3.5	5.5	7.5	dB
			Gain = 8dB	6.2	8.2	10.2	
			Gain = 11dB	9.0	11.0	13.0	
			Gain = 14dB	12.0	14.0	16.0	
			Gain = 17dB	15.0	17.0	19.0	
			Gain = 20dB	18.0	20.0	22.0	
Output offset voltage	V$_{OSCTL2}$	CTLSAMPI	CTLSAMPI = open, Gain = 5dB	−30	0	+30	mV
LPF cut-off frequency	F$_{CCTL}$	CTLSAMPI	12kHz, f$_{DC}$ − 3dB	8	12	24	kHz
			20kHz, f$_{DC}$ − 3dB	12	20	42	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Comparator level[2]	V_{CCTL}	CTLSAMPI	Comparator level = +100mV$_{0-p}$	80	110	140	mV
			Comparator level = +150mV$_{0-p}$	110	150	190	
			Comparator level = +200mV$_{0-p}$	160	200	240	
			Comparator level = +250mV$_{0-p}$	210	250	290	
			Comparator level = +300mV$_{0-p}$	250	290	330	
			Comparator level = +400mV$_{0-p}$	340	380	420	
			Comparator level = +500mV$_{0-p}$	420	470	520	
			Comparator level = +600mV$_{0-p}$	530	570	610	
			Comparator level = +1000mV$_{0-p}$	850	920	990	
			Comparator level = −100mV$_{0-p}$	−90	−120	−150	
			Comparator level = −150mV$_{0-p}$	−110	−130	−190	
			Comparator level = −200mV$_{0-p}$	−150	−190	−230	
			Comparator level = −250mV$_{0-p}$	−200	−240	−280	
			Comparator level = −300mV$_{0-p}$	−240	−280	−320	
			Comparator level = −400mV$_{0-p}$	−340	−380	−420	
			Comparator level = −500mV$_{0-p}$	−430	−480	−530	
			Comparator level = −600mV$_{0-p}$	−540	−580	−620	
			Comparator level = −1000mV$_{0-p}$	−870	−970	−1070	

[1] The result after monitoring ANOUT pin when the electrolytic capacitor (10μF) is connected to CTLSAMPI.

[2] The reference value of the comparator level is CTLAGND.

(4) CTL amplifier characteristics (CTL1stAMP + CTL2ndAMP)

(AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[3]	A_{VCTL}	CTLHEAD (−) CTLHEAD (+)	CTLHEAD (−) = 0V, Gain = (16dB + 5dB)	17.0	20.5	23.5	dB
			CTLHEAD (−) = 0V, Gain = (55dB + 20dB)	70.5	74.5	77.0	
Input sensitivity	V_{SCTL}	CTLHEAD (−) CTLHEAD (+)	CTLHEAD (−) = 0V, Gain = (55dB + 20dB) Comparator = ±150mV$_{0-p}$	60	70	140	μVp-p

[3] The result when waveform is input from CTLHEAD (+) pin and ANOUT pin is monitored after performing coupling electrolytic capacitor (10μF) of CTLHEAD (−) and CTLHEAD (+), and coupling electrolytic capacitor (10μF) of HEADL (−) and HEADL (+), CTLFAMPI (−) and CTLFAMPI (+) , and CTLFAMPO and CTLSAMPI. Gain is maximum −1.5dB lowered when waveform is input from CTLHEAD (+) pin.

(5) RECCTL write circuit characteristics (AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Write current*1	I$_{OREC}$	CTLHEAD (−) CTLHEAD (+)	Write current 2.0mAp-p	0.8	1.8	3.6	mA
			Write current 3.0mAp-p	1.4	2.8	5.0	
			Write current 4.0mAp-p	2.0	3.8	7.0	
			Write current 5.0mAp-p	2.4	4.8	8.5	
			Write current 6.0mAp-p	3.0	6.0	10.0	
			Write current 7.0mAp-p	3.5	6.8	11.5	
			Write current 8.0mAp-p	4.5	7.8	13.0	
			Write current 9.0mAp-p	5.0	8.8	15.0	
			Write current 10.0mAp-p	5.5	7.7	17.0	

*1 The current which flows when CTLHEAD (−) and CTLHEAD (+) shorts.

(6) Auto threshold control circuit (ATC) characteristics

(AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
ATC peak hold circuit initialize voltage value*2	V$_{ATCINIT}$		Voltage = −150mV$_{0-P}$	−110	−150	−190	mV
			Voltage = −400mV$_{0-P}$	−350	−400	−450	
ATC comparator level offset voltage*3	V$_{ATCOFF}$		Gain = 1/6 (16.7%)		−70	−160	mV
			Gain = 1/5 (20%)		−90	−210	
			Gain = 1/4 (25%)		−90	−210	
			Gain = 1/3 (33.3%)		−70	−160	
			Gain = 2/5 (40%)		−90	−210	
			Gain = 1/2 (50%)		−70	−160	
			Gain = 3/5 (60%)		−90	−210	

*2 Reference is CTLAGND.
*3 Reference is CTLAGND.
When comparator level is generated using ATC, actual comparator level is as follows by the offset voltage inside of ATC.

Vin × gain + |offset voltage|

Example: Gain = 1/2
Vin × 1/2 + 160

(7) Schmitt characteristics (AMPV$_{DD}$ = V$_{DD}$ = 5.0V, AMPV$_{SS}$ = Vss = 0V, Ta = −20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
RTG schmitt width	S$_{RFG}$	RFG0, RFG1	Schmitt width 1Vp-p	820	920	1020	mV
CFG/DFG/DPG	S$_{CFG}$ S$_{DFG}$ S$_{DPG}$	CFG, DFG, DPG	Schmitt width 410mVp-p	180	300	420	mV
			Schmitt width 1Vp-p	700	900	1100	

Appendix

Fig. 13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format[*1]	CMOS schmitt	TTL schmitt

[*1] The input circuit format can be selected for PE3/SYNC pin.

Characteristics Curve

I$_{DD}$ vs. V$_{DD}$
(fc = 16MHz, Ta = 25°)

I$_{DD}$ – Supply current [mA]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- Sleep mode
- 32kHz mode (instruction)
- 32kHz Sleep mode

V$_{DD}$ – Supply voltage [V]

I$_{DD}$ vs. fc
(V$_{DD}$ = 5.0V, Ta = 25°)

I$_{DD}$ – Supply current [mA]

- 1/2 dividing mode
- 1/4 dividing mode
- 1/16 dividing mode
- Sleep mode

fc – System clock [MHz]

– 33 –
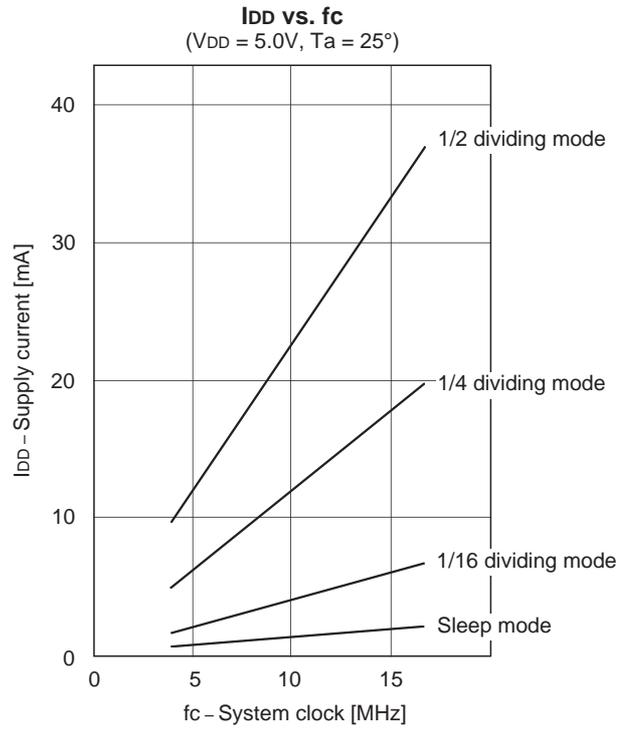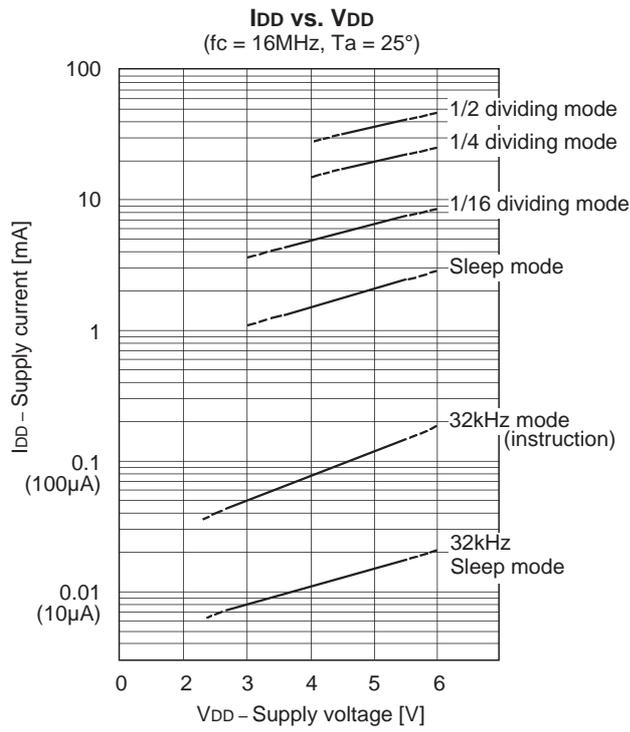
Package Outline   Unit: mm

100PIN QFP (PLASTIC)
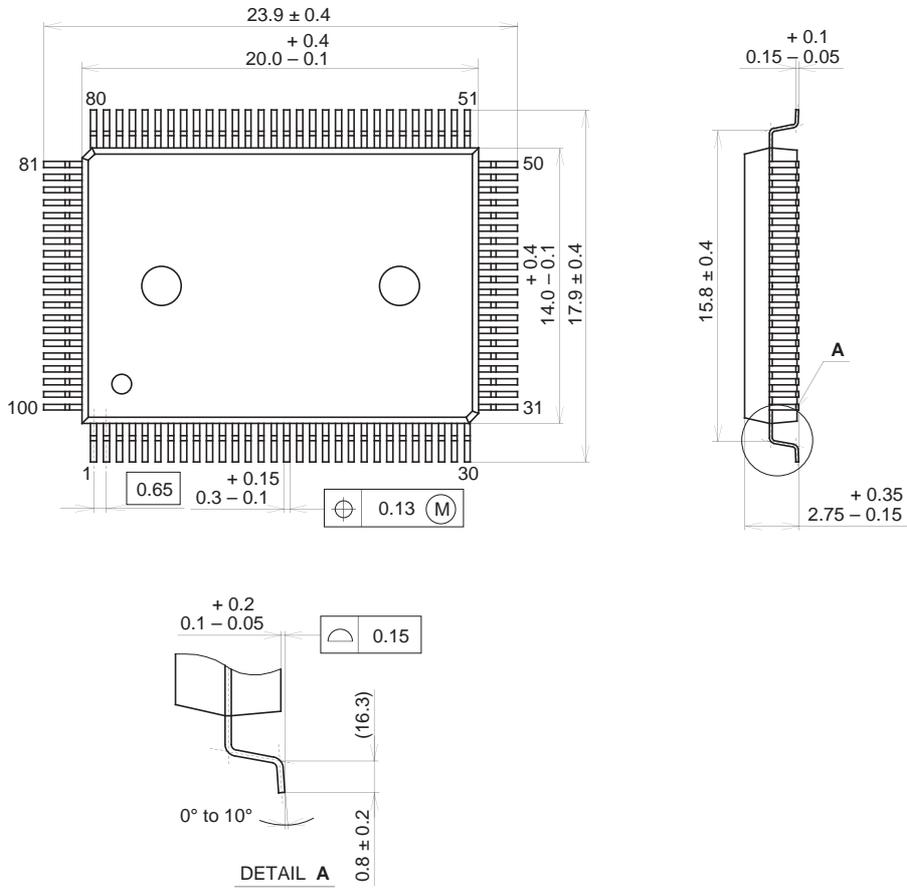
SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g