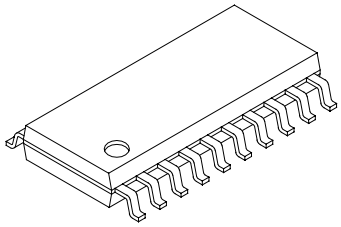
SONY

CXL1504M

CMOS-CCD 1H Delay Line for NTSC

20 pin SOP (Plastic)



Description

The CXL1504M is a delay line used in conjunction with an external low-pass filter. Through negative phase input and positive phase output 1H delay time is obtained for NTSC signals.

Features

- Single 5V power supply
- 14.3MHz driver
- Low power consumption at 160mW (Typ.)
- Built-in peripheral circuits
- Completely adjustment free

Functions

- 905.5-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Operating Voltage Range (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

Recommended Clock Conditions (Ta = 25°C)

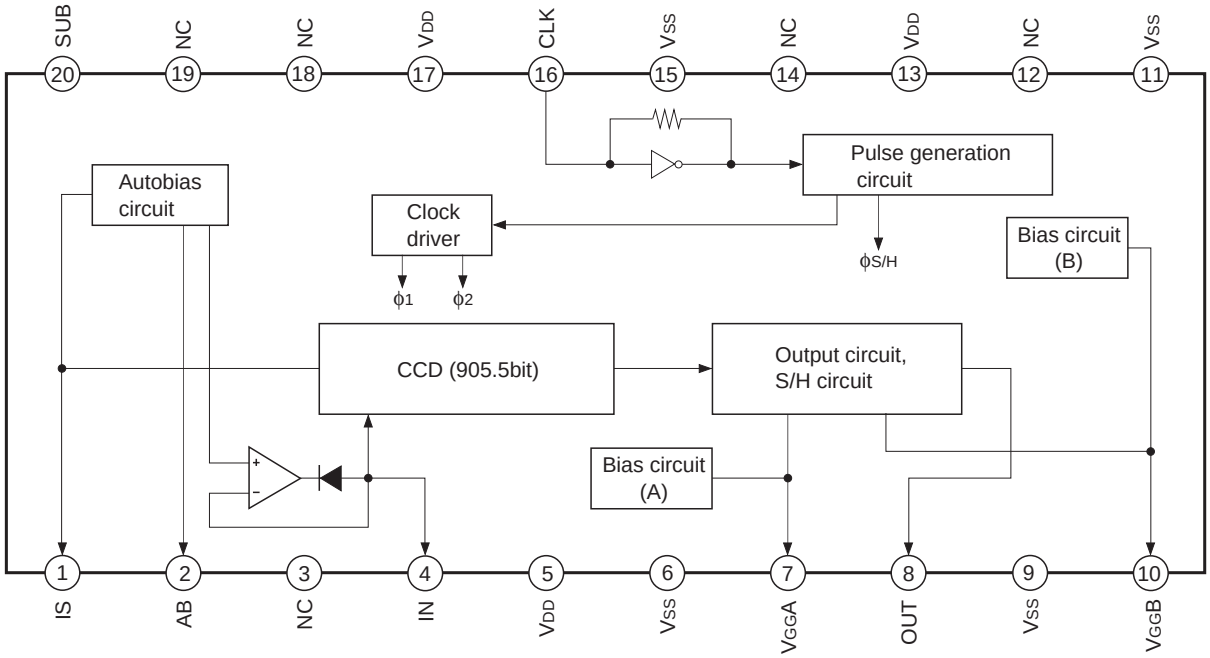
• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5Vp-p typ.)
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform	sine wave		

Input Signal Amplitude

	V_{SIG}	560	mVp-p (Max.)

E71217A78-PS

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description	Impedance [Ω]
1	IS	O	CCD bias DC output	600 to 2k
2	AB	O	Autobias DC output	2k to 20k
3	NC	—		
4	IN	I	Signal input (Negative phase signal)	> 100k (at no clamp)
5	V_{DD}	—	5V power supply (For clock driver)	
6	V_{SS}	—	GND	
7	$V_{GG}A$	O	Gate bias (A) DC output	2k to 10k
8	OUT	O	Signal output (Positive phase signal)	40 to 500
9	V_{SS}	—	GND	
10	$V_{GG}B$	O	Gate bias (B) DC output	2k to 10k
11	V_{SS}	—	GND	
12	NC	—		
13	V_{DD}	—	5V power supply (For analog system)	
14	NC	—		
15	V_{SS}	—	GND	
16	CLK	I	Clock input	4k to 50k
17	V_{DD}	—	5V power supply (For digital system)	
18	NC	—		
19	NC	—		
20	SUB	—	GND	

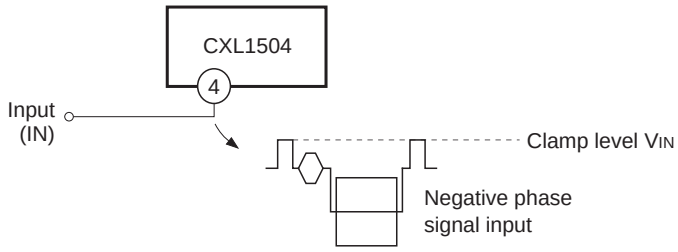
Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 14.318182MHz, V_{CLK} = 500mVp-p, sine wave)
See the Electrical Characteristics Test Circuits.

Item	Symbol	Test conditions	SW conditions				(Note 1) Bias conditions $V_{BIAS}1$ [V]	Min.	Typ.	Max.	Unit	Note
			1	2	3	4						
Supply current	I_{DD}	—	a	a	a	—	—	20	32	42	mA	2
Low frequency gain	GL	200kHz, 500mVp-p, sine wave	a	a	a	b	—	–5.0	–3.0	–1.0	dB	3
Frequency response	fr	200kHz ↔ 3.58MHz, 150mVp-p, sine wave	b ↕ c	a	b	b	V_{IN} – 0.2	–2.5	–1.3	0	dB	4
Differential gain	DG	5-staircase wave (See Note 5)	d	a	a	c	—	0	3	7	%	5
Differential phase	DP	5-staircase wave (See Note 5)	d	a	a	c	—	0	3	7	degree	5
S/H pulse coupling	CP	No signal input	—	b	b	a	V_{IN}	—	200	350	mVp-p	6
S/N ratio	S/N	50% white video signal (See Note 7)	e	a	a	d	—	54	56	—	dB	7

Notes

1) V_{IN} is defined as follows.
V_{IN} is the input signal clamp level, it clamps the video signal sync tip level.



V_{IN} is the pin voltage for Pin 4 at no-input signal. Testing is executed with a voltmeter under the follwing SW conditions.

Item	SW conditions				Test point
	1	2	3	4	
V_{IN}	—	b	a	—	V1

As V_{IN} varies with each IC, they are all subject to testing.

2) I_{DD} is the IC supply current value during clock and signal input.

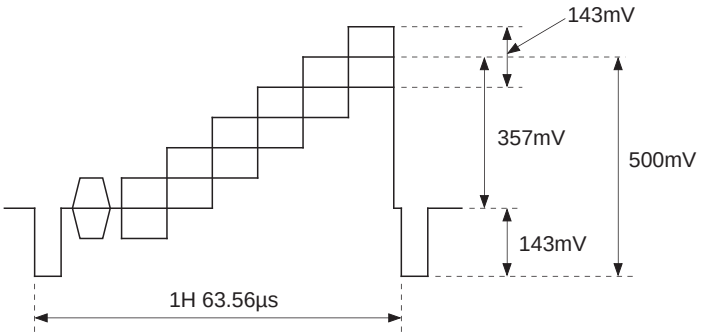
3) GL is the OUT pin output gain when a 500mVp-p, 200kHz sine wave is input to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

4) Indicates the dissipation at 3.58MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 3.58MHz sine wave is fed to same, calculation is made according to the following formula. The input part bias is tested at V_{IN} – 0.2V.

$$fr = 20 \log \frac{\text{OUT pin output voltage (3.58MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}} \quad [dB]$$

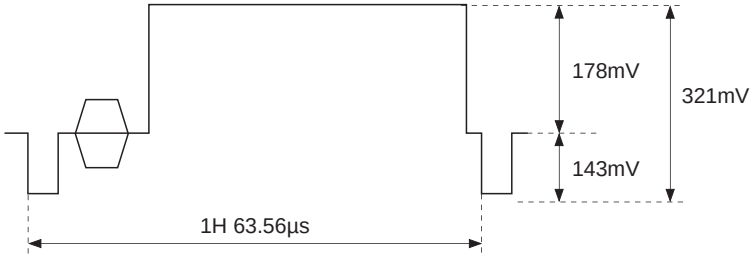
5) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the figure. below is input are tested at the vector scope.



IN pin input waveform is the inverted waveform in the figure above

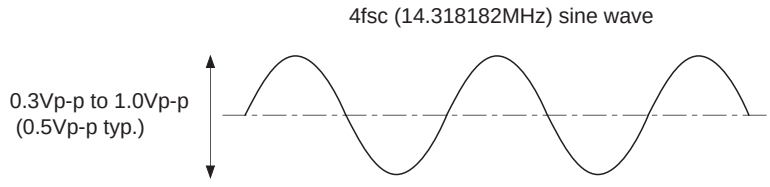
6) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at V_{IN}V.

7) S/N ratio during 50% white video signal input shown in figure. below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.

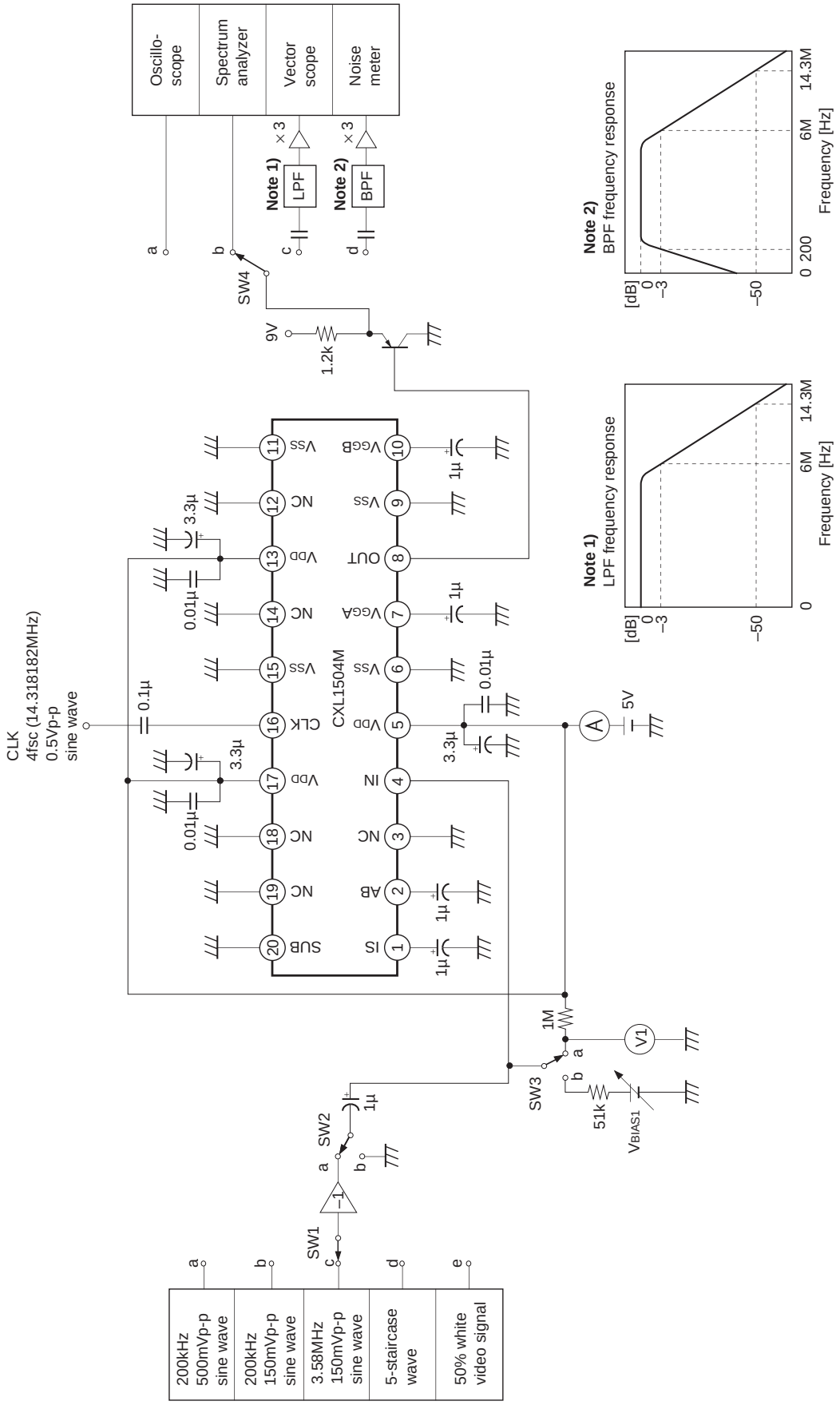


IN pin input waveform is the inverted waveform in the figure above

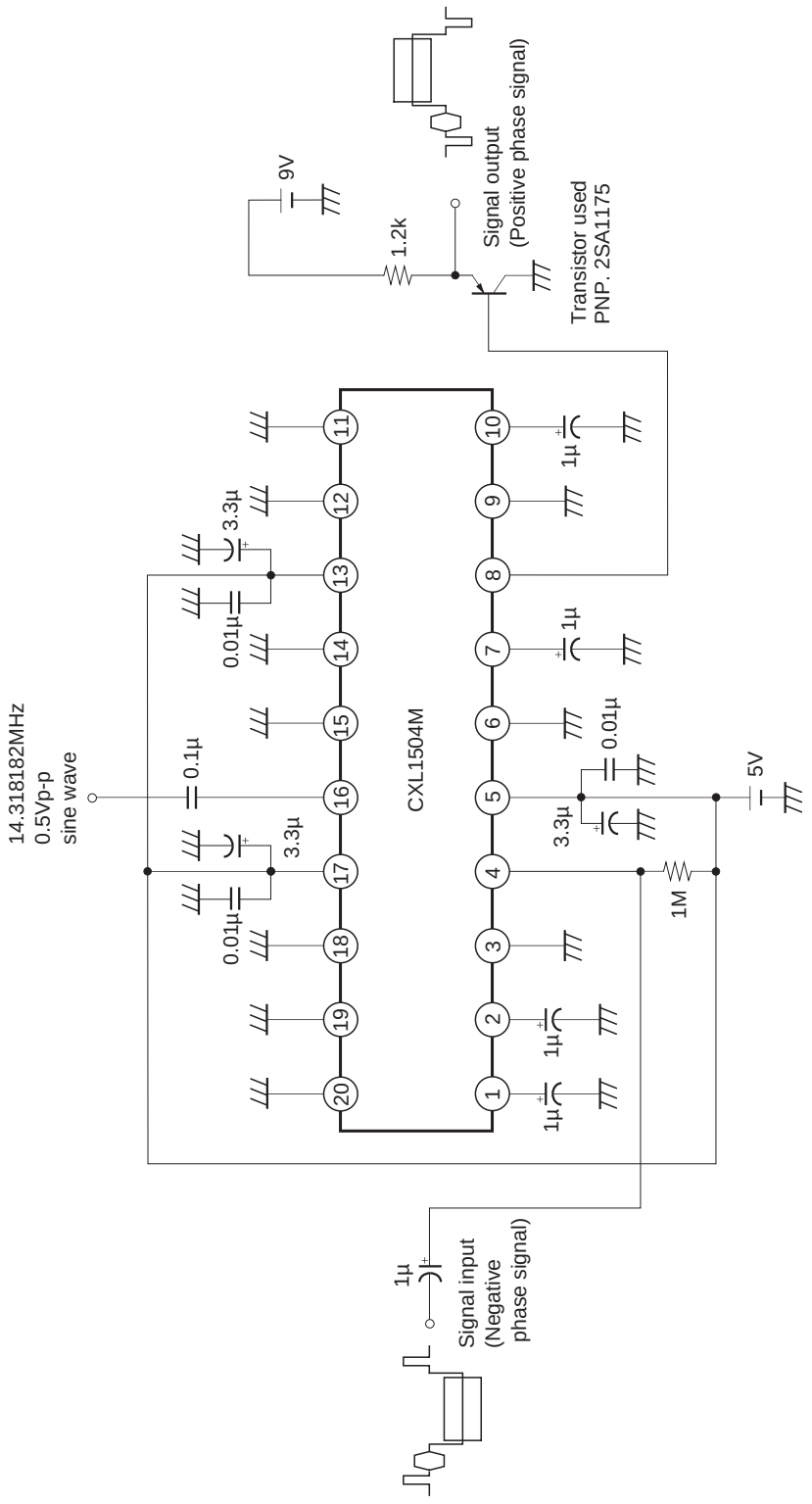
Clock



Electrical Characteristics Test Circuit



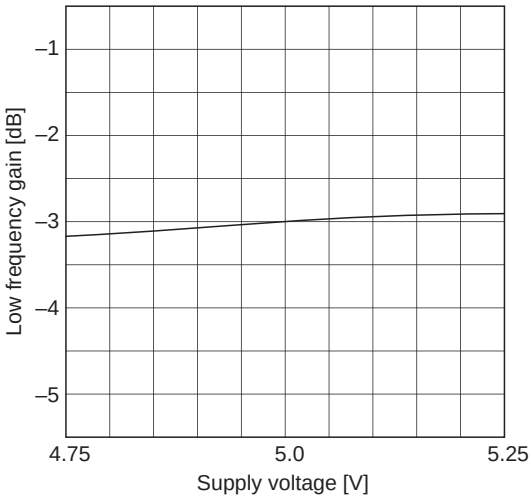
Application Circuit



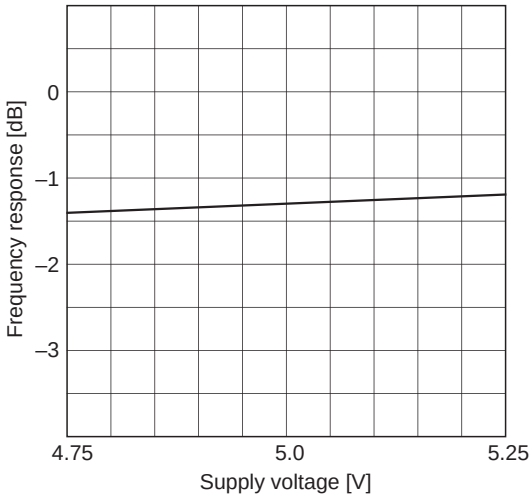
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

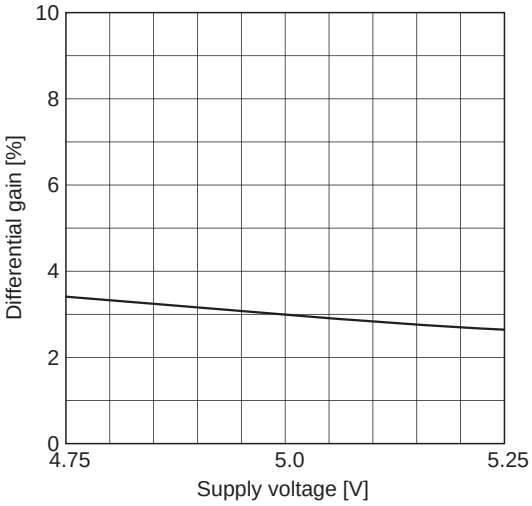
Low frequency gain vs. Supply voltage



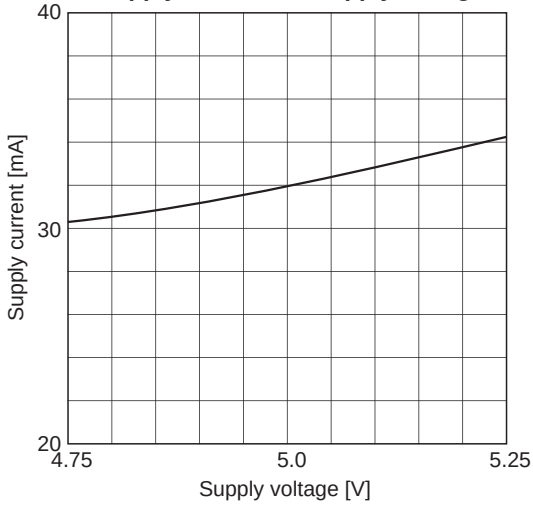
Frequency response vs. Supply voltage



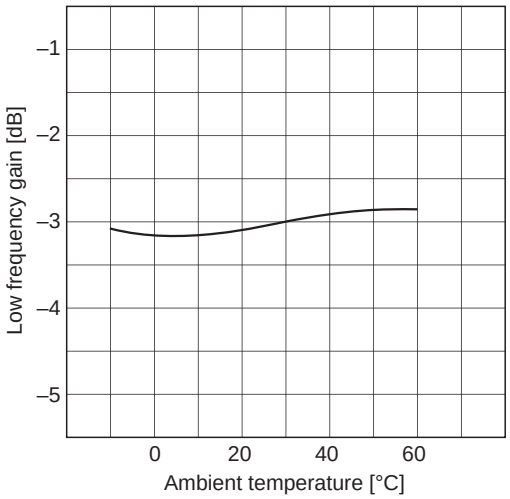
Differential gain vs. Supply voltage



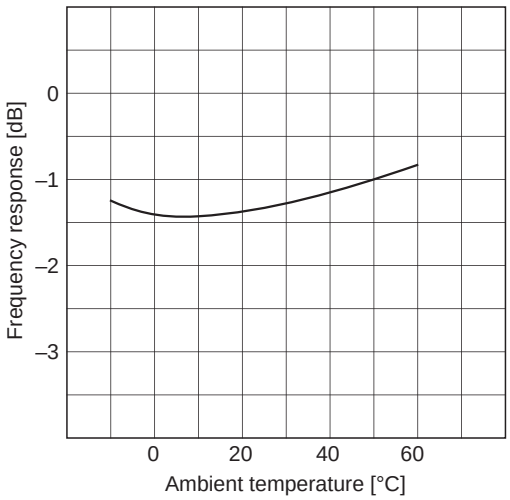
Supply current vs. Supply voltage



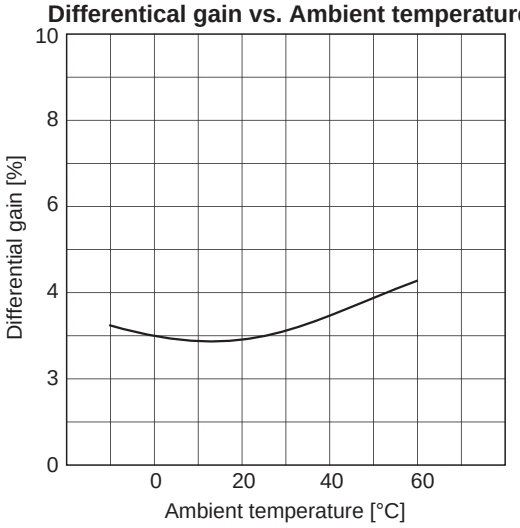
Low frequency gain vs. Ambient temperature



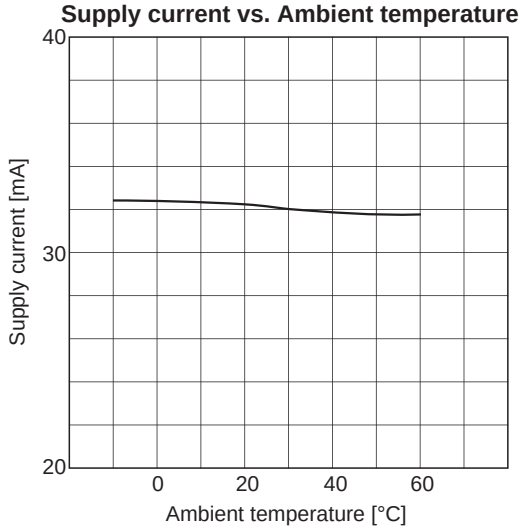
Frequency response vs. Ambient temperature



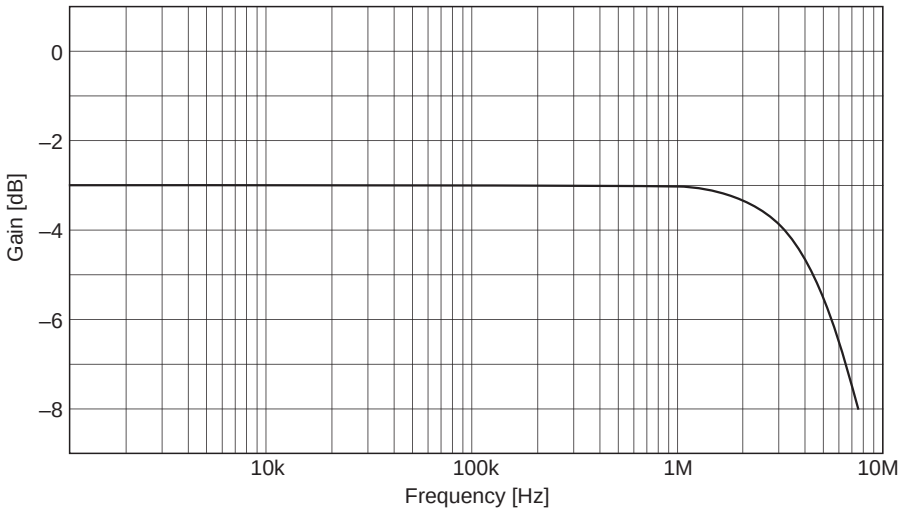
Differentical gain vs. Ambient temperature



Supply current vs. Ambient temperature

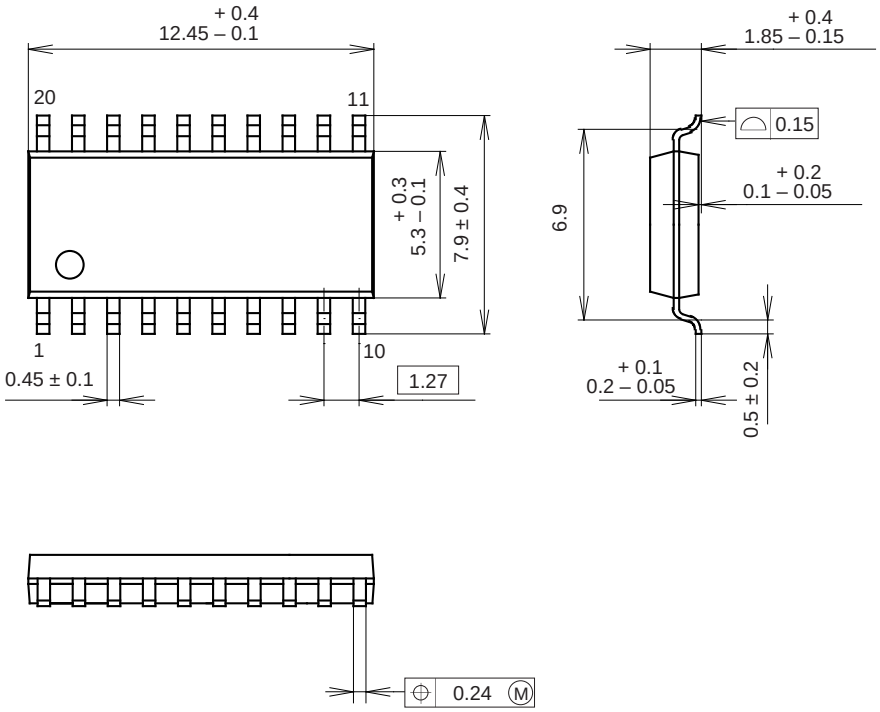


Frequency response



Package Outline Unit: mm

20PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	SOP020-P-0300
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g