SONY

# ICX080AK

## Diagonal 6mm (Type 1/3) CCD Image Sensor for NTSC Color Video Cameras

### Description

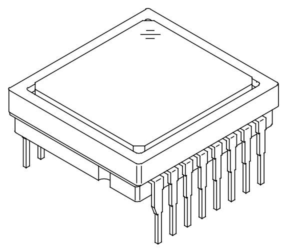
The ICX080AK is an interline CCD solid-state image sensor suitable for NTSC color video cameras. This chip conforms to DV standard SD mode, and has the optimal number of pixels for MPEG2 Main level. While achieving a horizontal resolution of 450 TV lines, the area has been expanded 33% in both vertical and horizontal directions, making the chip suitable for electronic vibration stabilizer and electronic panning/tilting. In addition, complete 16:9 wide aspect ratio images are provided with a high picture quality without requiring vertical interpolation.

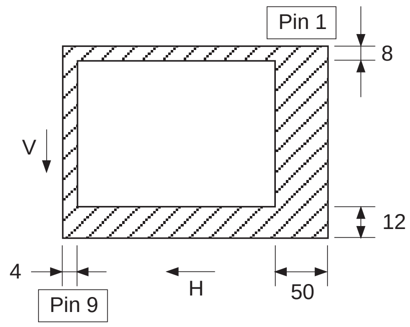
High sensitivity and low dark current are achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

This chip features a field period readout system and an electronic shutter with variable charge-storage time.

The package is a 16-pin DIP (Plastic), and both top and bottom surface reference can be assured at the same time.

16 pin DIP (Plastic)






**Optical black position (Top View)**

### Features

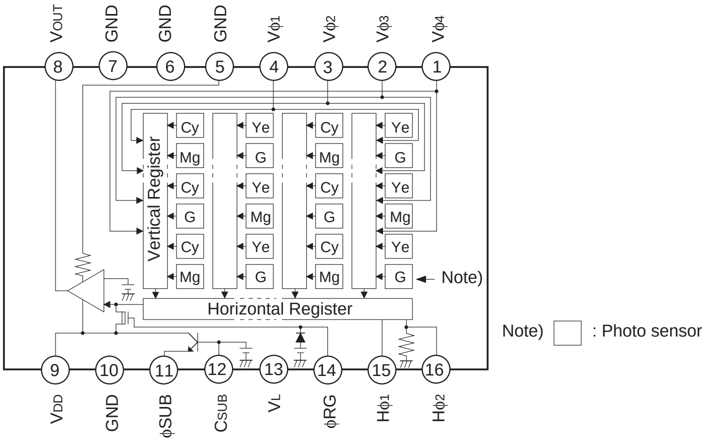
- Supports electronic vibration stabilizer and electronic panning/tilting (33%/one side)
- Supports electronic zoom
- Supports DV standard SD mode and MPEG2 Main level (13.5MHz)
- Supports 16:9 wide aspect ratio (for both 18MHz and 5fsc)
- Supply voltage: 12V
- Horizontal register and reset gate: 2.7 to 3.6V drive
- No voltage adjustment (Reset gate and substrate bias are not adjusted.)
- High resolution, high sensitivity, low dark current and low smear
- Excellent antiblooming characteristics
- Continuous variable-speed shutter (1/60 to 1/10000s)
- Supports short exit pupil distance (Recommended range: –20 to –100mm)
- Ye, Cy, Mg and G complementary color mosaic filters on chip
- 16-pin high precision plastic package (both top and bottom surface reference possible)

### Device Structure

| | | | |
|---|---|---|---|
| • Interline CCD image sensor | | | |
| • Image size: | | Diagonal 6mm (Type 1/3) | |
| • Total number of pixels: | | 1016 (H) x 674 (V) | approx. 680K pixels |
| • Total number of effective pixels: | | 962 (H) x 654 (V) | approx. 630K pixels |
| • Number of effective pixels: | 4:3 NTSC: | 711 (H) x 485 (V) | approx. 340K pixels |
| | 16:9 18MHz: | 948 (H) x 485 (V) | approx. 460K pixels |
| | 16:9 5fsc: | 942 (H) x 485 (V) | approx. 460K pixels |
| • Chip size: | | 5.90mm (H) x 4.92mm (V) | |
| • Unit cell size: | | 5.05µm (H) x 5.55µm (V) | |
| • Optical black: | | Horizontal (H) direction: | Front 4 pixels, rear 50 pixels |
| | | Vertical (V) direction: | Front 12 pixels, rear 8 pixels |
| • Number of dummy bits: | | Horizontal 28 | |
| | | Vertical 1 (even fields only) | |
| • Substrate material: | | Silicon | |

## Block Diagram and Pin Configuration

(Top View)




## Pin Description

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---|---|---|---|---|---|
| 1 | $V\phi_4$ | Vertical register transfer clock | 9 | $V_{DD}$ | Supply voltage |
| 2 | $V\phi_3$ | Vertical register transfer clock | 10 | GND | GND |
| 3 | $V\phi_2$ | Vertical register transfer clock | 11 | $\phi SUB$ | Substrate clock |
| 4 | $V\phi_1$ | Vertical register transfer clock | 12 | $C_{SUB}$ | Substrate bias *1 |
| 5 | GND | GND | 13 | $V_L$ | Protective transistor bias |
| 6 | GND | GND | 14 | $\phi RG$ | Reset gate clock |
| 7 | GND | GND | 15 | $H\phi_1$ | Horizontal register transfer clock |
| 8 | $V_{OUT}$ | Signal output | 16 | $H\phi_2$ | Horizontal register transfer clock |

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

## Absolute Maximum Ratings

| Item | | Ratings | Unit | Remarks |
|---|---|---|---|---|
| Against $\phi SUB$ | $V_{DD}$, $V_{OUT}$, $\phi RG$ – $\phi SUB$ | –40 to +10 | V | |
| | $V\phi_1$, $V\phi_3$ – $\phi SUB$ | –50 to +15 | V | |
| | $V\phi_2$, $V\phi_4$, $V_L$ – $\phi SUB$ | –50 to +0.3 | V | |
| | $H\phi_1$, $H\phi_2$, GND – $\phi SUB$ | –40 to +0.3 | V | |
| | $C_{SUB}$ – $\phi SUB$ | –25 to | V | |
| Against GND | $V_{DD}$, $V_{OUT}$, $\phi RG$, $C_{SUB}$ – GND | –0.3 to +18 | V | |
| | $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – GND | –10 to +18 | V | |
| | $H\phi_1$, $H\phi_2$ – GND | –10 to +5 | V | |
| Against $V_L$ | $V\phi_1$, $V\phi_3$ – $V_L$ | –0.3 to +28 | V | |
| | $V\phi_2$, $V\phi_4$, $H\phi_1$, $H\phi_2$, GND – $V_L$ | –0.3 to +15 | V | |
| Between input clock pins | Voltage difference between vertical clock input pins | to +15 | V | *2 |
| | $H\phi_1$ – $H\phi_2$ | –5 to +5 | V | |
| | $H\phi_1$, $H\phi_2$ – $V\phi_4$ | –13 to +13 | V | |
| Storage temperature | | –30 to +80 | °C | |
| Operating temperature | | –10 to +60 | °C | |

*2 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

### Bias Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 11.64 | 12.0 | 12.36 | V | |
| Protective transistor bias | $V_L$ | | *1 | | | |
| Substrate clock | $\phi SUB$ | | *2 | | | |
| Reset gate clock | $\phi RG$ | | *2 | | | |

*1 $V_L$ setting is the $V_{VL}$ voltage of the vertical transfer clock waveform, or the same power supply as the $V_L$ power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

### DC Characteristics

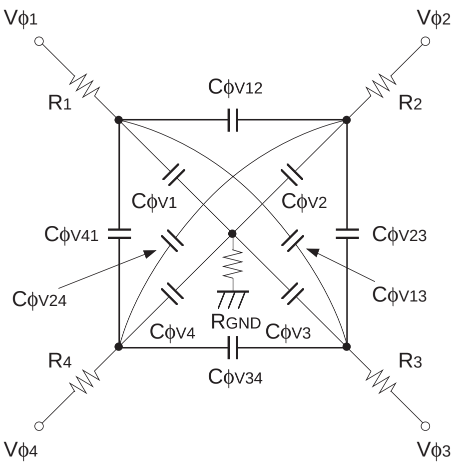
| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply current | $I_{DD}$ | | 6.0 | | mA | |

### Clock Voltage Conditions

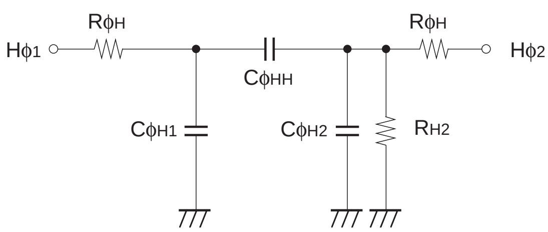
| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|---|---|---|---|---|---|---|---|
| Readout clock voltage | $V_{VT}$ | 11.64 | 12.0 | 12.36 | V | 1 | |
| Vertical transfer clock voltage | $V_{VH1}$, $V_{VH2}$ | –0.05 | 0 | 0.05 | V | 2 | $V_{VH} = (V_{VH1} + V_{VH2})/2$ |
| | $V_{VH3}$, $V_{VH4}$ | –0.2 | 0 | 0.05 | V | 2 | |
| | $V_{VL1}$, $V_{VL2}$, $V_{VL3}$, $V_{VL4}$ | –6.85 | –6.5 | –6.15 | V | 2 | $V_{VL} = (V_{VL3} + V_{VL4})/2$ |
| | $V_{\phi V}$ | 5.95 | 6.5 | 6.9 | V | 2 | $V_{\phi V} = V_{VH}n – V_{VL}n$ (n = 1 to 4) |
| | $V_{VH3} – V_{VH}$ | –0.25 | | 0.1 | V | 2 | |
| | $V_{VH4} – V_{VH}$ | –0.25 | | 0.1 | V | 2 | |
| | $V_{VHH}$ | | | 0.5 | V | 2 | High-level coupling |
| | $V_{VHL}$ | | | 0.5 | V | 2 | High-level coupling |
| | $V_{VLH}$ | | | 0.5 | V | 2 | Low-level coupling |
| | $V_{VLL}$ | | | 0.5 | V | 2 | Low-level coupling |
| Horizontal transfer clock voltage | $V_{\phi H}$ | 2.7 | 3.3 | 3.6 | V | 3 | |
| | $V_{HL}$ | –0.05 | 0 | 0.05 | V | 3 | |
| | $V_{CR}$ | 0.5 | 1.65 | | V | 3 | Cross-point voltage |
| Reset gate clock voltage | $V_{\phi RG}$ | 2.7 | 3.3 | 3.6 | V | 4 | |
| | $V_{RGLH} – V_{RGLL}$ | | | 0.4 | V | 4 | Low-level coupling |
| | $V_{RGL} – V_{RGLm}$ | | | 0.5 | V | 4 | Low-level coupling |
| Substrate clock voltage | $V_{\phi SUB}$ | 17.3 | 18.5 | 19.3 | V | 5 | |

### Clock Equivalent Circuit Constant

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Capacitance between vertical transfer clock and GND | $C_{\phi V1}$, $C_{\phi V3}$ | | 1000 | | pF | |
| | $C_{\phi V2}$, $C_{\phi V4}$ | | 560 | | pF | |
| Capacitance between vertical transfer clocks | $C_{\phi V12}$, $C_{\phi V34}$ | | 470 | | pF | |
| | $C_{\phi V23}$, $C_{\phi V41}$ | | 390 | | pF | |
| | $C_{\phi V13}$ | | 180 | | pF | |
| | $C_{\phi V24}$ | | 100 | | pF | |
| Capacitance between horizontal transfer clock and GND | $C_{\phi H1}$, $C_{\phi H2}$ | | 62 | | pF | |
| Capacitance between horizontal transfer clocks | $C_{\phi HH}$ | | 62 | | pF | |
| Capacitance between reset gate clock and GND | $C_{\phi RG}$ | | 12 | | pF | |
| Capacitance between substrate clock and GND | $C_{\phi SUB}$ | | 270 | | pF | |
| Vertical transfer clock series resistor | $R_1$, $R_2$, $R_3$, $R_4$ | | 82 | | Ω | |
| Vertical transfer clock ground resistor | $R_{GND}$ | | 15 | | Ω | |
| Horizontal transfer clock series resistor | $R_{\phi H}$ | | 3 | | Ω | |
| Horizontal transfer clock ground resistor | $R_{H2}$ | | 30 | | kΩ | |



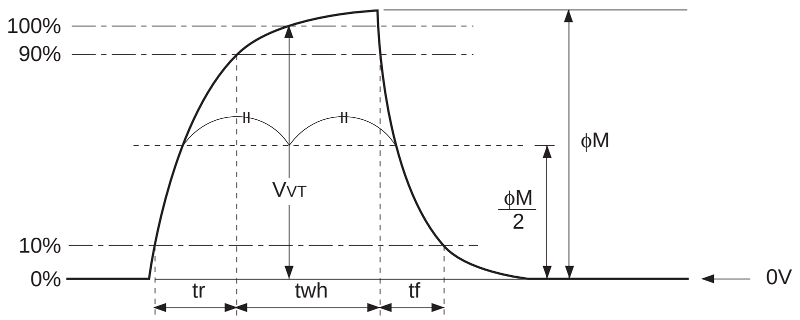

**Vertical transfer clock equivalent circuit**



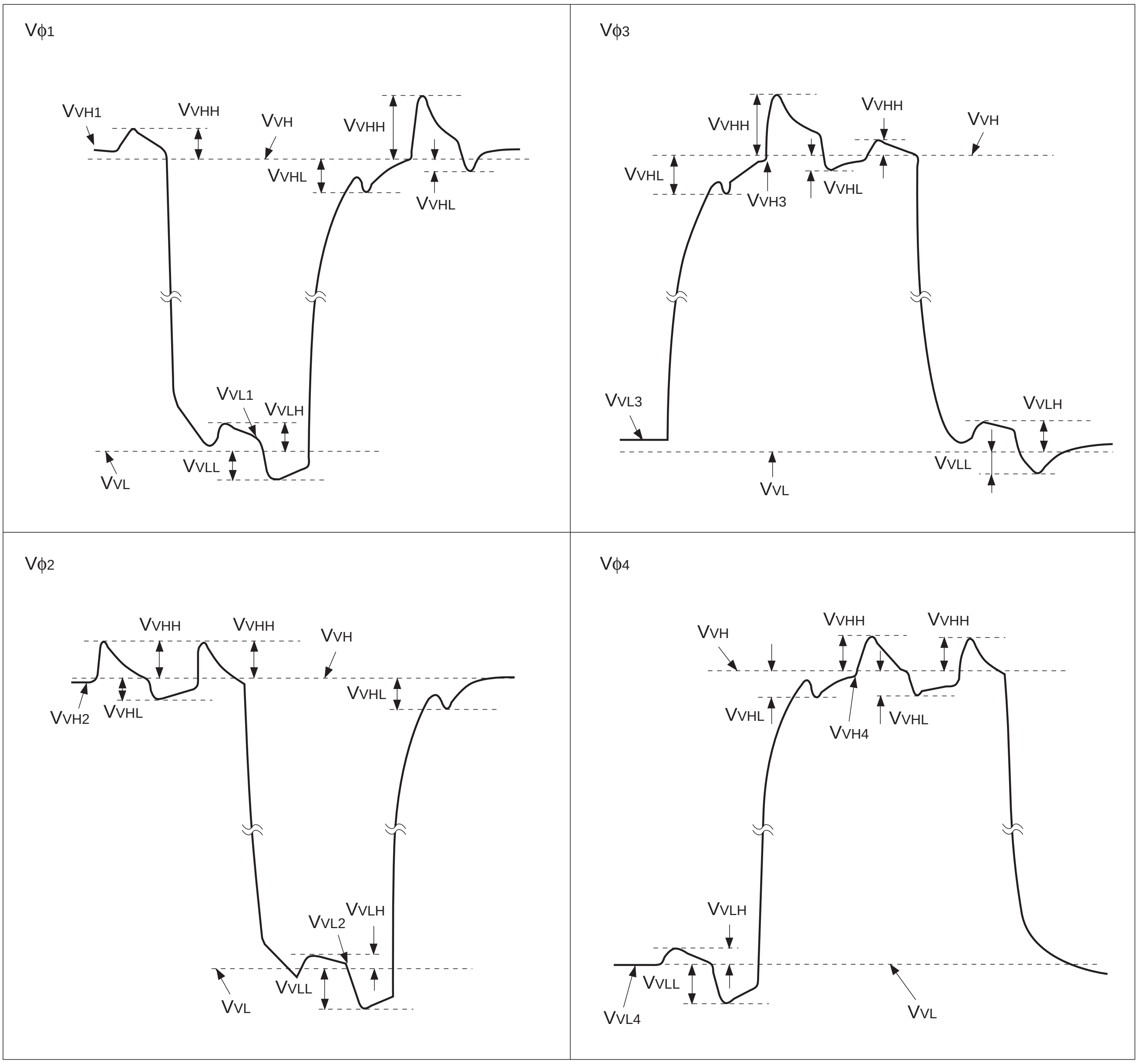

**Horizontal transfer clock equivalent circuit**

## Drive Clock Waveform Conditions

### (1) Readout clock waveform




### (2) Vertical transfer clock waveform

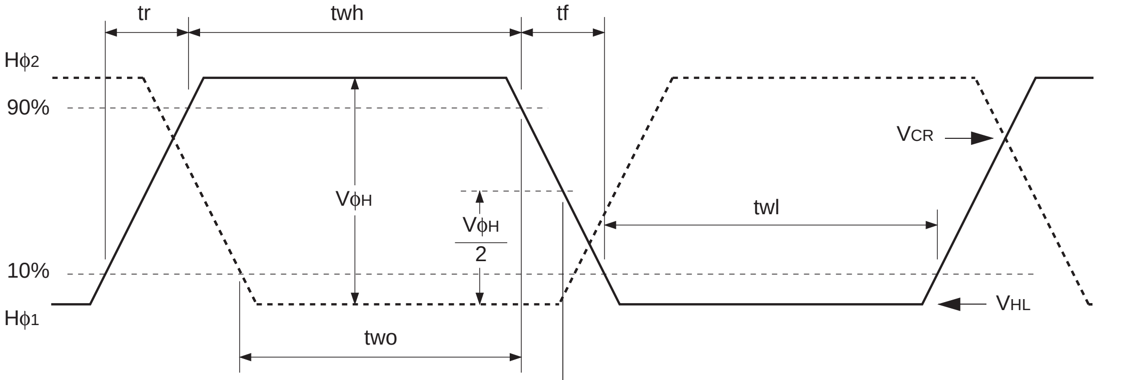



$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

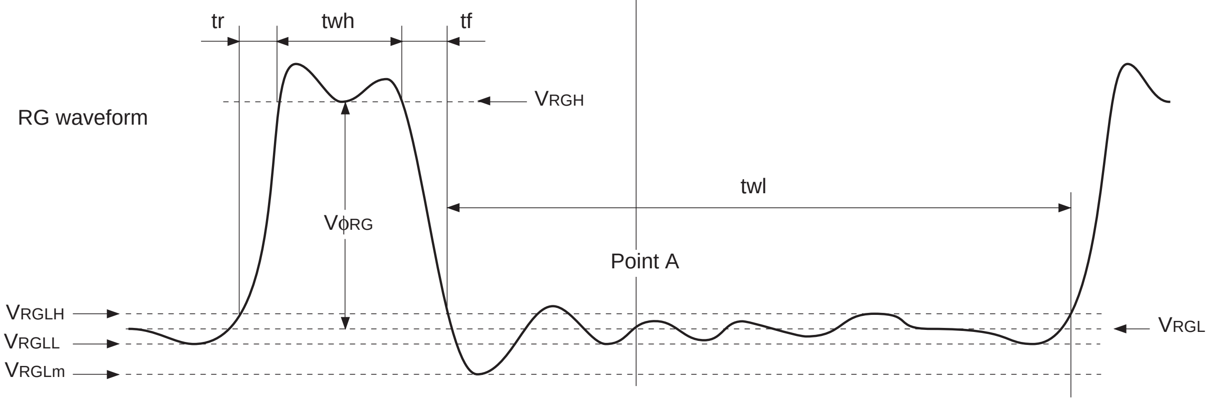
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

### (3) Horizontal transfer clock waveform




Cross-point voltage for the $H\phi_1$ rising side of the horizontal transfer clocks $H\phi_1$ and $H\phi_2$ waveforms is $V_{CR}$.
The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

### (4) Reset gate clock waveform




$V_{RGLH}$ is the maximum value and $V_{RGLL}$ is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, $V_{RGL}$ is the average value of $V_{RGLH}$ and $V_{RGLL}$.

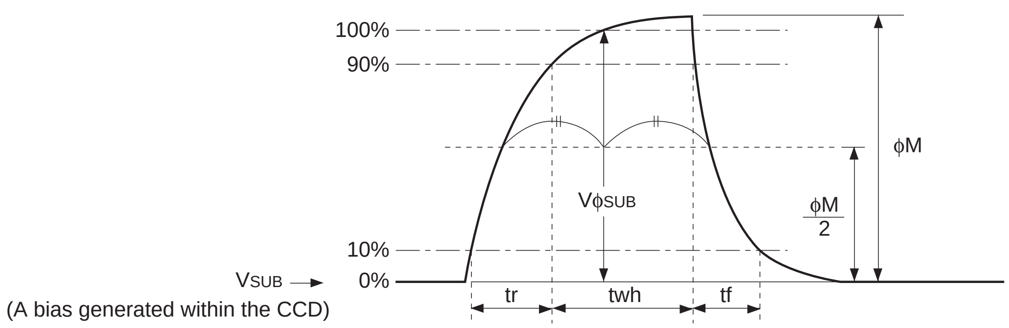
$$V_{RGL} = (V_{RGLH} + V_{RGLL}) /2$$

Assuming $V_{RGH}$ is the minimum value during the interval twh, then:

$$V\phi_{RG} = V_{RGH} - V_{RGL}.$$

Negative overshoot level during the falling edge of RG is $V_{RGLm}$.

### (5) Substrate clock waveform



### Clock Switching Characteristics

| Item | Symbol | twh | | | twl | | | tr | | | tf | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Readout clock | $V_T$ | 1.36 | 1.56 | | | | | | 0.5 | | | 0.5 | | μs | During readout |
| Vertical transfer clock | $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ | | | | | | | | | | 15 | | 250 | ns | During CXD1267AN used |
| Horizontal transfer clock: During imaging | $H\phi_1$ | 14 | 19.5 | | 14 | 19.5 | | | 8.5 | 14 | | 8.5 | 14 | ns | tf ≥ tr – 2ns |
| | $H\phi_2$ | 14 | 19.5 | | 14 | 19.5 | | | 8.5 | 14 | | 8.5 | 14 | | |
| Horizontal transfer clock: During parallel-serial conversion | $H\phi_1$ | | 5.56 | | | | | | 0.01 | | | 0.01 | | μs | |
| | $H\phi_2$ | | | | | 5.56 | | | 0.01 | | | 0.01 | | | |
| Reset gate clock | $\phi RG$ | 7 | 10 | | | 37 | | | 4 | | | 5 | | ns | |
| Substrate clock | $\phi SUB$ | 1.7 | 3.06 | | | | | | | 0.5 | | | 0.5 | μs | During drain charge |

| Item | Symbol | two | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Horizontal transfer clock | $H\phi_1$, $H\phi_2$ | 12 | 19.5 | | ns | |

**Spectral Sensitivity Characteristics** (excludes both lens characteristics and light source characteristics)

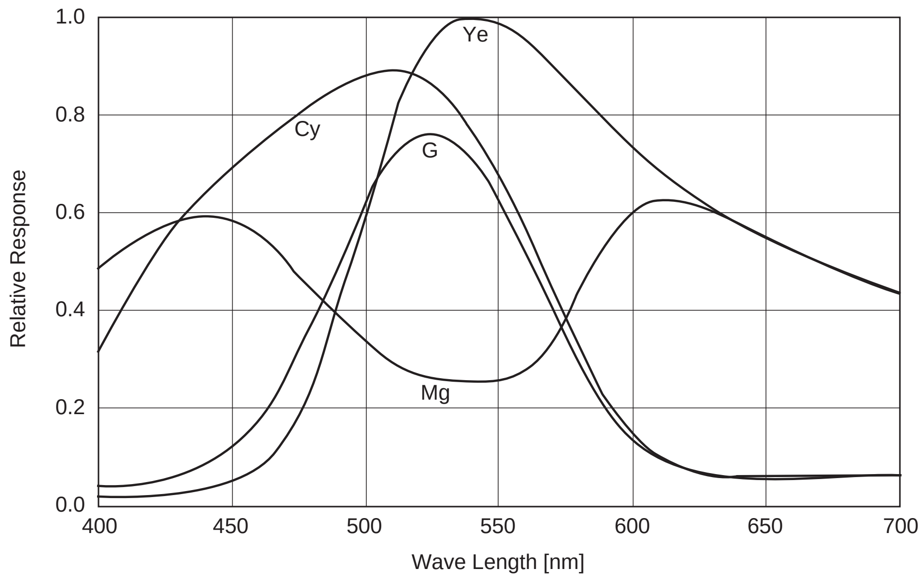
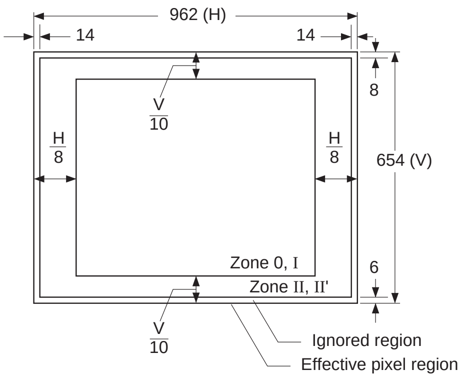


**Image Sensor Characteristics** (Ta = 25°C)

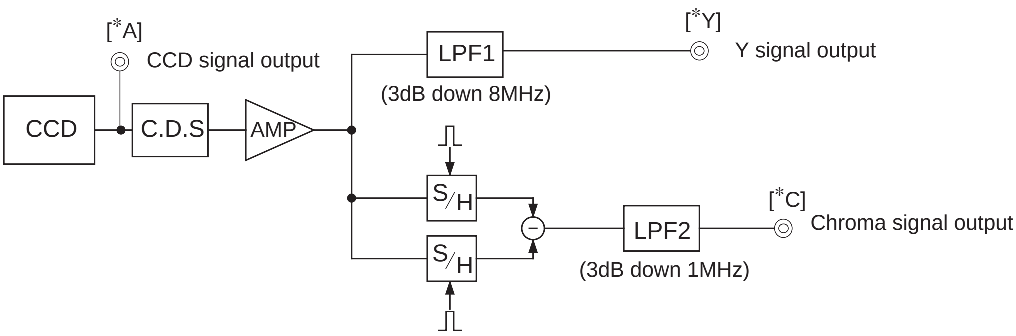
| Item | Symbol | Min. | Typ. | Max. | Unit | Measurement method | Remarks |
|---|---|---|---|---|---|---|---|
| Sensitivity | S | 240 | 300 | | mV | 1 | |
| Saturation signal | Ysat | 600 | | | mV | 2 | Ta = 60°C |
| Smear | Sm | | 0.009 | 0.015 | % | 3 | |
| Video signal shading | SHy | | | 20 | % | 4 | Zone 0 and I |
| | | | | 25 | % | 4 | Zone 0 to II' |
| Uniformity between video signal channels | ΔSr | | | 10 | % | 5 | |
| | ΔSb | | | 10 | % | 5 | |
| Dark signal | Ydt | | | 2 | mV | 6 | Ta = 60°C |
| Dark signal shading | ΔYdt | | | 1 | mV | 7 | Ta = 60°C, *1 |
| Flicker Y | Fy | | | 2 | % | 8 | |
| Flicker R-Y | Fcr | | | 5 | % | 8 | |
| Flicker B-Y | Fcb | | | 5 | % | 8 | |
| Line crawl R | Lcr | | | 3 | % | 9 | |
| Line crawl G | Lcg | | | 3 | % | 9 | |
| Line crawl B | Lcb | | | 3 | % | 9 | |
| Line crawl W | Lcw | | | 3 | % | 9 | |
| Lag | Lag | | | 0.5 | % | 10 | |

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

**Zone Definition of Video Signal Shading**




**Measurement System**




**Note)** Adjust the amplifier gain so that the gain between [*A] and [*Y], and between [*A] and [*C] equals 1.

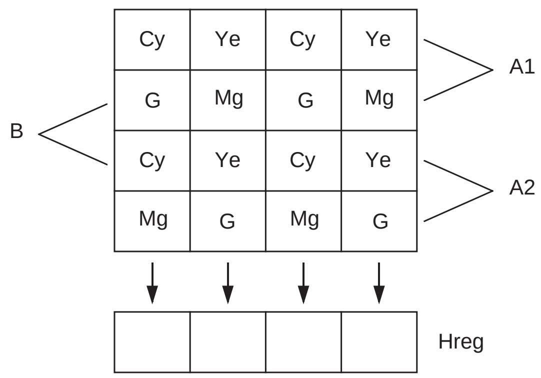
## Image Sensor Characteristics Measurement Method

### ◎ Measurement conditions

1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of Y signal output or chroma signal output of the measurement system.

### ◎ Color coding of this image sensor & Composition of luminance (Y) and chroma (color difference) signals




**Color Coding Diagram**

As shown in the left figure, fields are read out. The charge is mixed by pairs such as A1 and A2 in the A field. (pairs such as B in the B field)
As a result, the sequence of charges output as signals from the horizontal shift register (Hreg) is, for line A1, (G + Cy), (Mg + Ye), (G + Cy), and (Mg + Ye).

These signals are processed to form the Y signal and chroma (color difference) signal. The Y signal is formed by adding adjacent signals, and the chroma signal is formed by subtracting adjacent signals. In other words, the approximation:

$$Y = \{(G + Cy) + (Mg + Ye)\} \times 1/2$$
$$= 1/2 \{2B + 3G + 2R\}$$

is used for the Y signal, and the approximation:

$$R - Y = \{(Mg + Ye) - (G + Cy)\}$$
$$= \{2R - G\}$$

is used for the chroma (color difference) signal. For line A2, the signals output from Hreg in sequence are

(Mg + Cy), (G + Ye), (Mg + Cy), (G + Ye).

The Y signal is formed from these signals as follows:

$$Y = \{(G + Ye) + (Mg + Cy)\} \times 1/2$$
$$= 1/2 \{2B + 3G + 2R\}$$

This is balanced since it is formed in the same way as for line A1.
In a like manner, the chroma (color difference) signal is approximated as follows:

$$-(B - Y) = \{(G + Ye) - (Mg + Cy)\}$$
$$= -\{2B - G\}$$

In other words, the chroma signal can be retrieved according to the sequence of lines from R – Y and –(B – Y) in alternation. This is also true for the B field.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition I:
Use a pattern box (luminance 706cd/$m^2$, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –33mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the Y signal (Ys) at the center of the screen and substitute the value into the following formula.

$$S = Ys \times \frac{250}{60} \ [\text{mV}]$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of the Y signal output, 200mV, measure the minimum value of the Y signal.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the Y signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value YSm [mV] of the Y signal output and substitute the value into the following formula.

$$Sm = \frac{YSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \ [\%] \ \text{(1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Y signal output is 200mV. Then measure the maximum (Ymax [mV]) and minimum (Ymin [mV]) values of the Y signal and substitute the values into the following formula.

$$SHy = (Ymax – Ymin)/200 \times 100 \ [\%]$$

5. Uniformity between video signal channels
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then measure the maximum (Crmax, Cbmax [mV]) and minimum (Crmin, Cbmin [mV]) values of the R – Y and B – Y channels of the chroma signal and substitute the values into the following formula.

$$\Delta Sr = |(Crmax – Crmin)/200| \times 100 \ [\%]$$
$$\Delta Sb = |(Cbmax – Cbmin)/200| \times 100 \ [\%]$$

6. Dark signal
Measure the average value of the Y signal output (Ydt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
After measuring 6, measure the maximum (Ydmax [mV]) and minimum (Ydmin [mV]) values of the Y signal output and substitute the values into the following formula.

$\Delta$Ydt = Ydmax – Ydmin [mV]

8. Flicker
1) Fy
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then measure the difference in the signal level between fields ($\Delta$Yf [mV]). Then substitute the value into the following formula.

Fy = ($\Delta$Yf/200) x 100 [%]

2) Fcr, Fcb
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, insert an R and B filter, and then measure both the difference in the signal level between fields of the chroma signal ($\Delta$Cr, $\Delta$Cb) as well as the average value of the chroma signal output (CAr, CAb). Substitute the values into the following formula.

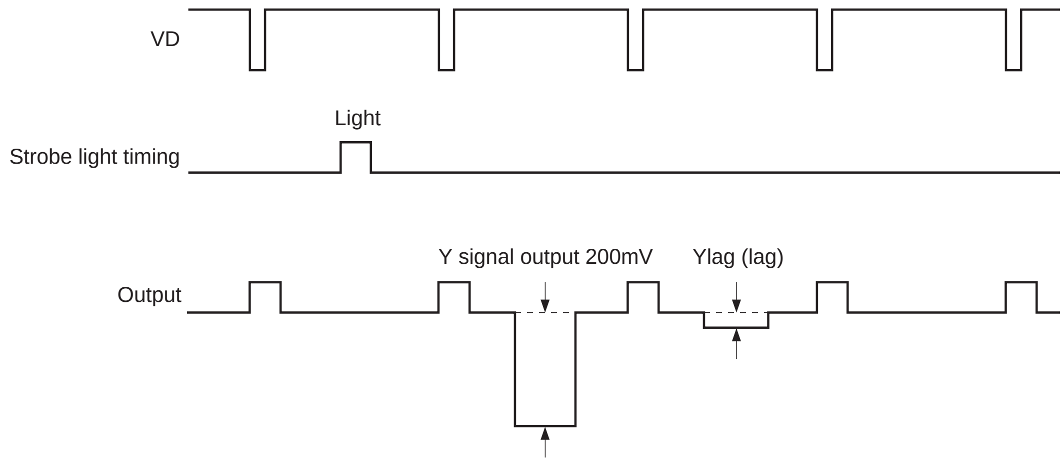
Fci = ($\Delta$Ci/CAi) x 100 [%]   (i = r, b)

9. Line crawls
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then insert a white subject and R, G, and B filters and measure the difference between Y signal lines for the same field ($\Delta$Ylw, $\Delta$Ylr, $\Delta$Ylg, $\Delta$Ylb [mV]). Substitute the values into the following formula.

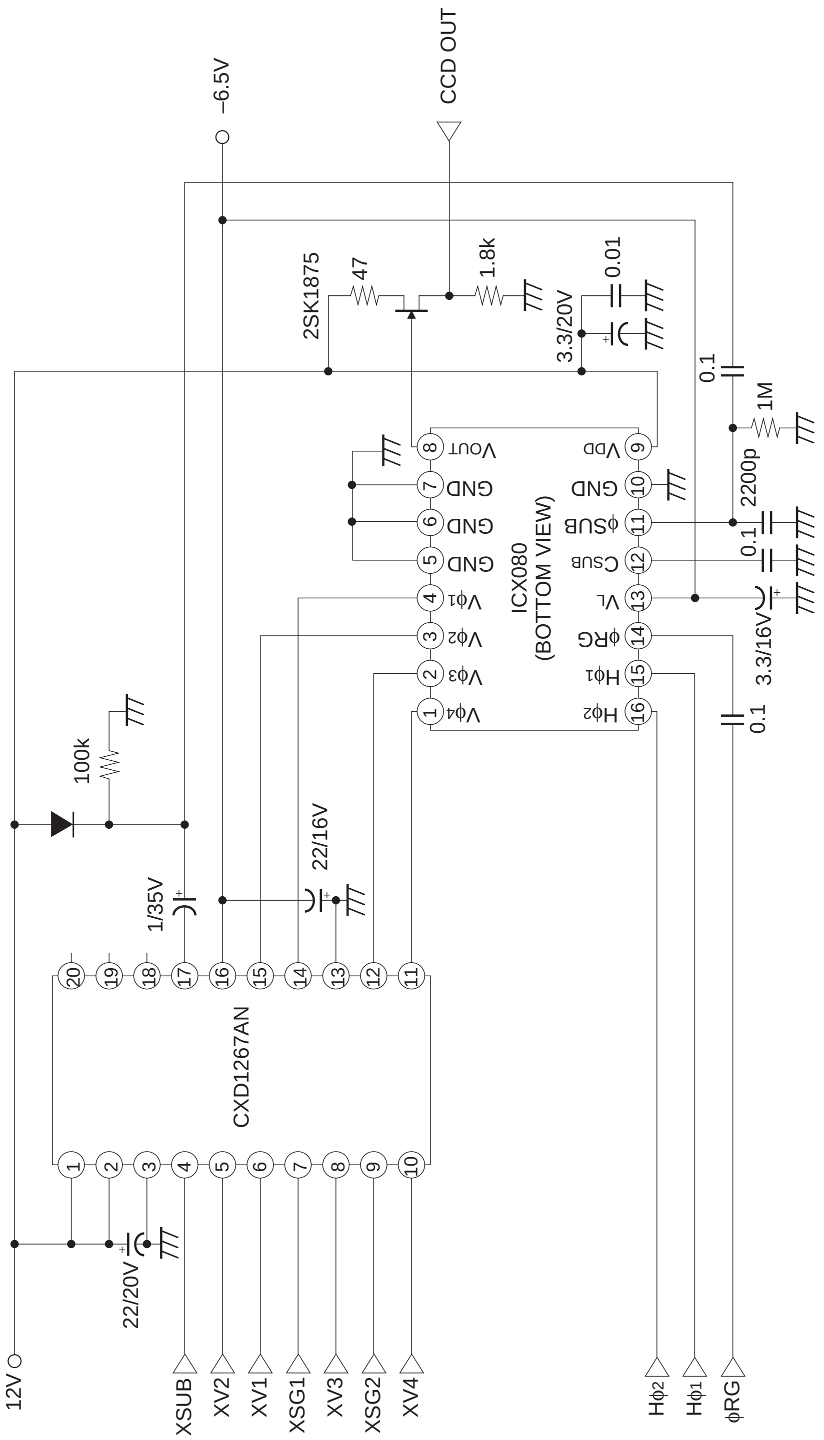
Lci = ($\Delta$Yli/200) x 100 [%]   (i = w, r, g, b)

10. Lag
Adjust the Y signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Ylag). Substitute the value into the following formula.

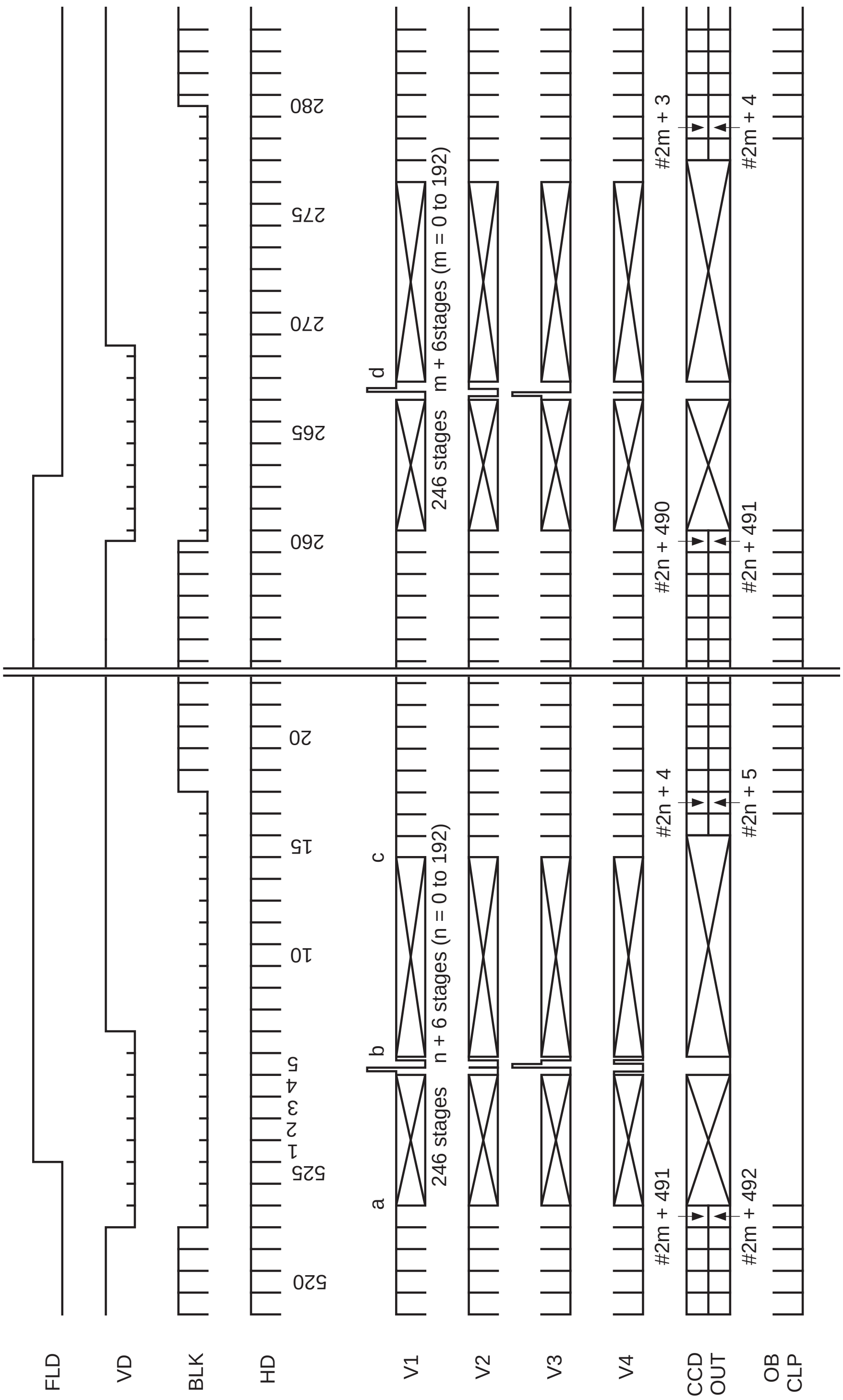
Lag = (Ylag/200) x 100 [%]



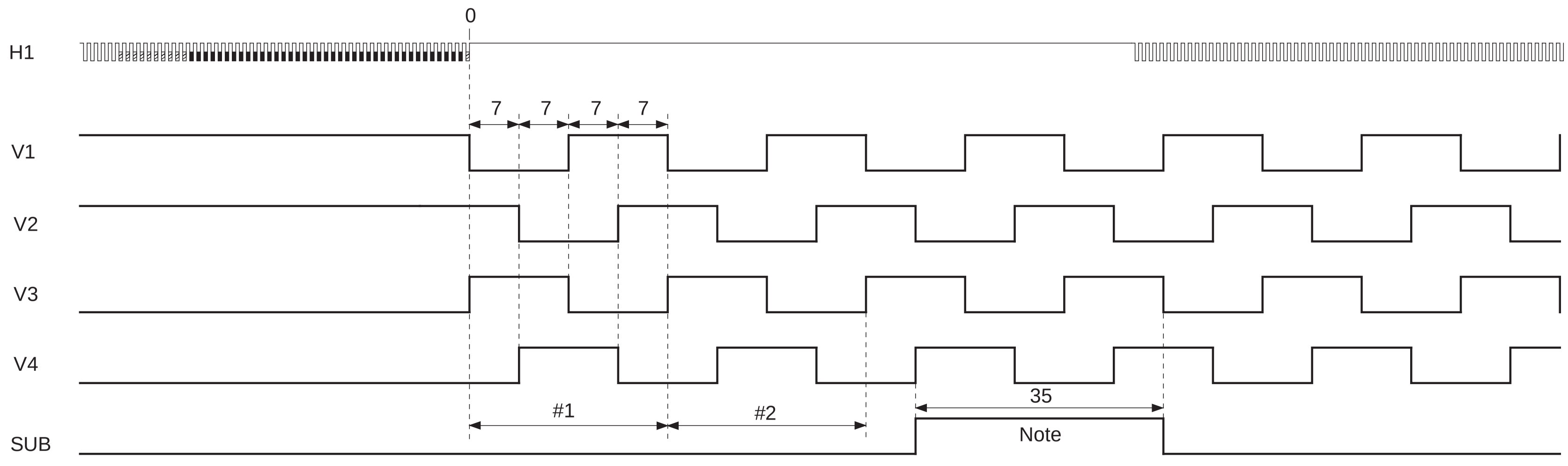
## Drive Circuit



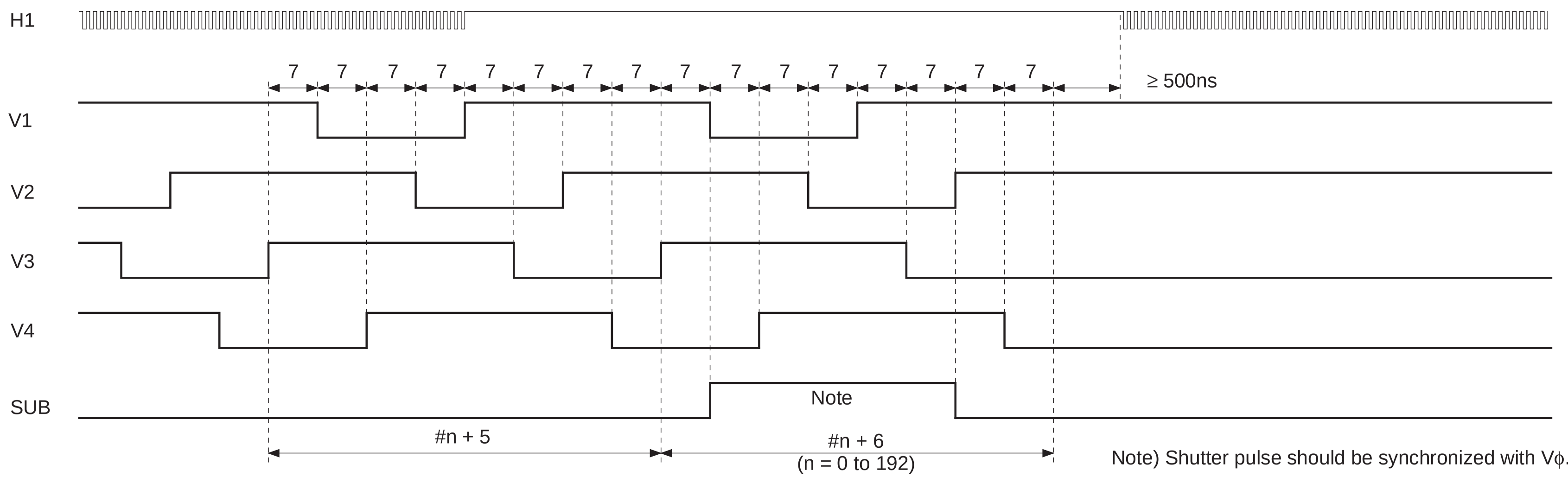
## Drive Timing Chart (Vertical Sync)



## Drive Timing Chart (Vertical Sync "a" Enlarged)

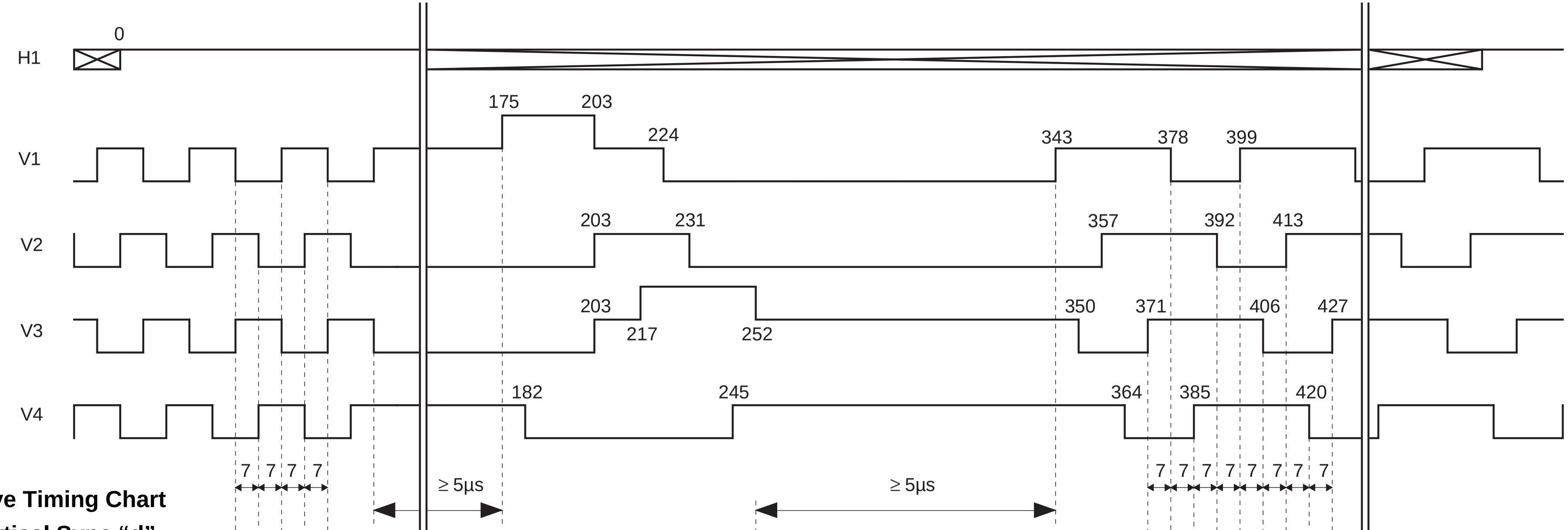



## Drive Timing Chart (Vertical Sync "c" Enlarged)

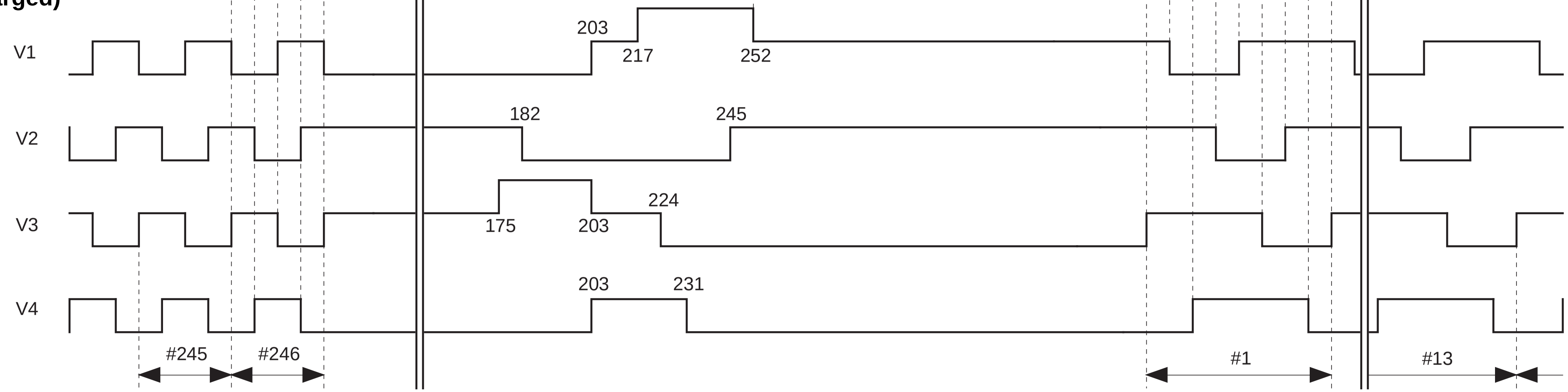



Note) Shutter pulse should be synchronized with Vϕ.

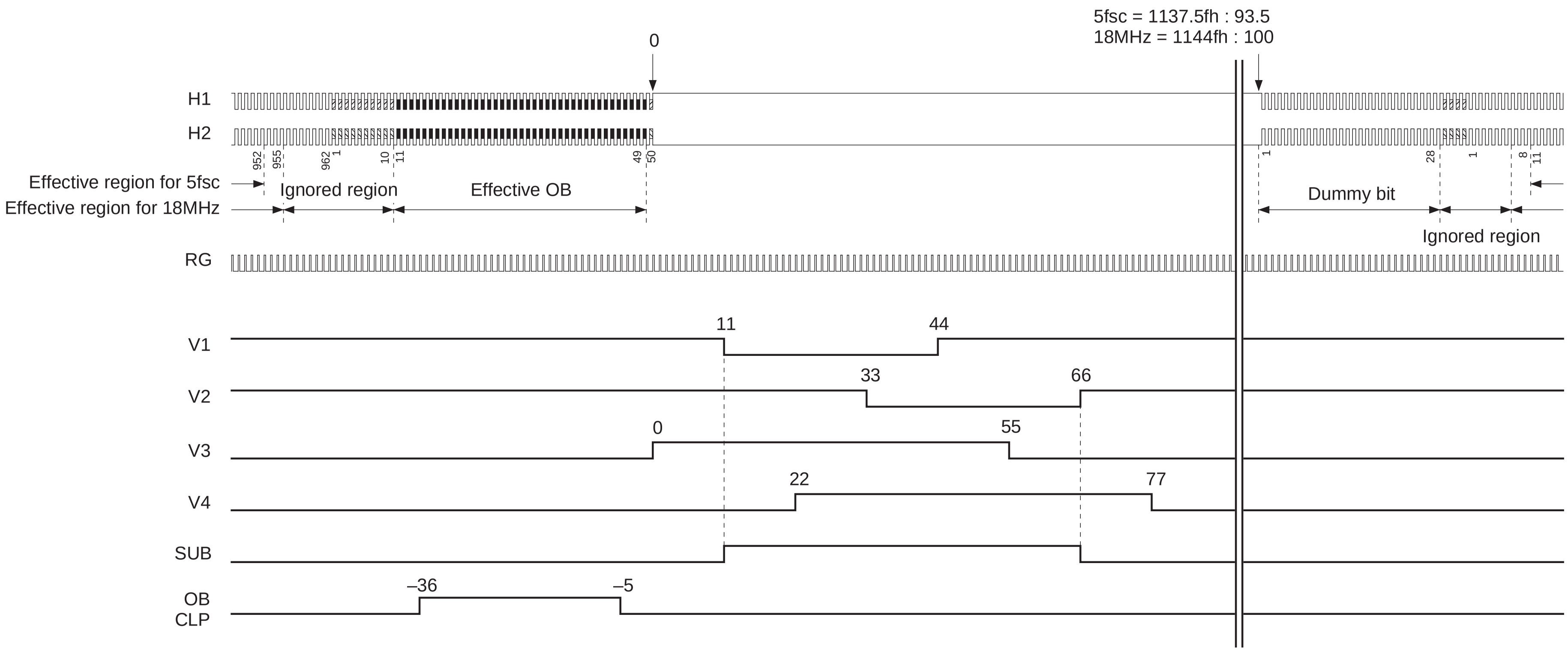
**Drive Timing Chart (Vertical Sync "b" Enlarged)**




**Drive Timing Chart (Vertical Sync "d" Enlarged)**



## Drive Timing Chart (Horizontal Sync)




Note) 1unit : 55.87ns (5fsc = 1137.5fh)
55.56ns (18MHz = 1144fh)

## Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

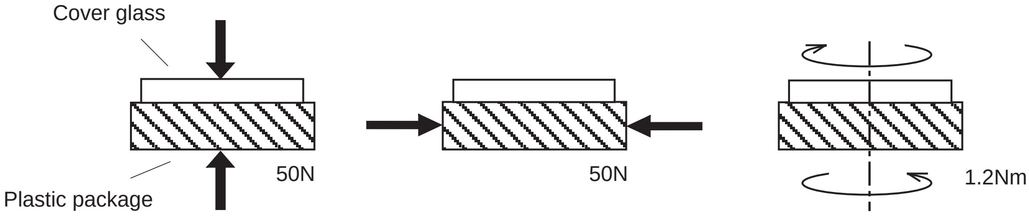
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)




**Compressive strength** **Torsional strength**

b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.

d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.

f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

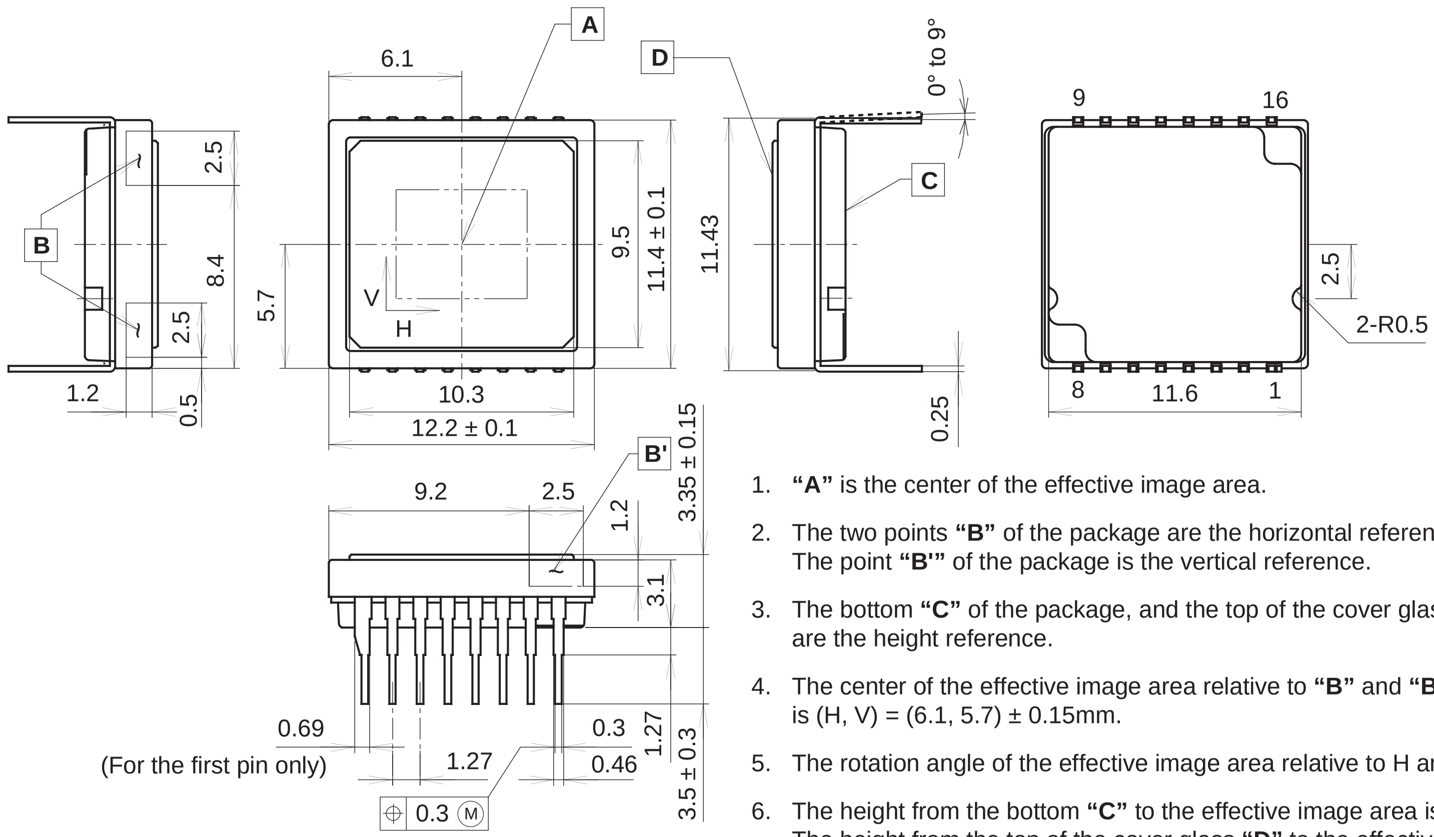
a) Do not expose to strong light (sun rays) for long periods, color filters will be discolored. When high luminance objects are imaged with the exposure level control by electronic-iris, the luminance of the image-plane may become excessive and discolor of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

**Package Outline** Unit: mm

16pin DIP (450mil)




PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | Plastic |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 0.9g |

1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.