SONY

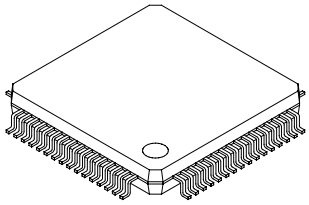
CXD3503R

Color Shading Correction IC for Liquid Crystal Projectors

Description

The CXD3503R is a color shading correction IC for Sony data projectors. Used together with the Sony LCD driver CXA2111R or CXA2112R, this IC corrects color shading caused by the LCD panel structure or the optical system. This IC has a built-in SRAM and D/A converter, and 16 horizontal and 13 vertical correction points can be set via a serial interface.

64 pin LQFP (Plastic)



Functions

- Generates the color shading correction signals for the high-temperature polysilicon TFT LCD panels used in Sony projectors
- Supports various SVGA, XGA and SXGA signals using 1/2 dot clock input
- Vertical output signal interpolation using an internal arithmetic circuit
- Automatic determination of eliminated lines during pulse eliminator display when used together with the Sony timing generator ICs CXD2464R or CXD3500R
- Supports up/down and/or right/left inversion
- Supports LCD panel display area switching conversion functions
- Standby and correction OFF functions

Applications

Liquid crystal projectors, etc.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.3 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Storage temperature	Tstg	–55 to +125	°C
• Operating temperature	Topr	–40 to +85	°C

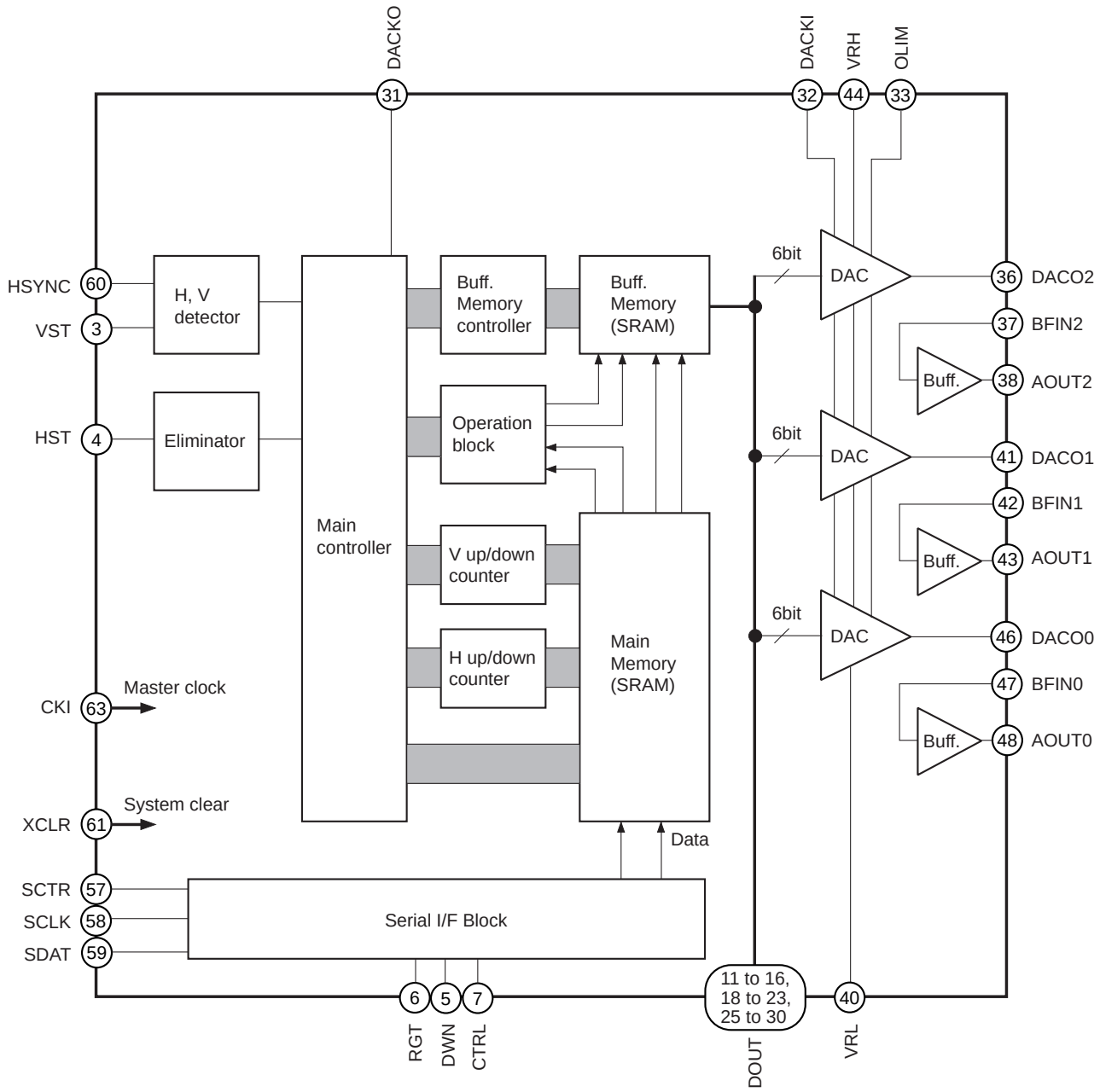
Recommended Operating Conditions

(Ta = –20 to +75°C, V_{SS} = 0V)

Supply voltage	V_{DD}	4.5 to 5.5	V

E99432-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Processing for internal input
1	NC	—	Not connected	—
2	NC	—	Not connected	—
3	VST	I	VST pulse input	—
4	HST	I	HST pulse input	—
5	DWN	I	Up/down inversion control input (H: down scan, L: up scan)	—
6	RGT	I	Right/left inversion control input (H: normal scan, L: reverse scan)	—
7	CTRL	I	Up/down and/or right/left inversion control signal (Serial settings selected when L.)	—
8	TEST0	I	Test (Leave open.)	L
9	TEST1	I	Test (Leave open.)	L
10	TEST2	I	Test (Leave open.)	L
11	DOUT00	O	Digital data output 00	—
12	DOUT01	O	Digital data output 01	—
13	DOUT02	O	Digital data output 02	—
14	DOUT03	O	Digital data output 03	—
15	DOUT04	O	Digital data output 04	—
16	DOUT05	O	Digital data output 05	—
17	$DV_{SS}0$	—	Digital GND	—
18	DOUT10	O	Digital data output 10	—
19	DOUT11	O	Digital data output 11	—
20	DOUT12	O	Digital data output 12	—
21	DOUT13	O	Digital data output 13	—
22	DOUT14	O	Digital data output 14	—
23	DOUT15	O	Digital data output 15	—
24	$DV_{DD}0$	—	Digital V_{DD} (5V)	—
25	DOUT20	O	Digital data output 20	—
26	DOUT21	O	Digital data output 21	—
27	DOUT22	O	Digital data output 22	—
28	DOUT23	O	Digital data output 23	—
29	DOUT24	O	Digital data output 24	—
30	DOUT25	O	Digital data output 25	—
31	DACKO	O	DAC clock output (Connect to DACKI.)	—
32	DACKI	I	DAC clock input (Connect to DACKO.)	—
33	OLIM	I	Digital data output limiter (H: Hi-Z, L: digital data output)	—
34	$DV_{DD}1$	—	Digital V_{DD} (5V)	—

Pin No.	Symbol	I/O	Description	Processing for internal input
35	$DV_{SS}1$	—	Digital GND	—
36	DACO2	O	DAC output 2	—
37	BFIN2	I	Buffer input 2	—
38	AOUT2	O	Correction signal output 2	—
39	AV_{SS}	—	Analog GND	—
40	VRL	I	DAC output low reference voltage input	—
41	DACO1	O	DAC output 1	—
42	BFIN1	I	Buffer input 1	—
43	AOUT1	O	Correction signal output 1	—
44	VRH	I	DAC output high reference voltage input	—
45	AV_{DD}	—	Analog power supply	—
46	DACO0	O	DAC output 0	—
47	BFIN0	I	Buffer input 0	—
48	AOUT0	O	Correction signal output 0	—
49	$DV_{SS}2$	—	Digital GND	—
50	NC	—	Not connected	—
51	NC	—	Not connected	—
52	NC	—	Not connected	—
53	NC	—	Not connected	—
54	NC	—	Not connected	—
55	NC	—	Not connected	—
56	$DV_{DD}2$	—	Digital V_{DD} (5V)	—
57	SCTR	I	Serial chip select input (serial transfer block)	—
58	SCLK	I	Serial clock input (serial transfer block)	—
59	SDAT	I	Serial data input (serial transfer block)	—
60	HSYNC	I	HSYNC input	—
61	XCLR	I	Clear (L: system clear)	H
62	$DV_{SS}3$	—	Digital GND	—
63	CKI	I	Master clock input	—
64	SLCK	I	Clock switching (H: Internal 1/2 frequency divider used.)	—

Electrical Characteristics

DC Characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
Input, output voltage	V_I, V_O		V_{SS}		V_{DD}	V	
Input voltage 1	V_{IH}	CMOS input	0.7V_{DD}			V	*1
	V_{IL}				0.3V_{DD}		
Input voltage 2	V_{IH}	CMOS input With pull-up resistor	0.7V_{DD}			V	*4
	V_{IL}				0.3V_{DD}		
Input voltage 3	V_{IH}	CMOS input With pull-down resistor	0.7V_{DD}			V	*2
	V_{IL}				0.3V_{DD}		
Input voltage 4	V_{IH}	TTL input	2.2			V	*5
	V_{IL}				0.8		
Input voltage 5	V_{IH}	TTL Schmitt input	2.5			V	*3
	V_{IL}				0.6		
Output voltage 1	V_{OH}	I_{OH} = –4mA	V_{DD} – 2.1			V	*6, *7
	V_{OL}	I_{OL} = 4mA			0.4		
Input leak current	I_{IL}	V_I = V_{DD}, V_{SS}	–10		10	µA	*1, *3, *5
Output leak current	I_{OZ}	During high impedance output	–10		10	µA	*7
Pull-up resistor	R_{UP}		60	120	240	kΩ	*4
Pull-down resistor	R_{DN}		45	90	180	kΩ	*2
Current consumption	I_{DD}	During 41MHz operation		60		mA	

(INPUT)

*1 CTRL, DACKI, DWN, HST, OLIM, RGT, SLCK, VST

*2 TEST0, 1, 2

*3 HSYNC, SCLK, SCTR, SDAT

*4 XCLR

*5 CKI

(OUTPUT)

*6 DACKO

*7 DOUT00 to 05, DOUT10 to 15, DOUT20 to 25

Note) AOUT0, 1 and 2, DACO0, 1 and 2, BFIN0, 1 and 2, VRH and VRL are not included in the DC characteristics.

AC Characteristics

External Clock Input AC Characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –40 to +85°C)

Symbol	Item	Min.	Typ.	Max.	Unit
t_{s0}	HSYNC setup time, activated by the rising edge of CKI	12	—	—	ns
t_{h0}	HSYNC hold time, activated by the rising edge of CKI	0.5	—	—	
t_{wL}/t_{wH}	CKI L/H level pulse width	—	50	—	%

Serial Transfer AC Characteristics

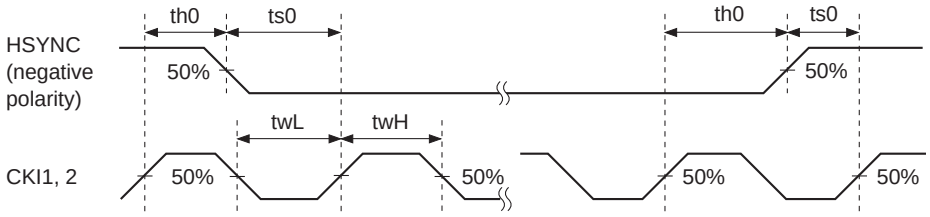
(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –40 to +85°C)

Symbol	Item	Min.	Typ.	Max.
t_{s0}	SCTR setup time, activated by the rising edge of SCLK	8Tns	—	—
t_{s1}	SDAT setup time, activated by the rising edge of SCLK	4Tns	—	—
t_{h0}	SCTR hold time, activated by the rising edge of SCLK	8Tns	—	—
t_{h1}	SDAT hold time, activated by the rising edge of SCLK	4Tns	—	—
t_{w1L}	SCLK L level pulse width	4Tns	—	—
t_{w1H}	SCLK H level pulse width	4Tns	—	—

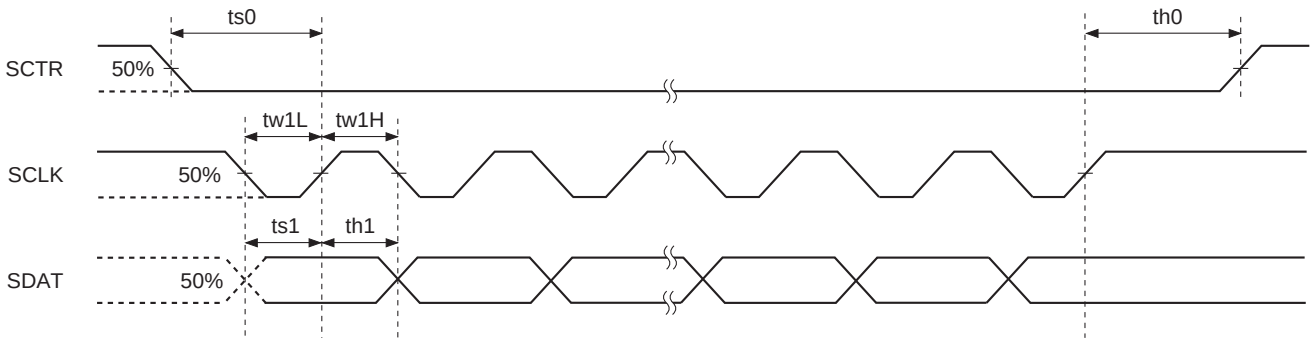
T: Input clock cycle

Timing Definition

External Clock Input AC Characteristics



Serial Transfer AC Characteristics



Electrical Characteristics (Analog Block)

6-bit D/A Converter part

(Ta = 25°C, V_{DD} = 5.0V, V_{SS} = 0V, VRH – VRL = 1.0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES	—	—	6	Bits
Conversion rate	F_S	—	—	30	MPS
Linearity error	E_L	—	—	±0.5	LSB
Differential linearity error	E_D	—	—	±0.5	LSB
Output resistance	R_O	140	213	286	Ω

Operational Amplifier part (Operating Temperature variation)

(V_{DD} = 5.0V, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Ta	–40	25	85	°C
Input offset voltage	V_{IO}	5	5	5	mV
Current consumption	I_{CC}	2.4	1.8	1.6	mA
Maximum output saturation voltage	Vopp	0 to 4.95	0 to 4.95	0 to 4.95	V
Input voltage range	V_{IN}	1.5 to 5.0	1.7 to 5.0	1.8 to 5.0	V
Slew rate	SR	39	31	28	V/µs

Operational Amplifier part (Supply Voltage variation)

(Ta = 25°C, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	V_{IO}	4.5	5.0	5.5	V
Input offset voltage	V_{IO}	5	5	5	mV
Current consumption	I_{CC}	1.4	1.8	2.4	mA
Maximum output saturation voltage	Vopp	0 to 4.45	0 to 4.95	0 to 5.43	V
Input voltage range	V_{IN}	1.7 to 4.5	1.7 to 5.0	1.9 to 5.5	V
Slew rate	SR	24	31	40	V/µs

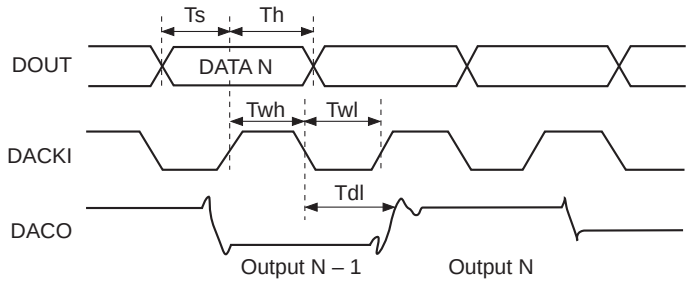
AC Characteristics

External Clock Input AC Characteristics

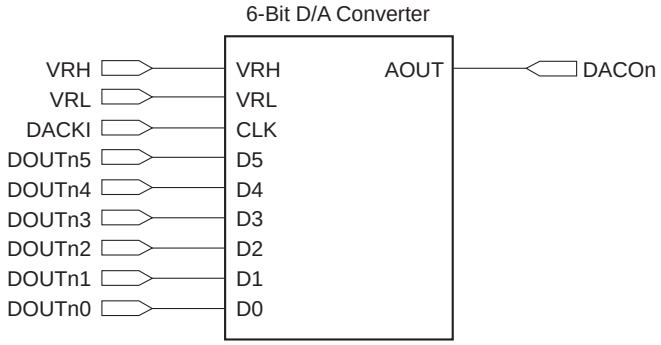
6-Bit D/A Converter (Ta = 25°C, V_{DD} = 5.0V, V_{SS} = 0V, VRH – VRL = 1.0V, C_L = 30pF)

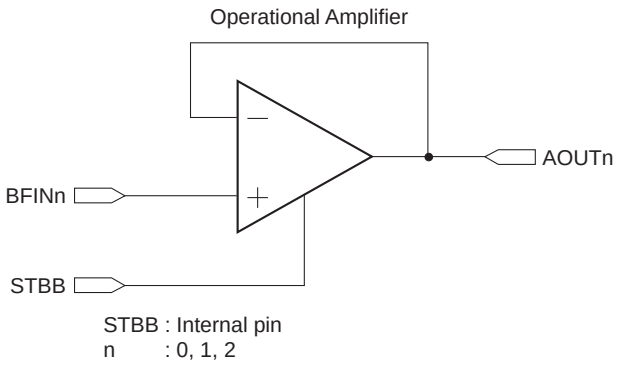
Item	Symbol	Min.	Typ.	Max.	Unit
Clock H level width	Twh	17	—	—	ns
Clock L level width	Twl	17	—	—	
Data setup time	Ts	10	—	—	
Data hold time	Th	10	—	—	
Output delay time	Tdl	—	35	—	

Timing Definition



Internal Structure





STBB : Internal pin
n : 0, 1, 2

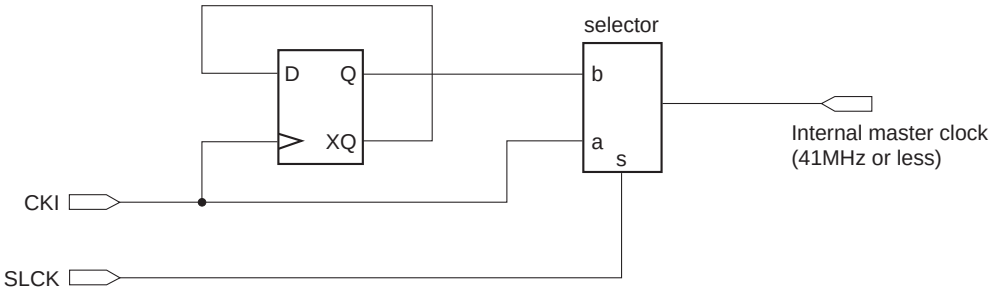
I/O Pin Description

Pin No.	Symbol	Description
3	VST	This pin is a reference of vertical output timing. Inputs the VST pulse from the timing generator IC.
4	HST	Inputs the HST pulse from the timing generator IC. When not rising pulse eliminator, connect to DV_{DD} and use it.
5	DWN	Up/down and/or right/left inversion control external input (H: normal scan, L: reverse scan) This setting is invalid when the internal register is used.
6	RGT	
7	CTRL	Up/down and/or right/left inversion control signal selection setting. (For the DWN and RGT control signals, Pins 5 and 6 are selected when CTRL is H, and the settings from the internal register made via the serial interface are selected when CTRL is L.)
11 to 16, 18 to 23, 25 to 30	DOUT00 to DOUT25	Digital data outputs. The data input to the DAC is output as is when OLIM (Pin 33) is L. Normally, output is not performed. Set OLIM to H and leave these open.
31	DACKO	Internal DAC clock input/output. DAC clock generated inside the IC is output from DACKO. Normally, input this DACKO output to DACKI.
32	DACKI	
33	OLIM	Digital data output limiter. When OLIM is L, the data input to the DAC is output from the DOUT00 to DOUT25 output pins. When OLIM is H, these output pins go to high impedance state.
36, 41, 46	DACO2, 1, 0	Analog outputs from the internal DAC. The output impedance varies from several ten to several thousand Ω depending on the output voltage level, so connect these pins to BFIN2, 1 and 0 (buffer inputs), respectively.
37, 42, 47	BFIN2, 1, 0	Internal operational amplifier buffer inputs. Connect to DACO2, 1 and 0, respectively.
38, 43, 48	AOUT2, 1, 0	Analog correction signal outputs
40	VRL	DAC L side reference voltage input (Input via buffer.)
44	VRH	DAC H side reference voltage input (Input via buffer.)
57	SCTR	Serial control inputs. Timing control and correction point data are all set by these pins. For details, see page 12 "Serial Transfer Operation".
58	SCLK	
59	SDAT	
60	HSYNC	This pin is a reference of horizontal output timing. Normally, input horizontal sync signal.
61	XCLR	System clear. Internal register is initialized by setting to L. Input pins are pulled up to H internally.
63	CKI	Master clock input. Input level is TTL.
64	SLCK	Clock switching (H: Clock obtained by 1/2 frequency-dividing CKI using the internal frequency divider is selected. L: CKI input is selected. The selected clock is an internal master clock.)
17, 35, 49, 62	DV_{SS}	Power supply inputs. Do not raise either analog power supply or digital power supply.
24, 34, 56	DV_{DD}	
39	AV_{SS}	
45	AV_{DD}	

Clock input (CKI: Pin 63)

The master clock input (CKI: Pin 63) of this IC supports TTL level input.

In addition, two modes can be set: a mode in which the CKI is used as is for the internal master clock (SLCK (Pin 64): L) and a mode in which CKI is halved using the internal frequency divider (SLCK: H). In the latter mode, all internal operation is at 1/2 clock, so "clock" in the description below refers to this 1/2 clock when SLCK is H. Internal operation is at a frequency up to 41 MHz, so when inputting a clock faster than this to CKI1, be sure to set SLCK to H.

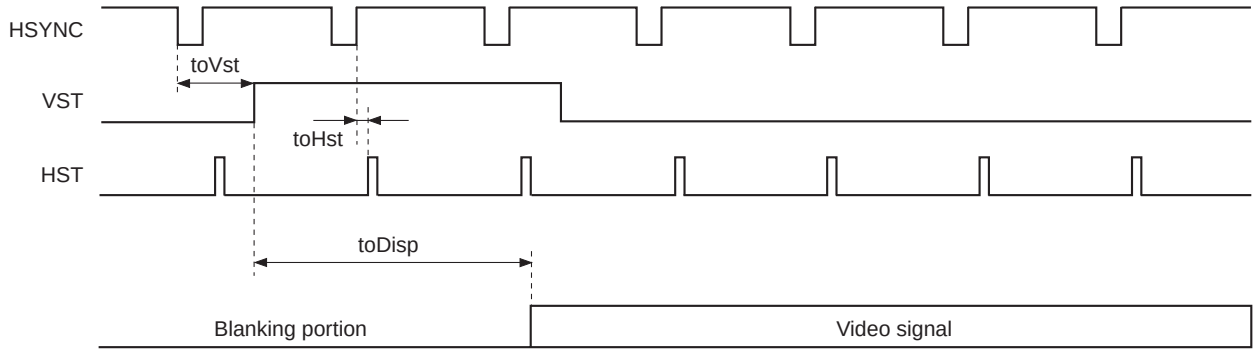


HSYNC, VST, HST

Input a standard horizontal sync signal to the input HSYNC (Pin 60).

At this time, the input polarity is not fixed and is set by the serial data setting HSYNCPOL. In addition, make sure the VST and HST pulses satisfy the following phase relationship. However, when not using pulse eliminator display, HST (Pin 4) can be fixed to H level.

Normally input the VST pulse to the LCD panel for the VST input.



toVst: VST shall rise 20 clocks or more after the front edge of HSYNC, and after the HST pulse.

toHst: The front edge of HST shall follow the rear edge of HSYNC

toDisp: There shall be 1.5H or more from the rise of VST to the start of the video signal.

The Sony timing generator ICs (CXD2464R, CXD3500R) pulses of the same name satisfy the above conditions.

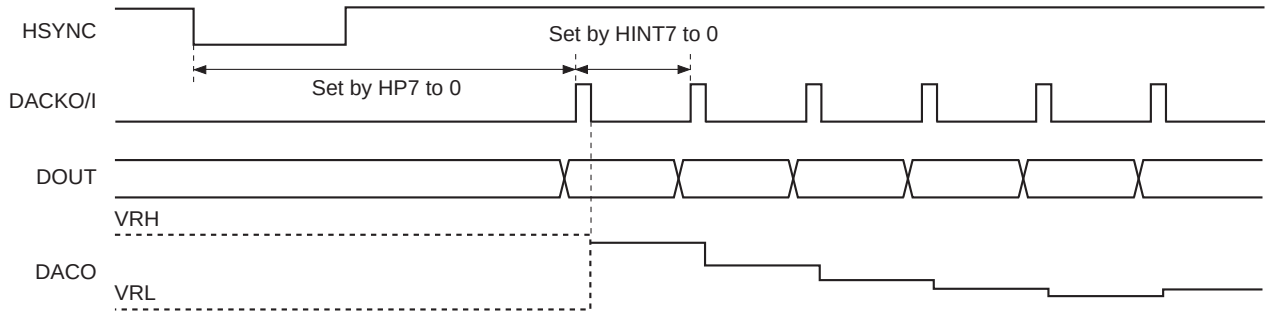
System clear pin input

Set the system clear pin (XCLR: Pin 61) to L and apply a forced reset in order to initialize the internal circuits during power-on.

Description of Output Correction Signal Operation

Horizontal direction

The correction data set in the SRAM by serial transfer is arithmetically processed inside the IC to determine the output position corresponding to the value set by serial register HP7 to 0 using the front edge of HSYNC as the reference. Interpolation is not performed for the horizontal direction, and interpolated data is output at the cycle set by serial register HINT7 to 0 for the vertical direction. In addition, the maximum amplitude of the correction signal output voltage is determined by VRH (Pin 44) and VRL (Pin 40). The internal DAC outputs at the resistive potential division (VRH to VRL: 213Ω typ.), so be sure to input to VRH and VRL via buffers having current capacity.



The internally generated digital data DOUT is input to the internal D/A converter, latched by the D/A converter clock input from DACKI, and output from DACO2, 1 and 0 as an analog signal.

Note) If edges remain, these level differences may appear as vertical stripes. Therefore, when using this as a correction signal, be sure to eliminate the edges using an LPF, etc. before input to the CXA2111R or CXA2112R.

Vertical direction

The vertical correction points set in the SRAM are arithmetically processed inside the IC to output interpolated data for the lines other than correction points.

	n	n + 1
	fm, n	fm_{+1}, n
m	$fm, n + \frac{1}{a}(fm_{+1}, n - fm, n)$	$fm, n_{+1} + \frac{1}{a}(fm_{+1}, n_{+1} - fm, n_{+1})$
	$fm, n + \frac{2}{a}(fm_{+1}, n - fm, n)$	$fm, n_{+1} + \frac{2}{a}(fm_{+1}, n_{+1} - fm, n_{+1})$
	≈	≈
m + 1	$fm, n + \frac{a-1}{a}(fm_{+1}, n - fm, n)$	$fm, n_{+1} + \frac{a-1}{a}(fm_{+1}, n_{+1} - fm, n_{+1})$
	fm_{+1}, n	fm_{+1}, n_{+1}

VINT line(s)

a' lines

fm, n: Correction data for point (m, n)

Vertical correction point interval
Set by VINT4 to 0 and ANM5 to 0
Assuming ANM5 to 0 = a,
$a' = VINT \times a$

Serial Transfer Operation

Control method

The operation timing of this IC is controlled by serial data.

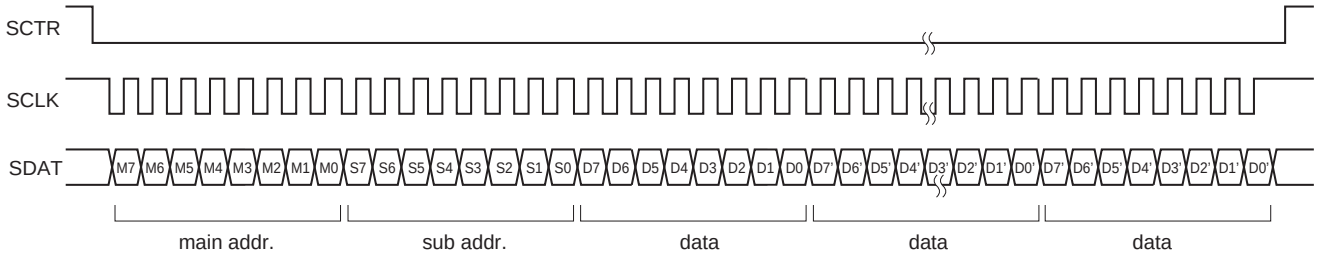
The control data is divided into 8-bit units. The first 8 bits are the main address, the next 8 bits are the sub address, and the subsequent data is 8-bit data blocks.

The main address specifies which of the blocks in the table below are to be set. Data is set in the blocks indicated by "1", so if the main address is set to "0F", the subsequent data is set in all data blocks.

In addition, the value set in the sub address sets the initial write address in the block specified by the main address. Thereafter, the write address is incremented by +1 while SCTR is L for each 8 bits of data from the address set by the sub address.

This makes it possible to set only the necessary data from an optional address.

The data set by serial register INIT5 to 0 is output in place of the correction data during serial transfer.



Main address table

Main address	Setting block
01h	Correction point data 0 (SRAM0)
02h	Correction point data 1 (SRAM1)
04h	Correction point data 2 (SRAM2)
08h	Timing control data

The SRAM numbers 0, 1 and 2 correspond to the DAC output DACO numbers 0, 1 and 2. The correction point data set in the SRAM is reflected to the outputs of the corresponding numbers.

Correction point data 0, 1 and 2

Correction point data is set in the 6-bit × 208 words (16 horizontal points, 13 vertical points) SRAM. The set correction data undergoes vertical interpolation and other arithmetic processing, and is then reflected to the DACO0, 1 and 2 outputs, respectively. The correction point data is 6 bits, and is set in D5, 4, 3, 2, 1 and 0. Setting to D7 and 6 is invalid.

See the figure on page 13 for the relationship between the correction point data position and the SRAM address.

Example) When the main address is set to 04 and the sub address is set to 08, data is written from address 08 of correction point data 2 (SRAM2), then the address is automatically incremented and written to the SRAM.

Timing control data

Main address 08h

Sub address	D7	D6	D5	D4	D3	D2	D1	D0
00h	HB3	HB2	HB1	HB0	HE3	HE2	HE1	HE0
01h	VB3	VB2	VB1	VB0	VE3	VE2	VE1	VE0
02h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
03h	HINT7	HINT6	HINT5	HINT4	HINT3	HINT2	HINT1	HINT0
04h	—	—	—	—	VP3	VP2	VP1	VP0
05h	—	—	—	VINT4	VINT3	VINT2	VINT1	VINT0
06h	—	—	ANM5	ANM4	ANM3	ANM2	ANM1	ANM0
07h	—	1/A6	1/A5	1/A4	1/A3	1/A2	1/A1	1/A0
08h	HSOFF	HPOL	VSPOL	DWN	RGT	DACKP2	DACKP1	DACKP0
09h	STBY1	STBY0	INIT5	INIT4	INIT3	INIT2	INIT1	INIT0

—: Setting invalid

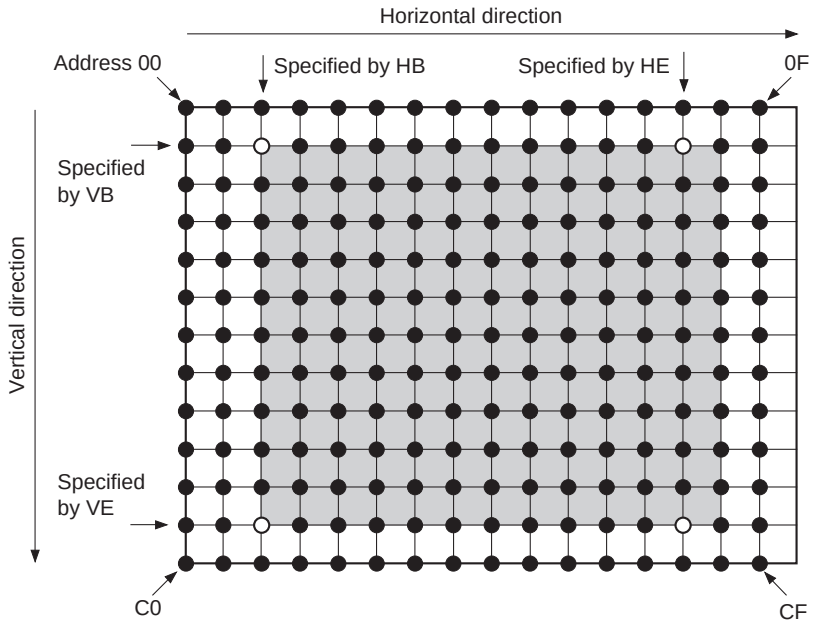
Data settings

HB3 to 0, HE3 to 0, VB3 to 0, VE3 to 0

These set the range of the correction point data to be used.

Expressed in model format, the correction points appear as shown in the figure below. To use only the shaded area, set HB: 2, HE: D, VB: 1 and VE: B.

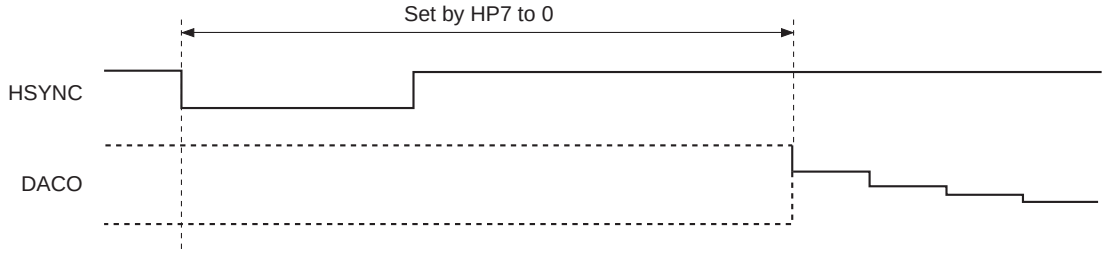
Normally set HB: 0, HE: F, VB: 0 and VE: D (16 × 13).



Dots in the lattice above represent correction points, and the white circles are the data settings.

HP7 to 0

This sets the correction signal output start position in the horizontal direction. The timing until the start of correction signal output is set using the front edge of HSYNC as the reference. However, do not set HP7 to 0 to a value of 54 or less, as the arithmetically processed correction signal may not be output correctly in this case. In addition, the waveform may be disturbed by the HP and HINT values and the VST phase. In these cases, eliminate the disturbance by adjusting the HP and DACKO phase.

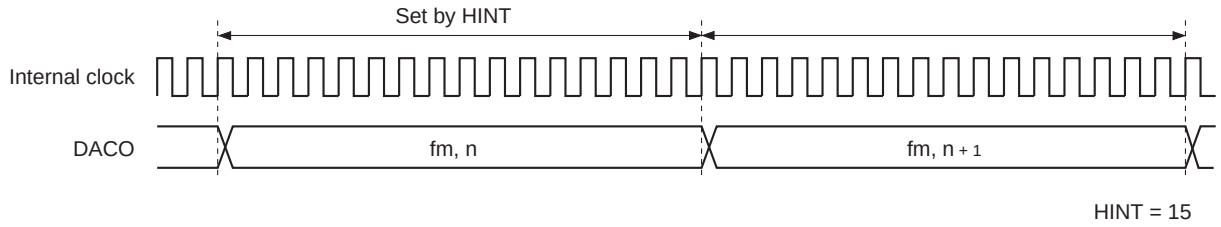


HINT7 to 0

This sets the correction point interval in the horizontal direction. Normally, when using 16 points in the horizontal direction, calculate the number of clocks at which the horizontal period can be divided into 16 sections taking into account the input clock and the system clock speed, and then set this value – 1. However, do not input a value of 11 or less to HINT7 to 0, as the internal arithmetic processing may not be able to keep up and the correct value may not be output in this case.

Example 1) Inputting a dot clock 40MHz signal to a SVGA panel (800 × 600)
If 1/2 the dot clock is input as the master clock and the mode without internal 1/2 frequency division (SLCK: L) is used:
HINT = (800 ÷ 16 ÷ 2) – 1 = 24

Example 2) Inputting a dot clock 65MHz signal to a XGA panel (1024 × 768)
If 1/2 the dot clock is input as the master clock and the mode with internal 1/2 frequency division (SLCK: H) is used:
HINT = (1024 ÷ 16 ÷ 4) – 1 = 15



VP3 to 0

This sets the correction signal output start position in the vertical direction. The number of line counted from the front edge of the VST pulse at which vertical arithmetic processing of the correction signal starts is set. The correction data for the initial line is output continuously only for the number of lines set by VP.

VINT4 to 0

This sets the arithmetic processing interval for vertical correction. Vertical correction arithmetic processing is performed every number of lines set by VINT. Normally set arithmetic processing for each line (VINT = 1).

ANM5 to 0

This sets the correction point interval in the vertical direction. There are 13 vertical correction points with respect to the actual panel display area switching, so this sets the number of lines at which correction points are spaced for the internal arithmetic processing.

Example) To use the full correction point data in the vertical direction, set the correction point interval ANM as follows.

SVGA panels:

ANM = 600 ÷ 12 = 50 (110010)

XGA panels:

ANM = 76 ÷ 12 = 64 (000000)

1/A6 to 0

This sets the inverse of ANM. Set the 6th to 12th digits below the decimal point in binary format with 7 bits. Linear interpolation with an accuracy of 1 bit is performed using this setting value.

Example) ANM = 50:

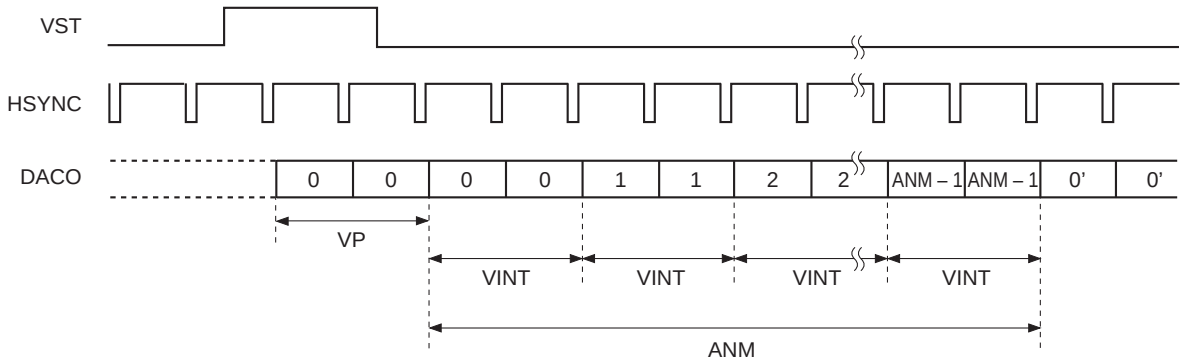
1/50 (decimal) = 0.000001010010 (binary)

Set the 6th to 12th digits.

Example) ANM = 64:

1/64 (decimal) = 0.000001000000 (binary)

Set the 6th to 12th digits.



HSOFF

This is the correction ON/OFF setting. When H, correction is on; when L, correction is off and the INIT5 to 0 data is output constantly. Normally set HSOFF to H.

HPOL

This sets the HSYNC input signal polarity. Set HPOL to H for positive polarity, and to L for negative polarity. Be sure to set the polarity correctly in accordance with the input signal.

VSPOL

This sets the VST input signal polarity. Set VSPOL to H for positive polarity, and to L for negative polarity. Be sure to set the polarity correctly in accordance with the input signal. The Sony timing generator ICs CXD2464R and CXD3500R output an inverse polarity VST pulse for up/down inverse drive of a SVGA panel. Therefore, take special care for the VST polarity when using this IC with a SVGA panel.

DWN, RGT

DWN and RGT set up/down and right/left inversion, respectively. Normal scan is supported when DWN is H and RGT is H, and up/down and/or right/left inversion of the panel is supported by reading the correction data set in the RAM in the reverse order when these are set to L, respectively. These settings can be controlled from the external pins of the same name DWN (Pin 5) and RGT (Pin 6) by setting CTRL (Pin 7) to H. In this case these serial settings are invalid.

DACKP2 to 0

This sets the DAC clock phase. Normally set to "2" to satisfy the internal DAC clock and data setup/hold specifications.

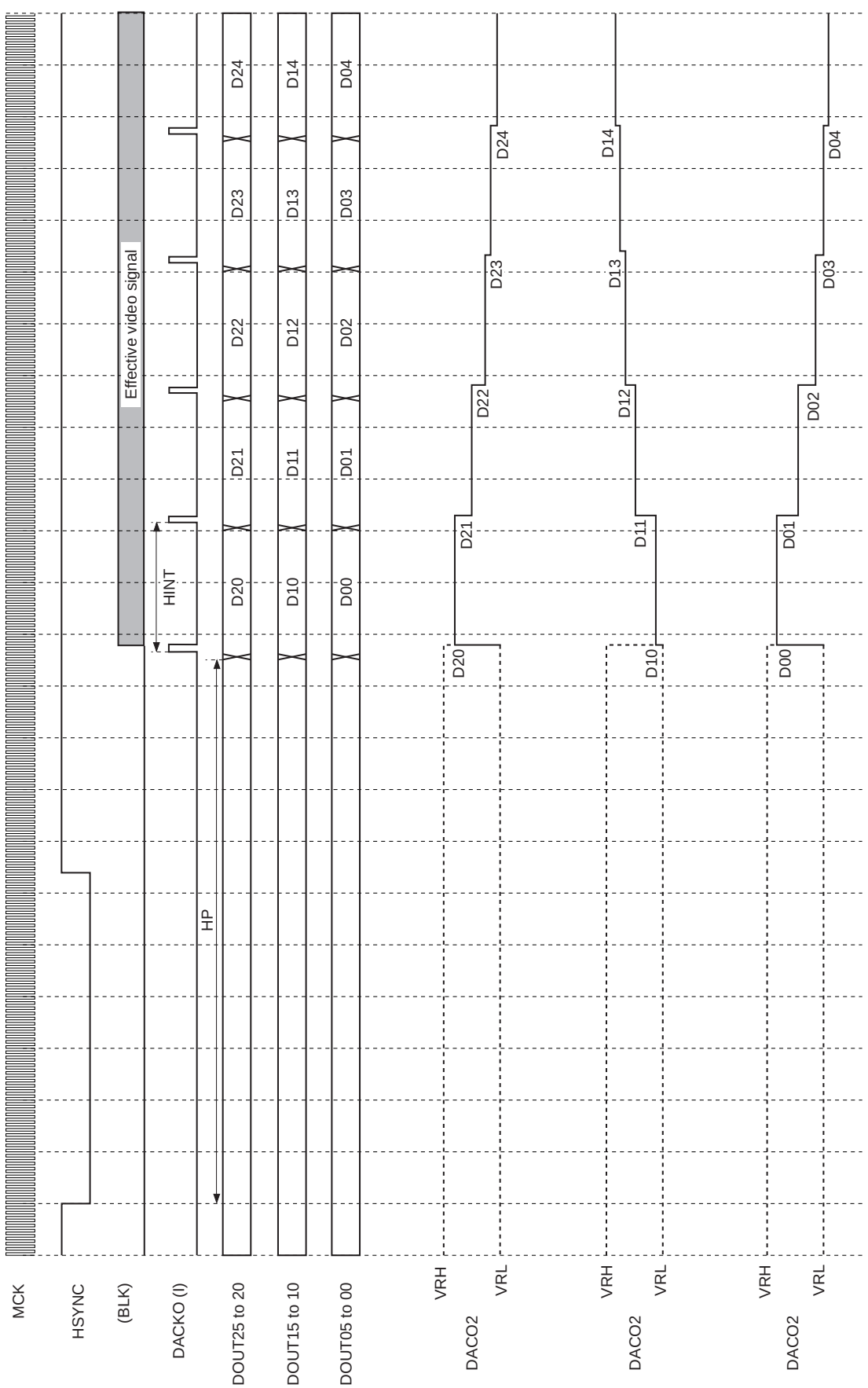
STBY1 and 0

This is the standby setting. Standby mode results when STBY1, 0 are set to H, L. At this time, the internal clock is supplied only to the serial interface block, and operation of all other blocks is stopped. Buffer outputs AOUT2, 1 and 0 and digital outputs DOUT25 to 20, 15 to 10 and 05 to 00 are all high impedance at this time.

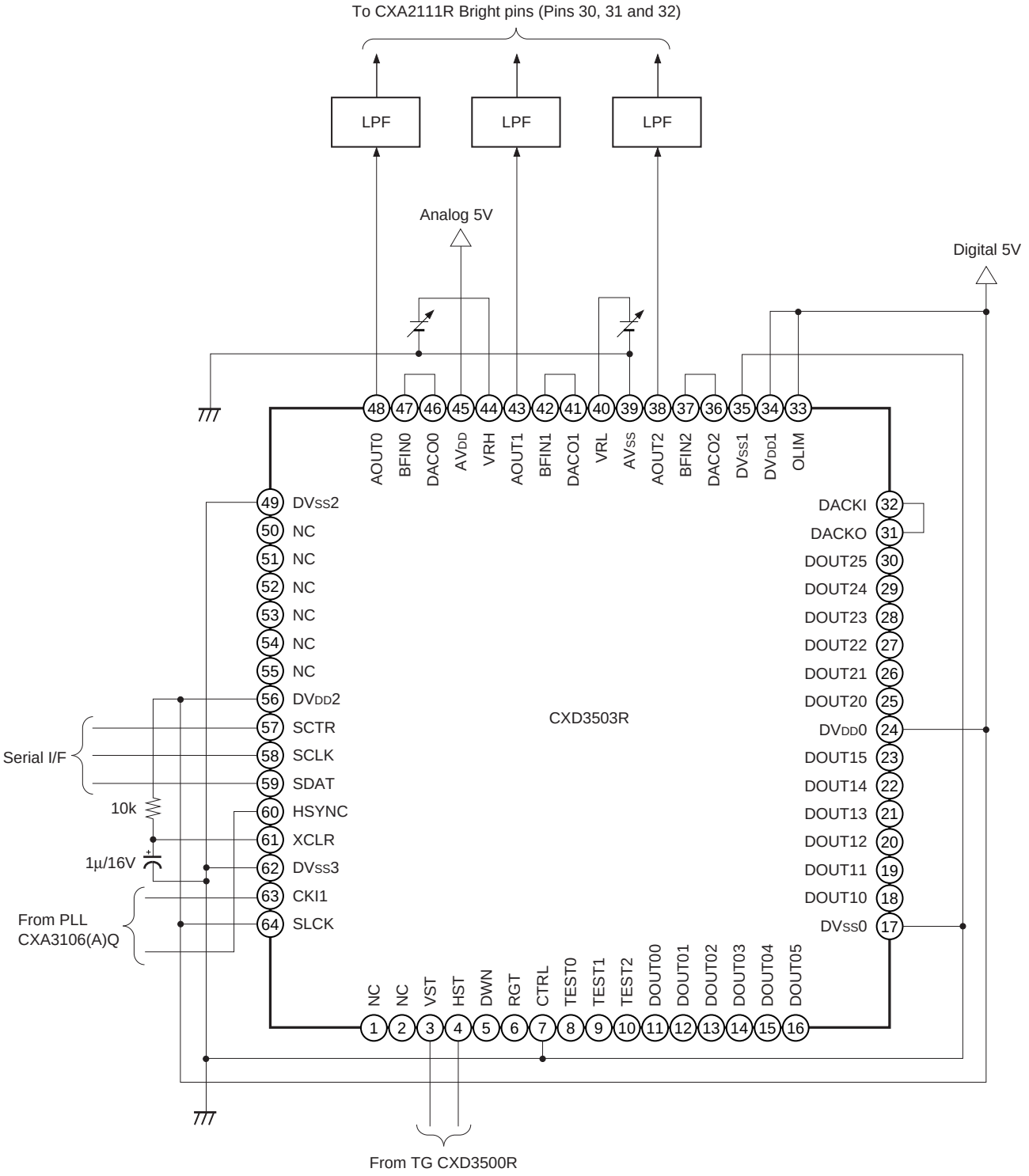
INIT5 to 0

This sets the DACO output level when correction is off. When serial data HSOFF is set to L, the data for this setting is output regardless of the correction data set in the RAM.

Timing Chart



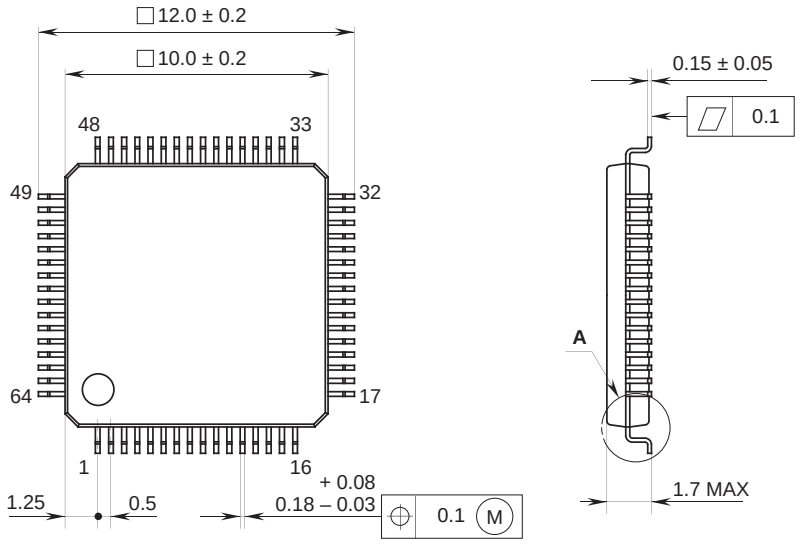
Application Circuit

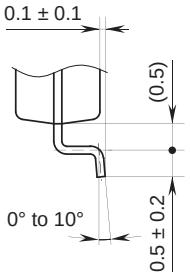


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g