SONY

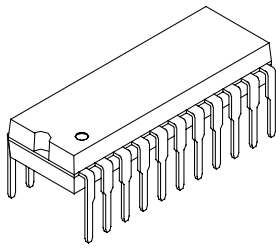
CXA2016S

Sync Identification for CRT Display

Description

The CXA2016S is used for sync signal identification and waveform shaping in the CRT computers display for multi-scan system. There are three types of sync input signals for identification: separate sync, composite sync, and sync on video signals.

22 pin SDIP (Plastic)



Features

- Power save function available (5 V power supply)
- Clamp pulse output position selectable among sync interval, back porch interval, and AUTO.
- Polarity information of sync signals is output.
- Polarity and amplitude of input signals:

	Polarity	Amplitude (Vp-p)
V. separate sync:	Positive/Negative	1 to 5
H. separate sync:	Positive/Negative	1 to 5
Composite sync:	Positive/Negative	1 to 5
Sync on video:		
Sync signals part of	Negative	0.2 to 0.4
Video part		0 to 1.4

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D	962	mW

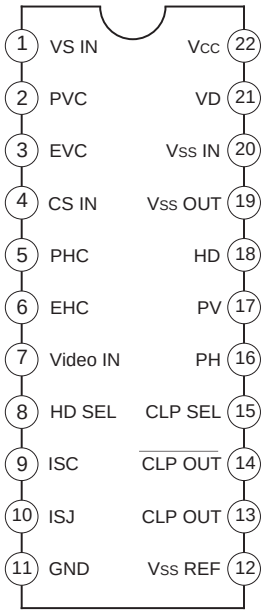
Operating Conditions

Supply voltage	V_{CC}	5 ± 0.25	V

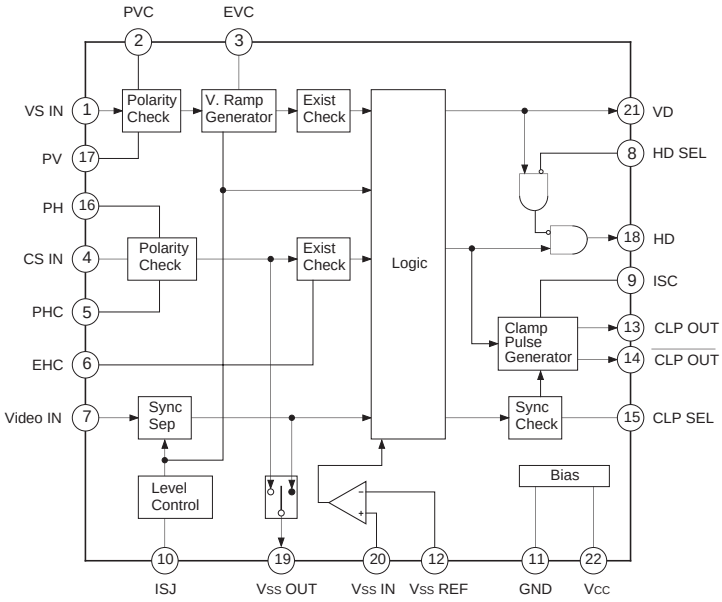
Applications

CRT display monitor

Pin Configuration (Top View)



Block Diagram



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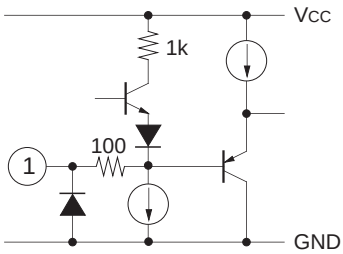
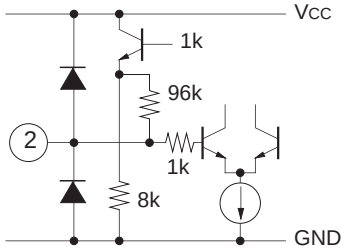
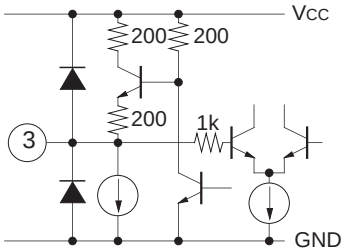
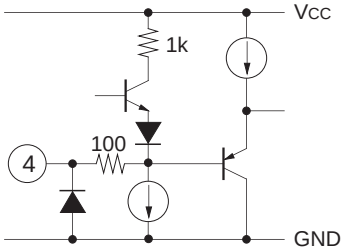
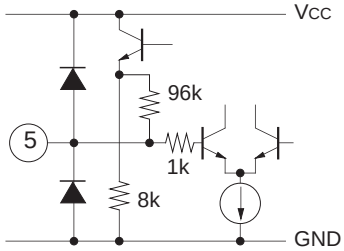
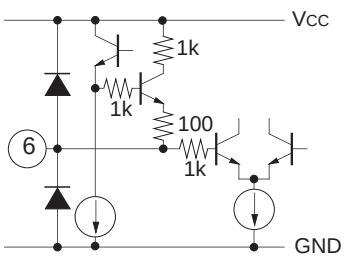
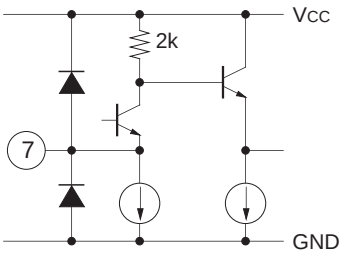
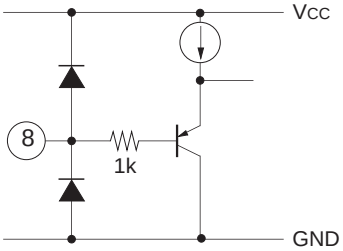
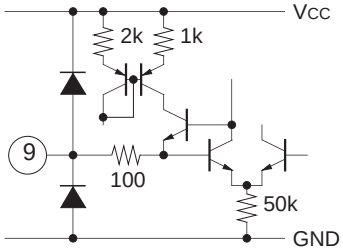
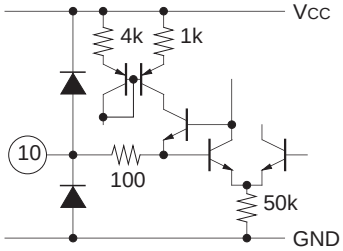
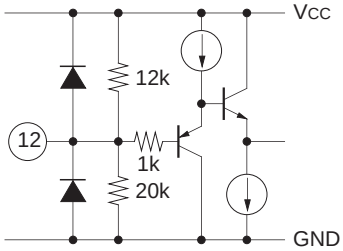
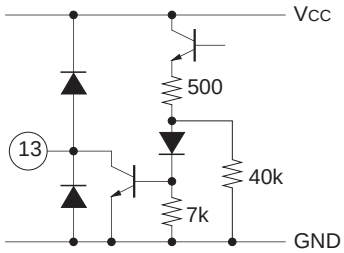
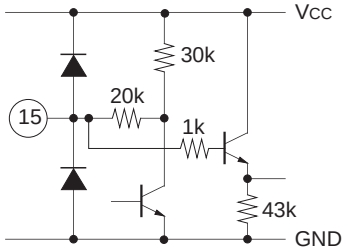
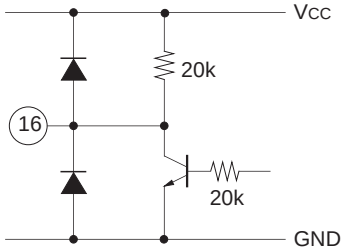
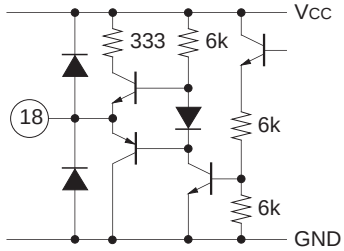
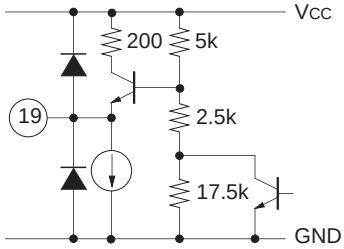
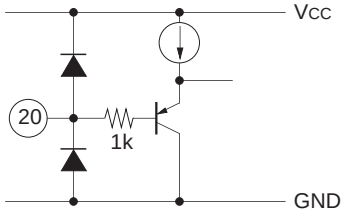
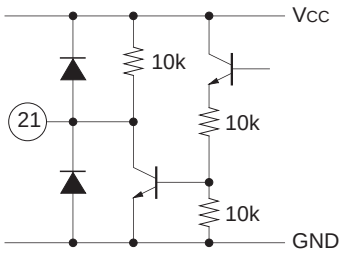
E95422B78-TE

Pin Description (Ta=25 °C, Vcc=5 V)

Pin No	Symbol	Pin voltage	Equivalent circuit	Description
1	VS IN	2.6 V		V. separate sync (positive/negative polarity) as capacitor input. Amplitude is 1 to 5 Vp-p.
2	PVC	—		This pin connects a 0.22 µF integrating capacitor for the vertical signal polarity check circuit to GND. When connecting the capacity at positive polarity, it is 2.9 V and at negative polarity, 120 mV.
3	EVC	—		V. ramp waveforms generation part of vertical signal exist check circuit. Generates ramp waveforms synchronously with the input signal cycle and connects 0.22 µF to GND.
4	CS IN	2.6 V		Inputs composite sync (positive/negative polarity) and H. separate sync (positive/negative polarity) as capacitor input. Amplitude is 1 to 5 Vp-p.
5	PHC	—		This pin connects a 0.1 µF integrating capacitor for the horizontal signal polarity check circuit to GND. When connecting the capacity at positive polarity, it is 2.6 V and at negative polarity, 350 mV.
6	EHC	—		A 33 kΩ resistance and a nearly peak hold circuit for 0.22 µF capacitor are connected to this pin for input signal exist check at CS IN input pin. When a signal is input at CS IN pin, a nearly peak hold is executed at 2.1 V to 2.7 V, a comparison is made with the 1.4 V reference voltage, and input signal exist is identified.

Pin No	Symbol	Pin voltage	Equivalent circuit	Description
7	Video IN	—		Inputs sync on video (sync at negative polarity). Connects in series a 1 µF capacitor and a 270 Ω resistance to input signals.
8	HD SEL	—		Selects output processing of HD (H. Drive Pulse) at a VD interval. Input at TTL level. When Low level is selected, HD is not output at a VD interval. When High level is selected, HD is output at the VD interval.
9	ISC	1.2 V		Resistance connecting pin for reference current source of clamp pulse output circuit, and connects 12 kΩ resistance to GND. When a 12 kΩ resistance is connected, a 100 µA current flows through this pin (pulse width is approximately 300 ns). Clamp pulse output pulse width is varied by changing the value of the resistance. *Use a metal film resistor with an accuracy of ±1 %
10	ISJ	1.2 V		Resistance connecting pin for reference current source and connecting 12 kΩ resistance to GND. When the resistance is connected, a 100 µA current flows through this pin. *Use a metal film resistor with an accuracy of ±1 %
11	GND	0 V	—	GND pin.
12	V_{SS} REF	3.125 V		Reference pin for V. sync separator of composite sync and video sync.

Pin No	Symbol	Pin voltage	Equivalent circuit	Description
13	CLP OUT	—		Clamp pulse output; Open collector-type pin at positive polarity.
14	$\overline{\text{CLP OUT}}$	—		Clamp pulse output; Open collector-type pin at negative polarity.
15	CLP SEL	—		Selects output position of a clamp pulse. Input at TTL level. When Low level is selected, a clamp pulse is output at a back porch interval. When High level is selected, clamp pulse is output at a sync interval. See the Description of Operation for Input/Output Matrix.
16 17	PH PV	—		Output polarity information of horizontal and vertical sync signals. See the Description of Operation for Input/Output Matrix.
18	HD	—		HD (H. Drive Pulse) output; Push-pull type pin at positive polarity.
19	Vss OUT	—		Composite sync or sync signal separated from video sync is output. Output is at positive polarity.
20	Vss IN	—		Input for V. sync separator comparator. Integrates the output at Pin 19 and inputs it.

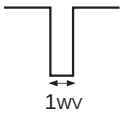
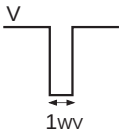
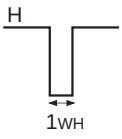
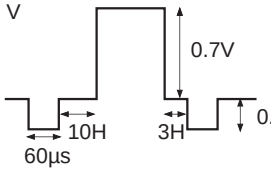
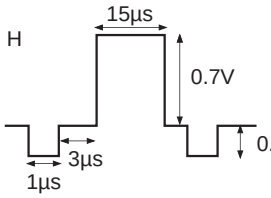
Pin No	Symbol	Pin voltage	Equivalent circuit	Description
21	VD	—		VD (V. Drive Pulse) output pin. Output is at positive polarity.
22	Vcc	5 V	—	Power supply pin.

Electrical Characteristics (Ta=25 °C, V_{CC}=5 V. See the Electrical Characteristics Measurement Circuit.)

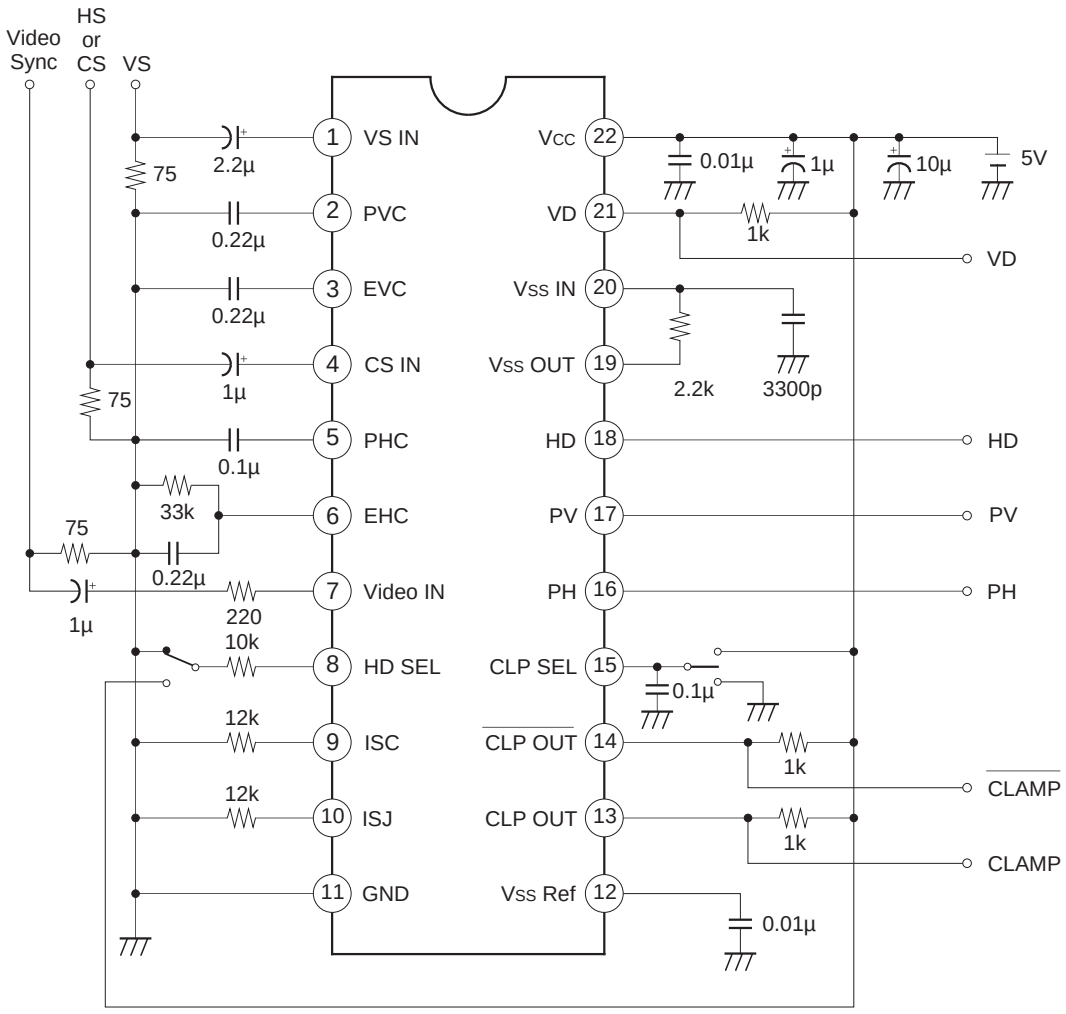
No.	Item	Symbol	Measurement contents	Measurement point	Min.	Typ.	Max.	Unit
1	VD output voltage	E_{VD}	Measure VD output peak value during V. separate sync input. Input signal A. (tw=60 µs)	VD (Pin 21)	High level			V
					4.3	4.9	—	
					Low level			
					—	0.1	0.4	
2	HD output voltage	E_{HD}	Measure HD output peak value during sync on video input. Input signal C. (tw=1 µs)	HD (Pin 18)	High level			V
					3.3	4.2	—	
					Low level			
					—	0.3	0.5	
3	Clamp pulse output voltage	E_{CP}	Measure clamp pulse output peak value during composite sync input. Input signal B. (tw=1 µs)	CLAMP (Pin 13)	High level			V
					4.3	4.9	—	
					Low level			
					—	0.3	0.8	
				$\overline{\text{CLAMP}}$ (Pin 14)	High level			V
					4.3	4.9	—	
					Low level			
					—	0.4	0.9	
4	Clamp pulse output pulse width	t_C	Measure clamp pulse output pulse width during composite sync input. Input signal B. (tw=1 µs)	CLAMP (Pin 13)	260	305	380	ns
				$\overline{\text{CLAMP}}$ (Pin 14)	260	310	380	ns
5	HD delay	thd	Measure delay difference between CS and HD during composite sync input. Or the time from CS (positive polarity) rise time (50 %) to HD output rise time (50 %). Input signal D.	HD (Pin 18)	—	75	100	ns
6	Clamp pulse delay	tcd1	Measure delay difference between HD and clamp pulse during composite sync input. Or the time from HD output fall time (50 %) to clamp pulse output rise time*1 (50 %). Input signal B.	CLAMP (Pin 13)	—	5.0	30	ns
				$\overline{\text{CLAMP}}$ (Pin 14)	—	5.0	30	
7	Polarity identification output voltage	P_N	Sync signal polarity information is output. Measure high level voltage. (No load)	PH, PV (Pins 16 and 17)	4.3	—	—	V
		P_P	Sync signal polarity information is output. Measure low level voltage. (No load)	PH, PV (Pins 16 and 17)	—	—	0.4	V
8	Current consumption	I_{CC}	V_{CC}=5 V. Measure current consumption during no signal input.	V_{CC} (Pin 22)	—	26.5	45	mA

*1 $\overline{\text{CLAMP}}$ is for the fall time.

Types of Signal Source

Signal	Item	V. SYNC IN (Pin 1)	Composite SYNC IN (Pin 4)	Video IN (Pin 7)
A	1	 fv=40 Hz twv=60 µs Negative logic 1 Vp-p		
B	3, 4, 6		 fv=40 Hz twv=60 µs Negative logic 1 Vp-p  fH=50 kHz twH=1 µs Negative logic 1 Vp-p	
C	2			 fv=40 Hz twv=60 µs  fH=50 kHz twH=1 µs
D	5		fH=50 kHz twH=1 µs Positive logic 1 Vp-p	

Electrical Characteristics Measurement Circuit



Description of Operation

Input signal

- VS IN (Pin 1)
  - f_V : 40 to 200 Hz
  - V_S : 1 to 5Vp-p (positive/negative polarity)
- HS IN (Pin 4)
  - f_H : 15k to 130 kHz
  - V_S : 1 to 5 Vp-p (positive/negative polarity)
- CS IN (Pin 4)
  - f_H : 15 k to 130 kHz
  - f_V : 40 to 200 Hz
  - V_S : 1 to 5 Vp-p (positive/negative polarity)
- Video IN (Pin 7)
  - f_H : 15 k to 130 kHz
  - f_V : 40 to 200 Hz
  - V_V : 0 to 1.4 Vp-p
  - V_S : 0.2 to 0.4 Vp-p

Clamp Pulse Output

- Clamp pulse (Pins 13 and 14) is output under the following conditions.
  Pin 13 is for open collector output and is at positive polarity.
  Pin 14 is for open collector output and is at negative polarity.
  td: Clamp pulse delays for 10 to 20 ns from HD.
  tw: Clamp pulse width varies depending on the value of the resistance connected to Pin 9.

<Conditions>

(1) When CS IN or Video IN is selected, a clamp pulse at the VD interval is not output.
(2) During H./V. Separate Sync, a clamp pulse at the VD interval is also output.
(3) When Pin 15 (CLP SEL) is connected to GND, a clamp pulse is output at the back porch interval. When Pin 15 (CLP SEL) is connected to V_{CC}, a clamp pulse is output at the SYNC interval. If a capacitor is connected between this pin and GND, the output position is automatically selected.

Clamp Pulse Input/Output Matrix

CLP SEL	VS IN	CS IN	Video IN	Clamp pulse output position
GND	*	*	*	Back porch interval
V_{CC}	*	*	*	SYNC interval
AUTO	*	—	O	Back porch interval
	*	O	—	SYNC interval
	*	—	—	(Back porch interval)

[O] indicates that input SYNC exists.
[—] indicates no signal (no SYNC).
[*] has no relation with input signal.

HD Select Function
When HD SEL is Low, HD at the VD interval is not output.
When HD SEL is High, HD at the VD interval is output.

During separate sync output, HD is output regardless of HD SEL.

Mode Matrix of SYNC Polarity Identification Signal

VS IN (Pin 1)	CS IN (Pin 4)	PV out (Pin 17)	PH out (Pin 16)
VS (positive polarity)	No signal	Low	Low
	HS (positive polarity)	Low	Low
	HS (negative polarity)	Low	High
VS (negative polarity)	No signal	High	Low
	HS (positive polarity)	High	Low
	HS (negative polarity)	High	High
No signal	No signal	Low	Low
	COMP (positive polarity)	Low	Low
	COMP (negative polarity)	Low	High

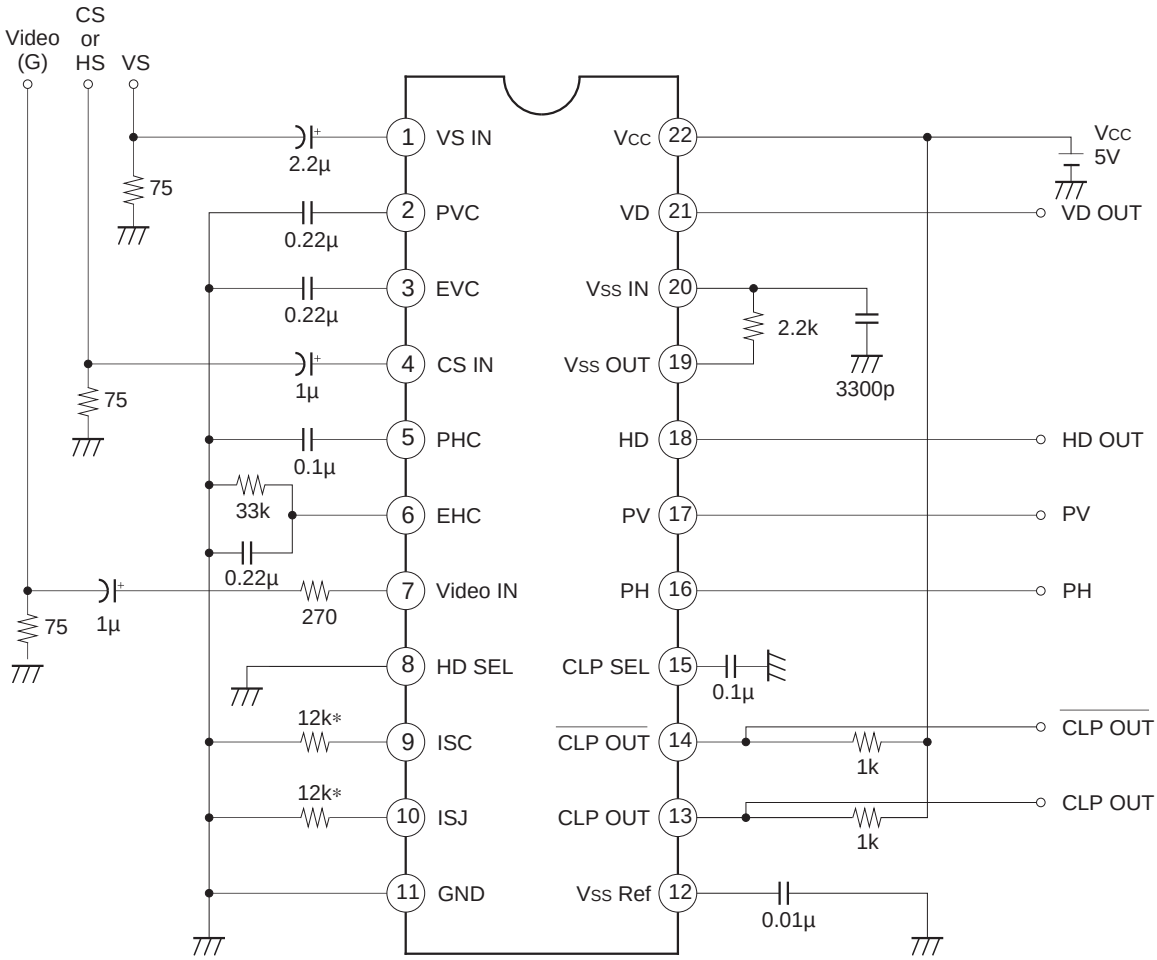
Low level: 0 to 0.4 V, High level: V_{CC}

Input/Output Matrix

VS IN	CS IN	Video IN	VD OUT	HD OUT
O	O	*	VS	CS
—	O	*	CS	CS
—	—	O	Video	Video
—	—	—	(Video)	(Video)
O	—	O	VS	Video
O	—	—	VS	(Video)

Note) The corresponding sync signals are input to VSIN and Video IN.
[O] indicates that input SYNC exists.
[—] indicates no signal.
[*] has no relation with input signal.

Application Circuit

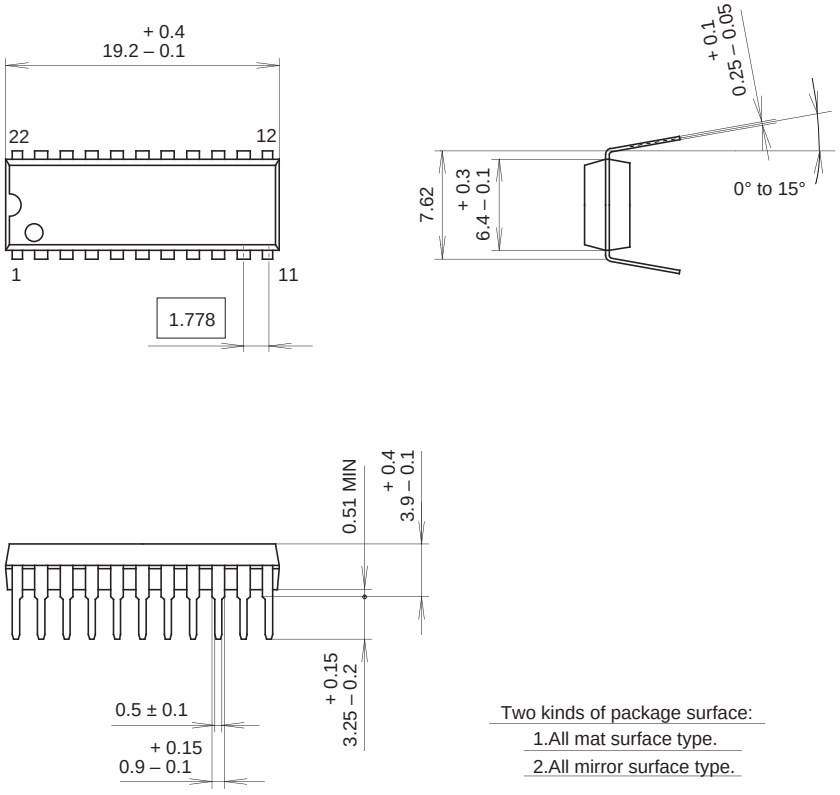


Use metal film resistor with an accuracy of ±1% for the resistor marked ∗.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

22PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

PACKAGE STRUCTURE

SONY CODE	SDIP-22P-01
EIAJ CODE	SDIP022-P-0300
JEDEC CODE	————

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.95g