SONY

CXD1913AQ

Digital Video Encoder

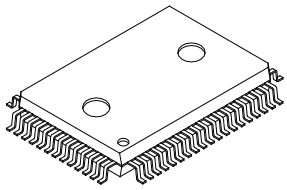
Description

The CXD1913AQ is a digital video encoder designed for video CD, car navigation system and other digital video applications. The device accepts ITU-R601 compatible Y, Cb, Cr data and also accepts ITU-R656-format Y, Cb, Cr data, and the data are encoded to composite video and separate Y/C video (S-Video) signal.

Features

- NTSC and PAL encoding mode
- Composite video and separate Y/C video (S-Video) signal outputs
- 8/16-bit pixel data input mode
- 13.5 Mpps pixel rate
- Interlace and non-interlace supported
- On-chip 100% color bar generator
- 10-bit 3 channels DACs
- Supports I^2C bus (400kHz) and SONY SIO
- Closed Caption (Line 21, Line 284) encoding
- VBID encoding
- Monolithic CMOS single 3.3V ± 5% and 5.0V ± 5% power supplies
- 64-pin plastic QFP package

64 pin QFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
• Output voltage	V_O	–0.3 to +7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C
	(Vss = 0V)		

Recommended Operating Conditions

• Logic supply voltage	DV_{DD}	3.3V ± 5%	
	DV_{DD}	5.0V ± 5%	
• Analog supply voltage	AV_{DD}	3.3V ± 5%	
	AV_{DD}	5.0V ± 5%	
• Input voltage	V_{IN}	Vss to V_{DD}	V
• Operating temperature	Topr	0 to +70	°C

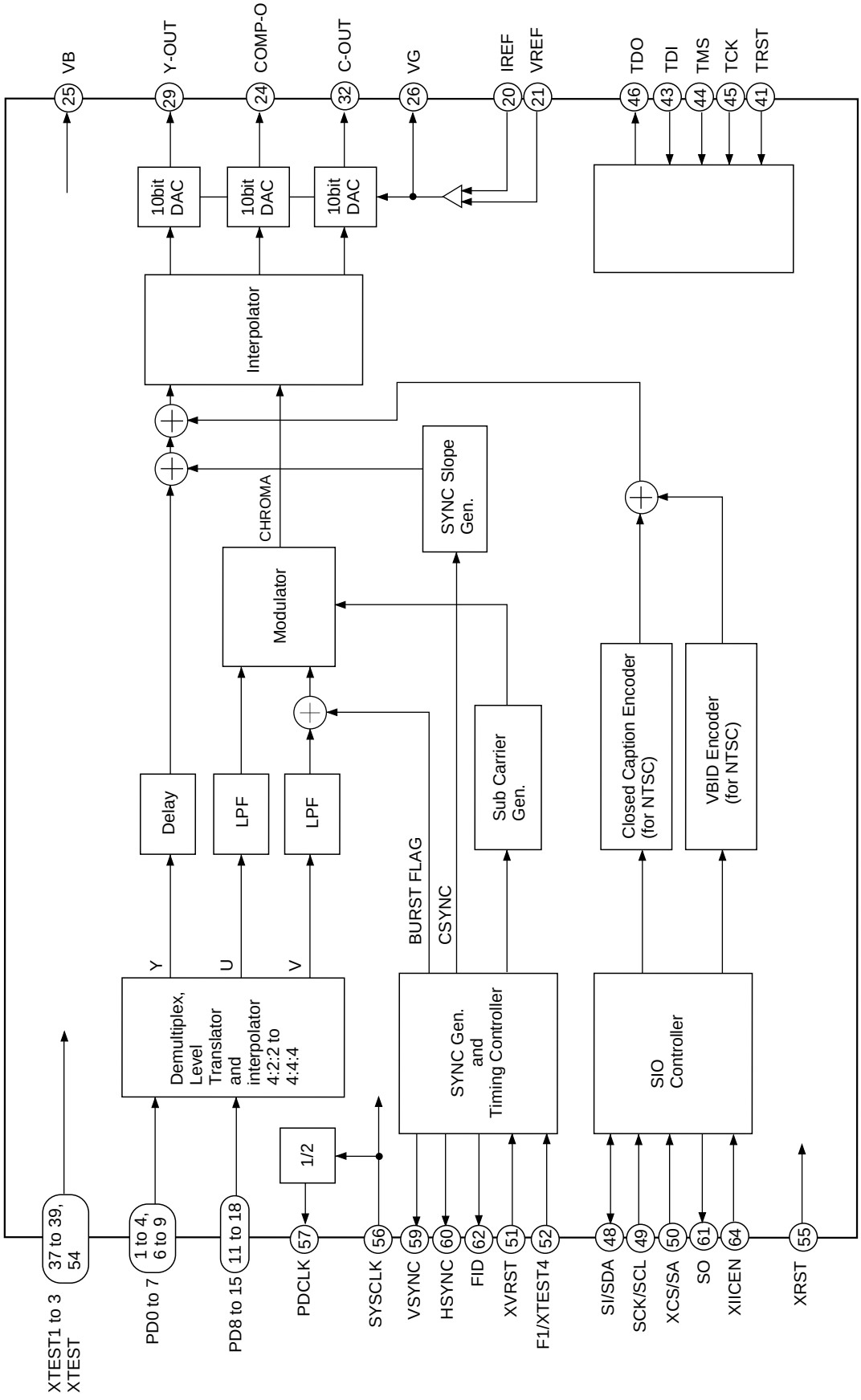
I/O Capacitance

• Input pin	C_I	11 (Max.)	pF
• Output pin	C_O	11 (Max.)	pF

Note) Test conditions: $V_{DD} = V_I = 0V$
f_M = 1MHz

E97918-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	PD7	I	8-bit pixel data input pins (PD0 to 7). When control register bit “PIF MODE” = “0”: These are inputs for multiplexed Y, Cb, and Cr signal. When control register bit “PIF MODE” = “1”: These are inputs for Y signal.
2	PD6	I	
3	PD5	I	
4	PD4	I	
5	V_{SS}	—	Digital ground
6	PD3	I	8-bit pixel data input pins (PD0 to 7). When control register bit “PIF MODE” = “0”: These are inputs for multiplexed Y, Cb, and Cr signal. When control register bit “PIF MODE” = “1” These are inputs for Y signal.
7	PD2	I	
8	PD1	I	
9	PD0	I	
10	V_{DD}	—	Digital power supply
11	PD15/TD7	I/O	8-bit pixel data input pins / Test data bus. When control register bit “PIF MODE” = “0”: These inputs are not used. When control register bit “PIF MODE” = “1”: These are inputs for multiplexed Cb and Cr signal. For test mode, it's used for internal circuit test data bus. Test mode is available only for device bender.
12	PD14/TD6	I/O	
13	PD13/TD5	I/O	
14	PD12/TD4	I/O	
15	PD11/TD3	I/O	
16	PD10/TD2	I/O	
17	PD9/TD1	I/O	
18	PD8/TD0	I/O	
19	V_{SS}	—	Digital ground
20	IREF	O	Reference current output. Connect resistance “16R” which is 16 times output resistance “R”.
21	VREF	I	Voltage reference input. Sets output full scale value.
22	$AV_{DD}1$	—	Analog power supply
23	$AV_{SS}1$	—	Analog ground
24	COMP-O	O	10-bit D/A converter output. This pin outputs composite signal.
25	VB	O	Connect to V_{SS} with a capacitor of approximately 0.1µF.
26	VG	O	Connect to AV_{DD} with a capacitor of approximately 0.1µF.
27	$AV_{DD}2$	—	Analog power supply
28	$AV_{SS}2$	—	Analog ground
29	Y-OUT	O	10-bit D/A converter output. This pin outputs luminance (Y) signal.
30	$AV_{DD}3$	—	Analog power supply
31	$AV_{SS}3$	—	Analog ground

Pin No.	Symbol	I/O	Description
32	C-OUT	O	10-bit D/A converter output. This pin outputs chroma (C) signal.
33	TD10	I/O	Test data bus. This pin should be open. For test mode, it's used for internal circuit test data bus. Test mode is available only for device bender.
34	V_{DD}	—	Digital power supply
35	TD9	I/O	Test data bus. These pins should be open. For test mode, it's used for internal circuit test data bus. Test mode is available only for device bender.
36	TD8	I/O	
37	XTEST1	I	Test mode control inputs. These pins are pulled up. Normally, these pins should be open.
38	XTEST2	I	
39	XTEST3	I	
40	V_{SS}	—	Digital ground
41	TRST	I	Test mode reset input. This pin is pulled up. For power on reset, set "L" for more than 40 clocks (SYSCLK).
42	V_{DD}	—	Digital power supply
43	TDI	I	Test mode control input. This pin is pulled up.
44	TMS	I	Test mode control input. This pin is pulled up.
45	TCK	I	Test mode control input. This pin should be "H" input.
46	TDO	O	Test data bus output. This pin should be open.
47	V_{SS}	—	Digital ground
48	SI/SDA	I	This pin's function is selected by XIICEN (Pin 64). When XIICEN = "H", this pin is SONY SIO mode; SI serial data input. When XIICEN = "L", this pin is I^2C bus mode; SDA input/output.
49	SCK/SCL	I	This pin's function is selected by XIICEN (Pin 64). When XIICEN = "H", this pin is SONY SIO mode; SCK serial clock input. When XIICEN = "L", this pin is I^2C bus mode; SCL input.
50	XCS/SA	I	This pin's function is selected by XIICEN (Pin 64). This pin is pulled up. When XIICEN = "H", this pin is SONY SIO mode; XCS chip select input. When XIICEN = "L", this pin is I^2C bus mode; SA slave address select input signal which selects I^2C bus slave address.
51	XVRST	I	Vertical sync reset input in active low. This pin is pulled up. This is used to synchronize external vertical sync and internal vertical sync. When XVRST is "L", internal digital sync generator is reset according to F1 status. Valid only for 8-bit mode (control register address 01H bit 4 "PF MODE" = "0").
52	F1/ XTEST4	I	This pin's function is selected by XTEST (Pin 54). When XTEST = "H", this pin is F1; field ID input. Field ID during vertical sync reset is indicated. "H" indicates 1st field. "L" indicates 2nd field. When XTEST = "L", XTEST4 input.

Pin No.	Symbol	I/O	Function
53	V_{DD}	—	Digital power supply
54	XTEST	I	Test mode control input. This pin is pulled up. Normally, this pin should be open.
55	XRST	I	System reset input in active low. For power on reset, set “L” for more than 40 clocks (SYSCLK).
56	SYSCLK	I	System clock input. To generate correct subcarrier frequency, precise 27MHz is required.
57	PDCLK	O	Pixel data clock output. This clock is divided in half from SYSCLK. This is used when 16-bit pixel data mode.
58	V_{SS}	—	Digital ground
59	VSYNC	O	Vertical sync signal output.
60	HSYNC	O	Horizontal sync signal output.
61	SO	O	This pin's function is selected by XIICEN (Pin 64). When XIICEN = “H”, this pin is SONY SIO mode; SO serial out output. When XIICEN = “L”, this pin is not used and output is high impedance.
62	FID	O	Field ID output. When control register bit “FIDS” = “1”: “L” indicates 1st field, “H” indicates 2nd field. When control register bit “FIDS” = “0”: “H” indicates 1st field, “L” indicates 2nd field.
63	V_{DD}	—	Digital power supply
64	XIICEN	I	Serial interface mode select input. This pin is pulled up. When XIICEN = “L”, Pins 48 to 50 and 61 are I^2C bus mode. When XIICEN = “H”, Pins 48 to 50 and 61 are SONY SIO mode.

Electrical Characteristics

DC characteristics

(Ta = 0 to +70°C, Vss = 0V)

Item	Symbol	Measurement conditionsConditions	Min.	Typ.	Max.	Unit	Pins
Input high voltage	V_{IH1}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	2.2 1.8			V	*1
Input low voltage	V_{IL1}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			0.8 0.5	V	*1
Input high voltage	V_{IH2}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	2.4 1.8			V	*2
Input low voltage	V_{IL2}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			0.8 0.5	V	*2
Input high voltage	V_{IH3}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	0.7V_{DD}			V	*3
Input low voltage	V_{IL3}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			0.3V_{DD}	V	*3
Output high voltage	V_{OH1}	I_{OH} = –2.4mA V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	V_{DD} – 0.8			V	*4
Output low voltage	V_{OL1}	I_{OL} = 4.8mA V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			0.4	V	*4
Output high voltage	V_{OH2}	I_{OH} = –1.2mA V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	V_{DD} – 0.8			V	*5
Output low voltage	V_{OL2}	I_{OL} = 2.4mA V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			0.4	V	*5
Input leak current	I_{IL1}	V_I = 0 to 5.25V V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	–10		10	µA	*6
Input leak current	I_{IL2}	V_I = 0V V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%	–40 –12	–100 –30	–240 –75	µA	*7
Supply current	I_{DD}	V_{DD} = 5.0V ± 5% V_{DD} = 3.3V ± 5%			70 *8 40 *8	mA	

*1 PD0 to 15, TD8 to 10, XTEST1 to 3, TRST, TDI, TCK, XCS/SA, XVRST, F1/XTEST4, XTEST, XRST, XIICEN

*2 SYSCLK

*3 SI/SDA, SCK/SCL

*4 PDCLK, VSYNC, HSYNC, FID, SO

*5 TDO, TD0 to 10

*6 PD0 to 15, TD8 to 10, TCK, SI/SDA, SCK/SCL, F1/XTEST4, XRST, SYSCLK

*7 XTEST1 to 3, TRST, TDI, TMS, XCS/SA, XVRST, XTEST, XIICEN

*8 Not include analog current

DAC characteristics 1 (AV_{DD} = 5.0V, R = 200Ω, V_{REF} = 2.0V, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Linearity error	E_L		–2.0		2.0	LSB
Differential linearity error	E_D		–1.0		1.0	LSB
Output full-scale current	I_{FS}		9.5	10.0	10.5	mA
Output offset voltage	V_{OS}				1	mV
Output full-scale voltage	V_{FS}		1.9	2.0	2.1	V
Precision guaranteed output voltage range	V_{OC}		1.9	2.0	2.1	V

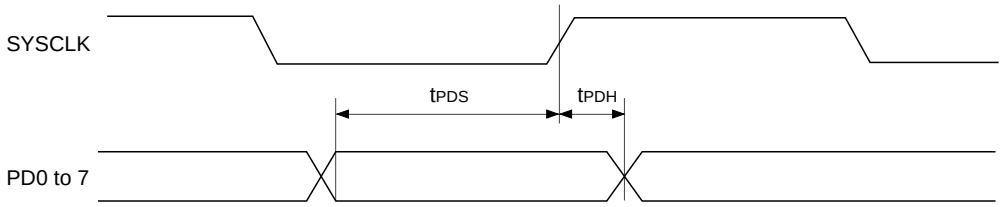
DAC characteristics 2 (AV_{DD} = 3.3V, R = 200Ω, V_{REF} = 1.35V, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Linearity error	E_L		–3.0		3.0	LSB
Differential linearity error	E_D		–1.5		1.5	LSB
Output full-scale current	I_{FS}		6.25	6.75	7.25	mA
Output offset voltage	V_{OS}				1	mV
Output full-scale voltage	V_{FS}		1.25	1.35	1.45	V
Precision guaranteed output voltage range	V_{OC}		1.25	1.35	1.45	V

AC characteristics

1. Pixel Data Interface

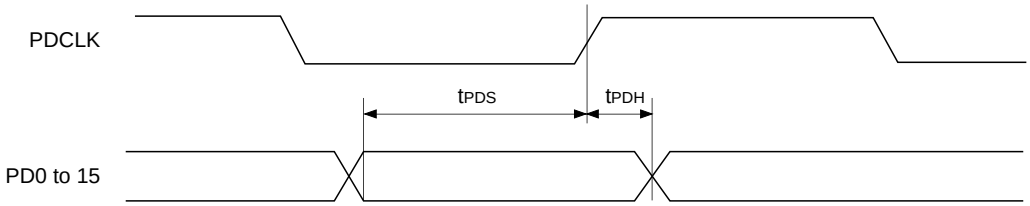
(1) 8-bit mode



(Ta = 0 to +70°C, V_{DD} = 3.3V ± 5%, 5.0V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to SYSCLK	t_{PDS}	10			ns
Pixel data hold time to SYSCLK	t_{PDH}	3			ns

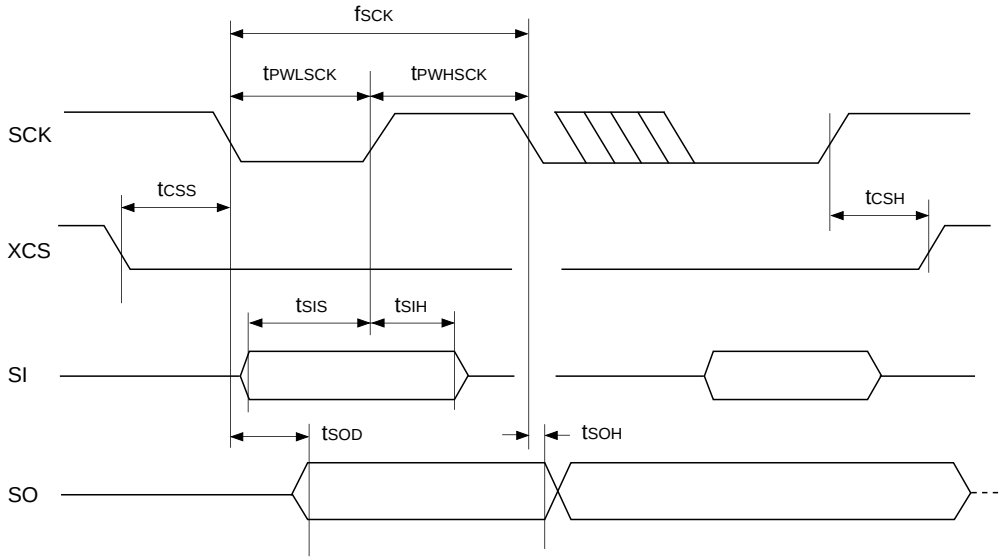
(2) 16-bit mode



(Ta = 0 to +70°C, V_{DD} = 3.3V ± 5%, 5.0V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to PDCLK	t_{PDS}	20			ns
Pixel data hold time to PDCLK	t_{PDH}	0			ns

2. Serial Port Interface



(Ta = 0 to +70°C, V_{DD} = 5.0V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock rate	f_{SCK}	DC		3	MHz
SCK pulse width Low	t_{PWLSCK}	100			ns
SCK pulse width High	t_{PWHSCK}	100			ns
Chip select setup time to SCK	t_{CSS}	150			ns
Chip select hold time to SCK	t_{CSH}	150			ns
Serial input setup time to SCK	t_{SIS}	50			ns
Serial input hold time to SCK	t_{SIH}	10			ns
Serial output delay time from SCK	t_{SOD} *			30	ns
Serial output hold time from SCK	t_{SOH} *	3			ns

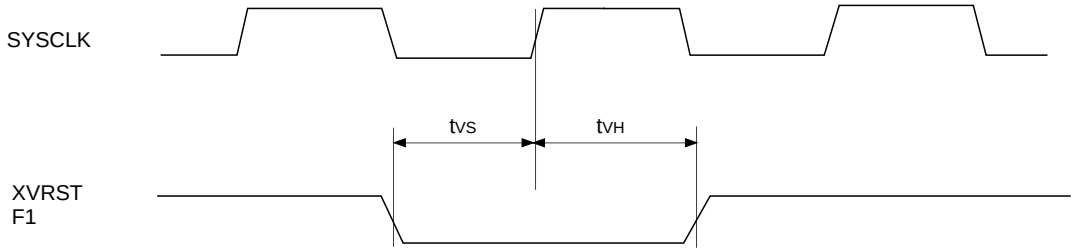
* C_L = 35pF

(Ta = 0 to +70°C, V_{DD} = 3.3V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock rate	f_{SCK}	DC		3	MHz
SCK pulse width Low	t_{PWLSCK}	100			ns
SCK pulse width High	t_{PWHSCK}	100			ns
Chip select setup time to SCK	t_{CSS}	150			ns
Chip select hold time to SCK	t_{CSH}	150			ns
Serial input setup time to SCK	t_{SIS}	50			ns
Serial input hold time to SCK	t_{SIH}	10			ns
Serial output delay time from SCK	t_{SOD} *			50	ns
Serial output hold time from SCK	t_{SOH} *	3			ns

* C_L = 35pF

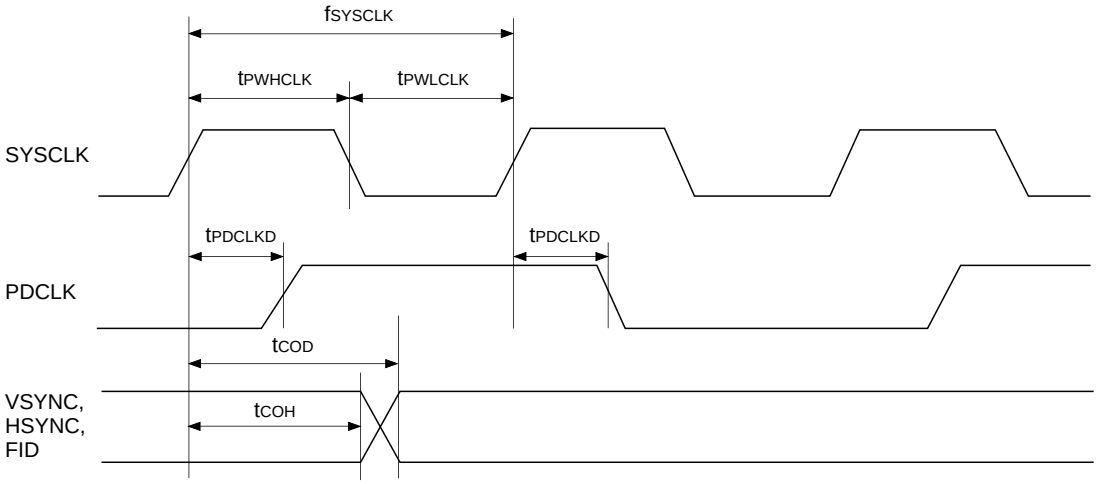
3. XVRST, F1



(Ta = 0 to +70°C, V_{DD} = 3.3V ± 5%, 5.0V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
XVRST setup time to SYSCLK	t_{VS}	20			ns
XVRST hold time to SYSCLK	t_{VH}	0			ns

4. SYSCLK, PDCLK, VSYNC, HSYNC, FID



(Ta = 0 to +70°C, V_{DD} = 5.0V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SYSCLK clock rate	f_{SYSCLK}		27		MHz
SYSCLK pulse width Low	t_{PWLCLK}	11			ns
SYSCLK pulse width High	t_{PWHCLK}	11			ns
PDCLK delay time from SYSCLK	t_{PDCLKD} *			15	ns
Control output delay time from SYSCLK	t_{COD} *			20	ns
Control output hold time from SYSCLK	t_{COH} *	3			ns

* C_L = 35pF

(Ta = 0 to +70°C, V_{DD} = 3.3V ± 5%, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SYSCLK clock rate	f_{SYSCLK}		27		MHz
SYSCLK pulse width Low	t_{PWLCLK}	11			ns
SYSCLK pulse width High	t_{PWHCLK}	11			ns
PDCLK delay time from SYSCLK	t_{PDCLKD} *			23	ns
Control output delay time from SYSCLK	t_{COD} *			25	ns
Control output hold time from SYSCLK	t_{COH} *	3			ns

* C_L = 35pF

Description of Functions

The CXD1913AQ converts digital parallel data (ITU-R601 Y, Cb, Cr) into analog TV signals in NTSC (RS170A) or PAL (ITU-R624; B, G, H, I) format.

The CXD1913AQ first receives image data in 8-bit parallel form (multiplexed Y, Cb, and Cr data), or in 16-bit parallel form (8-bit Y and 8-bit multiplexed Cb and Cr data). After demultiplexing, it converts Cb and Cr signals into U and V signals respectively, interpolates 4:2:2 to 4:4:4, and modulates the signals with the subcarrier generated by digital subcarrier generator.
Y signal and modulated chroma signal are oversampled (at double) to reduce sin (x)/(x) rolloff.
10-bit DACs are used for converting digital composite and Y/C signals into analog signals.

1. Pixel Input Format

Pixel input format is determined by Bit 4 (PIF MODE) of control register address 01H as shown in Table 1-1.
When PIF MODE is “0”, the image data (Y, Cb, Cr) input from PD0 to PD7 is sampled at the rising edge of SYSCLK.
When PIF MODE is “1”, Y data is input into PD0 to 7, multiplexed Cb and Cr data are input into PD8 to 15, and these respective data are sampled at the rising edge of PDCLK.

Table 1-1

PIF MODE	PD15 to 8	PD7 to 0
0 (8-bit mode)	NA	Y/Cb/Cr
1 (16-bit mode)	Cb/Cr	Y

Also, pixel input data sampling point is determined by Bits 3 and 2 (PIX TIM) of control register address 01H as shown in Table 1-2.

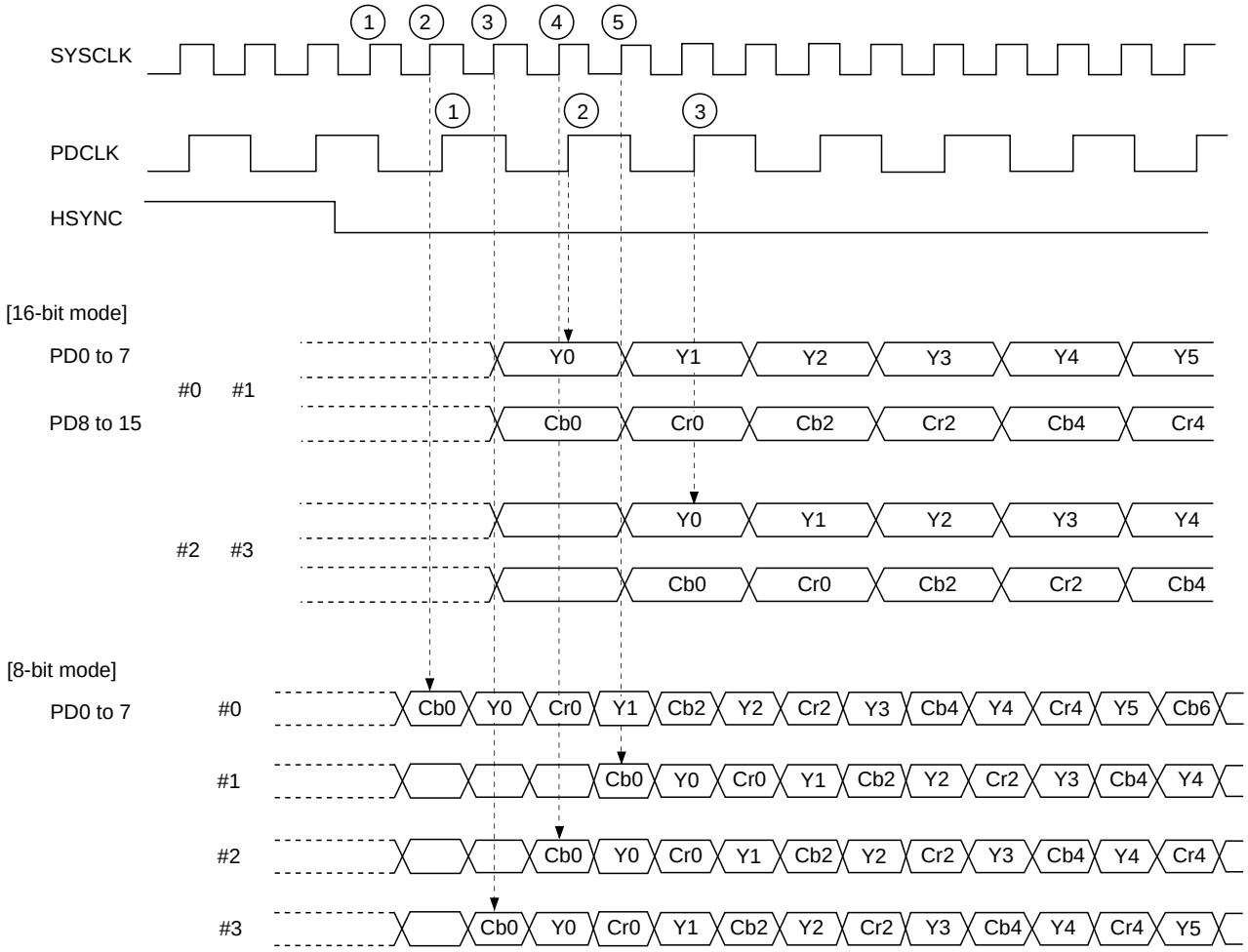
During 8-bit mode, the data, which is sampled at the timing phase (Fig 1-1: 8-bit mode #0 to #3) set at PIX TIM from the falling edge of HSYNC, is recognized as Cb0.
(in the default, the data, which is sampled at the rising edge of second SYSCLK from the falling edge of HSYNC), is recognized as Cb0.

During 16-bit mode, the data, which is sampled at the timing phase (Fig 1-1: 16-bit mode #0 to #3) set at PIX TIM from the falling edge of HSYNC, is recognized as Cb0.
(In the default, the data, which is sampled at the rising edge of second PDCLK from the falling edge of HSYNC), is recognized as Cb0.

Table 1-2

PIX TIM		Timing phase
0	0	#0 (default)
0	1	#1
1	0	#2
1	1	#3

Pixel Data Input Timing



PD0	Pixel data 0 (LSB)	PD8	Pixel data 0 (LSB)
PD1	Pixel data 1	PD9	Pixel data 1
:	:	:	:
PD7	Pixel data 7 (MSB)	PD15	Pixel data 7 (MSB)

Fig 1-1

2. Serial Interface

The CXD1913AQ supports both I²C bus (high-speed mode) and Sony serial interface. These modes can be selected by XIICEN input pin as shown in Table 2-1 below.

Table 2-1

XIICEN	H	L
	Sony SIO mode	I²C mode
SI/SDA	SI	SDA
SCK/SCL	SCK	SCL
XCS/SA	XCS	SA
SO	SO	Hi-Z

2-1. I²C bus interface

The CXD1913AQ becomes a slave transceiver of I²C bus, and supports the 7-bit slave address and the high-speed mode (400K bit/s).

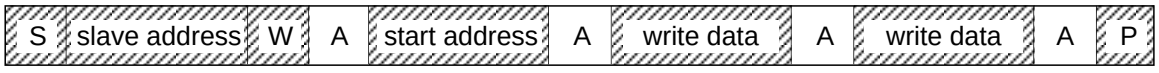
2-1-1. Slave address

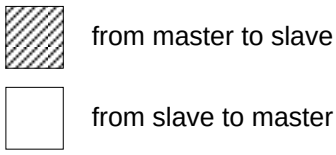
Two kinds of slave addresses (88H, 8CH) can be selected by the SA signal, as shown in Table 2-2 below.

Table 2-2

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	SA	0	X

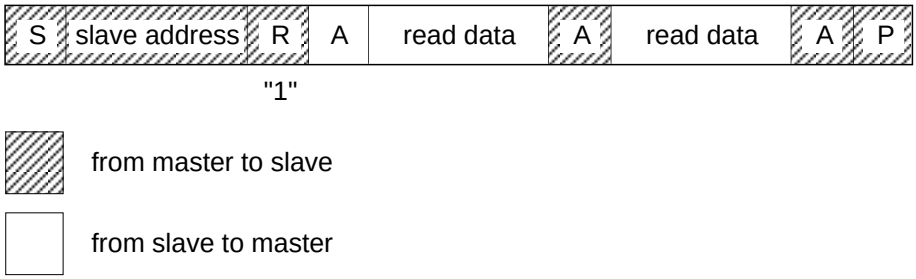
2-1-2. Write cycle





After the slave address is supplied from the master, the data in the next transfer cycle is set up inside the start address register of this IC as start address of the control register. In subsequent cycles, the data supplied from the master is written in the addresses indicated by the control register address. The set control register address is automatically incremented with the completed transfer of each byte of data.

2-1-3. Read cycle



After the slave address is supplied from the master, subsequent cycles change immediately to read cycles and only ID code (addresses 09H, 0AH) is read out. During the read cycle, the start address is automatically set to 09H.

Note) In the Sony SIO mode, addresses from 00H to 0AH can be read out.

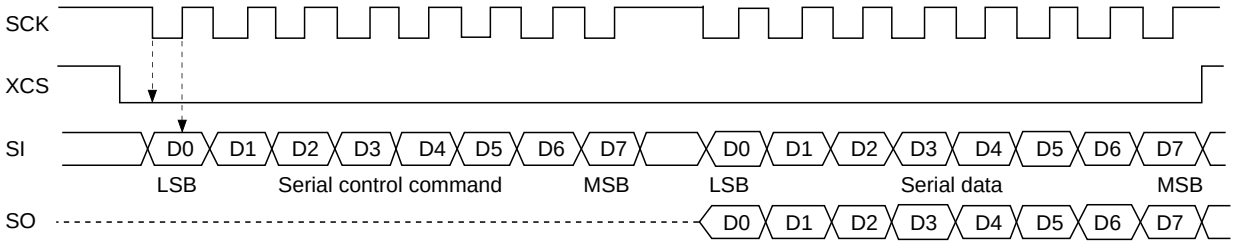
2-1-4. Handling of general call address (00H)

General call address is neglected and there is no ACK response.

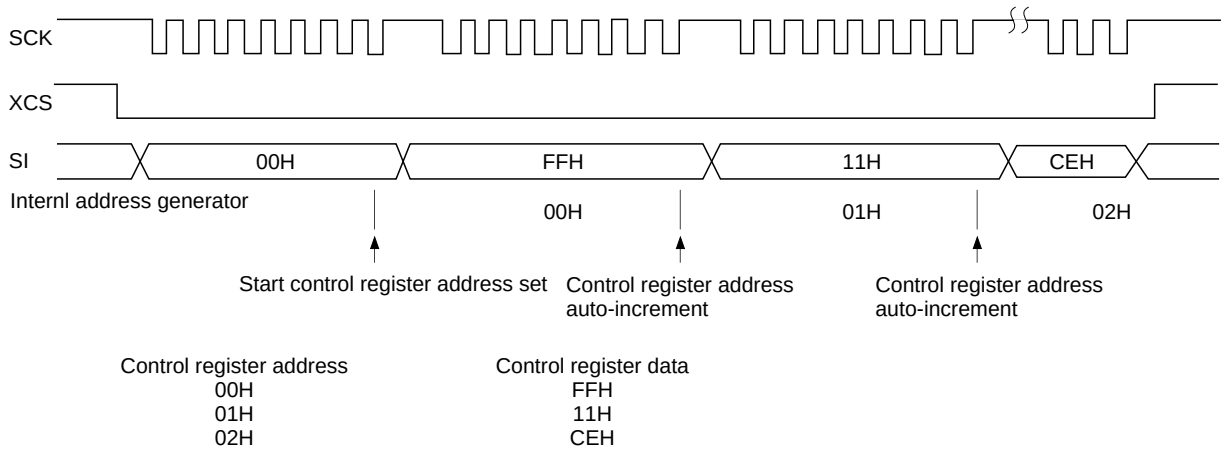
2-2. Sony serial interface

Sony serial interface uses SCK, XCS, SI and SO signals.
Serial interface is activated when XCS signal is “Low”, and samples serial input data at the rising edge of SCK. The first one byte after XCS activation is set up as a serial control command. The data includes a start control register address and direction of the serial interface. The control register address is automatically incremented with the transfer of each byte of data. In the write mode, the data of second byte and after are written in the addresses indicated by the address generated by the address generator of the CXD1913AQ. In the read mode, the serial input data is neglected and writing is not done.

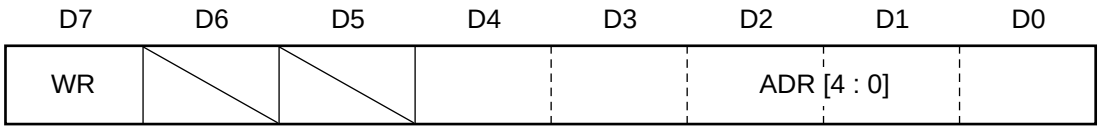
Serial Interface Timing



Serial Interface Sequence



2-1. Serial control command format



WR : Direction for serial interface
When this bit is “1”:
The serial interface is write mode.
Incoming serial data is set up inside the control register according to the control register address.
When this bit is “0”:
The serial interface is read mode.
The control register data is output to SO according to the control register address.

ADR [4 : 0] : Start control register address

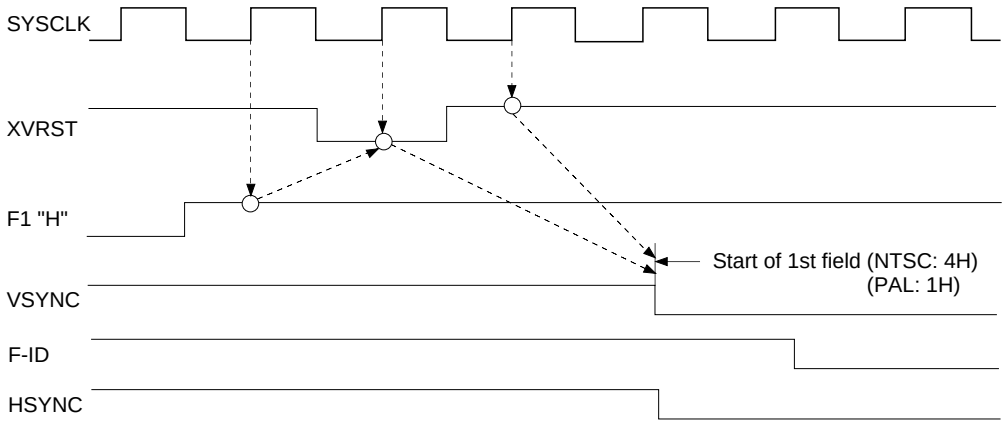
3. XVRST, F1

XVRST and F1 signals are used to synchronize with external V sync.

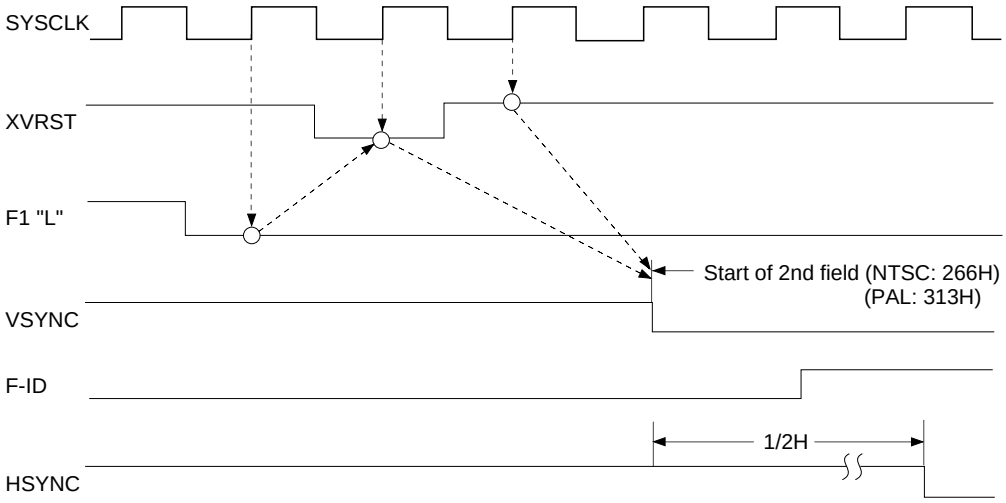
XVRST and F1 signals are sampled at the rising edge of SYSCLK in 8-bit mode.
F1 signal is sampled when XVRST is Low. When F1 is High, the internal sync generator is reset to the 1st field, and when F1 is Low, it is reset to the 2nd field. When XVRST is set at High, digital sync generator starts operation, and the sequence of 1st or 2nd field starts.

In 8bit mode

XVRST Timing (1st Field)



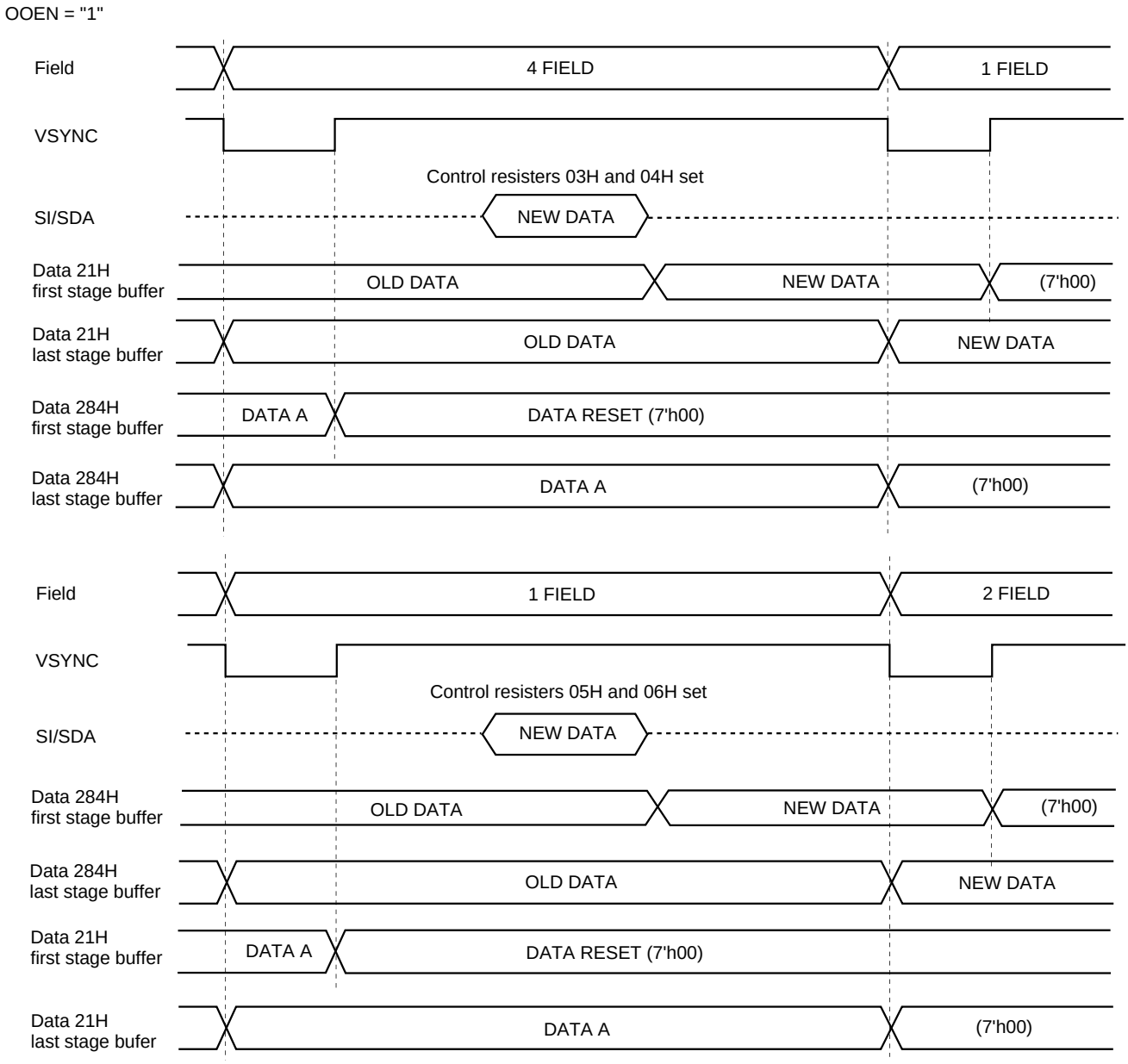
XVRST Timing (2nd Field)

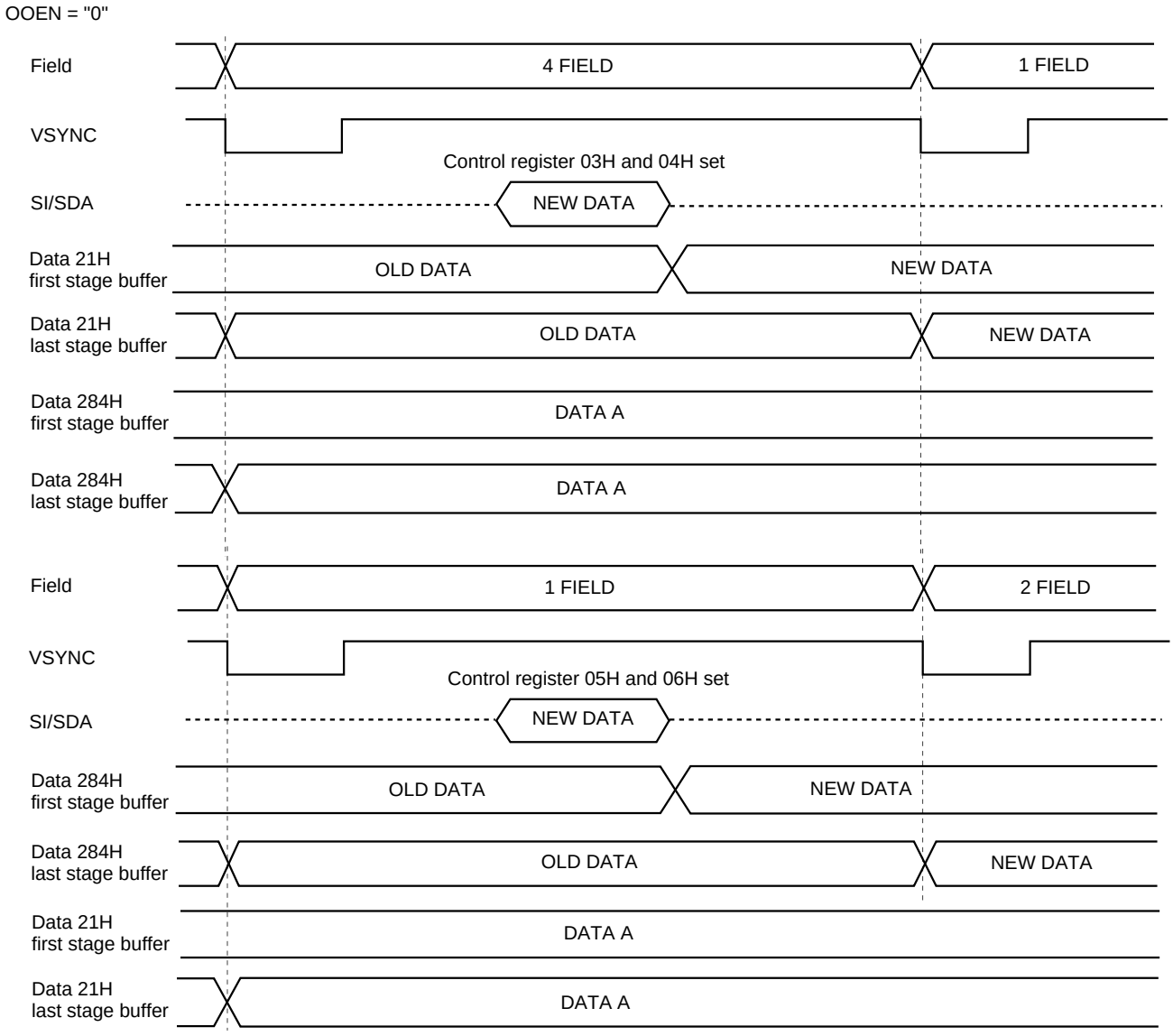


4. Closed Caption

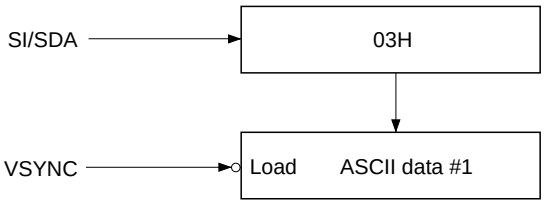
The CXD1913AQ supports closed caption encoding.
ASCII data for closed caption encodes line 21 and line 284 by adding parity bit to ASCII data (data #1 and data #2 for line 21, data #1 and data #2 for line 284) which is set up for control registers 03H, 04H, 05H and 06H. Control registers 03H to 06H are double-buffered and ASCII data which is set up by serial interface is synchronized with VSYNC.
ASCII data reset ON/OFF can be selected in synchronized with VSYNC by setting control register address 02H bit (OOEN).
When OOEN = "1", the first stage buffer ASCII data is cleared at the rising edge of the field in the next VSYNC where data renewed.
When OOEN = "0" (default), closed caption data is maintained.

Closed Caption Data Renewal Timing

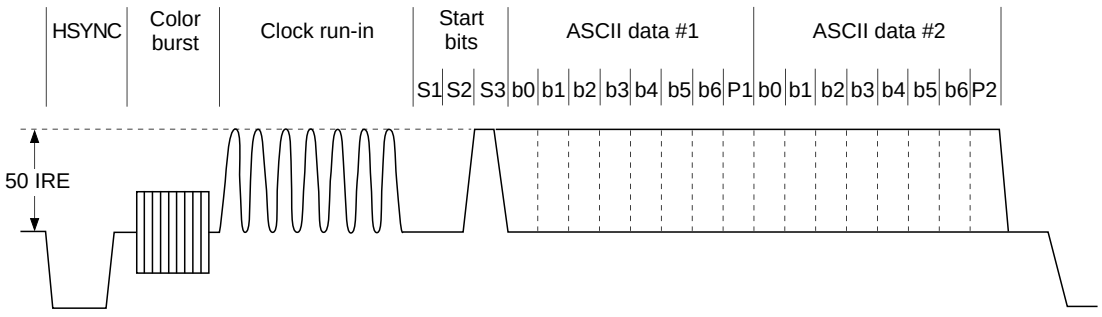




Double Buffer for Closed Caption



Closed Caption Signal Waveform



5. VBID (Video ID)

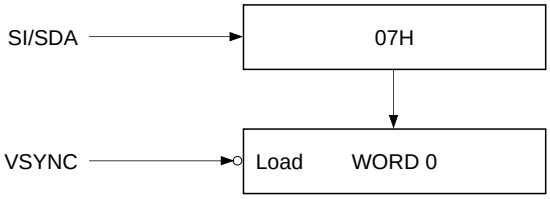
The CXD1913AQ supports Video ID (Provisional standard of EIAJ, CPX-1204) encording to perform aspect ratio identification. VBID is 14-bit data as shown in Table 5-1, and adding 6-bit CRCC results total 20 bits. This data is put on 20H and 283H in the vertical blanking period of NTSC video signal.
Encordes by adding CRCC to the VBID data which is set up for control registers 07H and 08H by serial interface. Control registers 07H and 08H are double-buffered and data which is set up by serial interface is synchronized with VSYNC.

Table 5-1

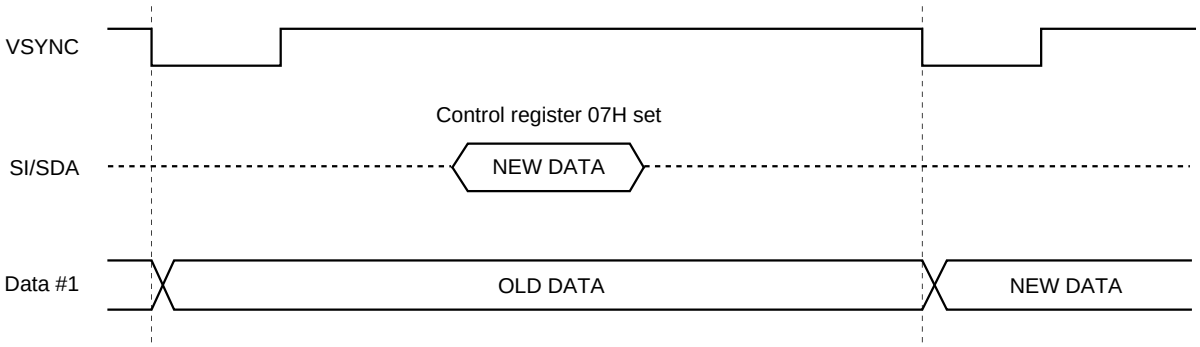
		bit-No.	Contents		
				"1"	"0"
WORD 0	A	1 2 3	Transmission aspect ratio Image display format Undefined	Full mode (16:9) Letter box	4:3 Normal
	B	4 5 6	Identification information for video and other signals (aural signal, etc.) which is propagated at the same with video		
WORD 1		4-bit width	Identification signal subordinated to WORD 0		
WORD 2		4-bit width	Identification signal and information subordinated to WORD 0		

(Provisional standard of EIAJ, CPX-1204)

VBID Double Buffer

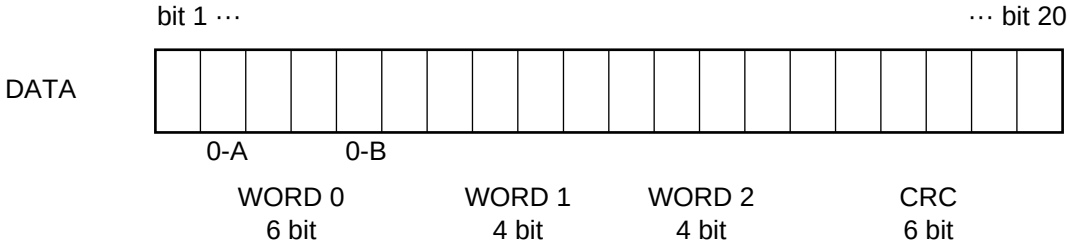


VBID Data Renewal Timing

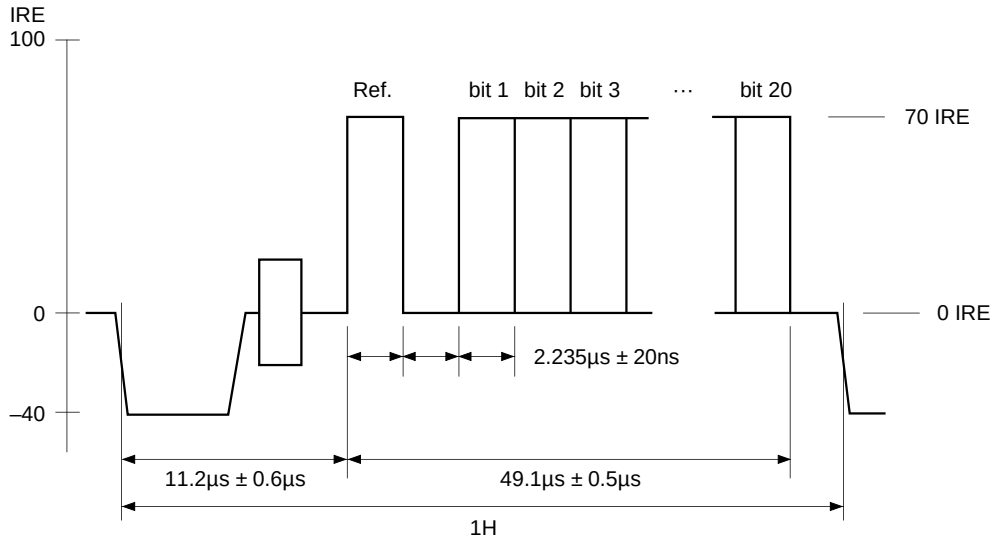


VBID Code Layout

20-bit data is configured with WORD 0 = 6 bits; its contents are WORD 0-A = 3 bits and WORD 0-B = 3 bits. And 20-bit data, with WORD 1 = 4 bits, WORD 2 = 4 bits and CRC = 6 bits.



VBID Signal Waveform

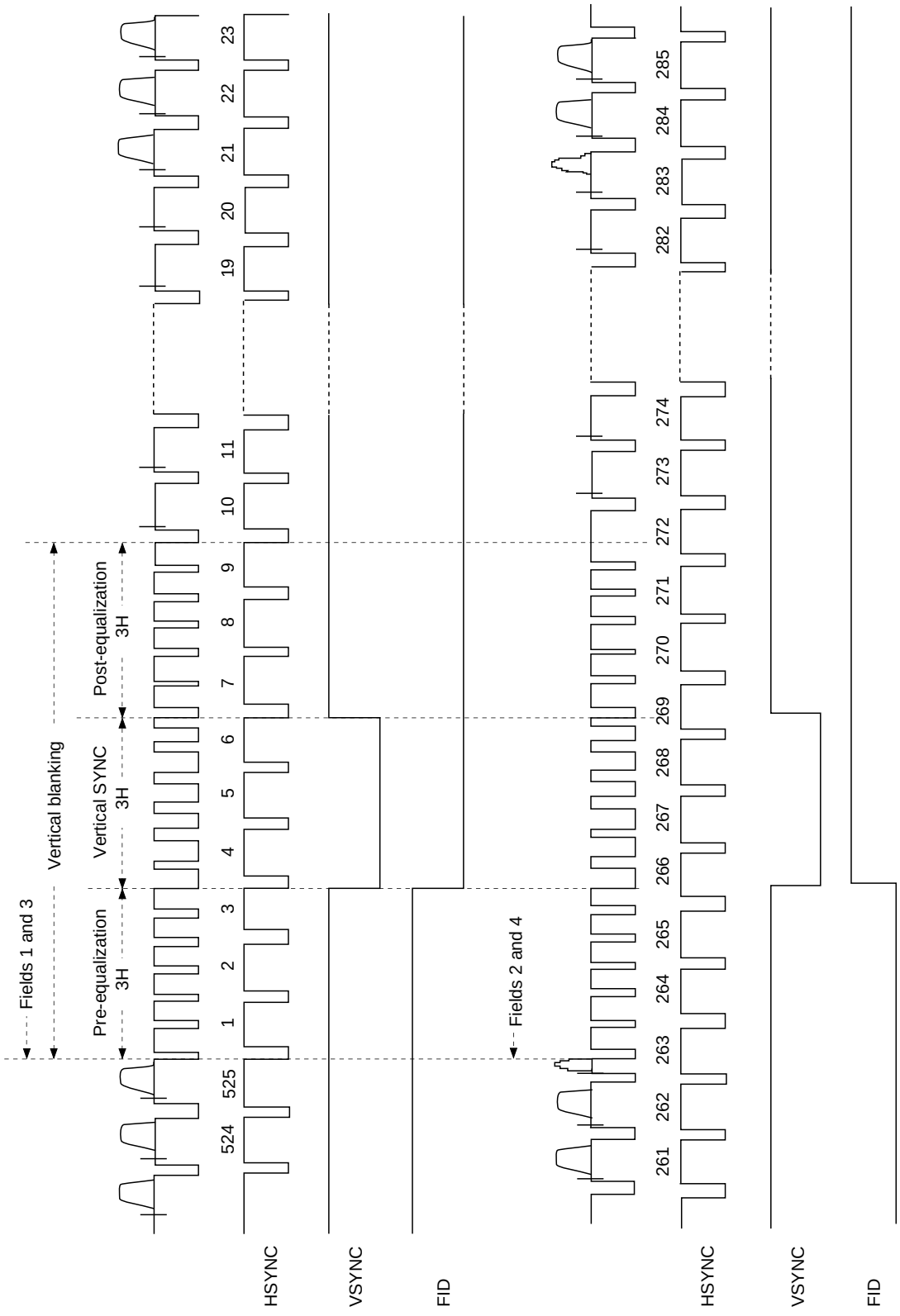


6. Interlace and Non interlace Supported

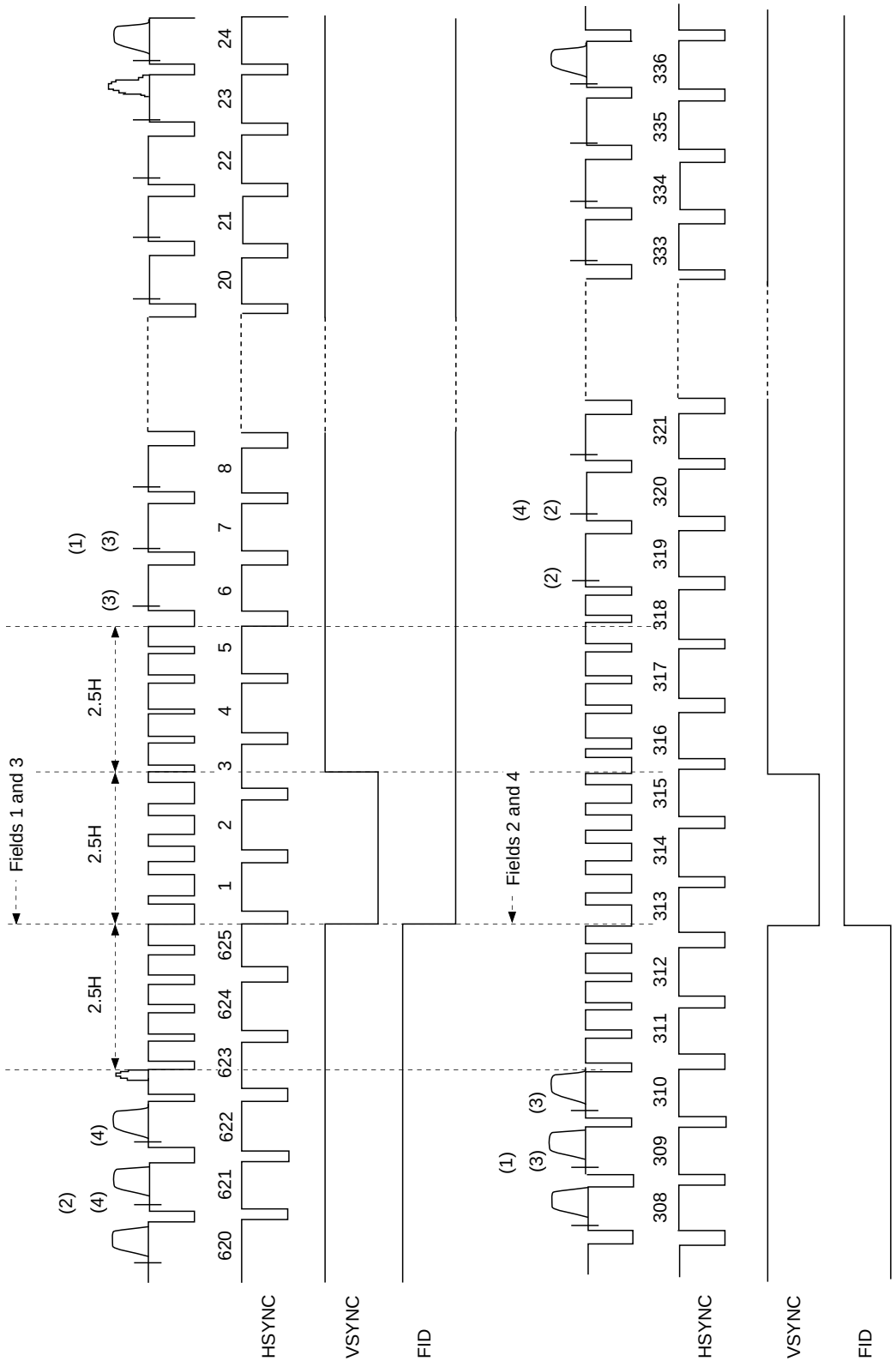
The CXD1913AQ can select interlace output or non interlace output by the set of Bit 1 (INTERLS) of control register address 01H.

Register set value INTERLS	Scan mode	Number of lines/field	
		NTSC	PAL
0	Non interlace	262	312
1	Interlace	262.5	312.5

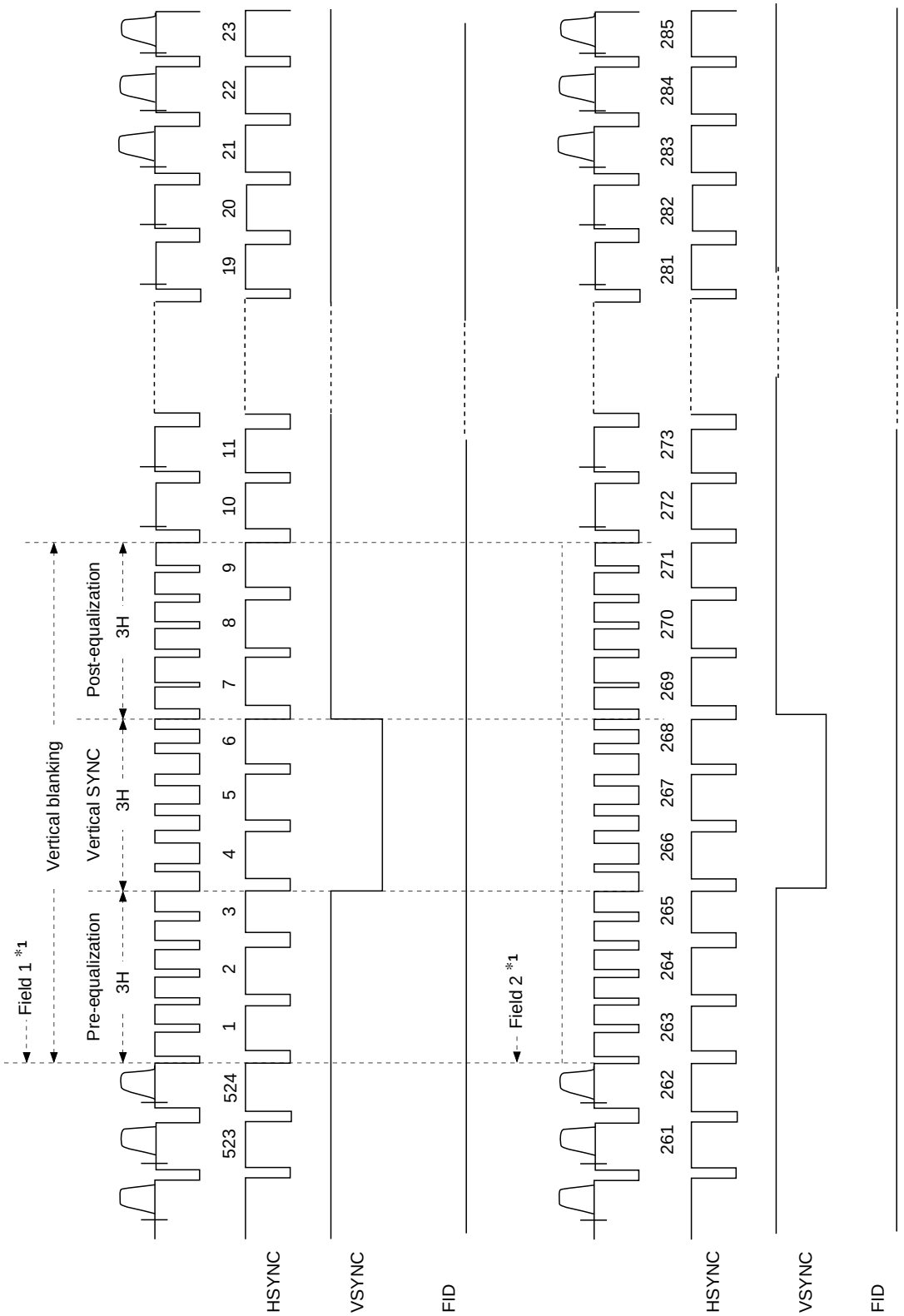
NTSC Vertical Interval (Interlace)



PAL Vertical Interval (Interlace)

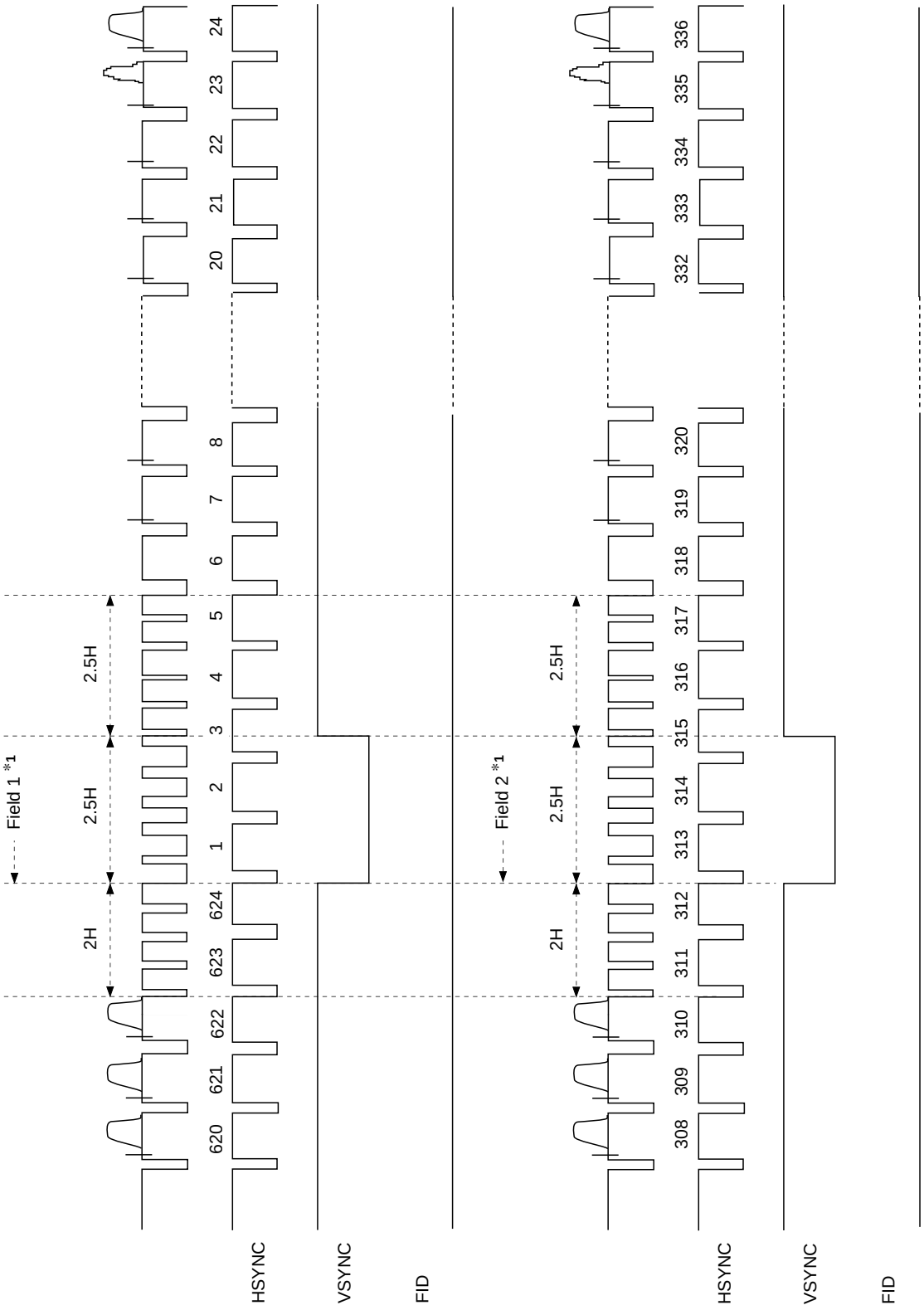


NTSC Vertical Interval (Non interlace)



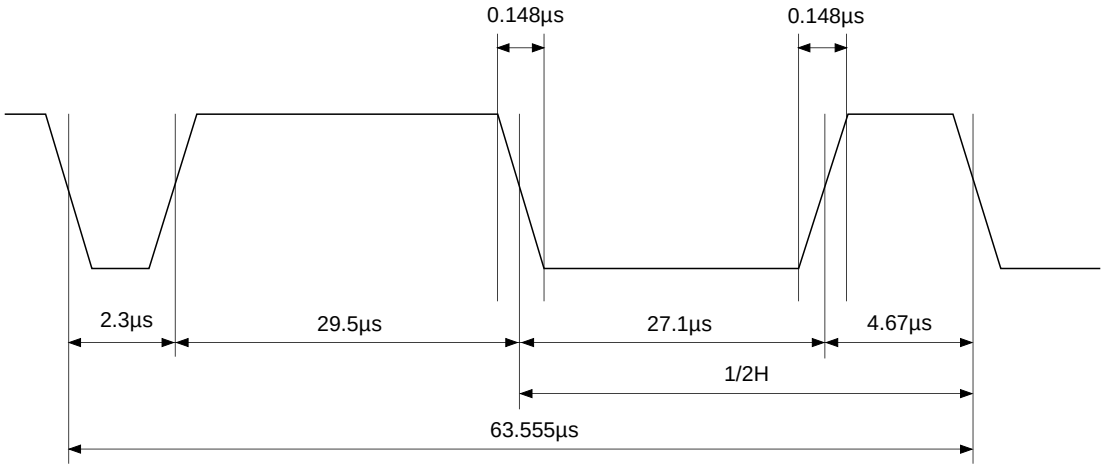
*1 "Field 1" or "Field 2" is used for the convenience of the description of frame.

PAL Vertical Interval (Non interlace)

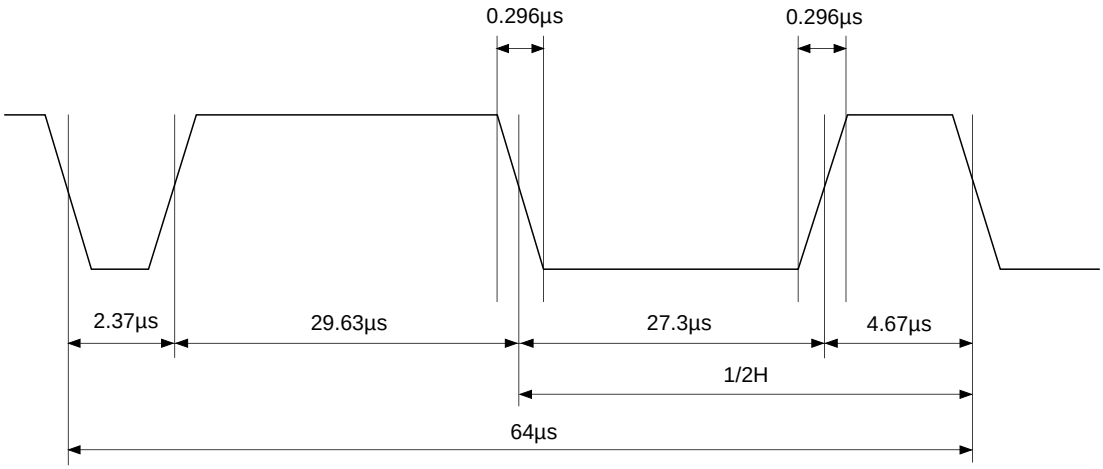


*1 "Field 1" or "Field 2" is used for the convenience of the description of frame.

Vertical Synchronization Timing



NTSC Equalizing & Synchronizing Pulses



PAL Equalizing & Synchronizing Pulses

Control Register Map

In case "0" or "1" is indicated on the map below, fix that value.

BIT

Function Selection #1

	7	6	5	4	3	2	1	0	
Address 00H	FIDS	MASK EN	PIX EN	1	CBAR	SET UP	0	ENC MODE	R/W

ENC MODE Encoding mode
0 : PAL encoding mode
1 : NTSC encoding mode (Default)

SET UP Set up enable
0 : Non set-up level, black = blanking level
1 : 7.5 IRE set-up level insertion (Default)

CBAR Color bar enable
0 : on-chip color bar output enable (ITU-R100% color bar)
1 : on-chip color bar output disable (Default)

When CBAR = "0", on-chip color bar generator is valid, and output is ITU-R100% color bar output.
When CBAR = "1", input pixel data is valid, and output obeys input pixel data.

PIX EN Pixel data enable
0 : Disable input pixel data
1 : Enable input pixel data (Default)

When input pixel data is disabled, output becomes blanking level or black level regardless of input PD0 to PD15.

MASK EN Mask enable
0 : When V-blanking, pixel data through
1 : When V-blanking, pixel data reject (Default)

When MASK EN = “0”, input pixel data during V-blanking interval are valid, and output obeys input pixel data.
When MASK EN = “1”, input pixel data during V-blanking interval are all invalid, and output becomes blanking level.

FIDS FID polarity select
0 : 1st field “H”, 2nd field “L”
1 : 1st field ”L“, 2nd field “H” (Default)

BIT

Function Selection #2

	7	6	5	4	3	2	1	0	
Address 01H	DAC MODE		0	PIF MODE	PIX TIME		INTERLS	FREE RUN	R/W

FREE RUN Free run
0 : SCH timing is reset every 4 fields for NTSC and every 8 fields for PAL (Default)
1 : No SCH timing reset

INTERLS Interlace
0 : Interlace (Default)
1 : Non interlace

PIX TIME Pixel input timing (See the diagram on Page 13.)
0 0 : #0 (Default)
0 1 : #1
1 0 : #2
1 1 : #3

PIF MODE Pixel input format
0 : 8-bit mode Multiplexed Y, Cb, Cr (4:2:2) (Default)
1 : 16-bit mode Y and multiplexed Cb, Cr (4:2:2)

DAC MODE DAC output activity
0 0 : Non-active
0 1 : Y-OUT and C-OUT active
1 0 : Comp-out active
1 1 : Both active (Default)

BIT

Function Selection #3

	7	6	5	4	3	2	1	0	
Address 02H	0	0	0	0	VBID	OOEN	CC MODE		R/W

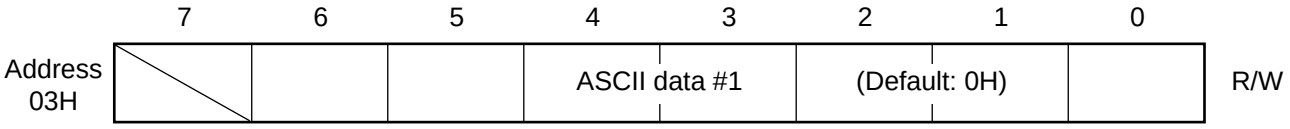
CC MODE Closed caption encoding mode
0 0 : Disable closed caption encoding (Default)
0 1 : Enable encoding in 1st field (Line 21)
1 0 : Enable encoding in 2nd field (Line 284)
1 1 : Enable encoding in both fields

OOEN Closed caption data reset
0 : Non reset (Default)
1 : Data reset synchronized with VSYNC

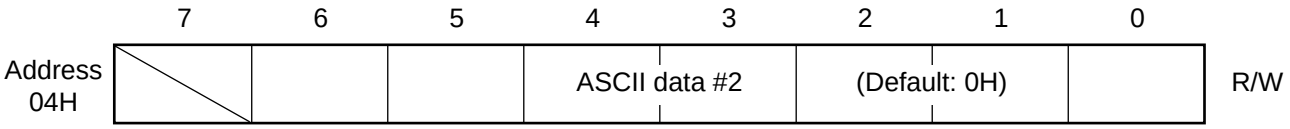
VBID VBID encode mode
0 : Disable encoding of VBID (Default)
1 : Enable encoding of VBID

BIT

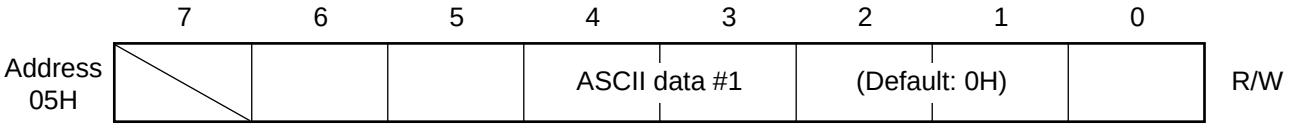
Closed Caption Character #1 for 21H



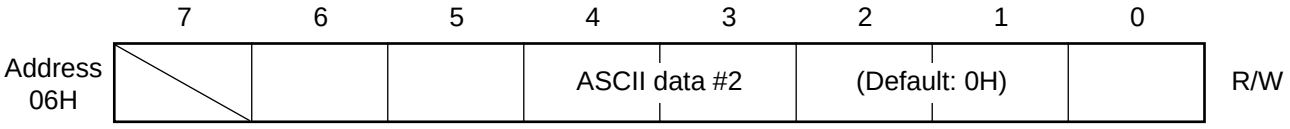
Closed Caption Character #2 for 21H



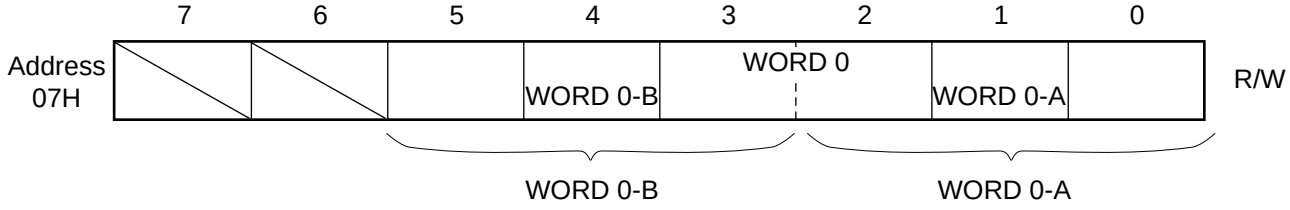
Closed Caption Character #1 for 284H



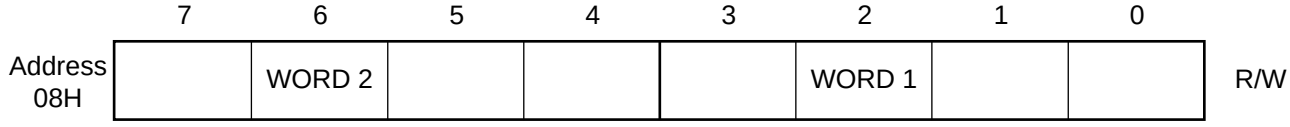
Closed Caption Character #2 for 284H



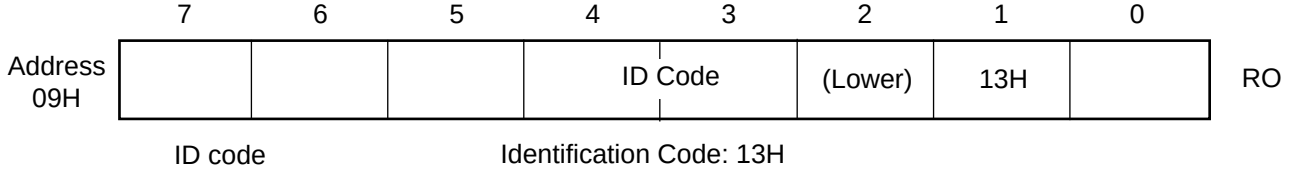
VBID#1



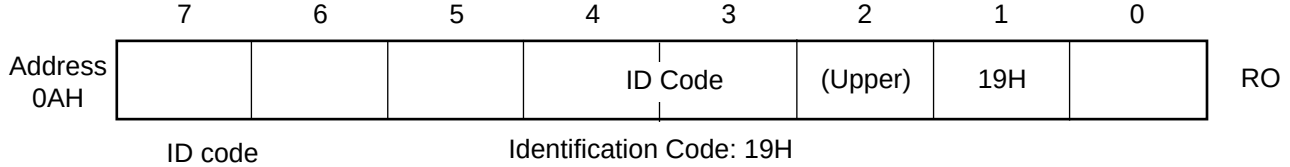
VBID#2



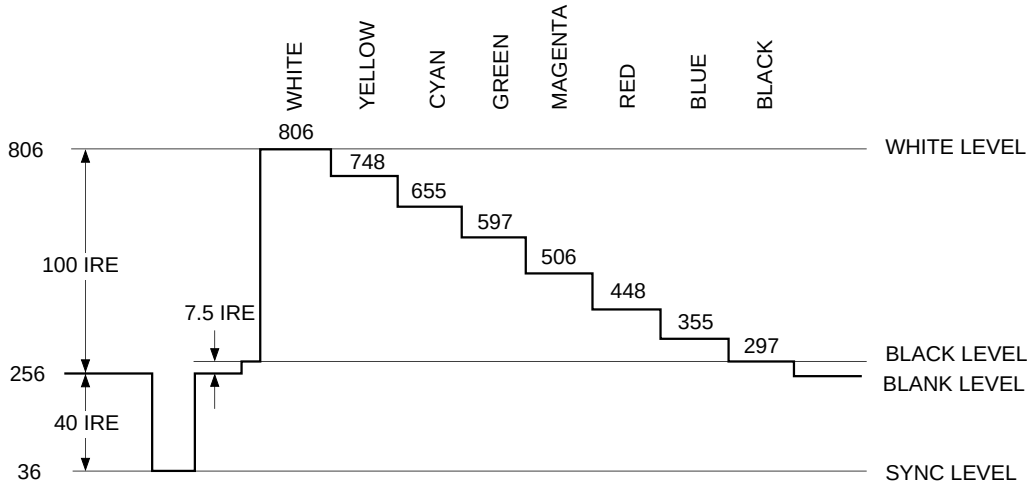
Device ID#1



Device ID#2

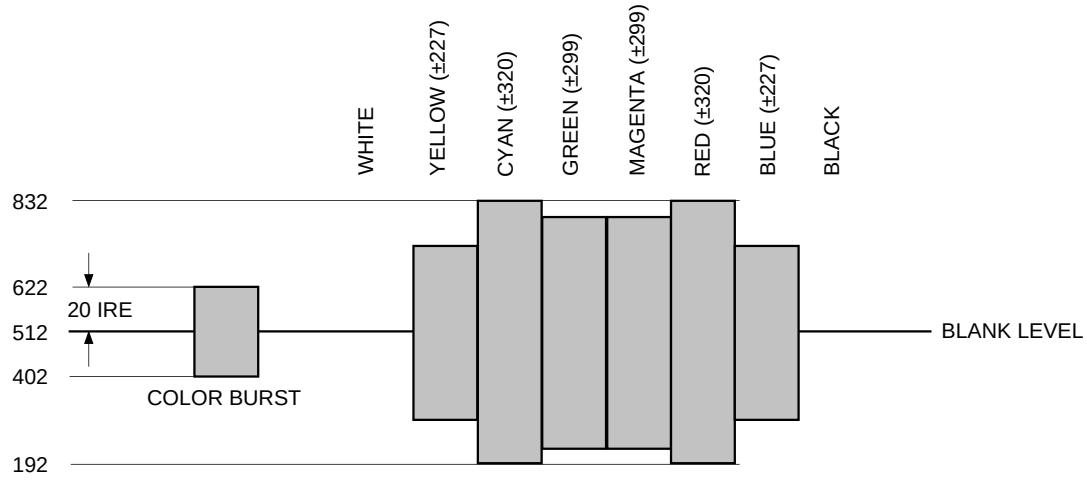


Video Timing



NTSC Y (Luminance) Video Output Waveform

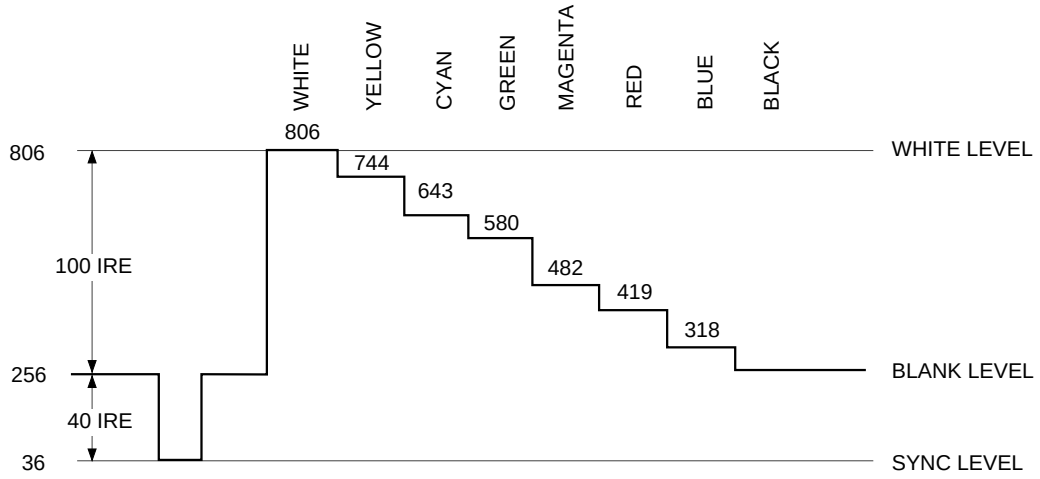
7.5 IRE SETUP



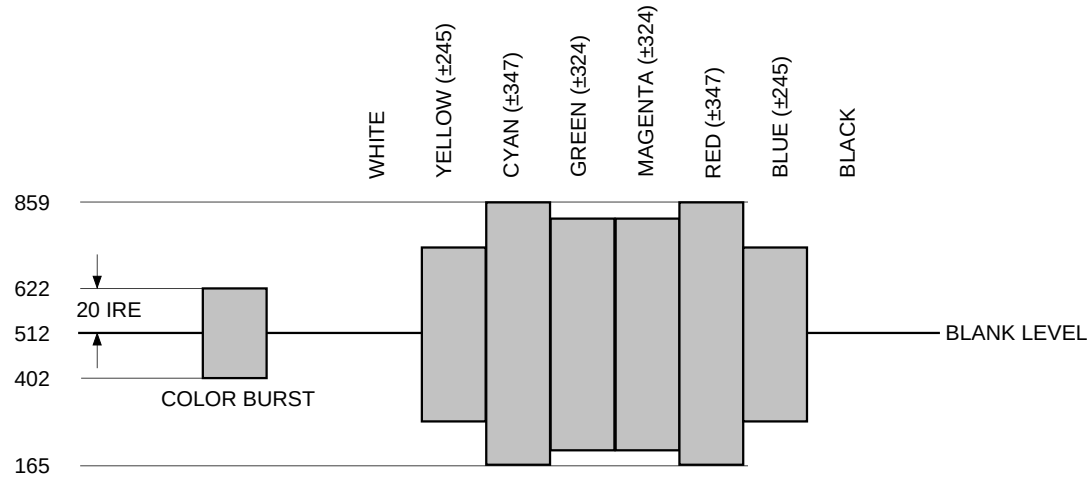
NTSC C (Chroma) Video Output Waveform

7.5 IRE SETUP

Video Timing

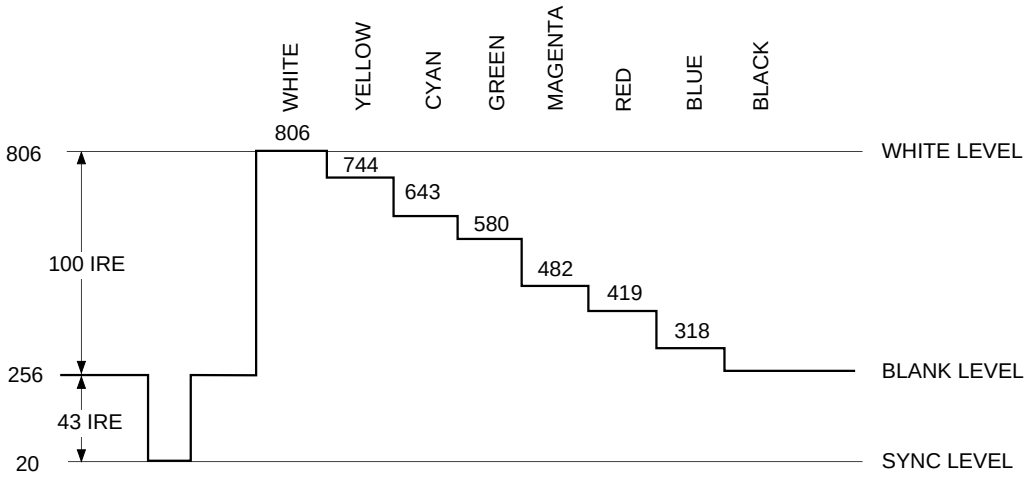


NTSC Y (Luminance) Video Output Waveform
No SETUP

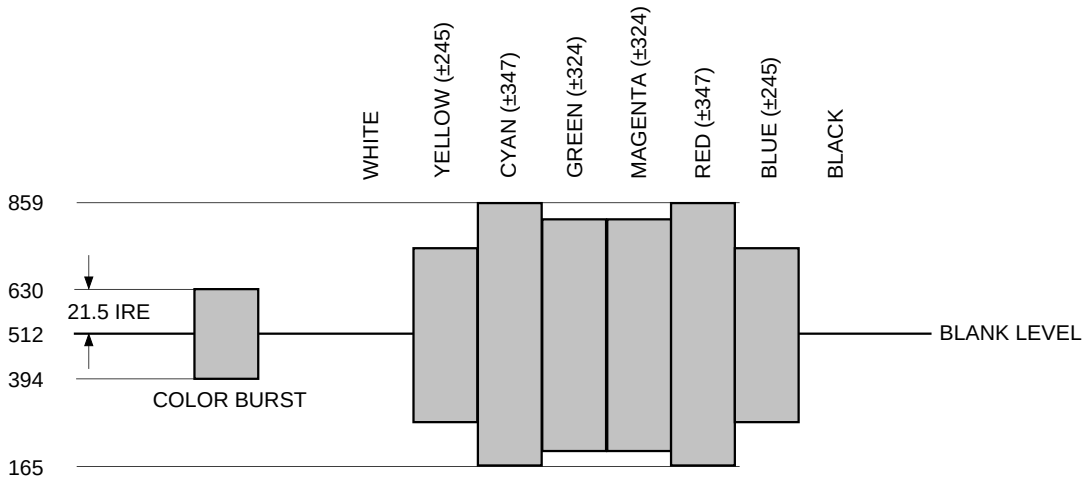


NTSC C (Chroma) Video Output Waveform
No SETUP

Video Timing

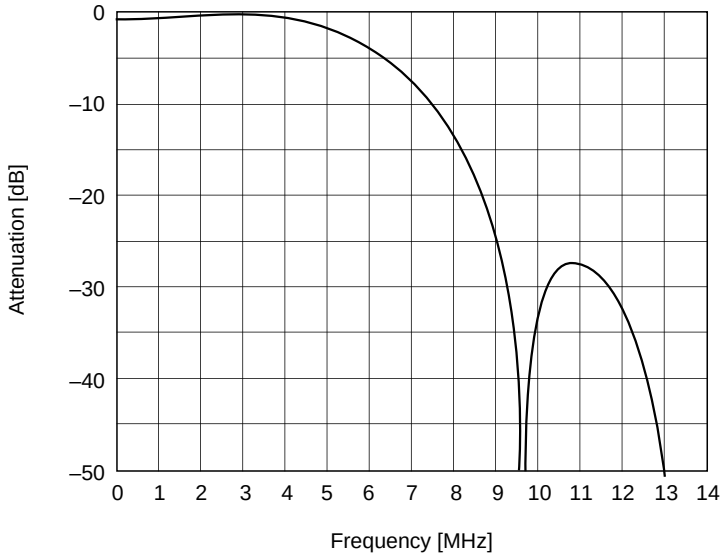


PAL Y (Luminance) Video Output Waveform

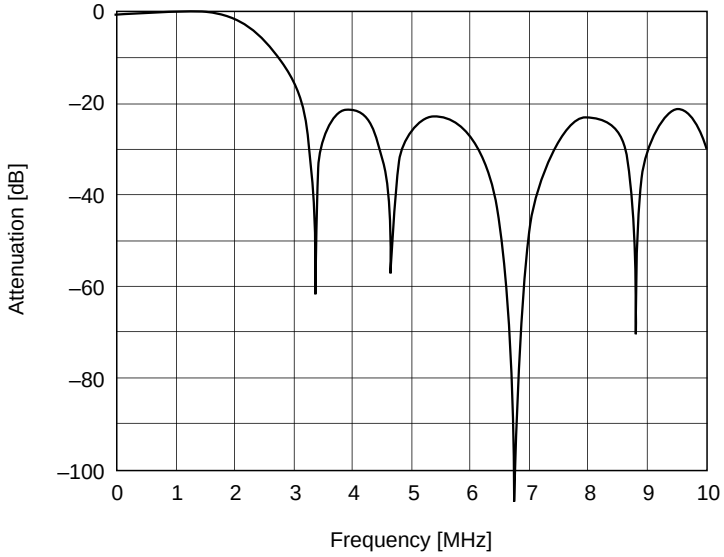


PAL C (Chroma) Video Output Waveform

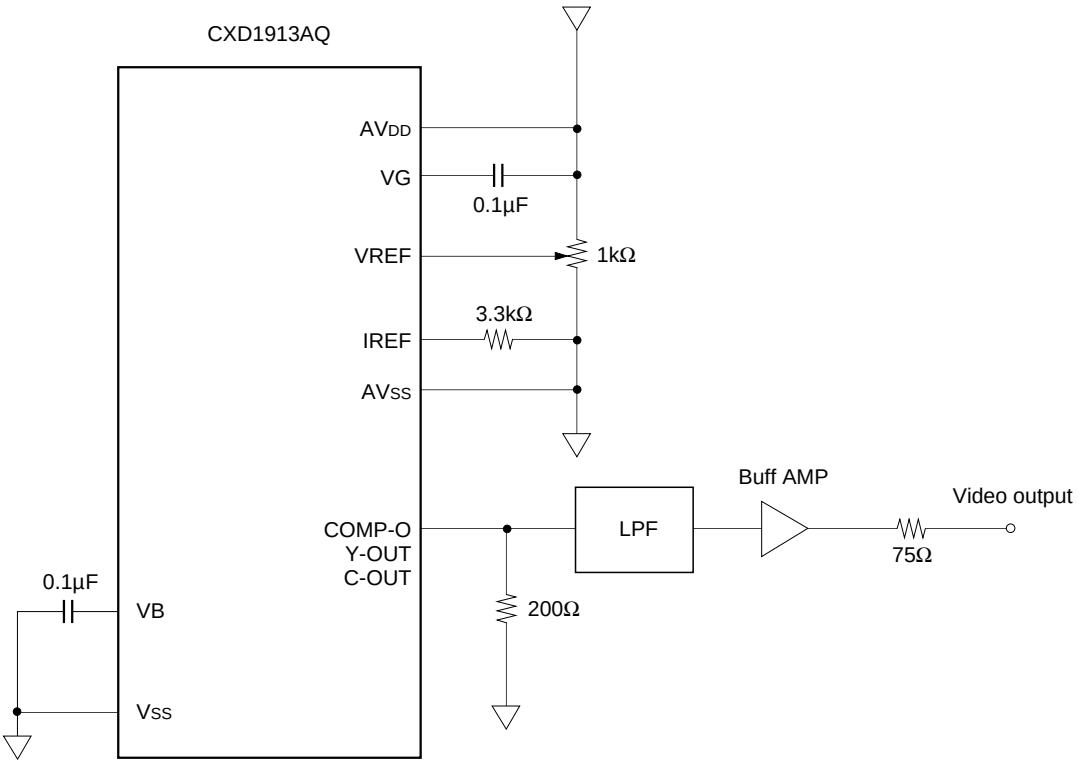
Interpolation Filter Characteristics



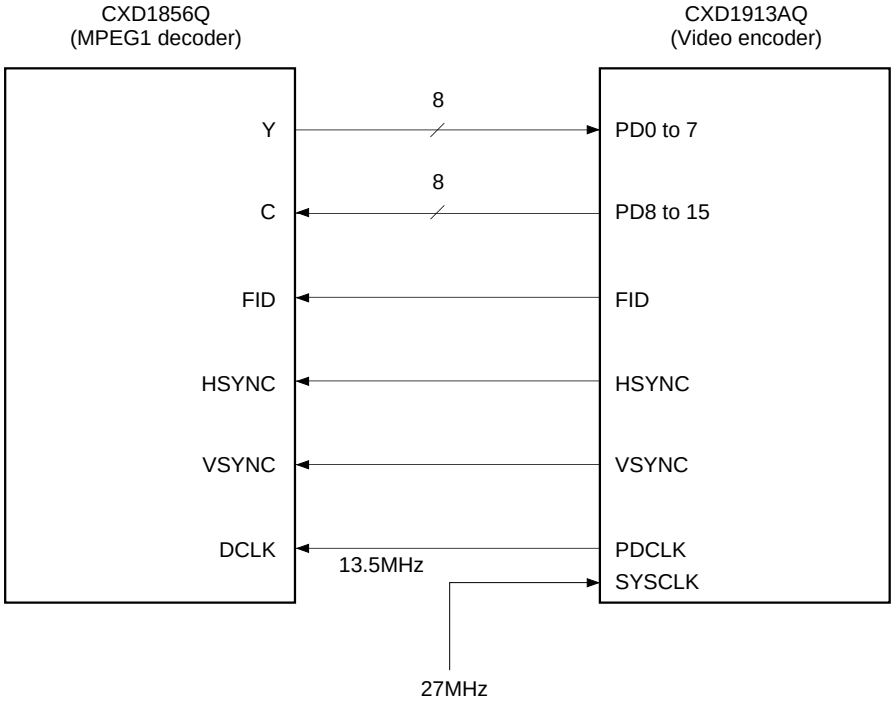
Chrominance Filter Characteristics



Application Circuit 1



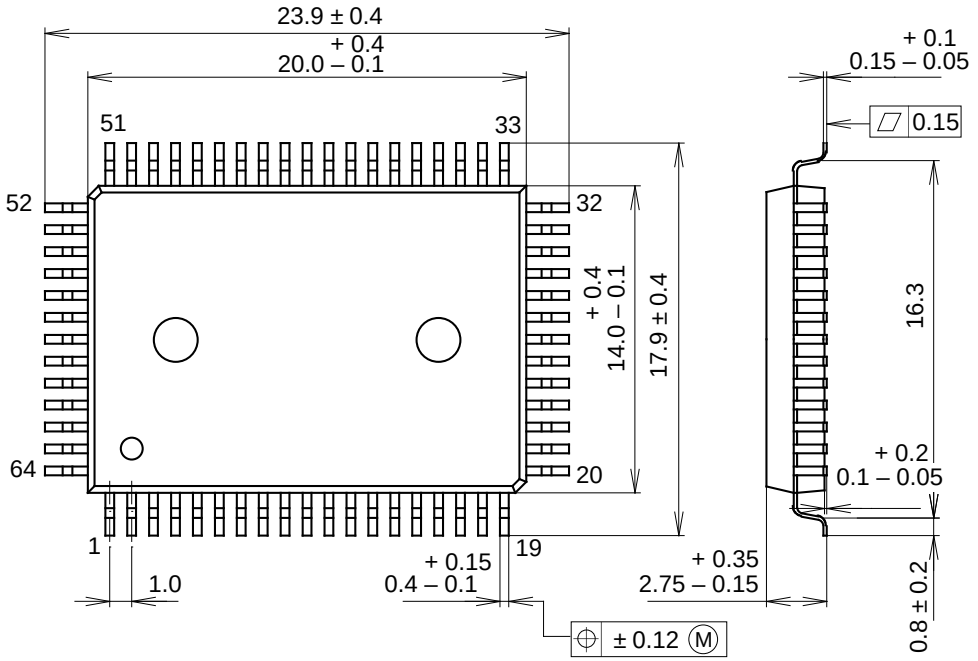
Application Circuit 2



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	∗QFP064-P-1420-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.5g