SONY

CXD1915R

Digital Video Encoder

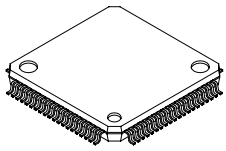
Description

The CXD1915R is a digital video encoder designed for DVDs, set top boxes, digital VCRs and other digital video equipment. This device accepts ITU-R601 format Y, Cb and Cr data and ITU-R656 format Y, Cb and Cr data, and the data are encoded to composite video and separate Y/C video (S-video) signals and converted to RGB/YUV signals.

Features

- NTSC, PAL, MPAL and 4.43NTSC encoding modes
- Composite video and separate Y/C video (S-video) signal output
- R, G, B/Y, U, V (BetaCam/SMPTE level) signal output
- 8/16-bit pixel data input modes
- 13.5Mpps pixel rate
- 12.27 and 14.75Mpps square pixel rates
- External synchronization using HSYNC, VSYNC and FID inputs, or internal synchronization
- Supports interlace and non-interlace modes
- On-chip 100% color bar generator
- OSD function
- ITU-R656 code signal EAV decoding
- Supports I^2C bus (400kHz) and Sony SIO
- Closed Caption (line 21, line 284) encoding
- VBID encoding
- WSS encoding
- 10-bit 6-channel DAC
- Macrovision Pay-Per-View copy protection system Rev. 7.1.L1*1
- Monolithic CMOS single 3.3V power supply
- 80-pin plastic LQFP

80 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to +7.0	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

(V_{SS} = 0V)

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.3 ± 0.3	V
• Input voltage	V_{IN}	V_{SS} to 5.5	V
• Operating temperature	Topr	0 to +70	°C

I/O Capacitance

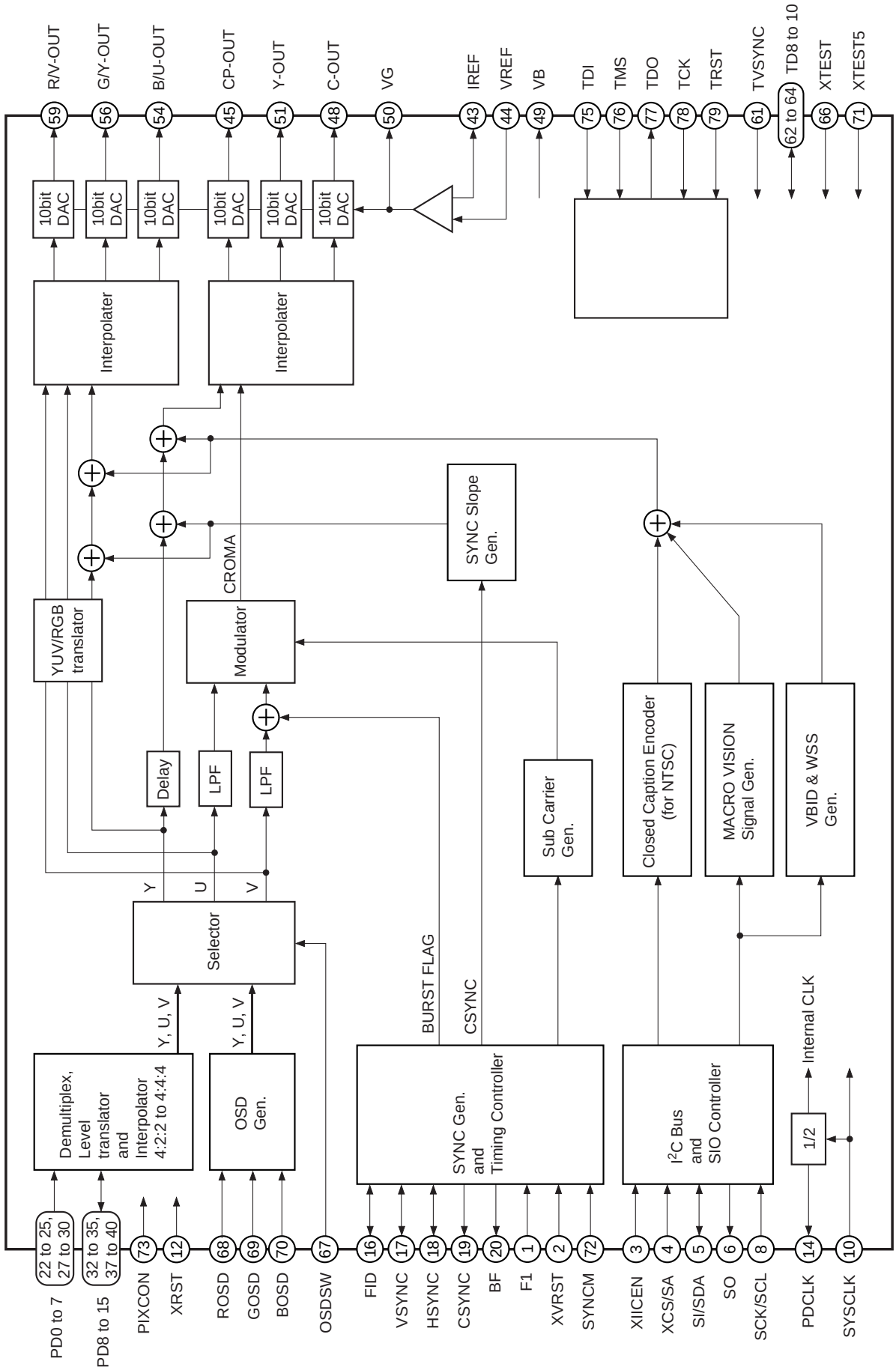
• Input capacitance	C_I	9 (Max.)	pF
• Output capacitance	C_O	11 (Max.)	pF

Note) Test conditions: V_{DD} = V_I = 0V, f_M = 1MHz

*1 This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anticopy process in the device is licensed by Macrovision for non-commercial home use only. Reverse engineering or disassembly is prohibited.

E99422-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	F1	I	Field ID input. This signal indicates the field ID when resetting the vertical sync. High indicates 1st field. Low indicates 2nd field.
2	XVRST	I	Vertical sync reset input in active Low. This pin is pulled up. This is used for synchronizing the phases of the external and internal vertical sync signals. When XVRST = Low, the internal digital sync generator is reset according to the F1 status.
3	XIICEN	I	Serial interface mode select input. This pin is pulled up. When XIICEN = Low, Pins 4, 5, 6 and 8 are I^2C bus mode. When XIICEN = High, Pins 4, 5, 6 and 8 are Sony SIO mode.
4	XCS/SA	I	This pin's function is selected by XIICEN (Pin 3). This pin is pulled up. When XIICEN = High, this pin is Sony SIO mode; XCS chip select input. When XIICEN = Low, this pin is I^2C bus mode; SA slave address select input signal which selects the I^2C bus slave address.
5	SI/SDA	I/O	This pin's function is selected by XIICEN (Pin 3). When XIICEN = High, this pin is Sony SIO mode; SI serial data input. When XIICEN = Low, this pin is I^2C bus mode; SDA input/output.
6	SO	O	This pin's function is selected by XIICEN (Pin 3). When XIICEN = High, this pin is Sony SIO mode; SO serial output. When XIICEN = Low, this pin is not used and output is high impedance.
7	$V_{SS}1$	—	Digital ground.
8	SCK/SCL	I	This pin's function is selected by XIICEN (Pin 3). When XIICEN = High, this pin is Sony SIO mode; SCK serial clock input. When XIICEN = Low, this pin is I2C bus mode; SCL input.
9	$V_{SS}2$	—	Digital ground.
10	SYSCLK	I	System clock input. To generate the correct subcarrier frequency, precise 27MHz is required.
11	$V_{SS}3$	—	Digital ground.
12	XRST	I	System reset input in active Low. Set to Low for 40 clocks (SYSCLK) or more during power-on reset.
13	$V_{SS}4$	—	Digital ground.
14	PDCLK	O	Pixel data clock signal output for 13.5MHz. A 13.5MHz signal frequency divided from the system clock (SYSCLK) is output and used as the clock signal when 16-bit pixel data is input.
15	$V_{DD}1$	—	Digital power supply.
16	FID	I/O	Field ID input/output. When SYNCM (Pin 72) = High, the CXD1915R is set to master mode and outputs as follows. When control register bit "FIDS" = "1": Low indicates 1st field and High indicates 2nd field. When control register bit "FIDS" = "0": High indicates 1st field and Low indicates 2nd field. When SYNCM (Pin 72) = Low, the CXD1915R is set to slave mode and this pin becomes the field ID input.

Pin No.	Symbol	I/O	Description
17	VSYNC	I/O	Vertical sync signal input/output. When SYNCM (Pin 72) = High, this pin is the vertical sync signal output. When SYNCM = Low, this pin is the vertical sync signal input, and the falling edge is detected during the 1st field to reset the internal circuits.
18	HSYNC	I/O	Horizontal sync signal input/output. When SYNCM (Pin 72) = High, this pin is the horizontal sync signal output. When SYNCM = Low, this pin is the horizontal sync signal input, and the falling edge is detected during the 1st field to reset the internal circuits.
19	CSYNC	O	Composite sync output when using RGB output.
20	BF	O	Burst flag output. The burst flag is synchronized with the composite video signal (CP-OUT) and indicates its color burst signal position.
21	$V_{SS}5$	—	Digital ground.
22	PD0	I	8-bit pixel data inputs, or lower 8-bit pixel data inputs when 16-bit pixel data is input. [PD0 to PD7] When control register bit "PIF MODE" = "0", these are multiplexed Y, Cb, and Cr signal inputs. When control register bit "PIF MODE" = "1", these are Y signal inputs.
23	PD1	I	
24	PD2	I	
25	PD3	I	
26	$V_{DD}2$	—	Digital power supply.
27	PD4	I	8-bit pixel data inputs, or lower 8-bit pixel data inputs when 16-bit pixel data is input. [PD0 to PD7] When control register bit "PIF MODE" = "0", these are multiplexed Y, Cb, and Cr signal inputs. When control register bit "PIF MODE" = "1", these are Y signal inputs.
28	PD5	I	
29	PD6	I	
30	PD7	I	
31	$V_{SS}6$	—	Digital ground.
32	PD8/TD0	I/O	Upper 8-bit pixel data inputs when 16-bit pixel data is input/test data bus. [PD8 to PD15] When control register bit "PIF MODE" = "0", these inputs are not used. When control register bit "PIF MODE" = "1", these are multiplexed Cb and Cr signal inputs. In test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
33	PD9/TD1	I/O	
34	PD10/TD2	I/O	
35	PD11/TD3	I/O	
36	$V_{SS}7$	—	Digital ground.
37	PD12/TD4	I/O	Upper 8-bit pixel data inputs when 16-bit pixel data is input/test data bus. [PD8 to PD15] When control register bit "PIF MODE" = "0", these inputs are not used. When control register bit "PIF MODE" = "1", these are multiplexed Cb and Cr signal inputs. In test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
38	PD13/TD5	I/O	
39	PD14/TD6	I/O	
40	PD15/TD7	I/O	
41	$V_{DD}3$	—	Digital power supply.
42	NC	—	Not connected inside the IC.
43	IREF	O	DAC reference current output. Connect resistance "16R" which is 16 times output resistance "R".
44	VREF	I	DAC reference voltage input. Sets the DAC output full-scale width.
45	CP-OUT	O	10-bit DAC output. This pin outputs the composite signal.

Pin No.	Symbol	I/O	Description
46	$AV_{DD}1$	—	Analog power supply.
47	$AV_{SS}1$	—	Analog ground.
48	C-OUT	O	10-bit DAC output. This pin outputs the chroma (C) signal.
49	VB	O	Connect to ground via a capacitor of approximately 0.1µF.
50	VG	O	Connect to analog power supply via a capacitor of approximately 0.1µF.
51	Y-OUT	O	10-bit DAC output. This pin outputs the luminance (Y) signal.
52	$AV_{DD}2$	—	Analog power supply.
53	$AV_{SS}2$	—	Analog ground.
54	B-OUT	O	10-bit DAC output. This pin outputs the B and U signals.
55	$AV_{SS}4$	—	Analog ground.
56	G-OUT	O	10-bit DAC output. This pin outputs the G and Y signals.
57	$AV_{DD}3$	—	Analog power supply.
58	$AV_{SS}3$	—	Analog ground.
59	R-OUT	O	10-bit DAC output. This pin outputs the R and V signals.
60	$V_{SS}8$	—	Digital ground.
61	TVSYNC	I	Test pin. This pin is pulled up. Normally this pin should be open.
62	TD8	I/O	Test data inputs/outputs. These pins should be open. In test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
63	TD9	I/O	
64	TD10	I/O	
65	$V_{DD}4$	—	Digital power supply.
66	XTEST	I	Test mode control. This pin is pulled up. Normally this pin should be open.
67	OSDSW/ XTEST1	I	These pins are pulled up. The functions of these pins are selected by XTEST (Pin 66). When XTEST = High, these are OSD data inputs. When XTEST = Low, these are test mode control inputs. The test mode is available only for the device vendor.
68	ROSD/ XTEST2	I	
69	GOSD/ XTEST3	I	
70	BOSD/ XTEST4	I	
71	XTEST5	I	Test pin. This pin is pulled up. Normally this pin should be open.
72	SYNCM	I	Master/slave switching. This pin is pulled up. When SYNCM = High, the CXD1915R is set to master mode. When SYNCM = Low, the CXD1915R is set to slave mode.
73	PIXCON	I	Control register bit "PIX_EN" default value control. This pin is pulled up.
74	$V_{SS}9$	—	Digital ground.
75	TDI	I	Test mode control input. This pin is pulled up.

Pin No.	Symbol	I/O	Description
76	TMS	I	Test mode control input. This pin is pulled up.
77	TDO	O	Test output. This pin should be open.
78	TCK	I	Test mode control input. Fix to High.
79	TRST	I	Test mode reset input. Set to Low for 40 clocks (SYSCLK) or more during power-on reset.
80	$V_{DD}5$	—	Digital power supply.

Electrical Characteristics

DC Characteristics

(Ta = 0 to +70°C, V_{SS} = 0V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Measurement pins
Input High voltage	$V_{IH}1$	V_{DD} = 3.3 ± 0.3V	0.7V_{DD}		*8	V	*1
Input Low voltage	$V_{IL}1$	V_{DD} = 3.3 ± 0.3V			0.2V_{DD}	V	*1
Input High voltage	$V_{IH}2$	V_{DD} = 3.3 ± 0.3V	0.7V_{DD}		*8	V	*2
Input Low voltage	$V_{IL}2$	V_{DD} = 3.3 ± 0.3V			0.3V_{DD}	V	*2
Output High voltage	$V_{OH}1$	I_{OH} = –8.0mA V_{DD} = 3.3 ± 0.3V	V_{DD} – 0.4			V	*3
Output Low voltage	$V_{OL}1$	I_{OL} = 8.0mA V_{DD} = 3.3 ± 0.3V			0.4	V	*3
Output High voltage	$V_{OH}2$	I_{OH} = –4.0mA V_{DD} = 3.3 ± 0.3V	V_{DD} – 0.4			V	*4
Output Low voltage	$V_{OL}2$	I_{OL} = 4.0mA V_{DD} = 3.3 ± 0.3V			0.4	V	*4
Output High voltage	$V_{OH}3$	I_{OH} = –2.0mA V_{DD} = 3.3 ± 0.3V	2.4			V	*5
Output Low voltage	$V_{OL}3$	I_{OL} = 4.0mA V_{DD} = 3.3 ± 0.3V			0.4	V	*5
Input leak current	$I_{IL}1$	V_I = 0V V_{DD} = 3.3 ± 0.3V	–240	–100	–40	µA	*6
Input leak current	I_I2	V_I = 0 to 5.5V V_{DD} = 3.3 ± 0.3V	–40		40	µA	*7
Supply current	I_{DD}	V_{DD} = 3.3 ± 0.3V			35*9	mA	

Notes:

*1 F1, XVRST, XIICEN, XCS/SA, SYSCLK, XRST, FID, VSYNC, HSYNC, PD0 to PD15, TVSYNC, TD8 to TD10, XTEST, OSDSW, ROSD, GOSD, BOSD, XTEST5, SYNCM, PIXCON, TDI, TMS, TCK, TRST

*2 SI/SDA, SCK/SCL

*3 SO, PDCLK, CSYNC, BF

*4 TDO

*5 FID, VSYNC, HSYNC, TD0 to TD10

*6 XVRST, XIICEN, XCS, TVSYNC, XTEST, OSDSW, ROSD, GOSD, BOSD, XTEST5, SYNCM, PIXCON, TDI, TMS

*7 F1, SI/SDA, SCK/SCL, SYSCLK, XRST, FID, VSYNC, HSYNC, PD0 to PD15, TD8 to TD10, TCK, TRST

*8 The CXD1915R supports input from 5V devices.

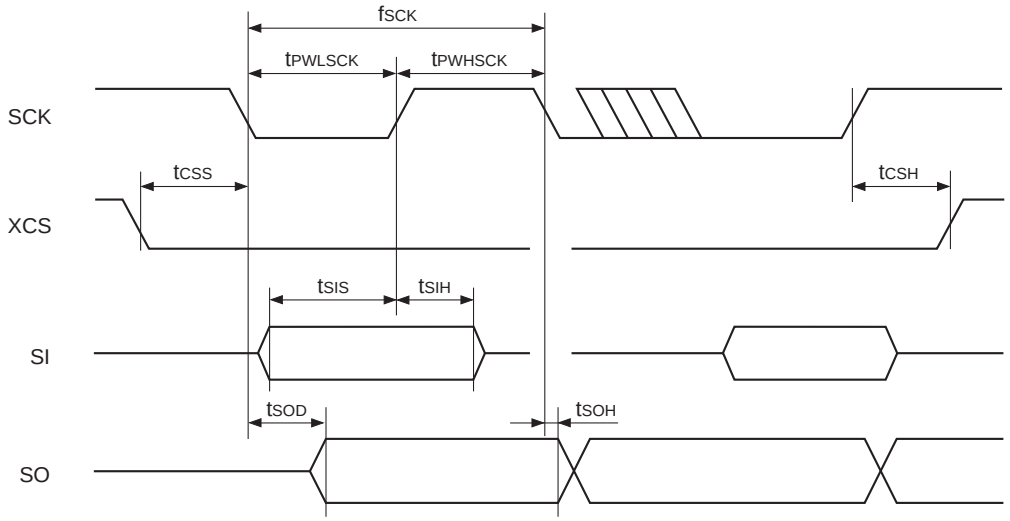
*9 Not including analog current

DAC Characteristics (AV_{DD} = 3.3V, R = 200Ω, V_{REF} = 1.35V, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Linearity error	E_L		–2.4		2.4	LSB
Differential linearity error	E_D		–0.9		0.9	LSB
Output full-scale current	I_{FS}		6.25	6.75	7.25	mA
Output offset voltage	V_{OS}				2	mV
Output full-scale voltage	V_{FS}		1.20	1.35	1.50	V
Precision guaranteed output voltage range	V_{OC}		1.20	1.35	1.50	V

AC Characteristics

1. Serial port interface

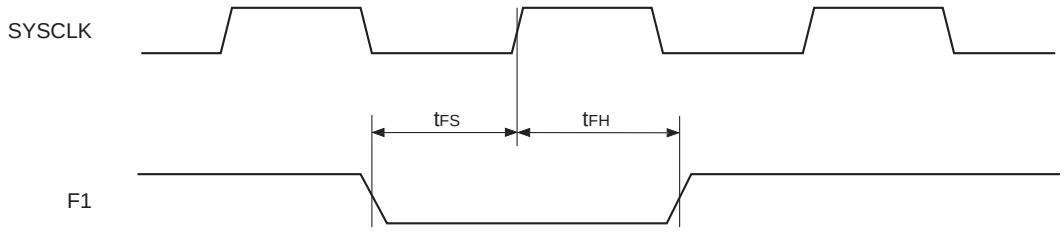


(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock rate	f_{SCK}	DC		3	MHz
SCK pulse width Low	t_{PWLSCK}	100			ns
SCK pulse width High	t_{PWHSCK}	100			ns
Chip select setup time to SCK	t_{CSS}	150			ns
Chip select hold time to SCK	t_{CSH}	150			ns
Serial input setup time to SCK	t_{SIS}	50			ns
Serial input hold time to SCK	t_{SIH}	10			ns
Serial output delay time from SCK	t_{SOD}*			30	ns
Serial output hold time from SCK	t_{SOH}*	3			ns

* C_L = 35pF

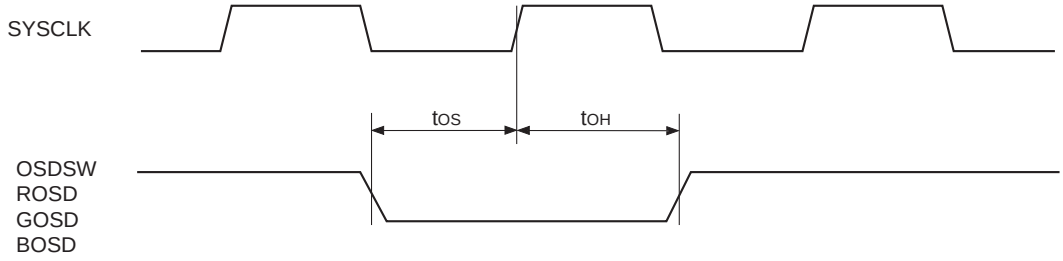
2. F1



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
F1 setup time to SYSCLK	t_{FS}	10			ns
F1 hold time to SYSCLK	t_{FH}	0			ns

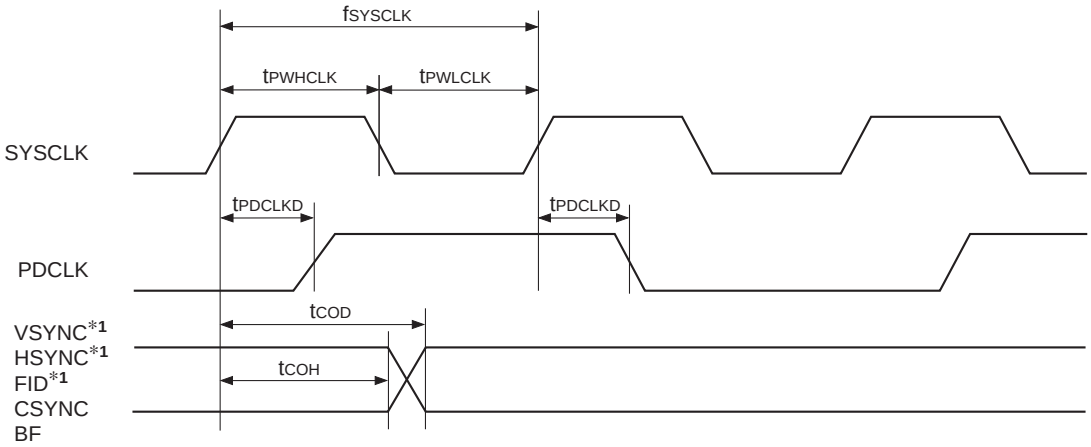
3. OSDSW, ROSD, GOSD, BOSD



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
OSD setup time to SYSCLK	t_{OS}	10			ns
OSD hold time to SYSCLK	t_{OH}	0			ns

4. SYSCLK, PDCLK, BF, CSYNC, HSYNC, VSYNC, FID



*1 In master mode

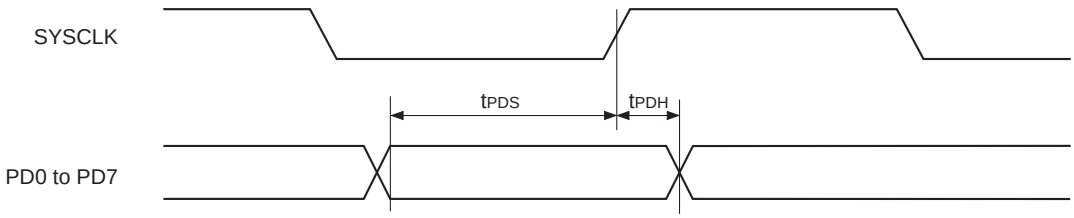
(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SYSCLK clock rate	f_{SYSCLK}		27		MHz
SYSCLK pulse width Low	t_{PWLCLK}	11			ns
SYSCLK pulse width High	t_{PWHCLK}	11			ns
PDCLK delay time from SYSCLK	t_{PDCLKD}*			20	ns
Control output delay time from SYSCLK	t_{COD}*			26	ns
Control output hold time from SYSCLK	t_{COH}*	3			ns

* C_L = 35pF

5. 8-bit mode

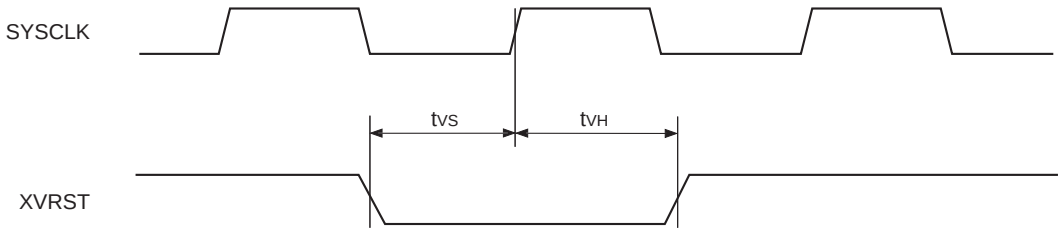
(1) Pixel data interface



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to SYSCLK	t_{PDS}	11			ns
Pixel data hold time to SYSCLK	t_{PDH}	0			ns

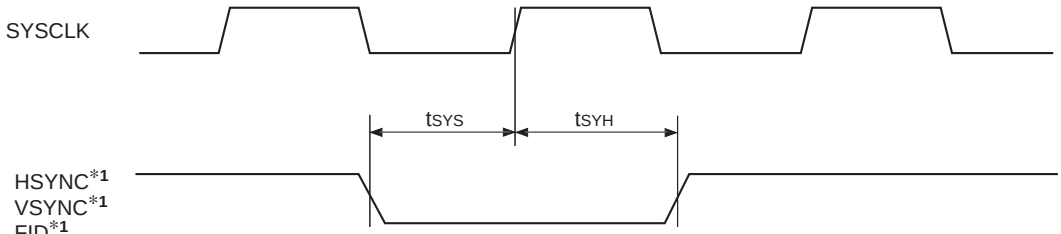
(2) XVRST



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
XVRST setup time to SYSCLK	t_{VS}	10			ns
XVRST hold time to SYSCLK	t_{VH}	0			ns

(3) HSYNC, VSYNC, FID



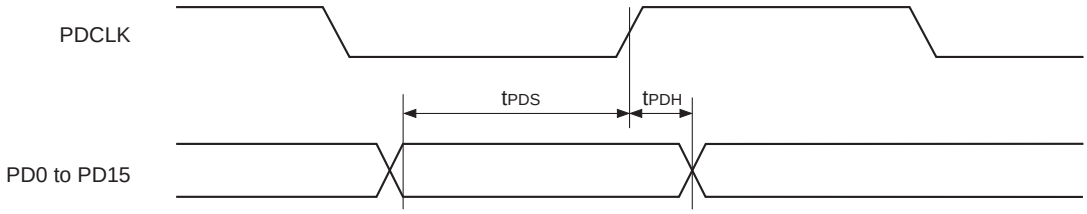
*1 In slave mode

(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Sync signal setup time to SYSCLK	t_{SYS}	10			ns
Sync signal hold time to SYSCLK	t_{SYH}	0			ns

6. 16-bit mode

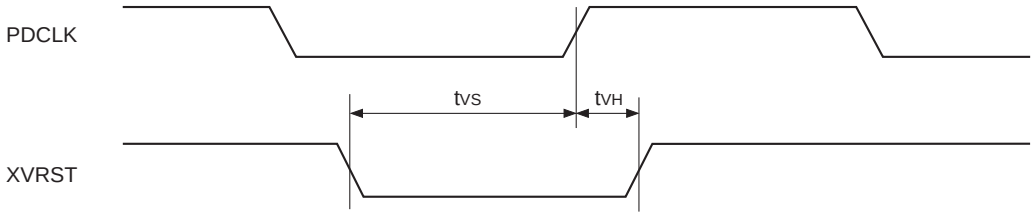
(1) Pixel data interface



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to PDCLK	t_{PDS}	23			ns
Pixel data hold time to PDCLK	t_{PDH}	0			ns

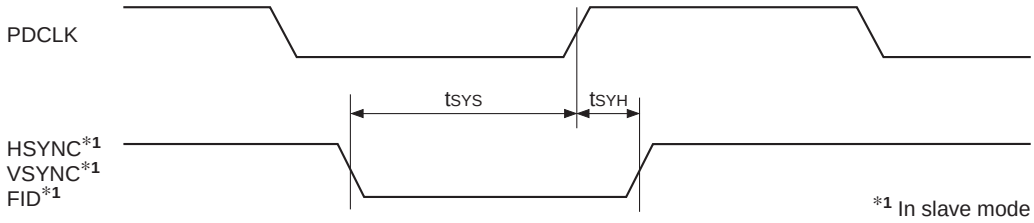
(2) XVRST



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
XVRST setup time to PDCLK	t_{VS}	20			ns
XVRST hold time to PDCLK	t_{VH}	0			ns

(3) HSYNC, VSYNC, FID



(Ta = 0 to +70°C, V_{DD} = 3.3 ± 0.3V, Vss = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Sync signal setup time to PDCLK	t_{SYS}	20			ns
Sync signal hold time to PDCLK	t_{SYH}	0			ns

Description of Functions

The CXD1915R converts digital parallel data (ITU-R601 Y, Cb, Cr) into analog TV signals in NTSC (RS170A) or PAL (ITU-R624; B, G, H, I) format.
The CXD1915R first receives image data in 8-bit parallel form (multiplexed Y, Cb, and Cr data), or in 16-bit parallel form (8-bit Y and 8-bit multiplexed Cb and Cr data). After demultiplexing, it converts the Cb and Cr signals into the U and V signals, respectively, interpolates 4:2:2 to 4:4:4, and then modulates the signals with the digital subcarrier inside the CXD1915R to create the chroma (C) signal.
The Y and chroma (C) signals are oversampled at double speed to reduce SIN (X)/(X) roll-off, and then added to become the digital composite signal.
The 10-bit DAC converts the digital composite, Y/C, U, V, and RGB signals into analog signals.

1. Pixel input format

The pixel input format is selected according to the value of bit 4 (PIF MODE) of control register address 01H as shown in Table 1-1 below.
When "PIF MODE" is "0", the image data (multiplexed Y, Cb, and Cr data) input from PD0 to PD7 are sampled at the rising edge of SYSCLK as shown in the chart on the following page. When "PIF MODE" is "1", the image data (PD0 to PD7: Y data, PD8 to PD15: multiplexed Cb and Cr data) input from PD0 to PD15 are sampled at the rising edge of PDCLK.

PIF Mode	PD15 to 8	PD7 to 0
0 (8 bit mode)	NA	Y/Cb/Cr
1 (16 bit mode)	Cb/Cr	Y

Table 1-1

Also, the pixel input data timing is determined according to bits 3 and 2 (PIX TIM) of control register address 01H as shown in Table 1-2 below.

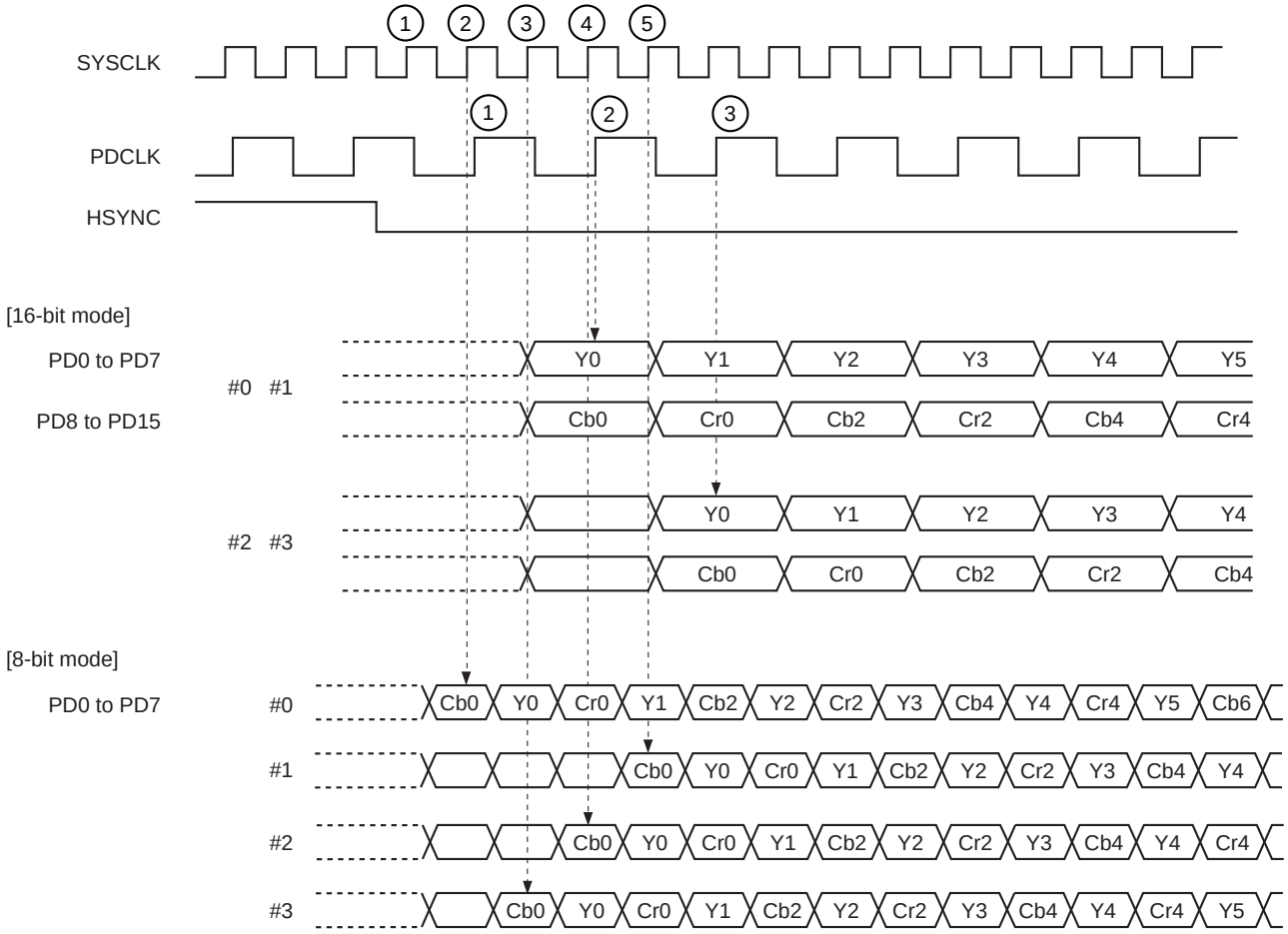
When "PIF MODE" is "0", Cb0 of the image data (Cb0, Y0, Cr0 and Y1) input from PD0 to PD7 is sampled at the respective rising edge of SYSCLK after the fall of HSYNC.
(Default: Cb0 is sampled at the rising edge of the second SYSCLK after the fall of HSYNC.)

When "PIF MODE" is "1", Y0 and Y1 data are input to PD0 to PD7, multiplexed Cb0 and Cr0 data are input to PD8 to PD15, and Y0 and Cb0 are sampled at the respective rising edge of PDCLK after the fall of HSYNC.
(Default: Y0 and Cb0 are sampled at the rising edge of the second PDCLK after the fall of HSYNC.)

PIX TIM		Timing phase
0	0	#0 (default)
0	1	#1
1	0	#2
1	1	#3

Table 1-2

Pixel Data Input Timing



PD0	Pixel data 0 (LSB)	PD8	Pixel data 0 (LSB)
PD1	Pixel data 1	PD9	Pixel data 1
:	:	:	:
PD7	Pixel data 7 (MSB)	PD15	Pixel data 7 (MSB)

2. Serial interface

The CXD1915R supports both the I²C bus (high-speed mode) and Sony serial interface modes. These modes can be selected by the XIICEN input pin as shown in Table 2-1 below.

XIICEN	H	L
	SONY SIO Mode	I²C Mode
SI/SDA	SI	SDA
SCK/SCL	SCK	SCL
XCS/SA	XCS	SA
SO	SO	High-Z

Table 2-1

2-1. I²C bus interface

The CXD1915R becomes an I2C bus slave transceiver, and supports the 7-bit slave address and the high-speed mode (400K bits/s).

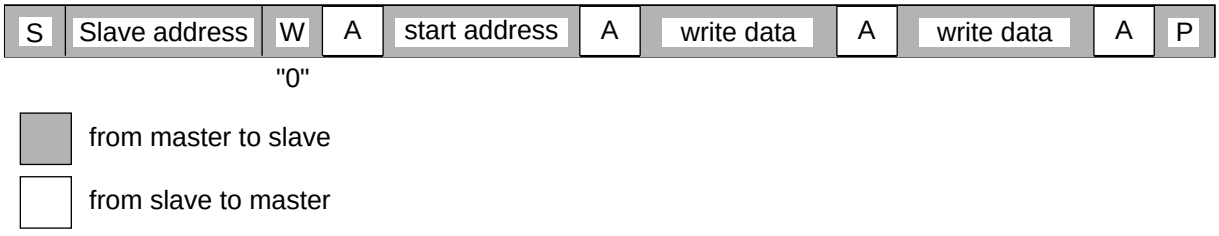
2-1-1 Slave address

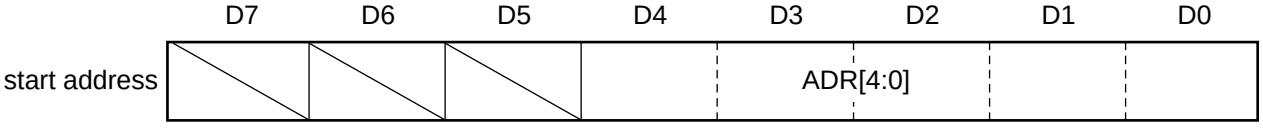
Two kinds of slave address (88H, 8CH) can be selected by the SA signal as shown in Table 2-2 below.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	SA	0	X

Table 2-2

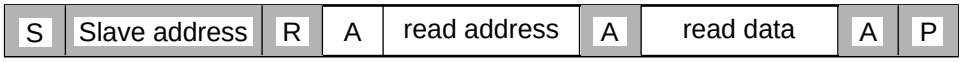
2-1-2. Write cycle





After the slave address is supplied from the master, the data in the next transfer cycle is set up inside the start address register of this IC as the start address of the control register. In subsequent cycles, the data supplied from the master is written in the addresses indicated by the control register address. The set control register address is automatically incremented with the transfer completion of each byte of data.

2-1-3. Read cycle



from master to slave

from slave to master

After the slave address is supplied from the master, subsequent cycles change immediately to read cycles and only the ID code (address 0CH, 0DH) is read out. During the read cycle, the start address is automatically set to 0CH.

Note: In Sony SIO mode, addresses from 00H to 0DH can be read out.

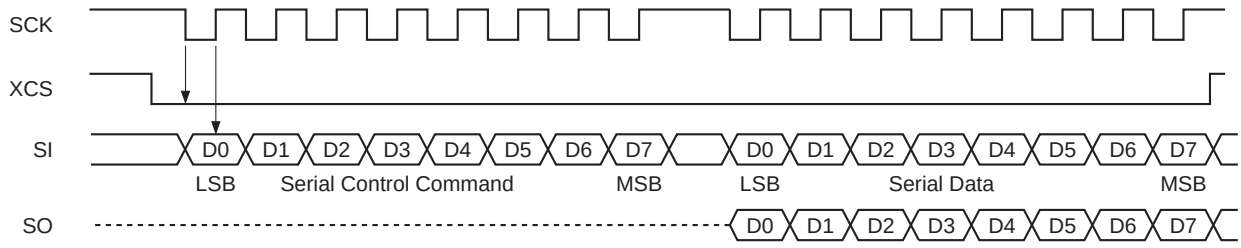
2-1-4. Handling of general call address (00H)

The general call address is ignored and there is no ACK response.

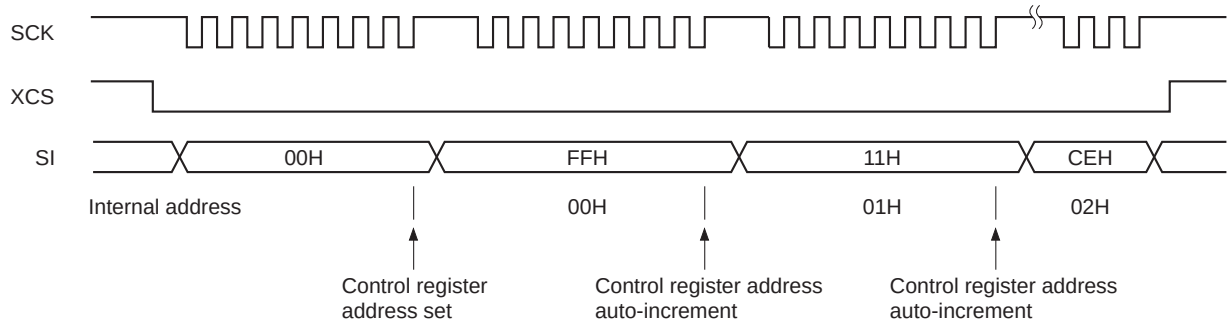
2-2. Sony serial interface

The Sony serial interface uses the SCK, XCS, SI and SO signals.
The serial interface is active when the XCS signal is Low and transmits and receives signals to and from the host.
The first byte after the XCS signal becomes Low is set up as a serial control command. Its data includes a control register address and read/write mode information for the interface. (See 2-2-1. Serial control command format.)
The control register address is automatically incremented with the transfer completion of each byte of data. In write mode, the SI signal of the serial input data is sampled at the rising edge of the SCK signal. In read mode, the register value is read out as the SO signal of the serial output data at the falling edge of the SCK signal, and is variable. In this case, the SI signal of the serial input data is ignored.

Serial Interface Timing

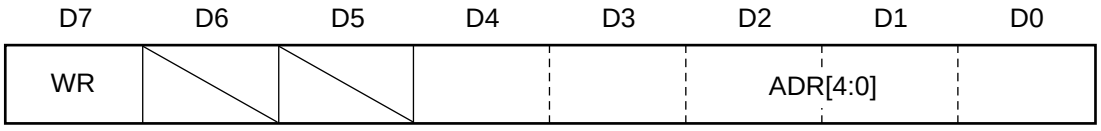


Serial Interface Sequence



Control Register Address	Control Register Data
00H	FFH
01H	11H
02H	CEH

2-2-1. Serial control command format



WR: Read/write mode
When this bit is "1":
The serial interface is write mode, and the SI signal of the serial input data is written in the register.
When this bit is "0":
The serial interface is read mode, and the register value is read out as the SO signal of the serial output data.

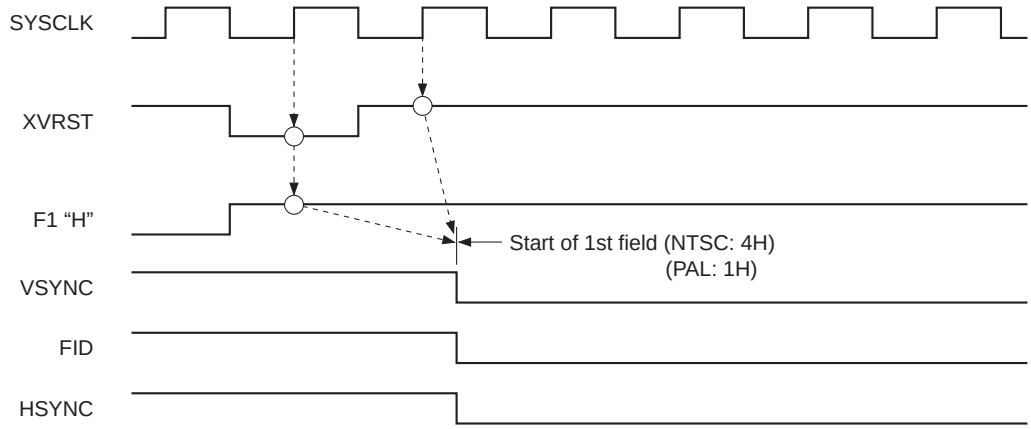
ADR[4:0]: Control register address setting (Initial value of the address)

3. XVRST, F1

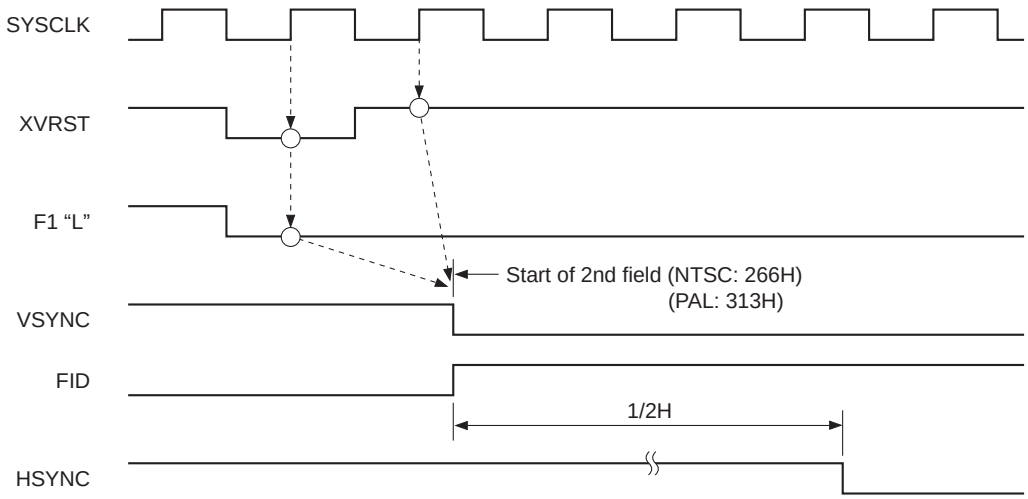
The XVRST and F1 signals are used to synchronize with the external V sync.
The XVRST and F1 signals are sampled at the rising edge of SYSCLK, and the F1 signal is sampled when XVRST is Low. When F1 is High, the internal sync generator is reset to the 1st field, and when F1 is Low, it is reset to the 2nd field. When XVRST is set to High, the digital sync generator starts operation, and the sequence of the 1st or 2nd field starts.

[8-bit mode]

XVRST Timing (1st Field)

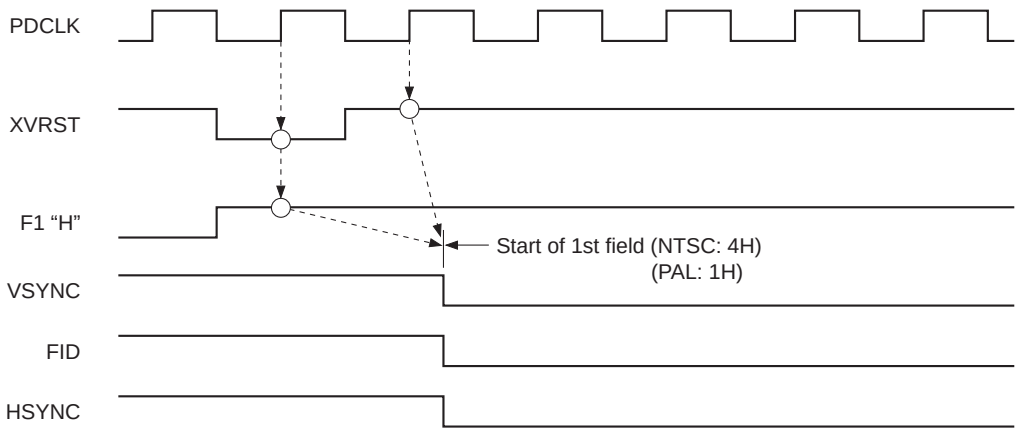


XVRST Timing (2nd Field)

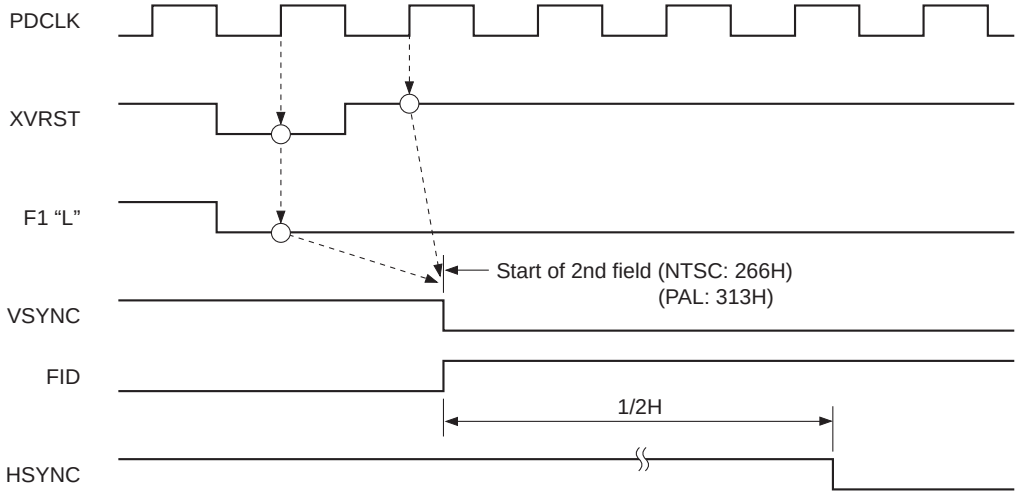


[16-bit mode]

XVRST Timing (1st Field)



XVRST Timing (2nd Field)



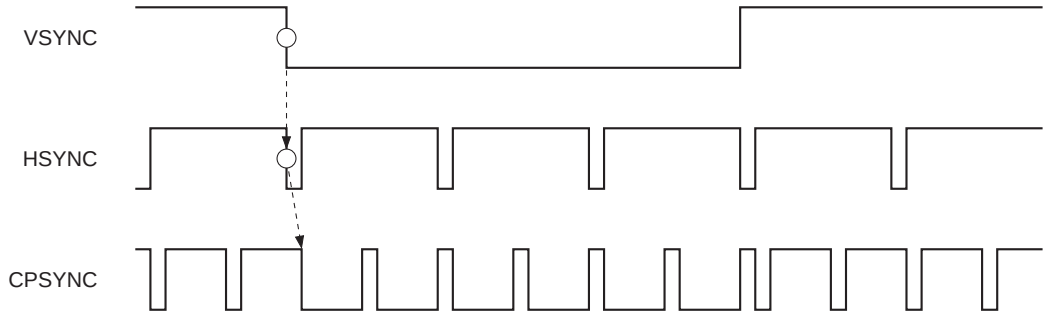
4. External synchronization

The CXD1915R can select master or slave operation using the SYNCM input pin.
When the SYNCM signal is Low, the CXD1915R is set to slave mode, and synchronizes to an external source using the HSYNC, VSYNC and FID I/O pin inputs.
The signal combinations used for external synchronization are set by bit 7 (SSEL) of control register 03H.

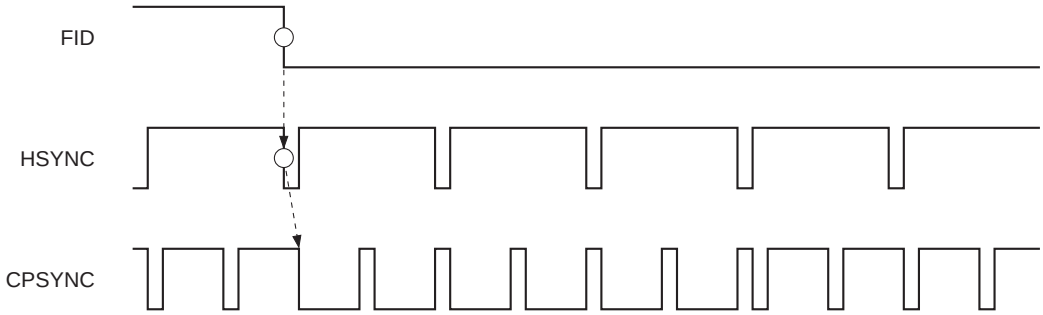
Register setting	HSYNC	VSYNC	FID
1	Used	Ignored	Used
0 (default)	Used	Used	Ignored

4-1. V synchronization

4-1-1. When SSEL = 0 (default), the CXD1915R identifies the data as the 1st field when the falling edges of the HSYNC and VSYNC signals match, or as the 2nd field when the falling edges do not match. The CXD1915R performs synchronization reset only during the 1st field.



4-1-2. When SSEL = 1, operation is reset to the 1st field at the falling edge of the FID signal. In this case, set bit 7 (FIDS) of control register 00H to High (default).



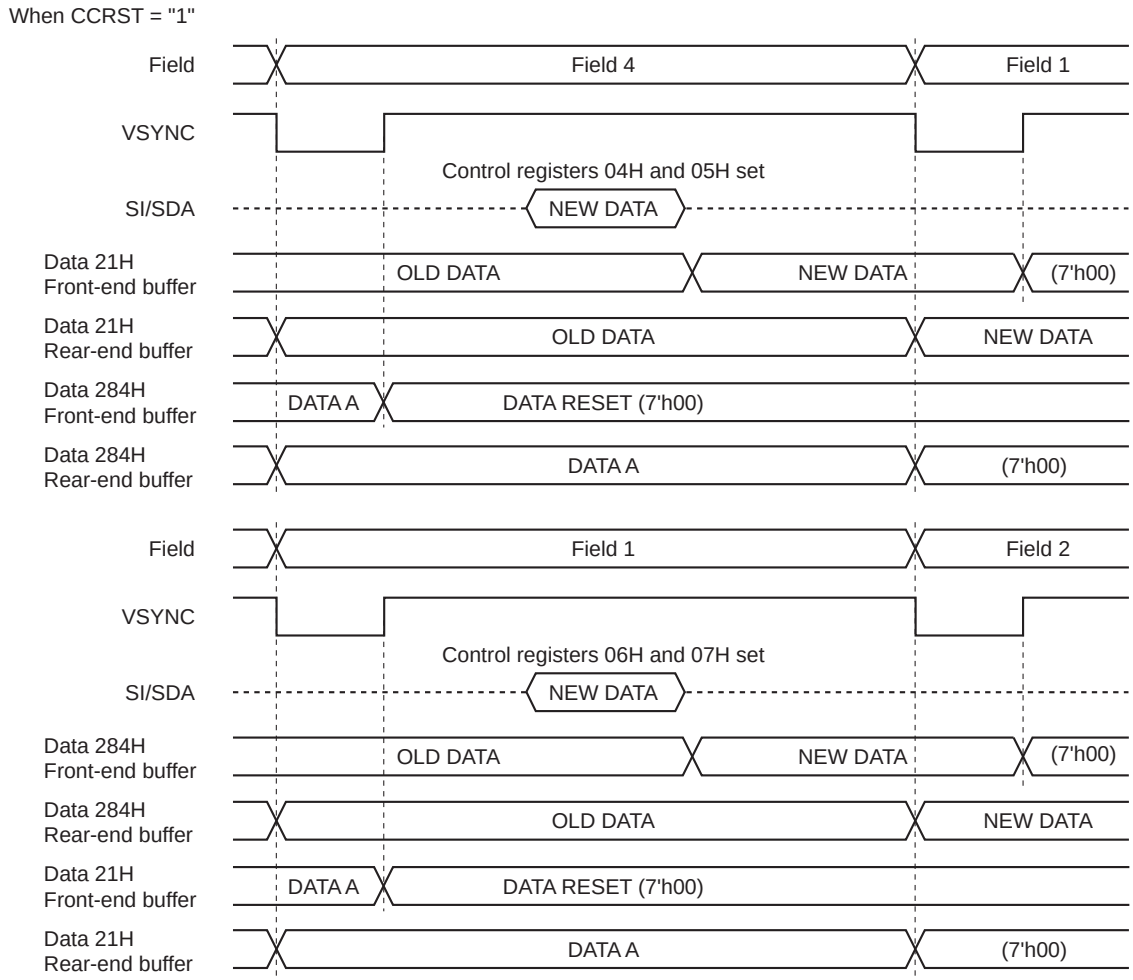
4-2. H synchronization

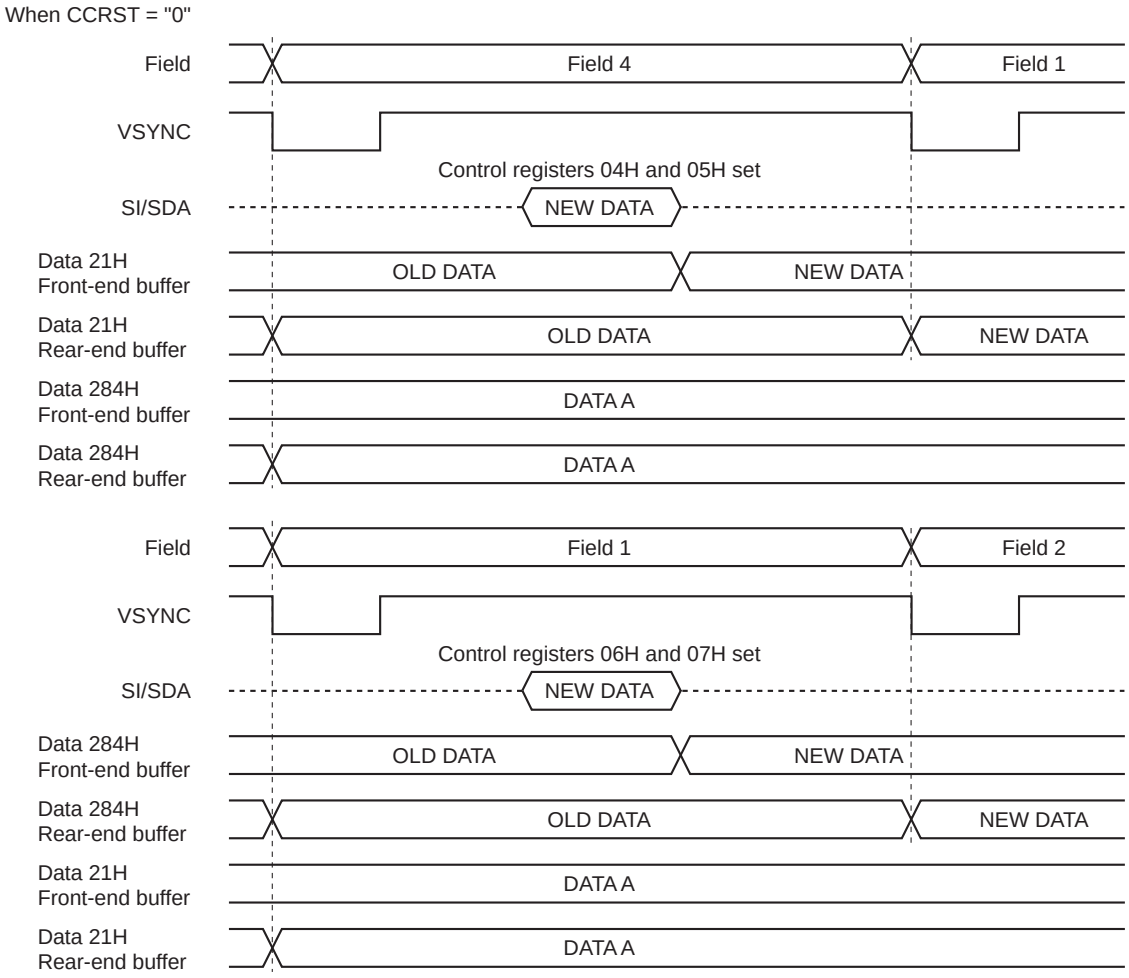
The horizontal line is reset by detecting the falling edge of the HSYNC signal.
Be sure to perform reset at the precise period.

5. Closed caption

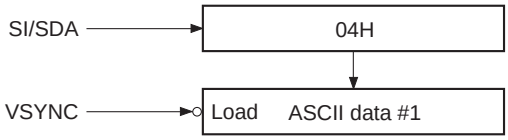
The CXD1915R supports closed caption encoding.
ASCII data for closed captions are encoded in line 21 and line 284 by adding a parity bit to every ASCII data set up in control registers 04H, 05H (data #1 and #2 for line 21) and 06H, 07H (data #1 and #2 for line 284). The control registers (04H to 07H) are double-buffered and ASCII data, which are set up by the serial interface, are synchronized with the VSYNC signal.
Automatic reset on/off can be selected for ASCII data which has been synchronized with VSYNC by changing the setting of bit 5 (CCRST) of control register address 03H.
When CCRST = "1", the control registers (04H, 05H or 06H, 07H) are automatically reset in sync with the rise of the next VSYNC.
When CCRST = "0" (default), the control registers (04H, 05H or 06H, 07H) are not reset, and the data set last is held.

Closed Caption Data Renewal Timing

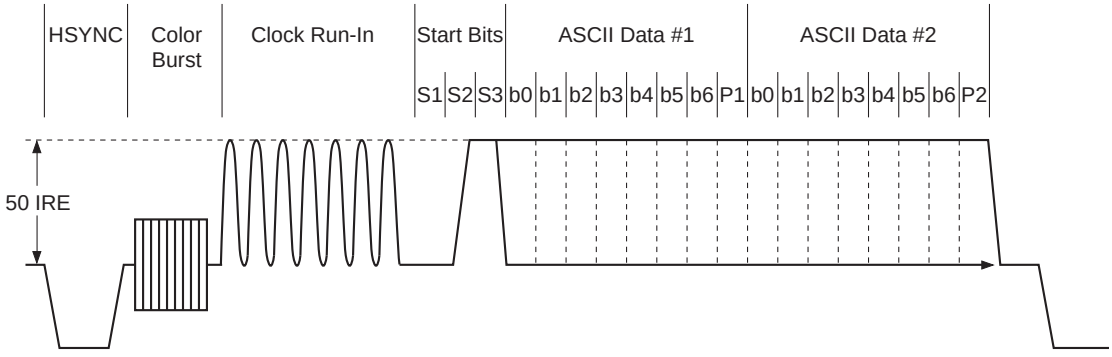




Double Buffer for Closed Caption



Closed Caption Signal Waveform



6. VBID (Video ID)

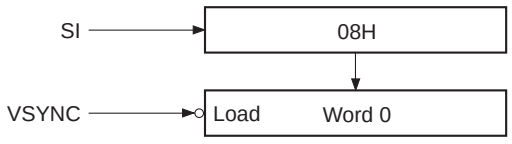
The CXD1915R supports encoding of Video ID (Provisional Standard EIAJ CPX-1204) to discriminate the aspect ratio. VBID is 14-bit data as shown in Table 6-1, and becomes 20-bit data with the addition of 6-bit CRCC. These data are superimposed on lines 20 and 283 during the vertical blanking period of NTSC video signals and output.

The data setting in Table 6-1 below is done by writing data in control registers (08H and 09H) via the serial interface. These control registers (08H and 09H) are double-buffered, and the VBID data are renewed in sync with the VSYNC signal.

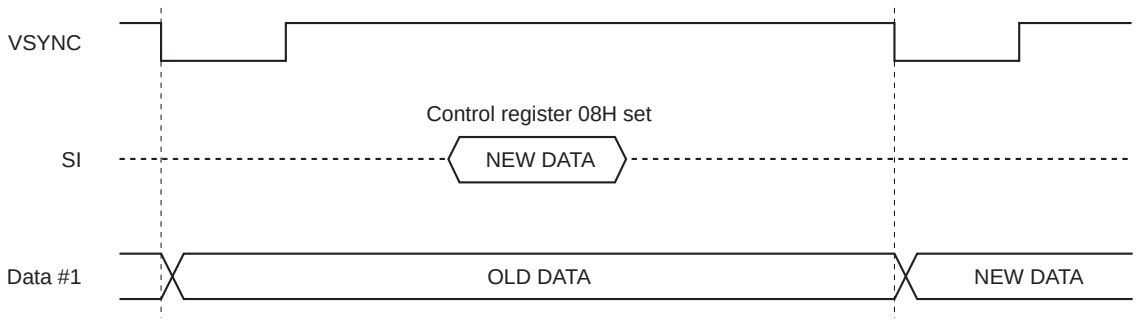
		bit-No.	Contents		
				"1"	"0"
Word 0	A	1 2 3	Transmission aspect ratio Image display format Undefined	Full-mode (16:9) Letter-box	4:3 Normal
	B	4 5 6	Identification information about video and other signals (audio signals, etc.) incidental to images which are transmitted simultaneously		
Word 1		4-bit width	Identification signal incidental to Word 0		
Word 2		4-bit width	Identification signal and information incidental to Word 0		

Table 6-1

Double Buffer for VBID

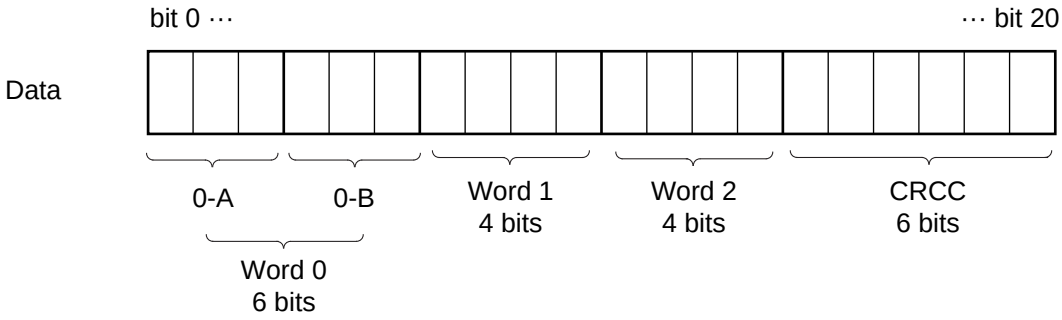


VBID Data Renewal Timing

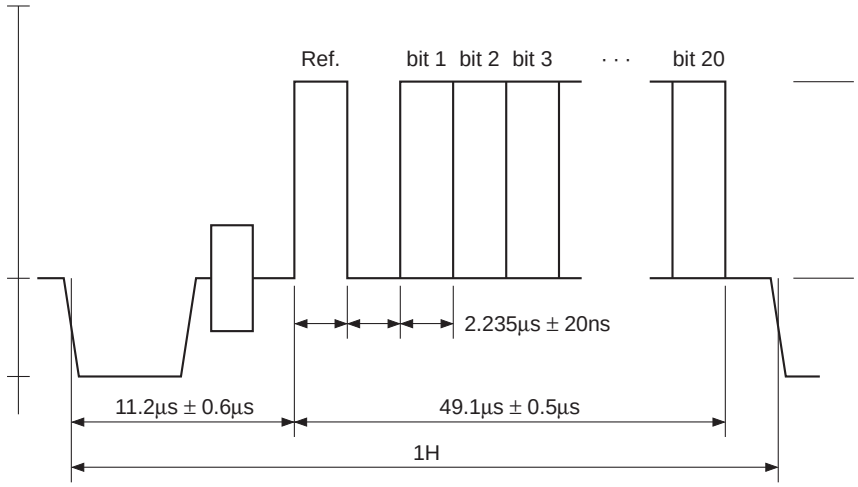


VBID Code Allocation

The VBID data are composed of Word 0 = 6 bits (Word 0-A = 3 bits and Word 0-B = 3 bits), Word 1 = 4 bits, Word 2 = 4 bits, and CRCC = 6 bits.



VBID Signal Waveform



7. WSS (Widescreen Signaling)

The CXD1915R supports WSS encoding to discriminate the aspect ratio. WSS is 14-bit data as shown in Table 7-1. These data are superimposed on line 23 during the vertical blanking period of PAL video signals and output.
The data setting in Table 7-1 below is done by writing data in control registers (0AH and 0BH) via the serial interface. These control registers (0AH and 0BH) are double-buffered, and the WSS data are renewed in sync with the VSYNC signal.

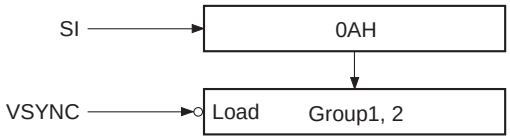
Group 1 Aspect ratio information (4 bits) b0 to b3	Group 2 PAL plus related information (4 bits) b4 to b7
0001 Normal 1000 Letter-box 14:9 Center 0100 Letter-box 14:9 Top 1101 Letter-box 16:9 Center 0010 Letter-box 16:9 Top 1011 Letter-box > 16:9 Center 0111 Full-mode 14:9 1110 Full-mode 16:9	bit 4 Camera/Film mode bits 5 to 7 Reserved (Color plus) (Helper) (BasebandHelper)

* b3 is odd parity.

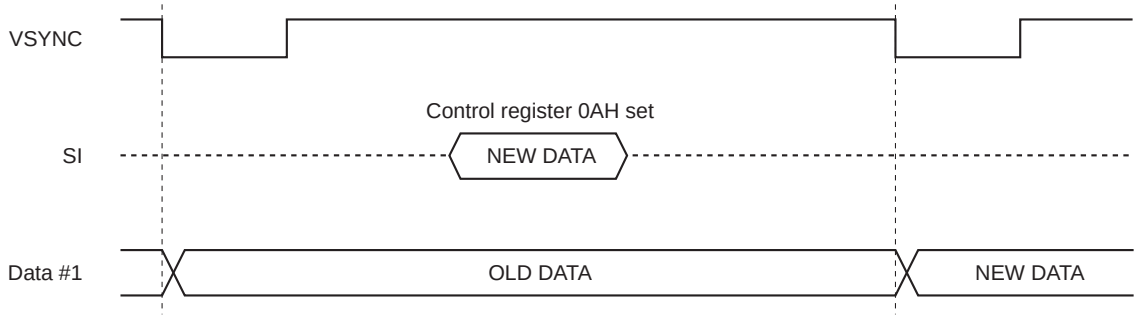
Group 3 Subtitle information (3 bits) b8 to b10	Group 4 Undefined (3 bits) b11 to b13
Bit 8 TeleText subtitle enable/disable Bits 9, 10 00 No subtitle 10 Subtitle inside screen 01 Subtitle in black portion 11 Reserved	Reserved

Table 7-1

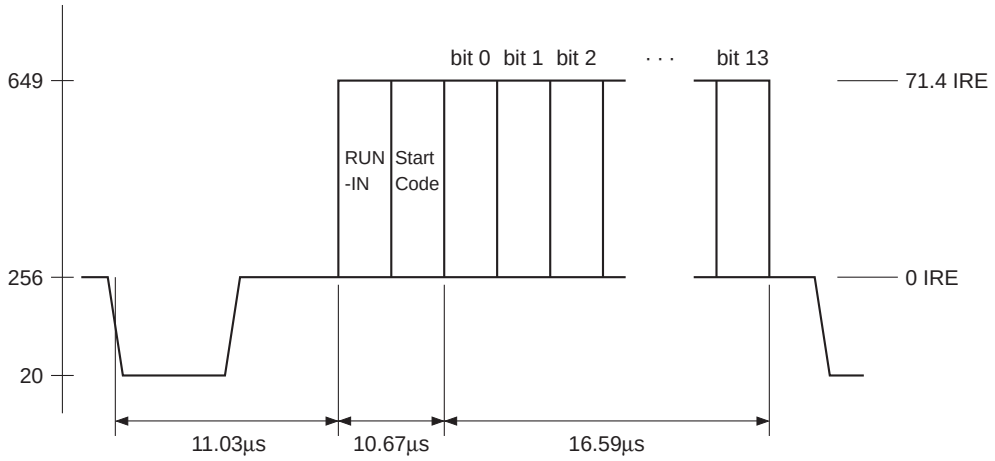
Double Buffer for WSS



WSS Data Renewal Timing



WSS Signal Waveform



8. RGB/YUV output

The CXD1915R has an RGB/YUV output function. RGB and YUV can be switched by setting bit 2 (RGB_UV) of control register address 03H.
Also, the UV level can be selected from BetaCam or SMPTE by setting bit 0 (BTCM) of address 03H. During RGB output, when bit 1 (GSYNC) of control register address 03H is "1", the sync signal is added to the G signal and output; when bit 1 (GSYNC) is "0", the sync signal is not added.

9. Support of interlace/non-interlace modes

The CXD1915R can be switched to the interlace and non-interlace modes by varying the setting of bit 1 (INTERLS) of control register address 01H. During the non-interlace mode, the 1st field is repeatedly output.

Register setting value INTERLS	Number of lines/field	
	NTSC	PAL
0 (non-interlace)	262	312
1 (interlace)	262.5	312.5

10. Support of NTSC, PAL, MPAL and 4.43NTSC

The CXD1915R can convert to NTSC, PAL, MPAL and 4.43NTSC analog TV signals by setting bits 2, 1 and 0 (ENC MODE) of control register address 00H.

Register setting value ENC MODE			Encoding mode	Number of lines/field	Subcarrier line phase difference	Subcarrier frequency [MHz]
0	0	0	PAL	625/50	±135°	4.4336 (10 ± 1cycles)
0	0	1	NTSC	525/60	±180°	3.5795 (9 ± 1cycles)
0	1	1	MPAL	525/60	±135°	3.5756 (9 ± 1cycles)
1	0	1	4.43NTSC	525/60	±180°	4.4336

11. OSD

The CXD1915R can be switched to OSD mode by setting bit 6 (OSDEN) of control register address 02H. At this time, if OSDSW (Pin 67) = 1, the OSD input pin is enabled.
Also, the luminance level can be selected from the four levels of 25%, 50%, 75% and 100% by varying the setting of bits 5 and 4 (Y_LEV) of control register address 02H. This allows 29-color (7 colors × 4 levels + black) OSD output. (Up to 8 colors can be displayed at once.)

Color	ROSD (Pin 68)	GOSD (Pin 69)	BOSD (Pin 70)
White	1	1	1
Yellow	1	1	0
Cyan	0	1	1
Green	0	1	0
Magenta	1	0	1
Red	1	0	0
Blue	0	0	1
Black	0	0	0

12. Support of square pixels

The CXD1915R can be switched to support square pixels by setting bit 4 (SQPIX) of control register address 00H.
MPAL and 4.43NTSC cannot be used in square pixel mode.

Register setting value SQPIX	Mode	Pixel clock frequency [MHz]	
		NTSC	PAL
0	Normal mode	13.5	13.5
1	Square pixel mode	12.272727	14.75

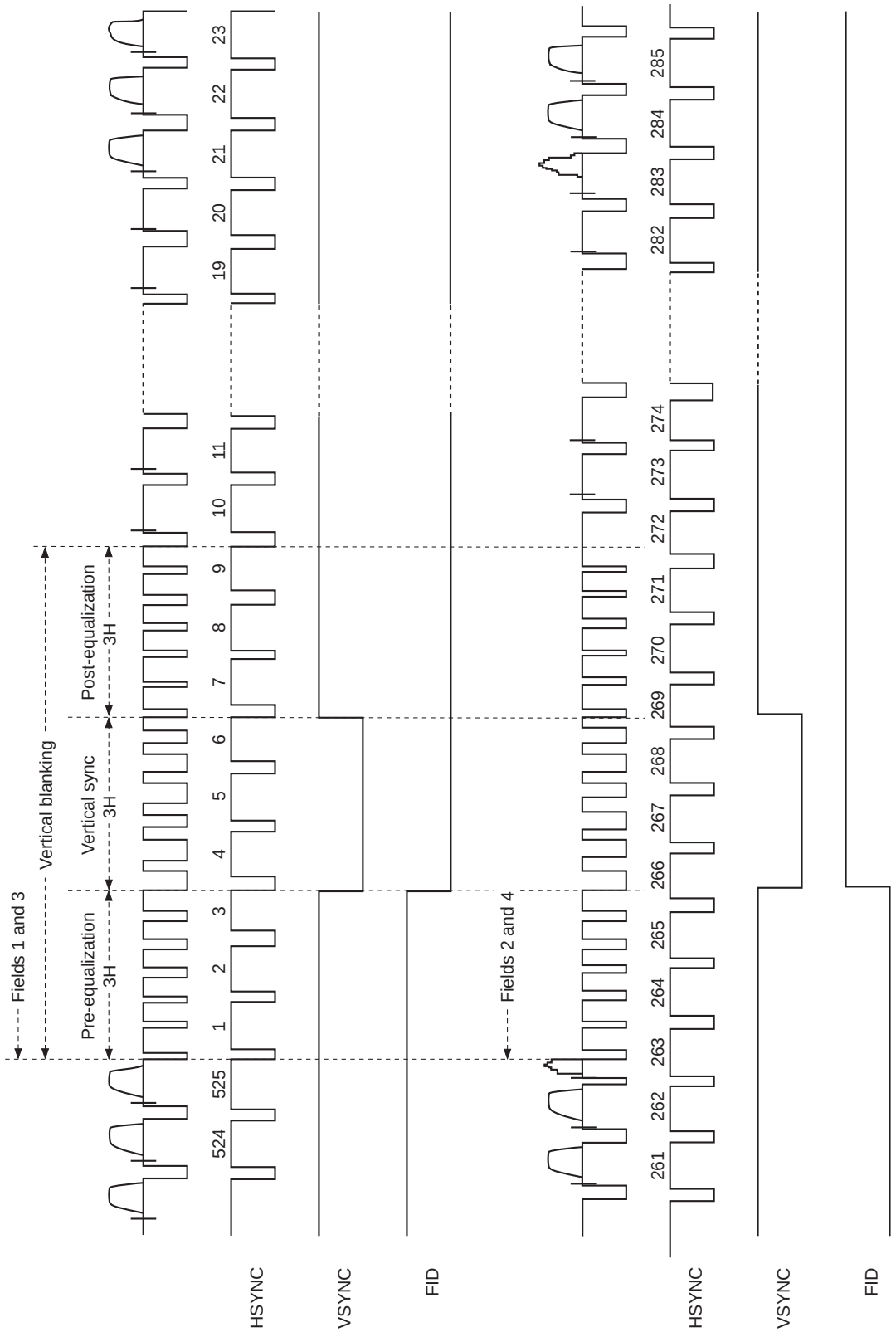
13. On-chip 100% color bar generator

The CXD1915R can display an ITU_R100% color bar from its internal generator by setting bit 7 (CBAR) of control register address 02H.

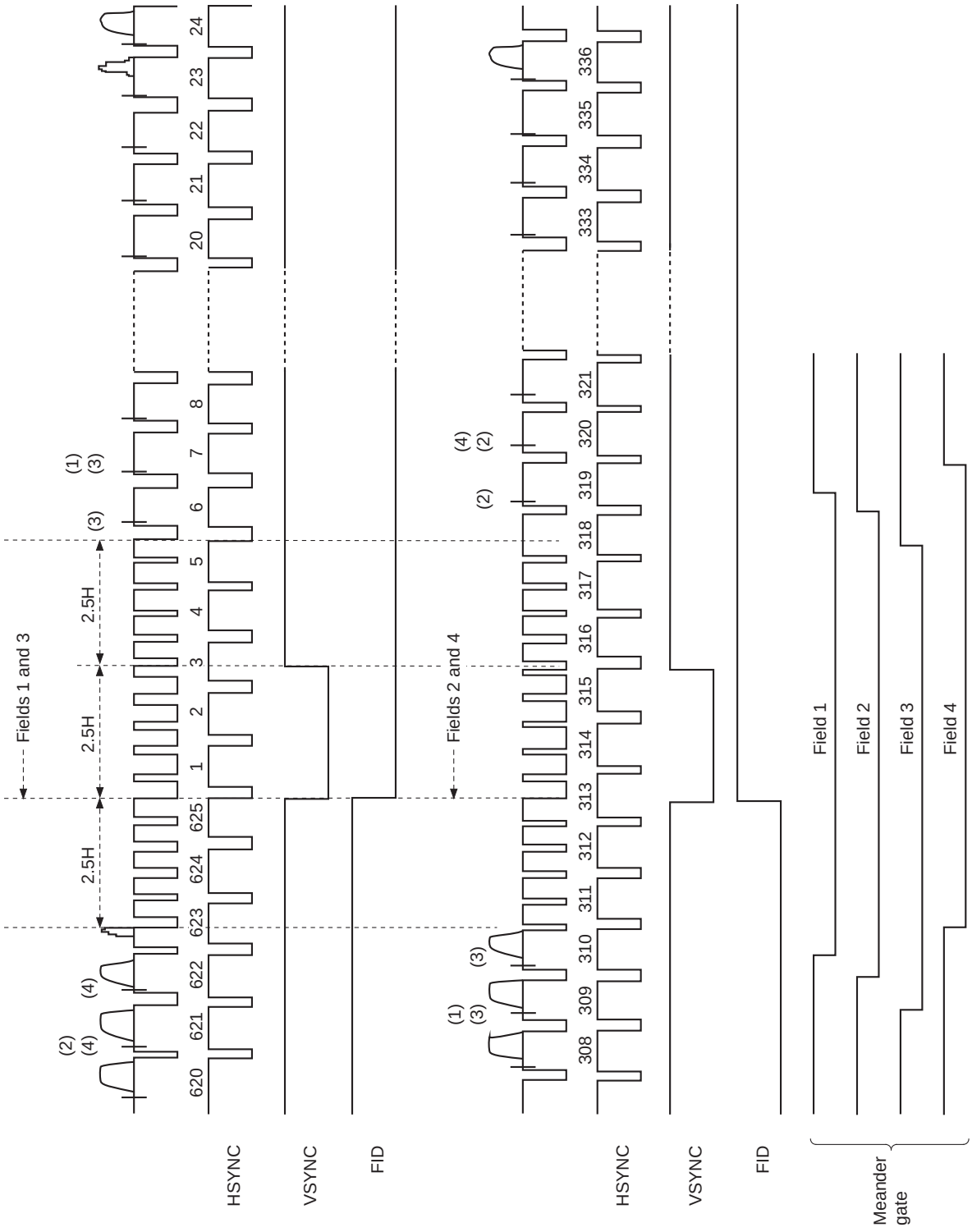
14. ITU-656EAV decoding

The CXD1915R decodes the EAV of the ITU-656 1st field and performs internal synchronization every 4 fields for NTSC or every 8 fields for PAL by setting bit 3 (D1 MODE) of control register address 03H.

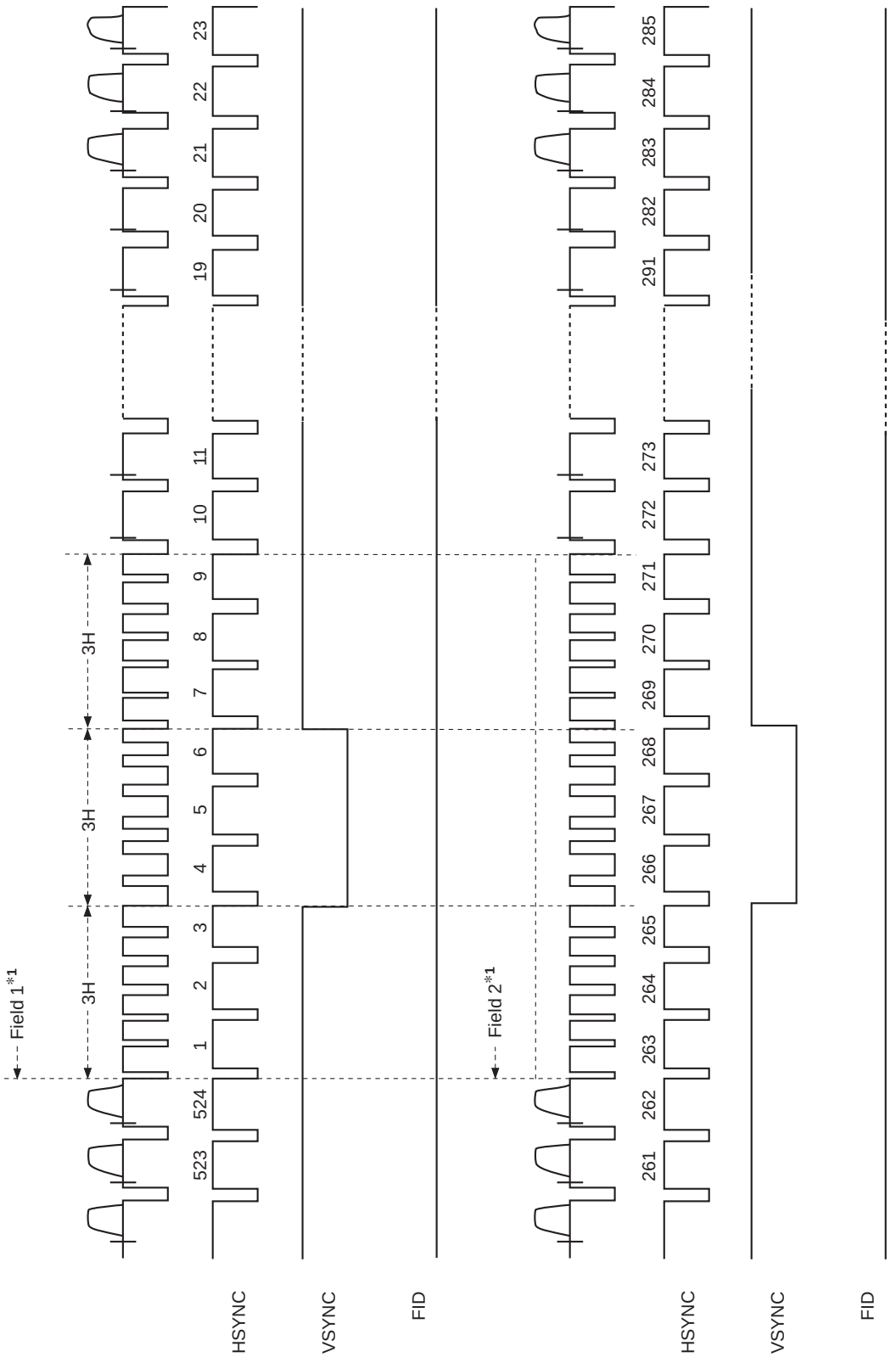
Signal Waveform of NTSC Vertical Blanking Period (Interlace mode)



Signal Waveform of PAL Vertical Blanking Period (Interlace mode)

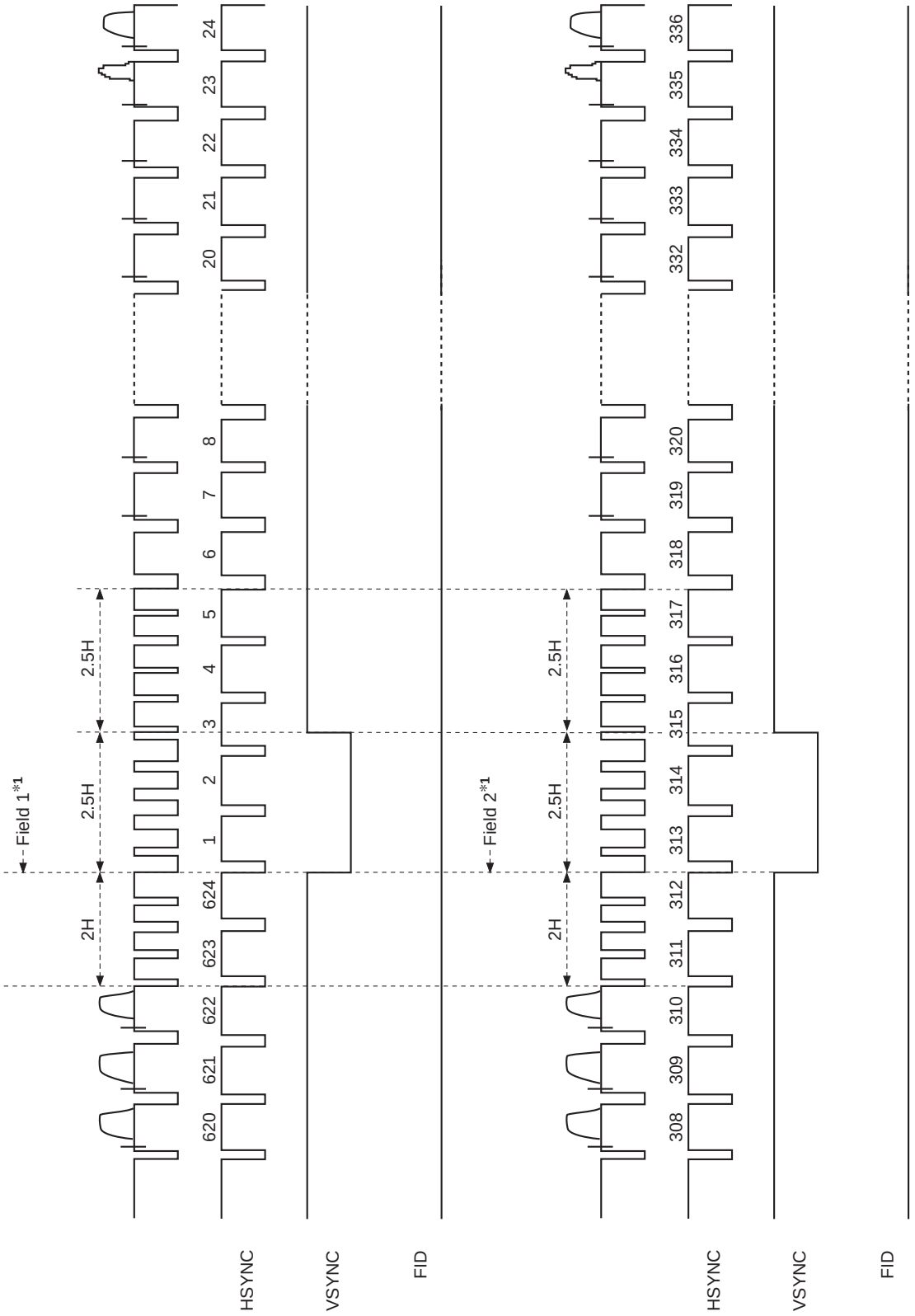


Signal Waveform of NTSC Vertical Blanking Period (Non-interlace mode)



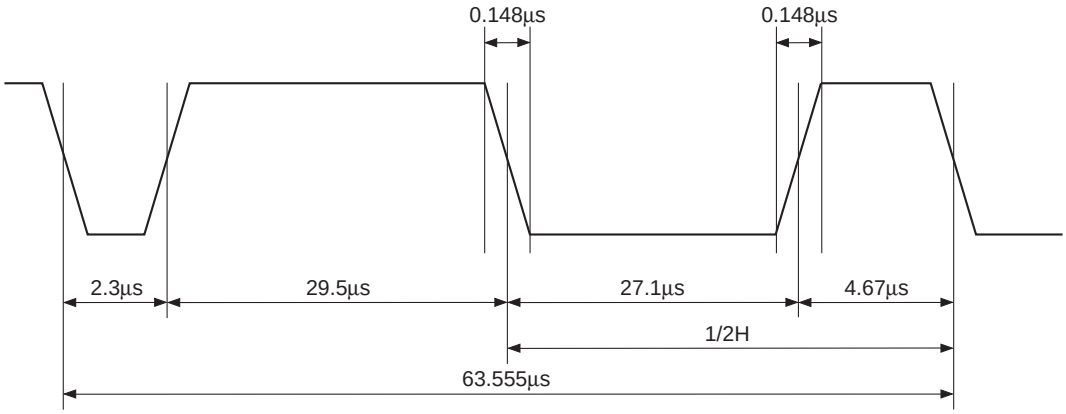
*1 No differentiation is made between Fields 1 and 2 to facilitate the frame description.

Signal Waveform of PAL Vertical Blanking Period (Non-interlace mode)

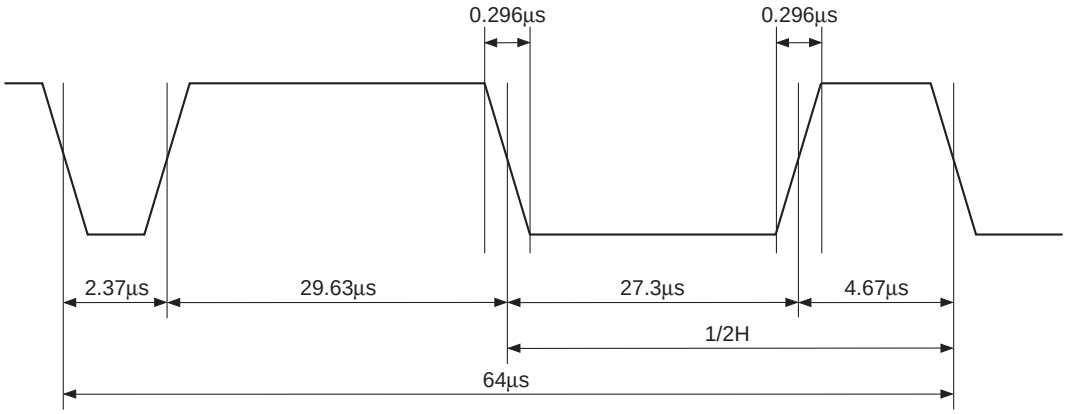


*1 No differentiation is made between Fields 1 and 2 to facilitate the frame description.

Sync Signal Timing



NTSC Equalizing Pulse and Sync Pulse Signal Waveform



PAL Equalizing Pulse and Sync Pulse Signal Waveform

Control Register Map

BIT

Function Selection #1

	7	6	5	4	3	2	1	0	
Address 00H	FIDS	MASK EN	PIX EN	SQPIX	SET UP	ENC MODE			R/W

ENC MODE Encoding mode
000: PAL encoding mode
001: NTSC encoding mode (Default)
010: Inhibit
011: MPAL encoding mode
100: Inhibit
101: 4.43NTSC encoding mode
110: Inhibit
111: Inhibit

SET UP Setup enable
0: No setup level, black level = blanking level
1: 7.5 IRE setup level insertion (Default)

SQPIX Square pixel
0: Disable square pixel mode (13.5MHz) (Default)
1: Enable square pixel mode

PIX EN Pixel data enable
PIXCON input pin = High 0: Disable input pixel data
1: Enable input pixel data (Default)
PIXCON input pin = Low 0: Disable input pixel data (Default)
1: Enable input pixel data

MASK EN Mask enable
0: Pixel data through during vertical blanking period
1: Pixel data reject during vertical blanking period (Default)

FIDS FID polarity select
SYNCM input pin = High
0: 1st field High, 2nd field Low
1: 1st field Low, 2nd field High (Default)
SYNCM input pin = Low
Fixed to "1".

BIT

Function Selection #2

	7	6	5	4	3	2	1	0	
Address 01H	DAC MODE			PIF MODE	PIX TIM		INTERLS	FREE RUN	R/W

FREERUN Free running
0: Reset applied every 4 fields during NTSC or every 8 fields during PAL and MPAL (Default)
1: No SCH timing reset

INTERLS Interlace mode switching
0: Non-interlace mode
1: Interlace mode (Default)

PIX TIM Pixel input timing
00: #0 (Default)
01: #1
10: #2
11: #3

PIF MODE Pixel input format
0: 8-bit mode, multiplexed Y, Cb, Cr (4:2:2) (Default)
1: 16-bit mode, Y and multiplexed Cb, Cr (4:2:2)

DAC MODE DAC output activity
000: Non-active
001: CP-Out active
010: Inhibit
011: Video signal (Y, C, CP) -Out active (Default)
100: Inhibit
101: R, G, B-Out and CP-Out active
110: Inhibit
111: All outputs active

BIT

Function Selection #3

	7	6	5 4	3	2	1 0	
Address 02H	CBAR	OSDEN	Y_LEV	VBID	WSS	CC Mode	R/W

CC MODE Closed caption encoding mode
00: Disable closed caption encoding (Default)
01: Enable encoding in 1st field (Line 21)
10: Enable encoding in 2nd field (Line 284)
11: Enable encoding in both fields

WSS WSS encoding enable
0: Disable WSS encoding (Default)
1: Enable WSS encoding

VBID VBID encoding mode
0: Disable VBID encoding (Default)
1: Enable VBID encoding

Y_LEV OSD luminance level select
00: 100% (Default)
01: 25%
10: 50%
11: 75%

OSDEN OSD enable
0: Disable OSD (Default)
1: Enable OSD

CBAR Color bar enable
0: Disable on-chip color bar output (Default)
1: Enable on-chip color bar output (ITU_R100% color bar)

Function Selection #4

	BIT 7	6	5	4	3	2	1	0	
Address 03H	SSEL	BF	CCRST		D1 MODE	RGB_UV	GSYNC	BTCM	R/W

BTCM UV output level control
0: SMPTE
1: BetaCam (Default)

GSYNC G-on SYNC enable
0: Disable (Default)
1: Enable

RGB_UV RGB/YUV output mode switching
0: YUV (Default)
1: RGB

D1 MODE ITU-R656 EAV decoding
0: Disable ITU-R656 EAV decoding (Default)
1: Enable ITU-R656 EAV decoding

CCRST Closed caption character reset enable
0: Disable (Default)
1: Enable

BF Burst flag enable
0: Disable burst flag
1: Enable burst flag (Default)

SSEL Sync select
Selects the sync signal used during slave mode.

	HSYNC	VSYNC	FID
0:	Used	Used	Ignored (Default)
1:	Used	Ignored	Used

BIT

Closed Caption Character #1 (Line 21H)

	7	6	5	4	3	2	1	0	
Address 04H				ASCII Data #1		(Default: 0H)			R/W

Closed Caption Character #2 (Line 21H)

	7	6	5	4	3	2	1	0	
Address 05H				ASCII Data #2		(Default: 0H)			R/W

Closed Caption Character #1 (Line 284H)

	7	6	5	4	3	2	1	0	
Address 06H				ASCII Data #1		(Default: 0H)			R/W

Closed Caption Character #2 (Line 284H)

	7	6	5	4	3	2	1	0	
Address 07H				ASCII Data #2		(Default: 0H)			R/W

VBID #1

	7	6	5	4	3	2	1	0	
Address 08H				Word 0-B	Word 0		Word 0-A		R/W

VBID #2

	7	6	5	4	3	2	1	0	
Address 09H		Word 2				Word 1			R/W

WSS #1

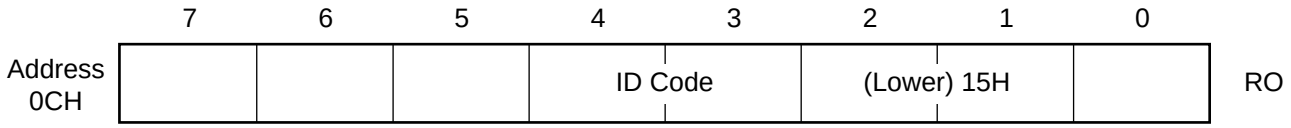
	7	6	5	4	3	2	1	0	
Address 0AH	bit 7	Group 2 bit 6	bit 5	bit 4	bit 3	bit 2	Group 1 bit 1	bit 0	R/W

WSS #2

	7	6	5	4	3	2	1	0	
Address 0BH			bit 13	Group 4 bit 12	bit 11	bit 10	Group 3 bit 9	bit 8	R/W

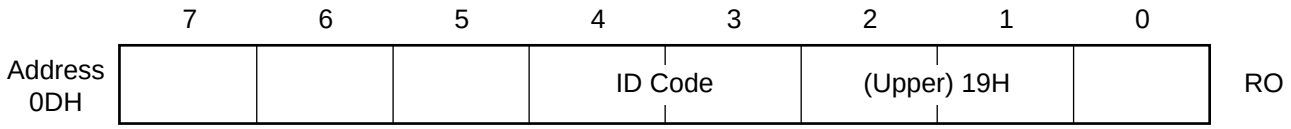
BIT

Device ID #1



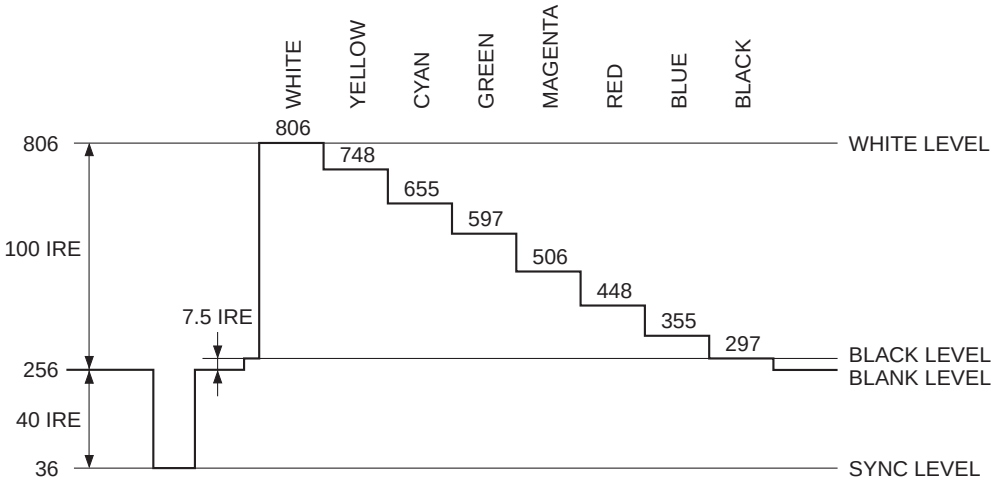
ID code Identification: 15H

Device ID #2

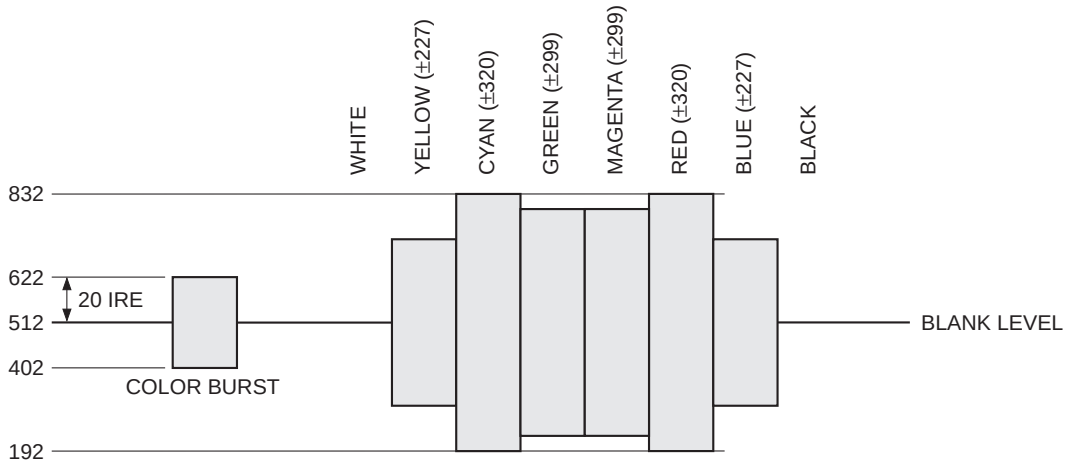


ID code Identification: 19H

Video Signal Timing (NTSC, 7.5 IRE Setup)

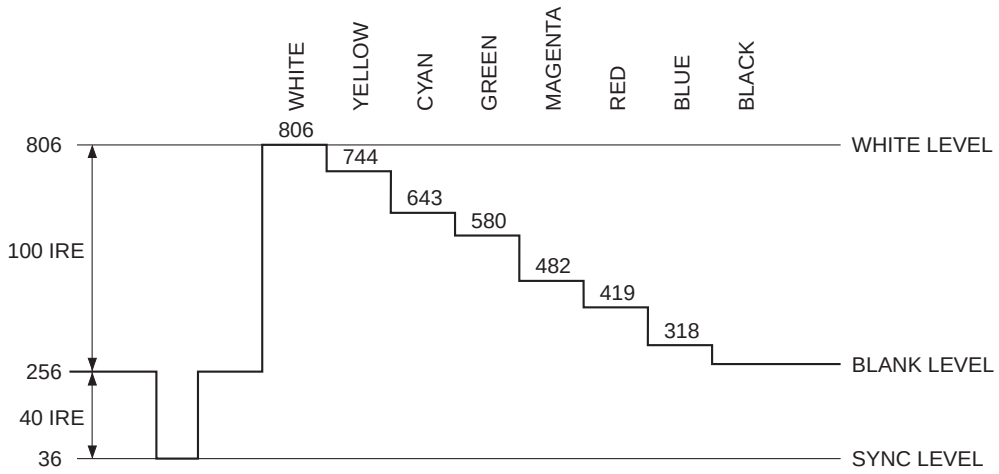


NTSC Y (luminance) signal output waveform
7.5 IRE setup

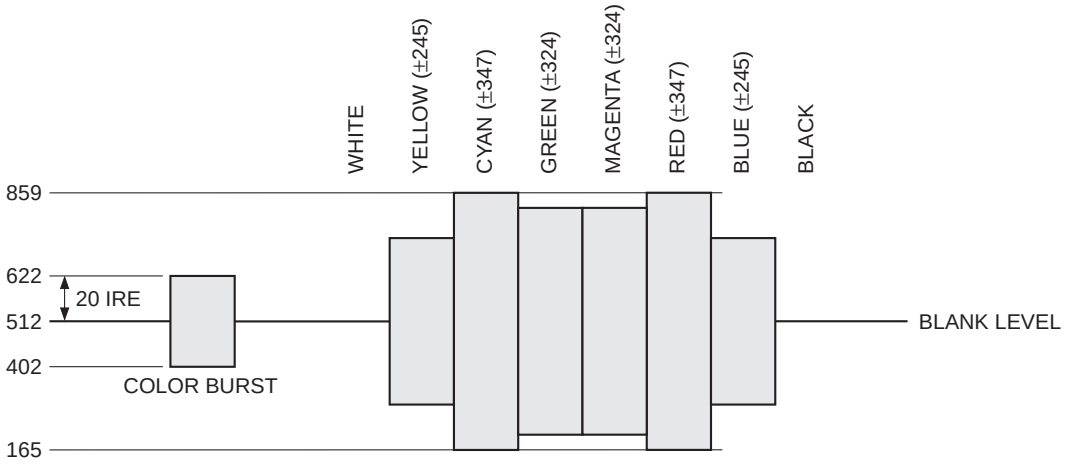


NTSC C (chroma) signal output waveform
7.5 IRE setup

Video Signal Timing (NTSC, No Setup)

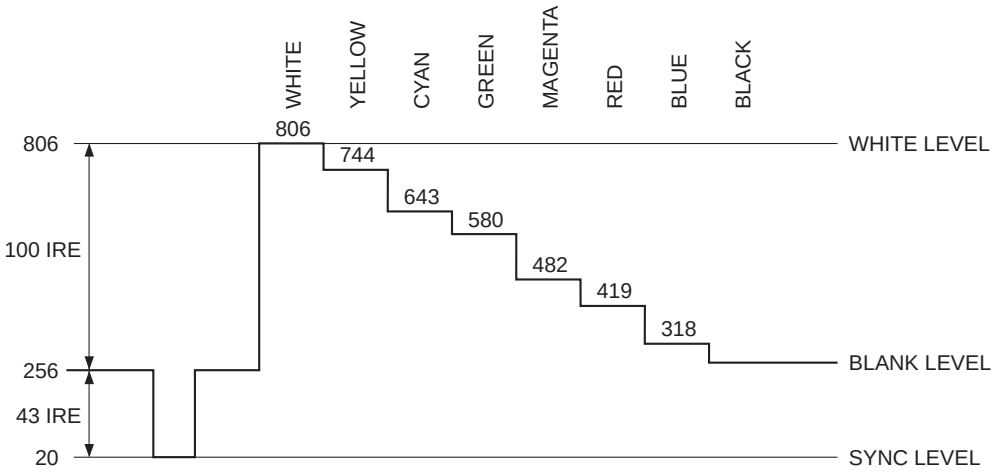


NTSC Y (luminance) signal output waveform

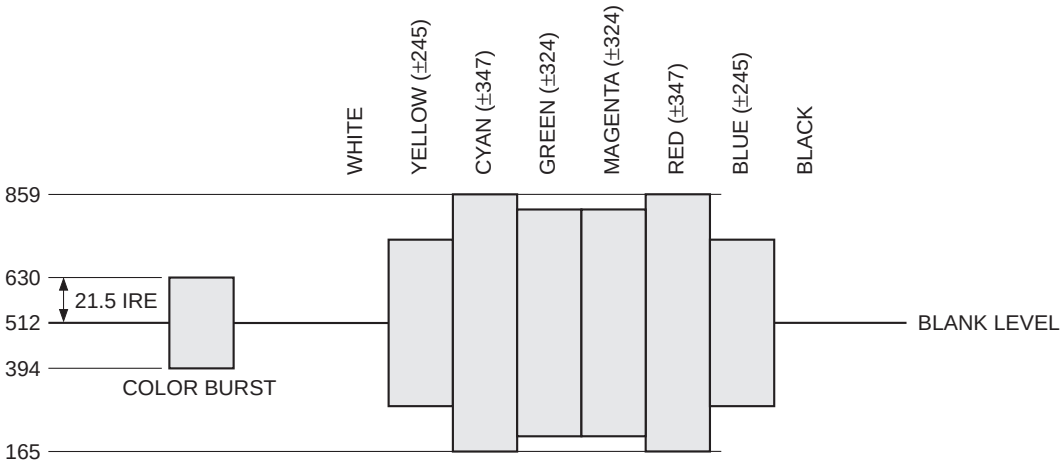


NTSC C (chroma) signal output waveform

Video Signal Timing (PAL)

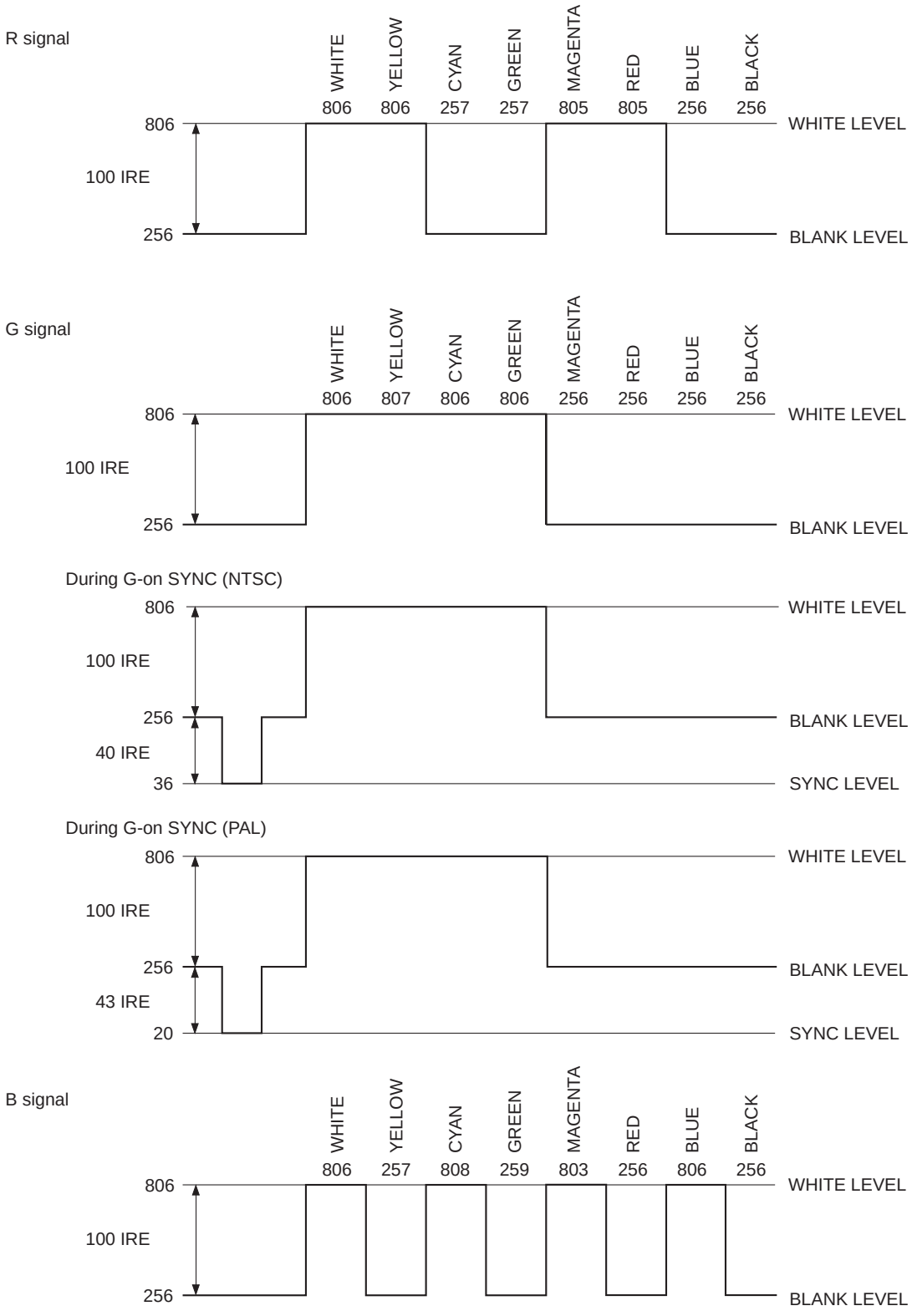


PAL Y (luminance) signal output waveform



PAL C (chroma) signal output waveform

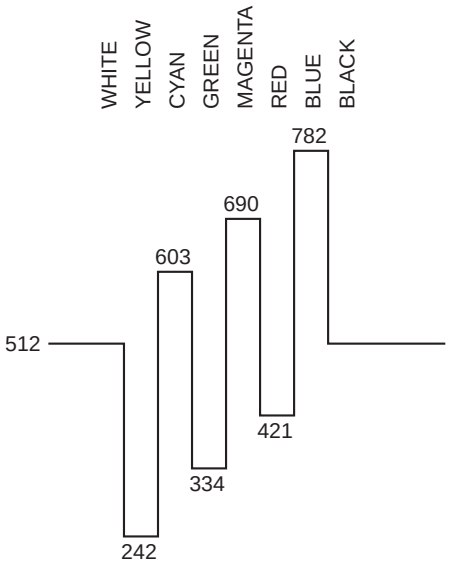
RGB Signal Output Waveform



UV Output Level

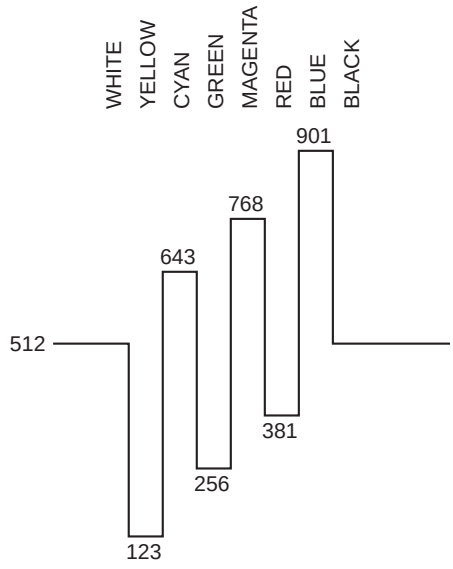
Color Difference (U) Signal

SMPTE LEVEL

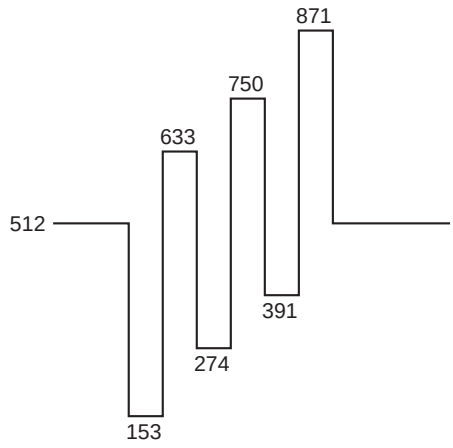


NTSC

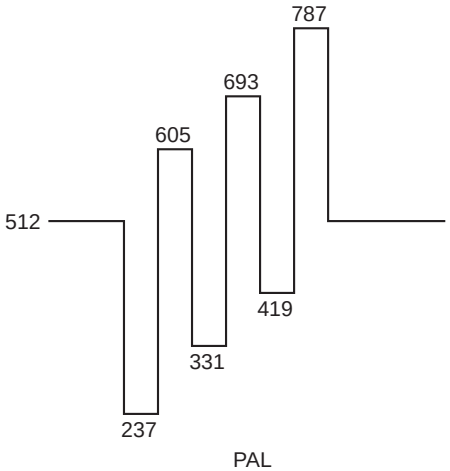
Beta Cam LEVEL



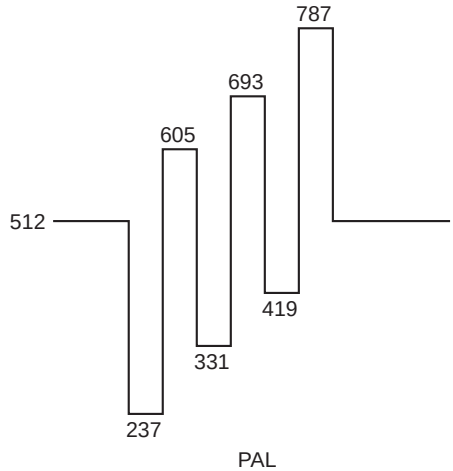
NTSC, No setup



NTSC, Setup



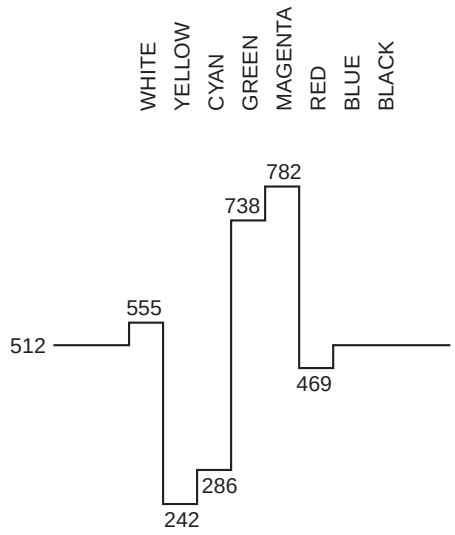
PAL



PAL

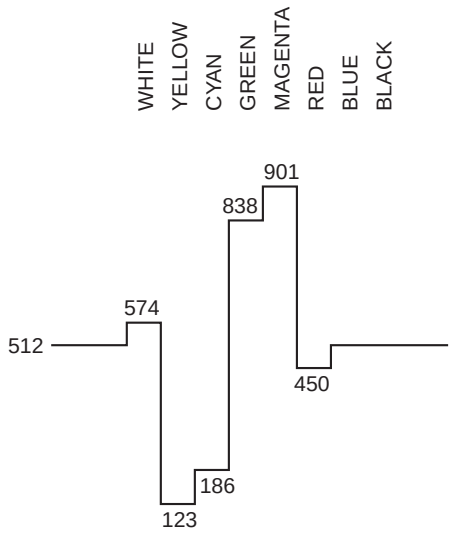
Color Difference (V) Signal

SMPTE LEVEL

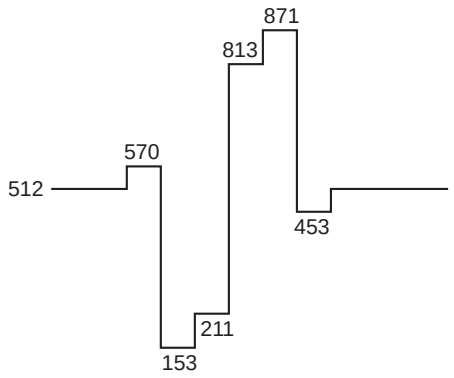


NTSC

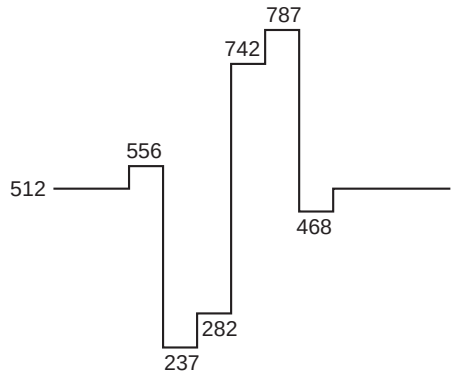
Beta Cam LEVEL



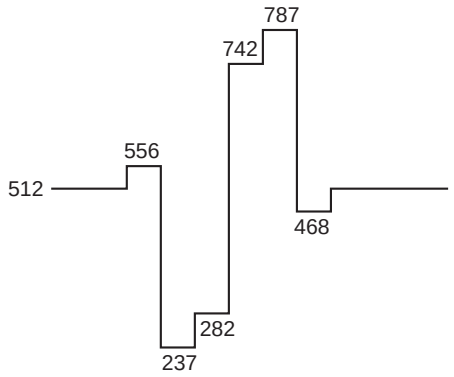
NTSC, No setup



NTSC, Setup

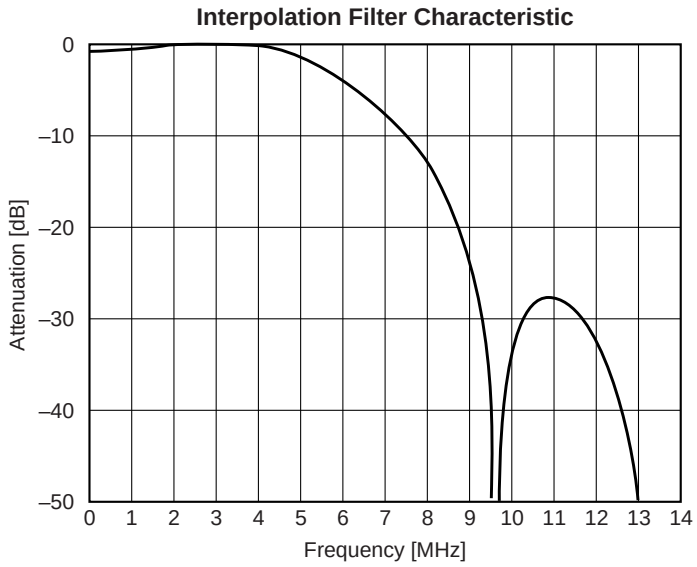


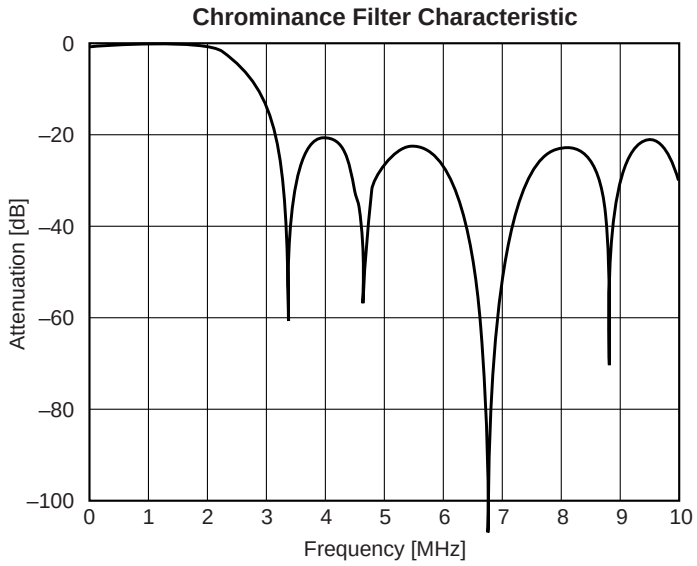
PAL



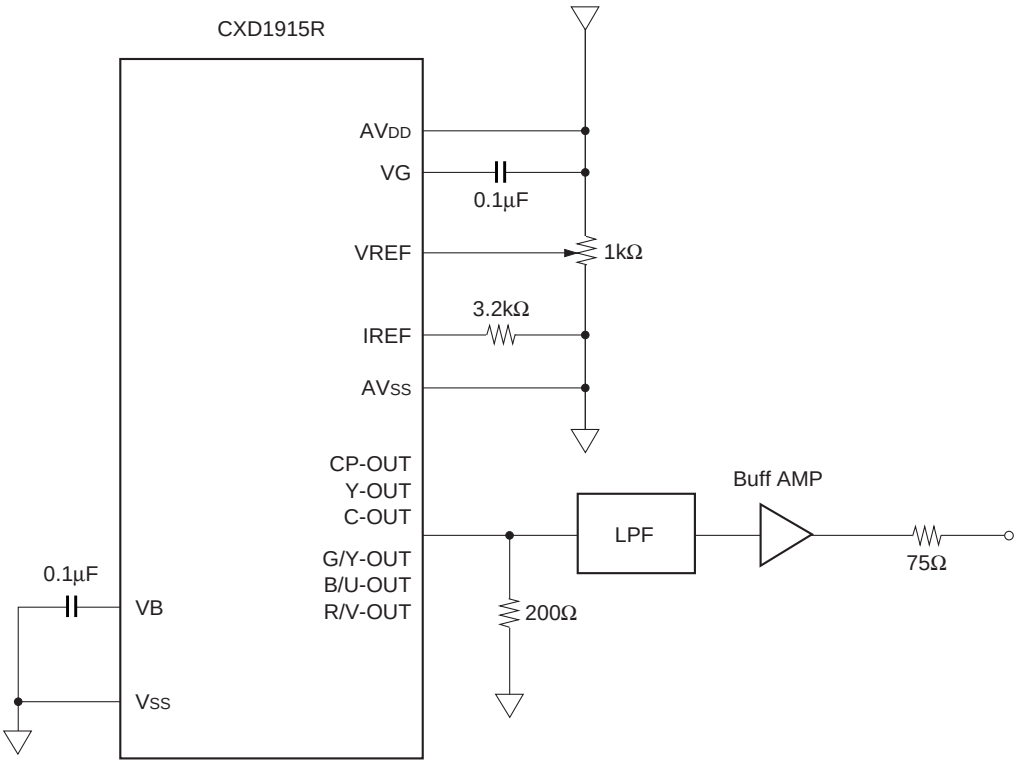
PAL

Internal Filter Characteristics

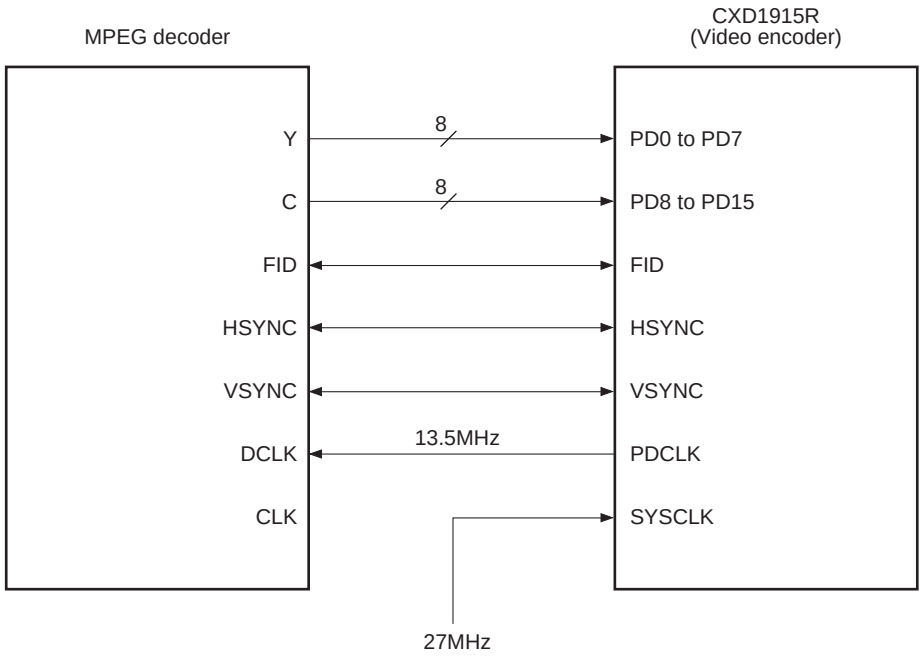




DAC Application Circuit



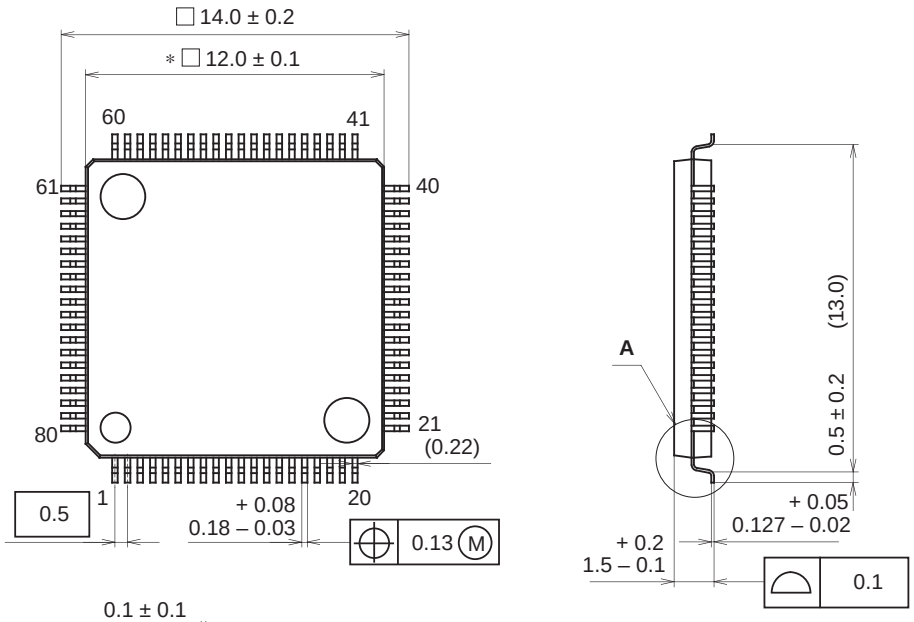
Application Circuit

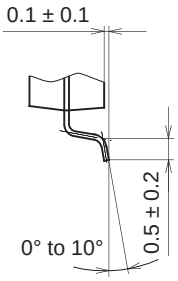


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN LQFP (PLASTIC)





DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-80P-L01
EIAJ CODE	LQFP080-P-1212
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5g