SONY

CXA3038N

IQ Detection IC for Digital Satellite Broadcast Tuner

Description

The CXA3038N is an IC for IQ-detection of DSS, DVB, and other digital satellite broadcast QPSK modulation signals in the 480 MHz band. It consists of an AGC amplifier circuit, oscillator circuit, phase shifter circuit, and phase comparison circuit. In addition, the chip has a PLL circuit for frequency control and built-in control data. It realizes high-accuracy oscillator frequencies through use of a low-cost LC resonance circuit.

Features

- Built-in PLL for controlling oscillator frequency.
- Oscillator frequency based at 479.5 MHz is adjustable in ±4 steps of 50 kHz using the voltage of the control pin.
- Reference OSC allows switching to 4 MHz or 10 MHz.
- Built-in output buffer for reference OSC.
- Low-impedance IQ output.
- AGC gain variation 35 dB.

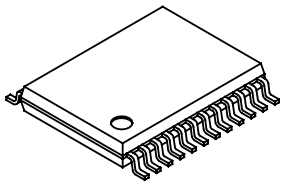
Applications

Digital satellite broadcast tuner

Structure

Bipolar silicon monolithic IC

24 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

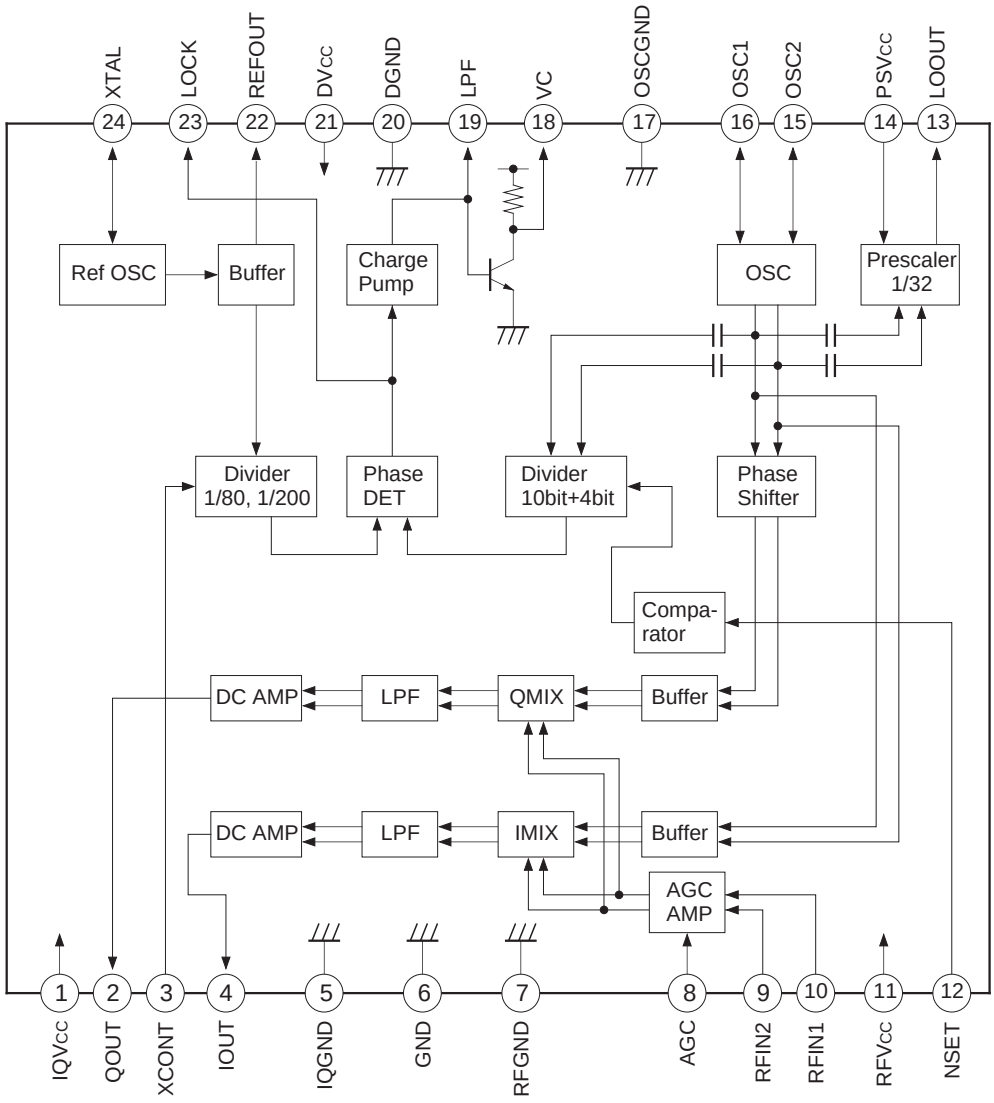
• Supply voltage	V_{CC}	–0.3 to 5.5	V
• Storage temperature	Tstg	–55 to +150	°C

Operating Conditions

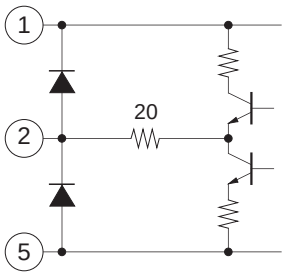
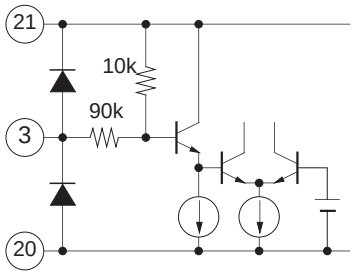
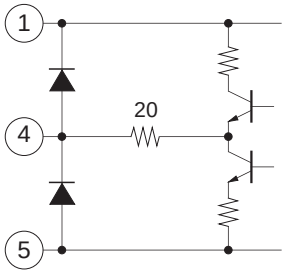
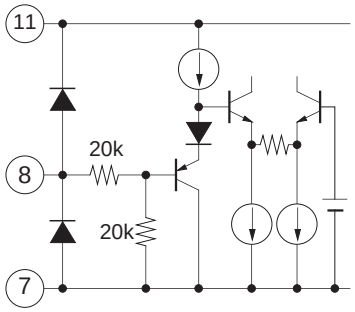
• Supply voltage	V_{CC}	4.75 to 5.30	V
• Operating temperature	Topr	–25 to +75	°C

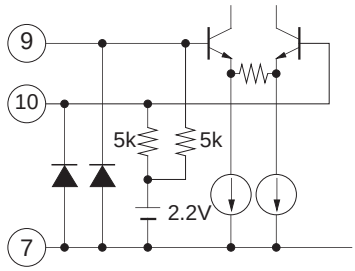
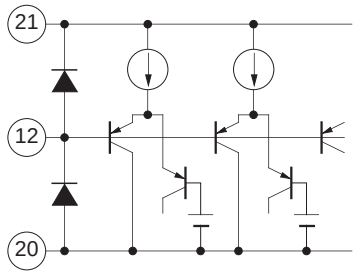
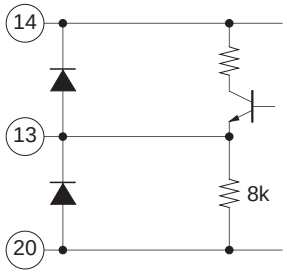
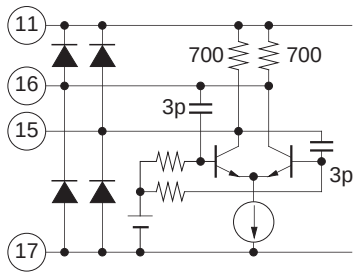
E97650A84-TE

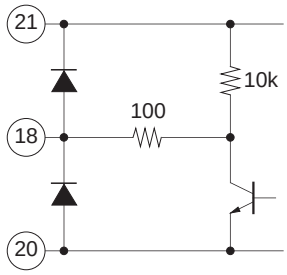
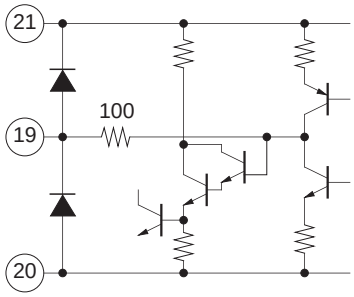
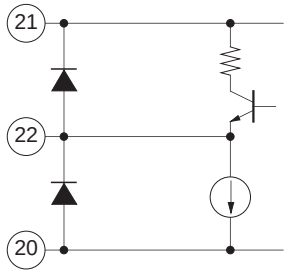
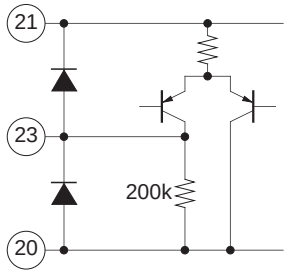
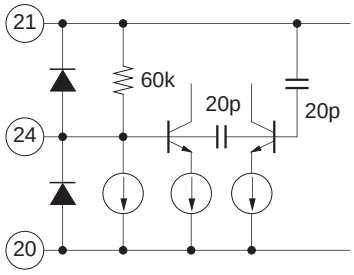
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
1	IQVCC	5 V		IQ output circuit VCC.
2	QOUT	2.7 V		Q output.
3	XCONT	Open or 5 V when using 4 MHz crystal ; 0 V when using 10 MHz crystal.		Switching pin for reference divider frequency-division ratio. This is set to 80 frequency divisions when open or connected to VCC; 200 frequency divisions when connected to GND.
4	IOUT	2.7 V		I output.
5	IQGND	0 V		IQ output circuit GND.
6	GND	0 V		GND.
7	RFGND	0 V		RF circuit (AGCAmp, MIXER) GND.
8	AGC	0 to 4 V		AGCAmp gain adjustment.

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
9	RFIN2	2.1 V		RF signal inputs.
10	RFIN1	2.1 V		
11	RFVCC	5 V		RF circuit (AGCAmp, MIXER, OSC) VCC.
12	NSET	1.6 V		OSC frequency fine-adjustment. The oscillator frequency based at 479.5 MHz is adjustable in ±4 steps of 50 kHz by applying a voltage of 0 to 5 V.
13	LOOUT	4 V		Output for OSC frequency signal divided into 32 frequency divisions.
14	PSVCC	5 V		VCC for 32 frequency division circuit. This is set to open when activating the built-in PLL.
15	OSC2	3.7 V		OSC pins. These pins connect the varicap diode and coil resonance circuit.
16	OSC1	3.7 V		
17	OSCGND	0 V		OSC circuit and phase shifter circuit GND.

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
18	VC	0.3 V to 5 V		Voltage output for varicap diode making up the VCO.
19	LPF	1.8 V to 3.7 V		Phase comparison output. This pin connects the loop filter.
20	DGND	0 V		PLL circuit GND.
21	DV_{CC}	5 V		PLL circuit V_{CC}.
22	REFOUT	4.1 V		REFOSC output.
23	LOCK	0.01 V when unlocked; 3.2 V when locked		PLL lock/unlock monitor.
24	XTAL	4.4 V		Crystal connection.

Electrical Characteristics

Circuit current (Ta=25 °C, V_{CC}=5 V, see the Electrical Characteristics Measurement Circuit.)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current A	I_{CCA}	Analog circuit current at no signal. Total current of IQV_{CC} and RFV_{CC}.	41	60	80	mA
Circuit current D	I_{CCD}	PLL circuit current. DV_{CC} current.	2	3.5	5.5	mA
Circuit current L	I_{CCPS}	32-frequency division circuit current at no signal. PSV_{CC} current.	1.1	1.6	2.4	mA

AC Characteristics (Ta=25 °C, V_{CC}=5 V, see the Electrical Characteristics Measurement Circuit.)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Input sensitivity	V_{IN}	Iout=10 MHz, 1 Vp-p		–50		dBm
Gain control range	G_{AGC}	Iout=10 MHz, 1 Vp-p, AGC=4 V-0 V	32.5	35	—	dB
Conversion gain	CG	RF=–50 dBm, Iout=10 MHz, AGC=4 V (Full gain)	52	54	57	dB
IQ phase error	BP	RF=–50 dBm, Iout=10 MHz, 1 Vp-p			±4	deg
IQ amplitude error	BV	RF=–50 dBm, Iout=10 MHz, 1 Vp-p			±0.5	dB
Phase frequency error	ΔfBP	RF=–50 dBm, Iout=0 MHz–15 MHz, 1 Vp-p			±0.5	deg
Amplitude frequency error	ΔfBV	RF=–50 dBm, Iout=0 MHz–15 MHz, 1 Vp-p			±0.1	dB
Cut-off frequency	f_C	RF=–50 dBm, Iout=From 1 Vp-p to 3 dB down		25		MHz
Maximum Q output	V_{QMAX}	RF=–30 dBm, Qout=10 MHz, AGC=4 V (Full gain)	2.5	3	3.5	Vp-p
Maximum I output	V_{IMAX}	RF=–30 dBm, Iout=10 MHz, AGC=4 V (Full gain)	2.5	3	3.5	Vp-p
Noise figure	NF	Iout=10 MHz, AGC=4 V (Full gain), DSB		9		dB
Third-order intermodulation distortion	IM3	RF1=489.5 MHz, RF2=490.5 MHz, Iout=1 Vp-p		32		dB
Local oscillation phase noise	CN	RF=–50 dBm, Iout=10 MHz, 1Vp-p, 10 kHz offset		–88		dBc/Hz
PLL reference leak	ref_{LK}	RF=–50 dBm, Iout=10 MHz, 1Vp-p, 50 kHz S/I		–81		dB
RF pin local oscillation leak	RF_{LK}	AGC=4 V, f=479.5 MHz		–21		dBm
QOUT pin local oscillation leak	Q_{LK1}	AGC=4 V, f=479.5 MHz		–34		dBm
	Q_{LK2}	AGC=0 V, f=479.5 MHz		–40		
IOUT pin local oscillation leak	I_{LK1}	AGC=4 V, f=479.5 MHz		–34		dBm
	I_{LK2}	AGC=0 V, f=479.5 MHz		–40		
REFout pin local oscillation leak	REFLK	f=479.5 MHz		–34		dBm
RF input admittance	rπ	f=479.5 MHz, AGC=4 V (Full gain)		1.25 k		Ω
	Cπ			1.4		pF

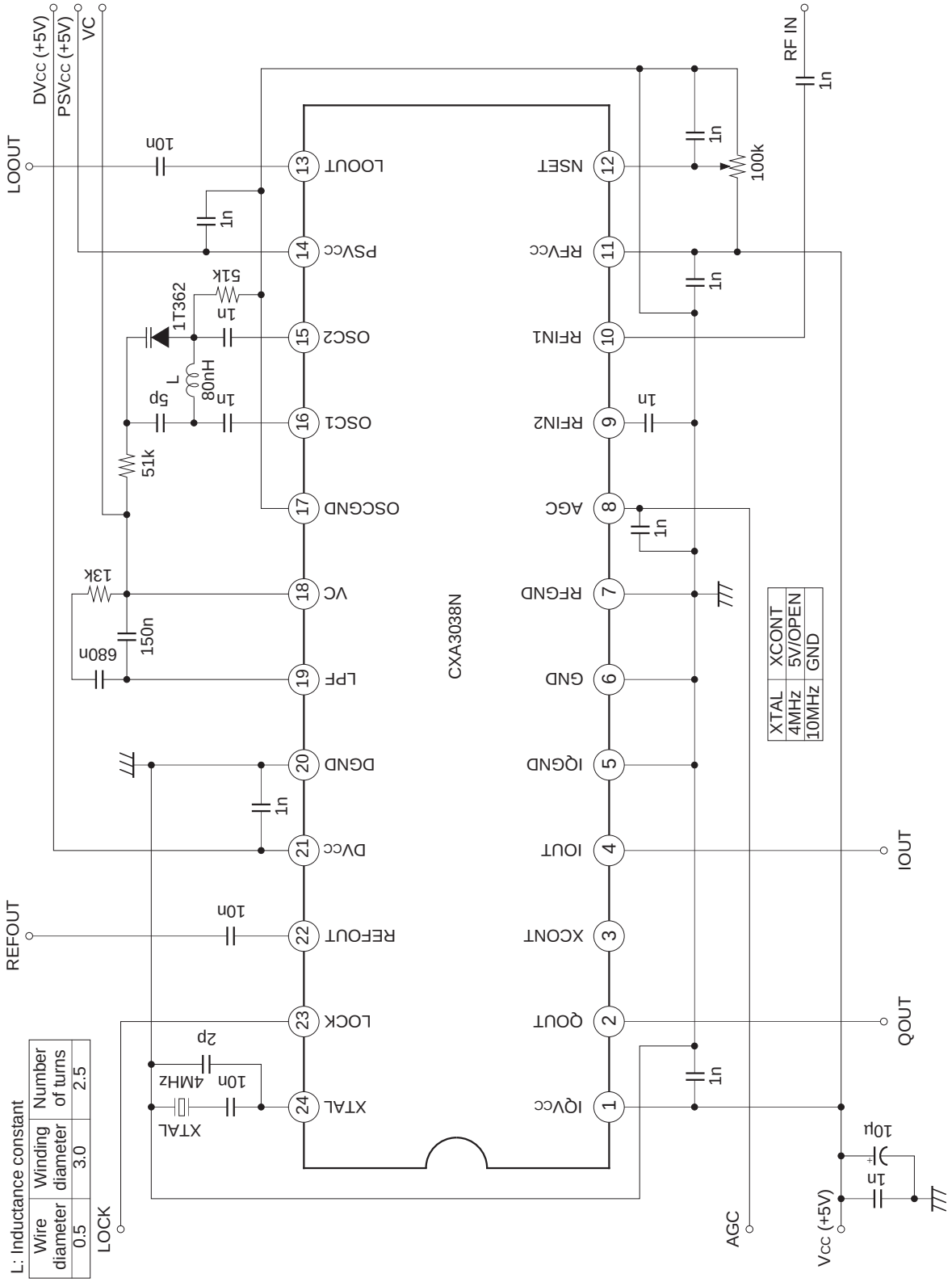
Measured value for untuned inputs.

Noise figure is the direct reading value from the NF meter.

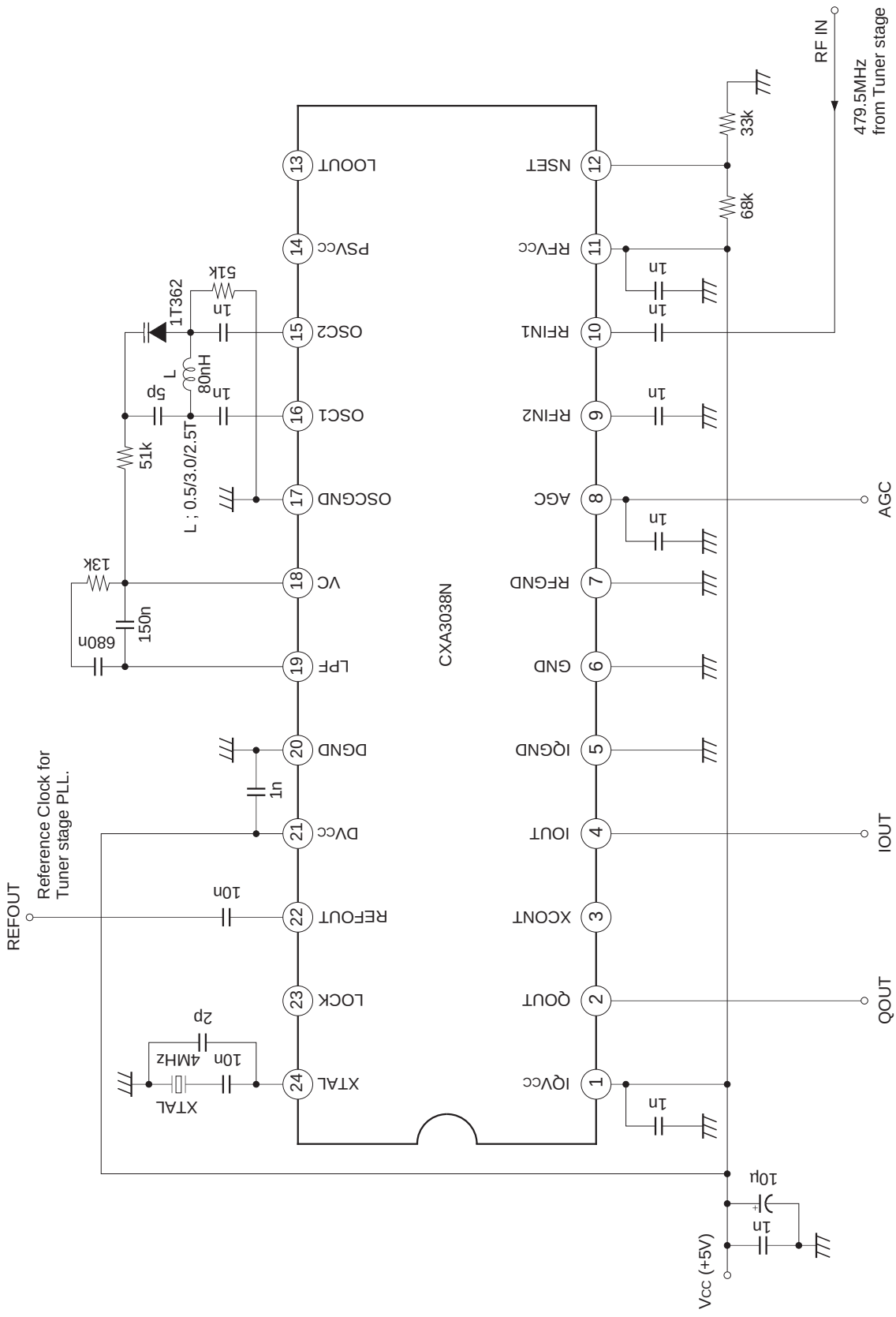
PLL Block (Ta=25 °C, V_{CC}=5 V, see the Electrical Characteristics Measurement Circuit.)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
LPF (charge pump)						
H output current	I_{LPFH}			–50		µA
L output current	I_{LPFL}			50		µA
VC						
Output voltage range	V_{VCH}	XCONT=OPEN, PLL lock	0.3		V_{CC}	V
LOCK						
H output voltage	V_{LH}	XTAL=4 MHz, XCONT=OPEN, PLL lock	2.8	3.2	4.2	V
L output voltage	V_{LL}	XTAL=4 MHz, XCONT=GND, PLL unlock	0	0.01	0.2	V
REFOUT						
Output frequency	f_{REF}	XTAL=4 MHz		4.000		MHz
Output amplitude	V_{REF}	XTAL=4 MHz	230	280	400	mVp-p
LOOUT (32 frequency divisions)						
Output frequency	f_{LO}	OSC=479.5 MHz during PLL lock		14.9844		MHz
Output amplitude	V_{LO}	OSC=479.5 MHz during PLL lock	300	380	500	mVp-p
OSC control						
479.7 MHz control voltage	f+4	NSET=0 V, $f_{0\ V}$–f_0=$f_{\Delta 4}$	0.597 V_{CC}		V_{CC}	V
479.65 MHz control voltage	f+3	NSET=0.4 V, $f_{0.4\ V}$–f_0=$f_{\Delta 3}$	0.517 V_{CC}		0.590 V_{CC}	V
479.6 MHz control voltage	f+2	NSET=0.8 V, $f_{0.8\ V}$–f_0=$f_{\Delta 2}$	0.438 V_{CC}		0.515 V_{CC}	V
479.55 MHz control voltage	f+1	NSET=1.2 V, $f_{1.2\ V}$–f_0=$f_{\Delta 1}$	0.358 V_{CC}		0.436 V_{CC}	V
479.5 MHz control voltage	f0	NSET=1.6 V	0.279 V_{CC}		0.356 V_{CC}	V
479.45 MHz control voltage	f–1	NSET=2.0 V, $f_{2.0\ V}$–f_0=$f_{\Delta -1}$	0.199 V_{CC}		0.277 V_{CC}	V
479.4 MHz control voltage	f–2	NSET=2.4 V, $f_{2.4\ V}$–f_0=$f_{\Delta -2}$	0.120 V_{CC}		0.197 V_{CC}	V
479.35 MHz control voltage	f–3	NSET=2.6 V, $f_{2.6\ V}$–f_0=$f_{\Delta -3}$	0.042 V_{CC}		0.118 V_{CC}	V
479.3 MHz control voltage	f–4	NSET=3.2 V, $f_{3.2\ V}$–f_0=$f_{\Delta -4}$	0		0.04 V_{CC}	V

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

(See the Electrical Characteristics Measurement Circuit.)

Oscillator circuit

- This is a differential amplification-type oscillator circuit, and it is oscillated by connecting an LC parallel resonance circuit via a coupling capacitance between Pin 15 and Pin 16.
  A varicap diode is used as a capacitor for the LC parallel resonance circuit to configure the VCO. Set the L value so that the OSC oscillation frequency is approximately 480 MHz when a voltage of 2.5 V is applied to the varicap diode.
- The oscillator signal is injected into the phase shifter circuit.

Phase shifter circuit

- This is a phase shifter having CR configuration.
  This circuit produces two local signals having a 90° phase difference at 479.5 MHz and injects these signals to the IQ mixer circuit.

AGC amplifier circuit

- An IF signal (480 MHz band) from the tuner stage is input to Pins 9 and 10.
  This IF signal which is input to Pins 9 and 10 is amplified by the AGC amplifier and injected into the IQ mixer circuit.
- The gain can be adjusted by applying the AGC voltage to Pin 8.
  The applied AGC voltage ranges from 0 to 4 V, with the minimum gain at 0 V and the maximum gain at 4 V.

IQ mixer circuit

- This is a double-balance mixer-type circuit consisting of two mixer circuits.
- The IF signal amplified by the AGC amplifier is converted into a base band signal by the local signal.

Low-pass filter circuit

- This is a low-pass filter with a CR configuration.
- The cut-off frequency is set at 25 MHz (–3 dB point).

Output amplifier circuit

- The signal is converted to a base band signal by the I and Q mixer circuits, and the high-frequency component is removed by the low-pass filter. This signal is then amplified by the output amplifier circuit and output to Pin 2 as a Q signal. In the same way, the I signal is output to Pin 4.
- The output is low impedance.

PLL circuit (when Pin 21 is connected to Vcc)

- A PLL is formed by connecting the anode of the LC parallel resonance circuit varicap diode to the Pin 18 output via a high resistance of approximately 10 kΩ and connecting a loop filter between Pin 18 and Pin 19.
- The PLL circuit consists of a main divider, reference divider, phase comparator, charge pump, and reference oscillator.
- The frequency dividing data is included in the main divider, making external data settings unnecessary.
- The reference frequency has been designed at 50 kHz.
- Fine adjustment of the VCO frequency can be performed by changing the frequency dividing value of the main divider through an applied voltage to Pin 12. This allows adjustment in ±4 steps at 50 kHz intervals based at 479.5 MHz as shown in the table below.

Pin 12 voltage [V]	Frequency dividing value	VCO oscillation frequency [MHz]
0.597 Vcc or more	9594	479.70
0.517Vcc to 0.595Vcc	9593	479.65
0.438Vcc to 0.515Vcc	9592	479.60
0.358Vcc to 0.436Vcc	9591	479.55
0.279Vcc to 0.356Vcc	9590	479.50
0.199Vcc to 0.277Vcc	9589	479.45
0.120Vcc to 0.197Vcc	9588	479.40
0.042Vcc to 0.118Vcc	9587	479.35
0 to 0.04Vcc	9586	479.30

- The reference divider has two types of frequency dividing data, 80 and 200.
- Either 4 MHz or 10 MHz can be selected for the crystal oscillator. When using the 4 MHz crystal oscillator, opening Pin 3 will select a frequency dividing value of 80 for the reference divider, and the reference frequency will become 50 kHz.

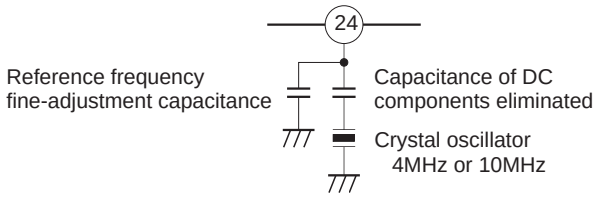
  In the same way, when using the 10 MHz crystal oscillator, connecting Pin 3 to GND will select a frequency dividing value of 200 for the reference divider, and the reference frequency will become 50 kHz.

  This is summarized in the table below.

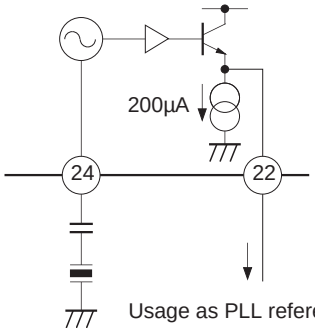
Crystal oscillator	Pin 3 voltage	Frequency dividing value of the reference divider	Reference frequency
4 MHz	Open	80	50 kHz
10 MHz	0.8 V or less	200	50 kHz

Reference oscillator circuit

- This is oscillated by connecting a crystal oscillator (4 MHz or 10 MHz) between Pin 24 and GND.
- The input capacitance of Pin 24 is approximately 14 pF. Therefore, a crystal with a load capacitance of 12 pF is recommended. When connecting a crystal with a large load capacitance of 16 pF or so, connect a low capacitance between Pin 24 and GND as shown in the figure below, and adjust the frequency.

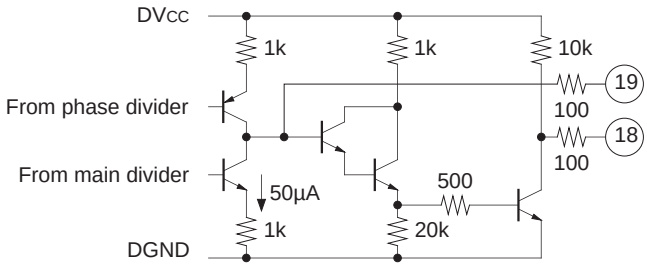


- The reference oscillator signal is sent to the reference buffer circuit and output from Pin 22 by the emitter follower. The reference oscillator signal becomes the PLL comparison frequency in the IC.
- The output amplitude is approximately 300 mVp-p.



Usage as PLL reference frequency for the tuner block

Charge pump circuit



- The output current of the charge pump has been designed at 50 µA.
- The Pin 18 output voltage ranges from approximately 0.3 V to V_{CC}.
- In the loop filter example for the Electrical Characteristics Measurement Circuit, the lockup time is approximately 25 ms.

32 frequency division circuit (when Pin 14 is connected to V_{CC})

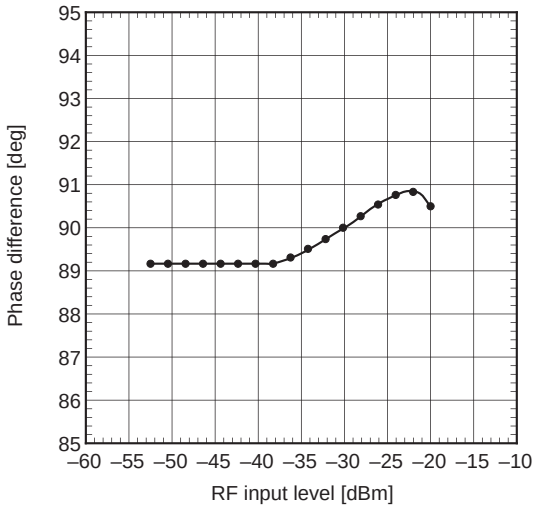
- An oscillation signal is sent from the oscillator circuit to the 32 frequency division circuit via a coupling capacitance. The 32 frequency division signal is output from Pin 13 by the counter.
- The output is approximately 400 mVp-p ECL output.

Notes on Operation

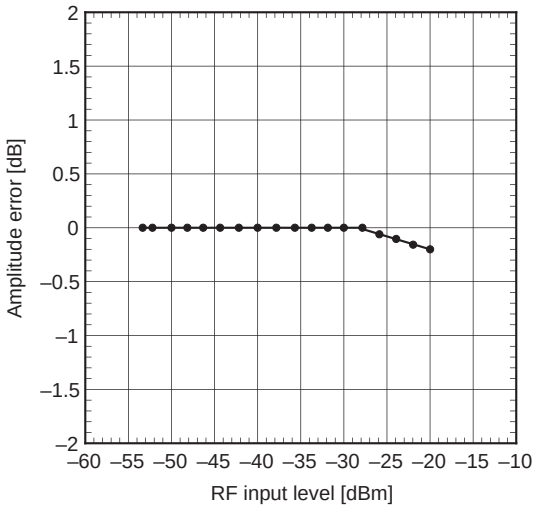
- These circuits use high-frequency processes, and the electrostatic strength is weak.
  Therefore, please be careful of surges and other excessive input.

- The IQ error may vary depending on the connection locations of the GND pattern and V_{CC}-GND bypass capacitors, oscillation amplitude of the oscillator circuit, and other factors.

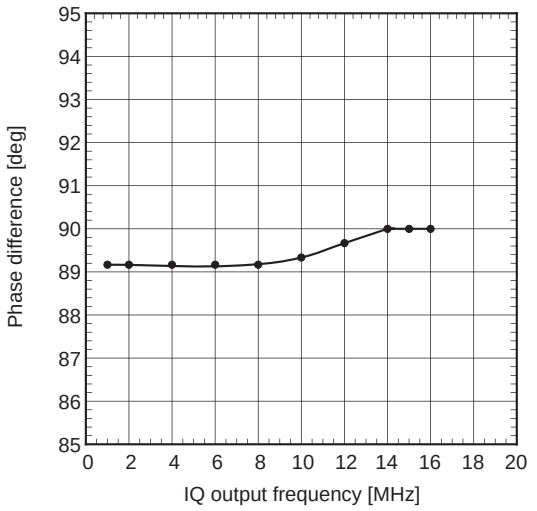
RF input level vs. Phase difference
IQ output frequency=1MHz, QOUT=1Vp-p



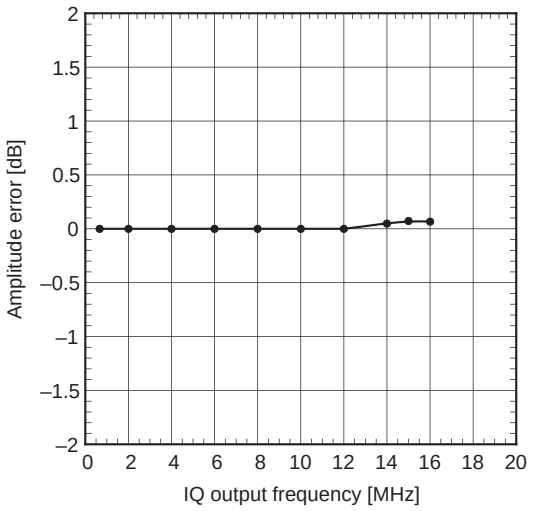
RF input level vs. Amplitude error
IQ output frequency=1MHz, QOUT=1Vp-p



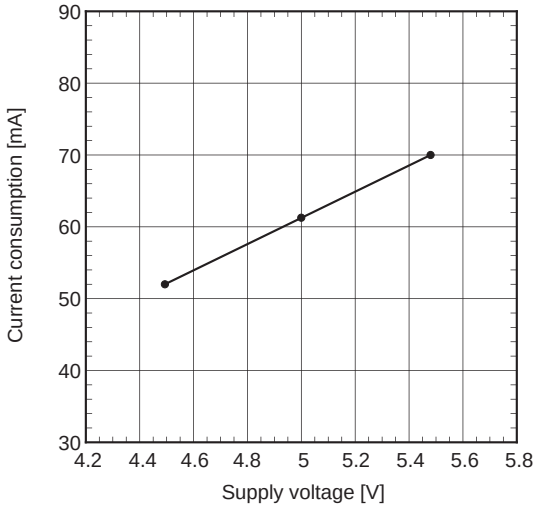
IQ output frequency vs. Phase difference
RF input level=–40dBm, QOUT=1Vp-p



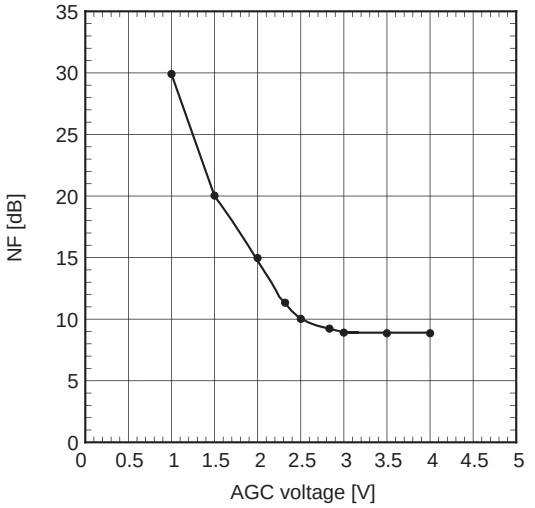
IQ output frequency vs. Amplitude error
RF input level=–40dBm, QOUT=1Vp-p



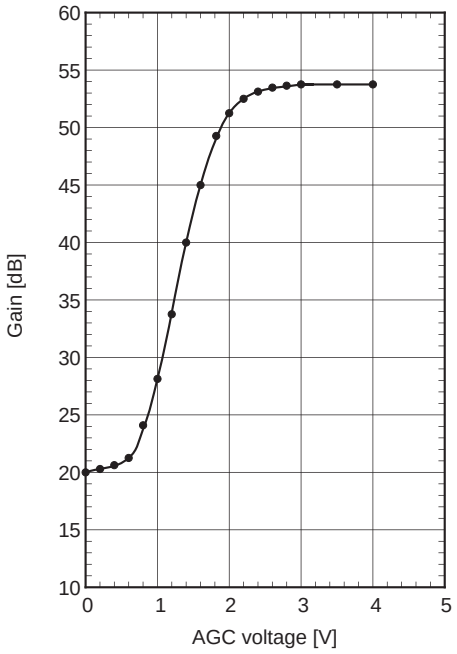
Supply voltage vs. Current consumption
During PLL operation



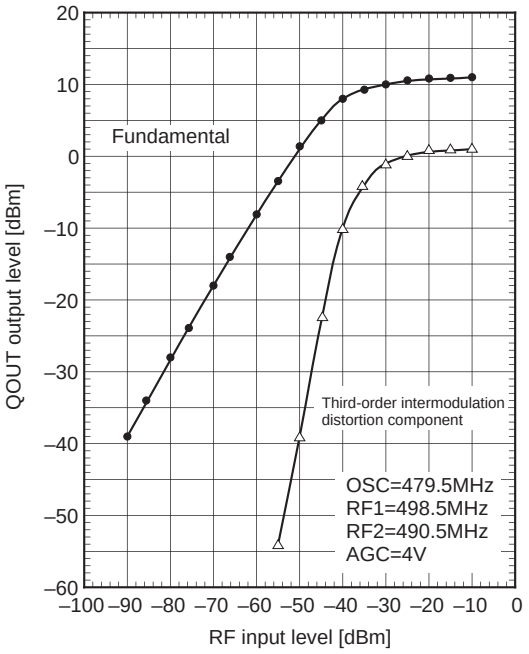
Noise figure characteristics
RF input level=–40dBm, QOUT=10MHz



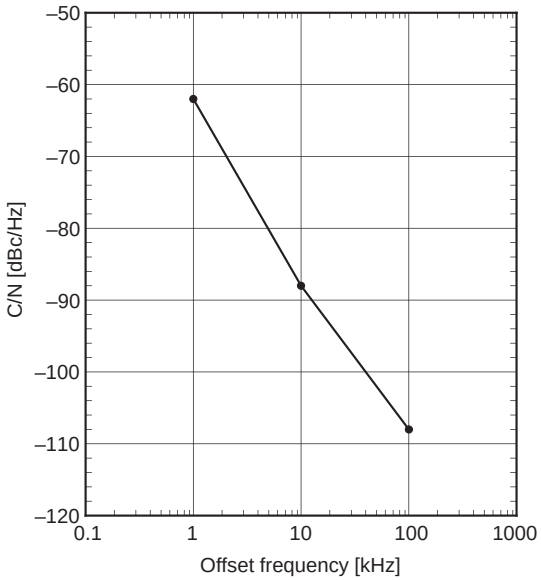
AGC voltage vs. Gain
RF input level=–40dBm, IQ output frequency=1MHz



Third-order intermodulation distortion characteristics

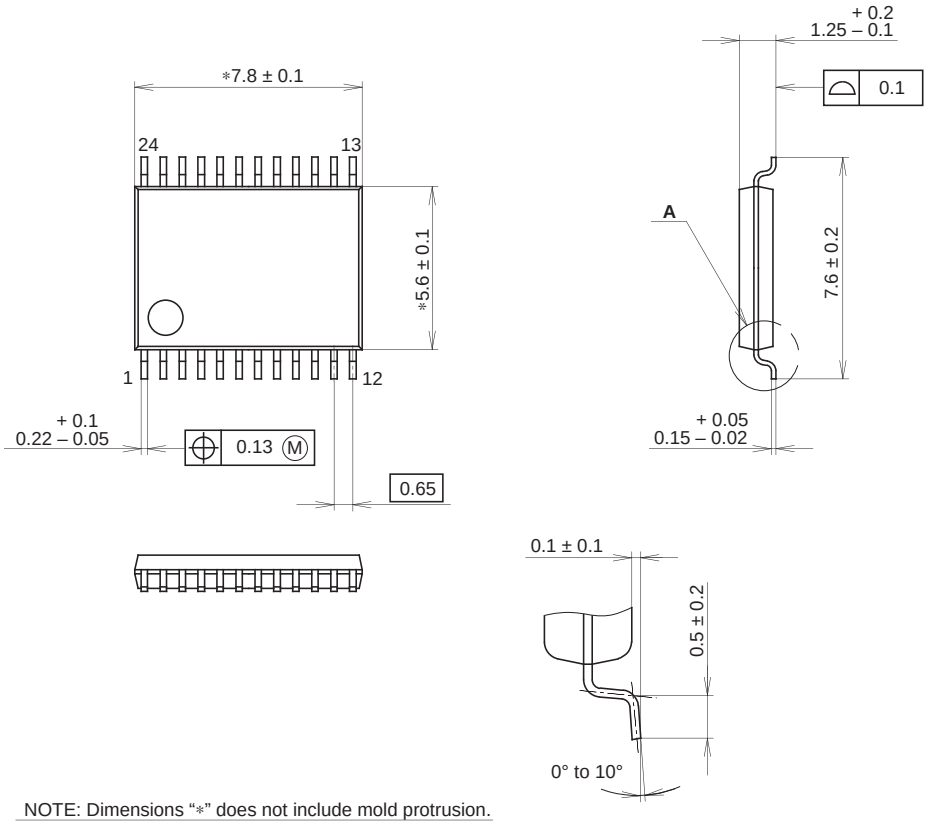


Phase noise characteristics
RF input level=–40dBm, QOUT=1 MHz, 1Vp-p



Package Outline Unit : mm

24PIN SSOP(PLASTIC)



NOTE: Dimensions "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).