SONY

CXD2930BR

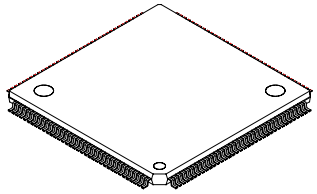
GPS LSI with Built-in 32-bit RISC CPU

Description

The CXD2930BR is a dedicated LSI for the GPS (Global Positioning System) satellite-based position measurement system. This LSI contains a 32-bit RISC CPU, RAM, UART, timer, etc.

This LSI, used together with an external ROM and RF LSI (CXA1951AQ), enables the configuration of a 3-chip system capable of measuring its position anywhere on the globe.

144 pin LQFP (Plastic)



Features

- 16-channel GPS receiver capable of simultaneously receiving 16 satellites
- Supports DARC system FM multiplexed differential GPS
- All-in-view measurement
- 2-satellite measurement
- Timer supporting GPS time
- High performance 32-bit RISC CPU
- 32K-byte RAM
- 3-channel UART
  - Baud rate generator
  - Supports 1.2K, 2.4K, 4.8K, 9.6K, 19.2K and 38.4K baud
  - Supports 1/2/4-byte buffer mode
- 23-bit general-purpose I/O port capable of defining input/output independently for each bit

Structure

Silicon gate CMOS IC

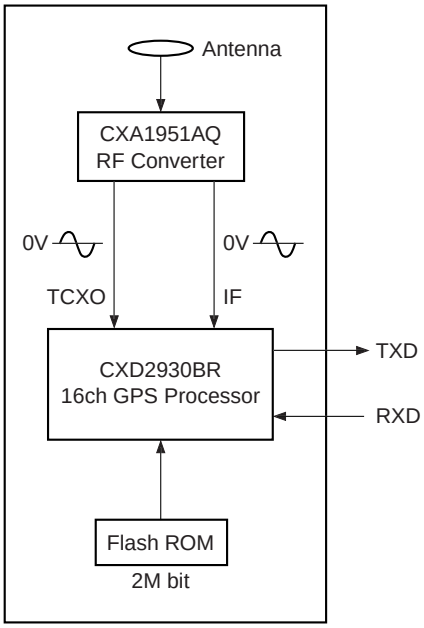
Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–40 to +85	°C

E98307A96-PS

Performance

- Reception frequency
  1575.42MHz (L1 band, CA code)
- Reception sensitivity (using the CXA1951AQ in the RF block)
  –130dBm or less
- Time to first fix* (time until initial measurement after power-on)
  Cold start (without ephemeris and almanac)
    35 to 60s
  Warm start (without ephemeris with almanac)
    34 to 50s
  Hot start (with ephemeris and almanac)
    6 to 20s
  Reacquisition time (interrupt recovery time)
    Less than 5 minutes: < 3 to 6s
    5 minutes or more: < 6 to 10s
- Positioning accuracy
  Stand alone (GPS unit only)
    1σ : < 30m
    3σ : < 90m
  DGPS (differential GPS)
    1σ : < 6m
    3σ : < 18m
- Measurement data update time
  Every 1s
- Communication method
  Sony standard serial communication
  Supports NMEA

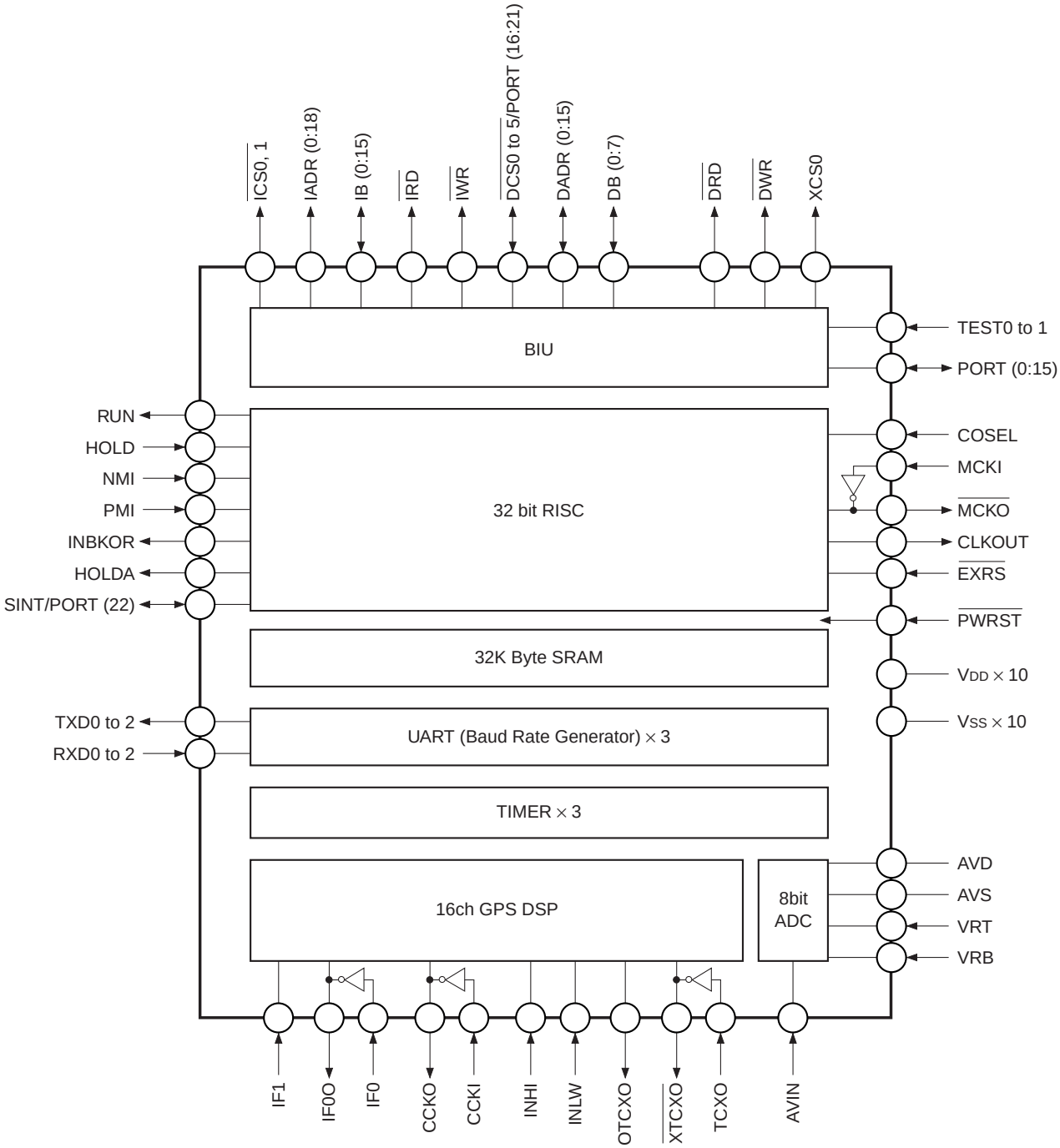


GPS Receiver System Diagram Using the CXD2930BR

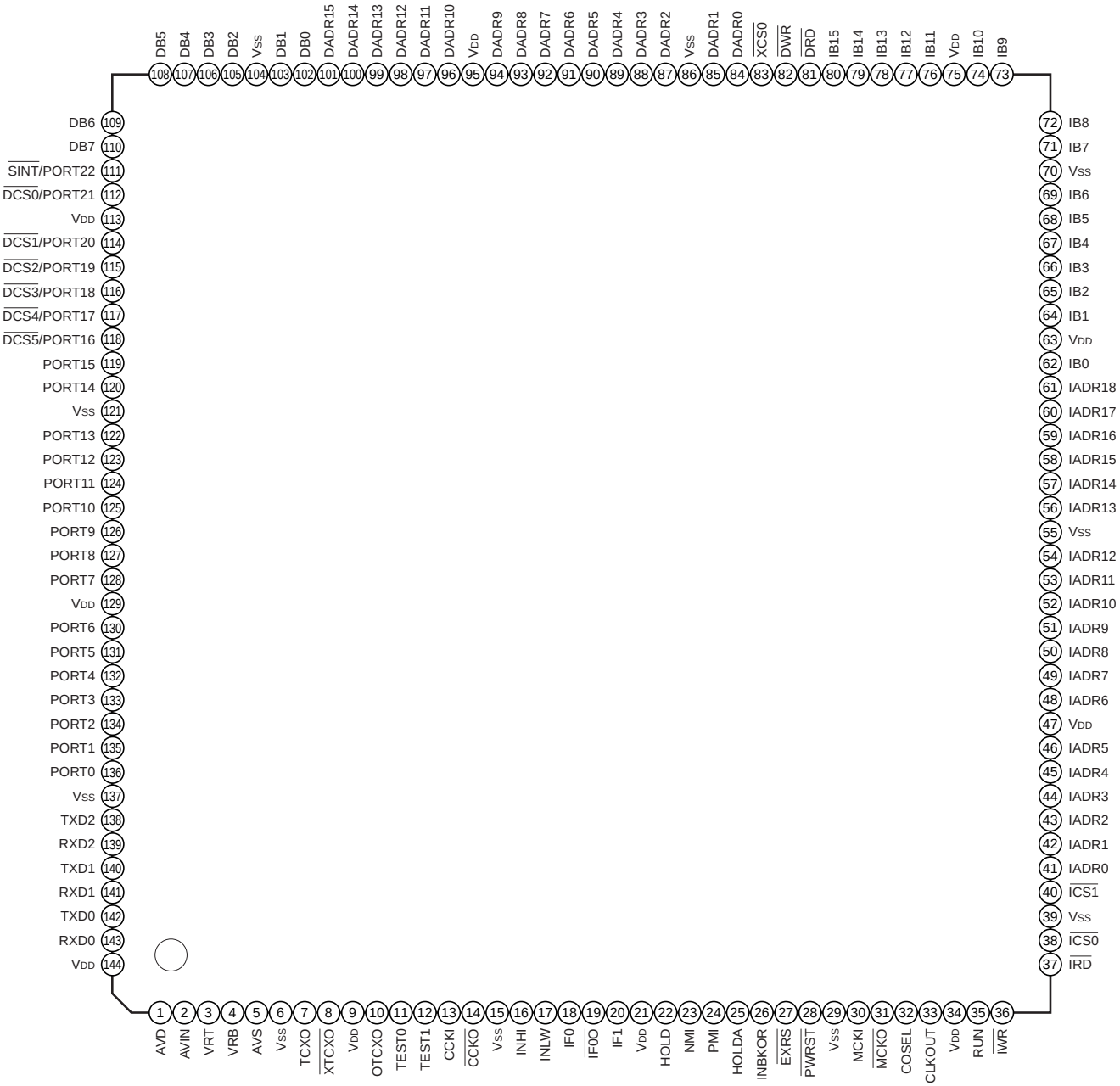
* The noted values may be exceeded depending on the operating environment and other conditions.

The above performance values are as of February 1998. Sony reserves the right to change performance without prior notice. Accordingly, the above performance values should be used only as reference data.

Block Diagram



Pin Configuration



Pin Configuration

Pin No.	Symbol	I/O	Description
1	AVD	—	A/D converter power supply.
2	AVIN	I	Analog input.
3	VRT	I	Reference input.
4	VRB	I	
5	AVS	—	A/D converter GND.
6	V_{SS}	I	GND
7	TCXO	I	TCXO binary conversion circuit/crystal oscillator.
8	$\overline{\text{XTCXO}}$	O	
9	V_{DD}	—	Power supply.
10	OTCXO	O	TCXO clock output.
11	TEST0	I	Test. Fixed to low level.
12	TEST1	I	
13	CCKI	I	Timer oscillation circuit. (32.768kHz ± 100ppm)
14	$\overline{\text{CCKO}}$	O	
15	V_{SS}	—	GND
16	INHI	I	Fixed to low level.
17	INLW	I	Fixed to low level.
18	IF0	I	IF signal binary conversion circuit.
19	IF0O	O	
20	IF1	I	IF signal input 1. Input the binary-converted input signal.
21	V_{DD}	—	Power supply.
22	HOLD	I	Hold input signal. Hold when high level.
23	NMI	I	Non maskable interrupt.
24	PMI	I	Power management interrupt.
25	HOLDA	O	Hold acknowledge signal.
26	INBKOR	O	Break signal for debugging.
27	$\overline{\text{EXRS}}$	I	Reset input signal.
28	$\overline{\text{PWRST}}$	I	Connect to main power supply. Leave open during backup.
29	V_{SS}	—	GND
30	MCK	I	CPU clock oscillation circuit.
31	$\overline{\text{MCKO}}$	O	
32	COSEL	I	CPU clock select signal. Selects TCXO clock when low level; MCK clock when high level.
33	CLKOUT	O	CPU clock output.

Pin No.	Symbol	I/O	Description
34	V_{DD}	—	Power supply.
35	RUN	O	Signal output indicating CPU operating status.
36	$\overline{IWR}$	O	Write signal output for instruction ROM.
37	$\overline{IRD}$	O	Read signal for instruction ROM.
38	$\overline{ICS0}$	O	Chip select 0 for instruction ROM.
39	V_{SS}	—	GND
40	$\overline{ICS1}$	O	Chip select 1 for instruction ROM.
41	IADR0	O	(LSB)
42	IADR1	O	Address signal for instruction ROM.
43	IADR2	O	
44	IADR3	O	
45	IADR4	O	
46	IADR5	O	
47	V_{DD}	—	Power supply.
48	IADR6	O	Address signal for instruction ROM.
49	IADR7	O	
50	IADR8	O	
51	IADR9	O	
52	IADR10	O	
53	IADR11	O	
54	IADR12	O	
55	V_{SS}	—	GND
56	IADR13	O	Address signal for instruction ROM.
57	IADR14	O	
58	IADR15	O	
59	IADR16	O	
60	IADR17	O	
61	IADR18	O	(MSB)
62	IB0	O	(LSB) Data bus I/O for instruction ROM.
63	V_{DD}	—	Power supply.
64	IB1	I/O	Data bus I/O for instruction ROM.
65	IB2	I/O	
66	IB3	I/O	
67	IB4	I/O	
68	IB5	I/O	
69	IB6	I/O	

Pin No.	Symbol	I/O	Description
70	V_{SS}	—	GND
71	IB7	I/O	Data bus I/O for instruction ROM.
72	IB8	I/O	
73	IB9	I/O	
74	IB10	I/O	
75	V_{DD}	—	Power supply.
76	IB11	I/O	Data bus I/O for instruction ROM.
77	IB12	I/O	
78	IB13	I/O	
79	IB14	I/O	
80	IB15	I/O	(MSB)
81	$\overline{DRD}$	O	Read signal for external expansion data memory.
82	$\overline{DWR}$	O	Write signal for external expansion data memory.
83	$\overline{XCS0}$	O	Chip select signal for external expansion data memory.
84	DADR0	I/O	(LSB) Address I/O for external expansion data memory.
85	DADR1	I/O	
86	V_{SS}	—	GND
87	DADR2	I/O	Address I/O for external expansion data memory.
88	DADR3	I/O	
89	DADR4	I/O	
90	DADR5	I/O	
91	DADR6	I/O	
92	DADR7	I/O	
93	DADR8	I/O	
94	DADR9	I/O	
95	V_{DD}	—	Power supply.
96	DADR10	I/O	Address I/O for external expansion data memory.
97	DADR11	I/O	
98	DADR12	I/O	
99	DADR13	I/O	
100	DADR14	I/O	
101	DADR15	I/O	
102	DB0	I/O	
103	DB1	I/O	(MSB)
104	V_{SS}	—	GND

Pin No.	Symbol	I/O	Description
105	DB2	I/O	(LSB)
106	DB3	I/O	
107	DB4	I/O	Data bus I/O for external expansion data memory.
108	DB5	I/O	
109	DB6	I/O	
110	DB7	I/O	(MSB)
111	$\overline{\text{SINT}}$/PORT22	I/O	External interrupt input signal/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
112	$\overline{\text{DCS0}}$/PORT21	I/O	Chip select for external expansion data memory/general-purpose I/O port. This pin can be used as a general-purpose I/O port according to the internal registers.
113	V_{DD}	—	Power supply.
114	$\overline{\text{DCS1}}$/PORT20	I/O	Chip select for external expansion data memory/general-purpose I/O port. These pins can be used as general-purpose I/O ports according to the internal registers.
115	$\overline{\text{DCS2}}$/PORT19	I/O	
116	$\overline{\text{DCS3}}$/PORT18	I/O	
117	$\overline{\text{DCS4}}$/PORT17	I/O	
118	$\overline{\text{DCS5}}$/PORT16	I/O	
119	PORT15	I/O	General-purpose I/O port.
120	PORT14	I/O	
121	V_{SS}	—	GND
122	PORT13	I/O	General-purpose I/O port.
123	PORT12	I/O	
124	PORT11	I/O	
125	PORT10	I/O	
126	PORT9	I/O	
127	PORT8	I/O	
128	PORT7	I/O	
129	V_{DD}	—	Power supply.
130	PORT6	I/O	General-purpose I/O port.
131	PORT5	I/O	
132	PORT4	I/O	
133	PORT3	I/O	
134	PORT2	I/O	
135	PORT1	I/O	
136	PORT0	I/O	

Pin No.	Symbol	I/O	Description
137	V_{SS}	—	GND
138	TXD2	O	UART transmission data output (channel 2).
139	RXD2	I	UART reception data input (channel 2).
140	TXD1	O	UART transmission data output (channel 1).
141	RXD1	I	UART reception data input (channel 1).
142	TXD0	O	UART transmission data output (channel 0).
143	RXD0	I	UART reception data input (channel 0).
144	V_{DD}	—	Power supply.

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to 4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

I/O Pin Capacitance

• Input capacitance	C_{IN}	9 (Max.)	pF
• Output capacitance	C_{OUT}	11 (Max.)	pF
• I/O capacitance	$C_{I/O}$	11 (Max.)	pF

Electrical Characteristics (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1) (CMOS level)	High level	V_{IH} (1)		0.7V_{DD}		V_{DD}	V	*1
	Low level	V_{IL} (1)				0.2V_{DD}	V	
Input voltage (2) (5V interface)	High level	V_{IH} (2)		0.7V_{DD}		5.5	V	*2
	Low level	V_{IL} (2)				0.2V_{DD}	V	
Output voltage (1)	High level	V_{OH} (1)	I_{OH} = –4.0mA	V_{DD} – 0.4			V	*3
	Low level	V_{OL} (1)	I_{OL} = 4.0mA			0.4	V	
Output voltage (2)	High level	V_{OH} (2)	I_{OH} = –8.0mA	V_{DD} – 0.4			V	*4
	Low level	V_{OL} (2)	I_{OL} = 8.0mA			0.4	V	
Output voltage (3)	High level	V_{OH} (3)	I_{OH} = –12.0mA	V_{DD} – 0.4			V	*5
	Low level	V_{OL} (3)	I_{OL} = 12.0mA			0.4	V	
Current consumption in standby mode		ISTB	V_{DD} = 3V		20	70	µA	
			V_{DD} = 1.5V		4	50		
Supply current		I_{DD}	f = 18.414MHz		55		mA	

Applicable pins

*1 Pins 11, 12, 16, 17, 20, 22, 23, 24, 32

*2 Pins 62, 64 to 69, 72 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122 to 128, 130 to 136, 139, 141, 143

*3 Pins 10, 25, 26, 33, 35, 41 to 46, 48 to 54, 56 to 61, 81 to 83, 138, 140, 142

*4 Pins 38, 40, 62, 64 to 69, 71 to 74, 76 to 80, 84, 85, 87 to 94, 96 to 103, 105 to 112, 114 to 120, 122 to 128, 130 to 136

*5 Pins 36, 37

Electrical Characteristics (IF and TCXO binary conversion pins) (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Logical Vth	LVth			$V_{DD}/2$		V	Pins 7, 18
Input amplitude	V_{IN}	f = 50MHz, sin wave	0.8			Vp-p	

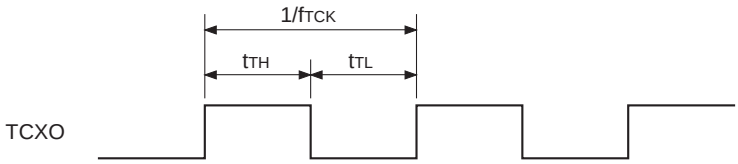
Electrical Characteristics (Crystal oscillator) (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Logical Vth		LVth			$V_{DD}/2$		V	Pin 30
Input voltage	High level	V_{IH}		$0.7V_{DD}$			V	
	Low level	V_{IL}				$0.2V_{DD}$	V	
Output voltage	High level	V_{OH}	I_{OH} = –3mA	$V_{DD}/2$			V	Pin 31
	Low level	V_{OL}	I_{OL} = 3mA			$V_{DD}/2$	V	

AC Characteristics

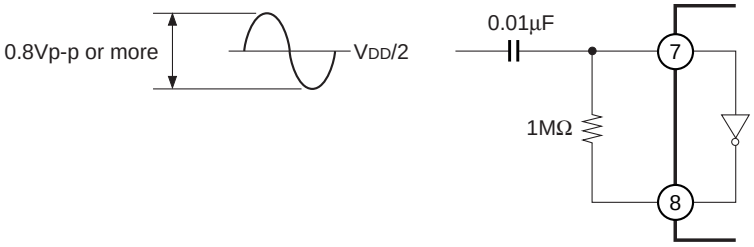
(1) When inputting a pulse to the TCXO pin (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)

When inputting a binary-converted signal

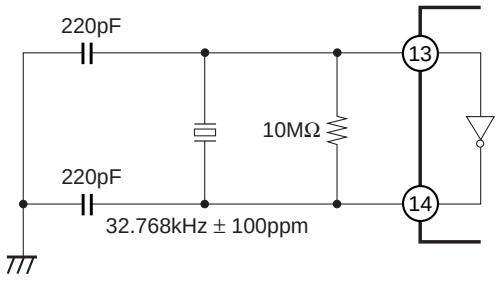


Item	Symbol	Min.	Typ.	Max.	Unit
TCXO clock frequency	f_{TCK}	Typ. – 3ppm	18.414	Typ. + 3ppm	MHz
TCXO clock pulse width	t_{TH}, t_{TL}	24.5		29.9	ns

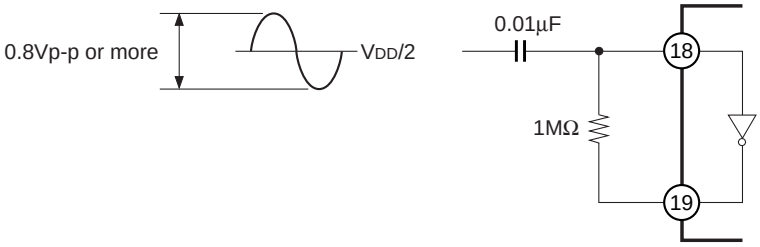
When performing binary conversion with the TCXO and XTCXO pins (Pins 7 and 8)



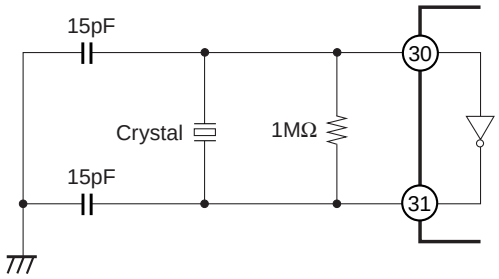
(2) When performing self-oscillation with the CCKI and CCKO pins (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



(3) IF signal input (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



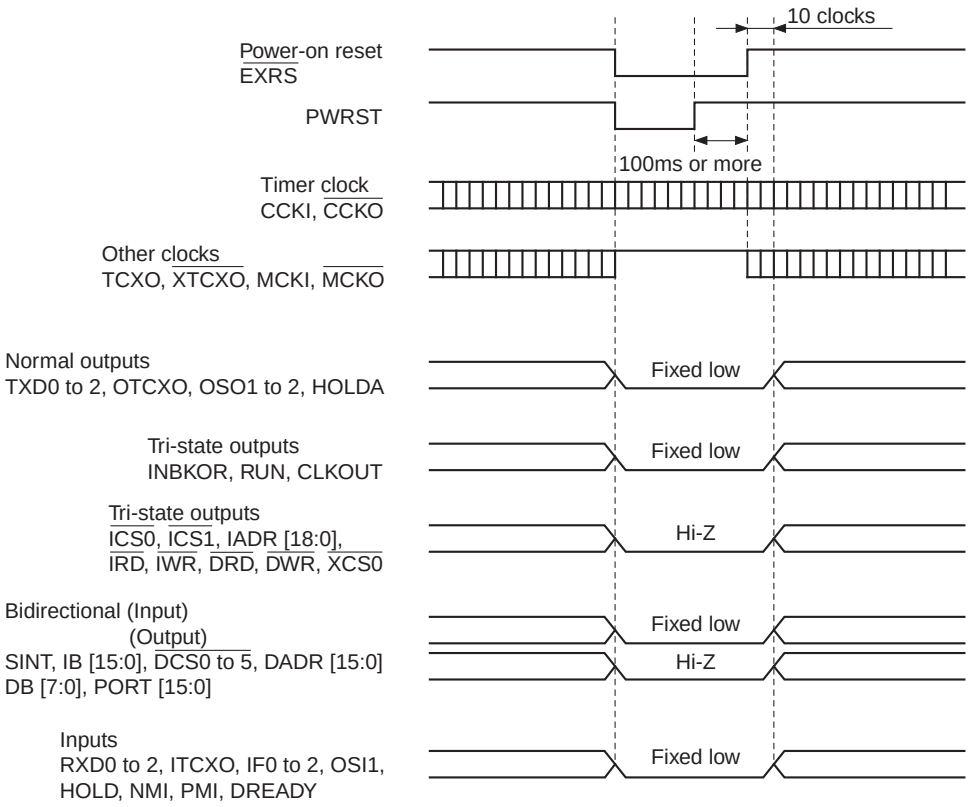
(4) When performing self-oscillation with the MCKI and $\overline{\text{MCKO}}$ pins (V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C)



Battery Backup Mode

The battery backup mode is activated when the power for the GPS receiver is turned off and power-on reset goes to low level. The timer clock continues to operate even when power-on reset goes low, but all other clocks are fixed high and the LSI is set to the low power consumption mode. At this time, the RAM data is held and the registers are initialized.

Battery backup mode is canceled by setting power-on reset to high.

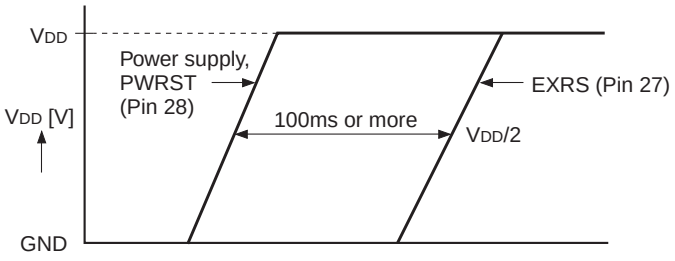


CXD2930BR Startup and Initialization

The CXD2930BR operation is started by setting the reset input signal EXRS (Pin 30) to high level. The timing should satisfy the conditions noted below.

1. During power-on (power-on reset)

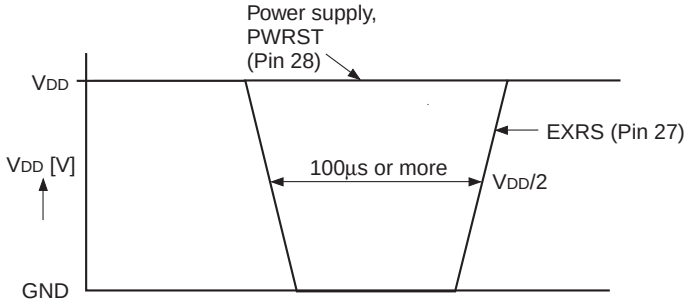
V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C



The PWRST (Pin 28) signal should rise simultaneously with the power supply. The EXRS (Pin 27) signal should rise 100ms or more after the power supply and the PWRST signal have risen.
Note that the PWRST signal should be left open during battery backup.

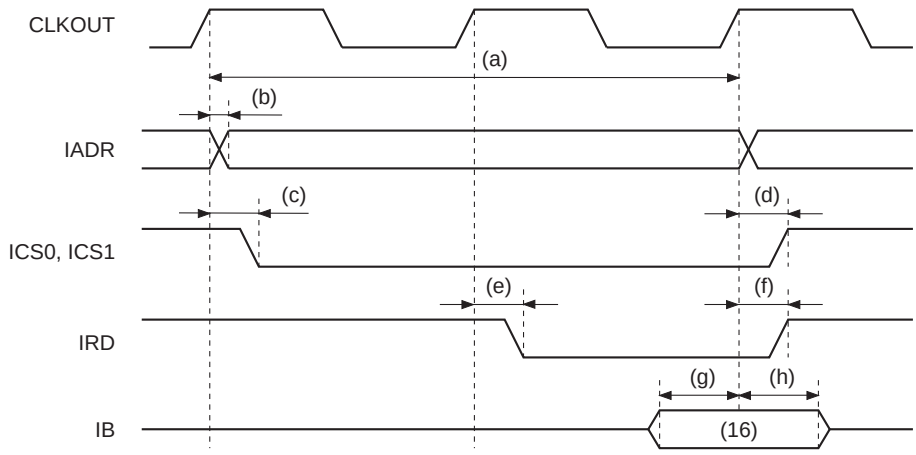
2. Initialization during operation

V_{DD} = 3.0 to 3.6V, Topr = –40 to +85°C



The internal registers can be initialized during operation by setting the EXRS (Pin 27) signal to low level for 100µs or more.
Keep the PWRST (Pin 28) signal at high level at this time.

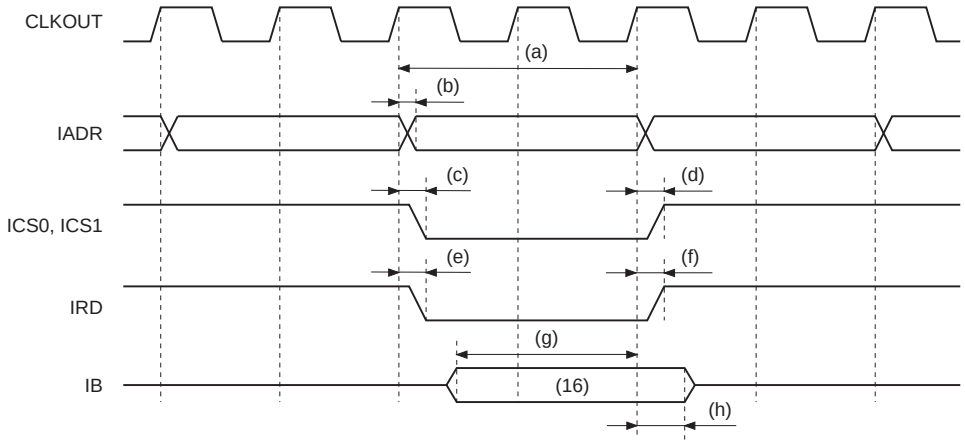
External Command Fetch Timing



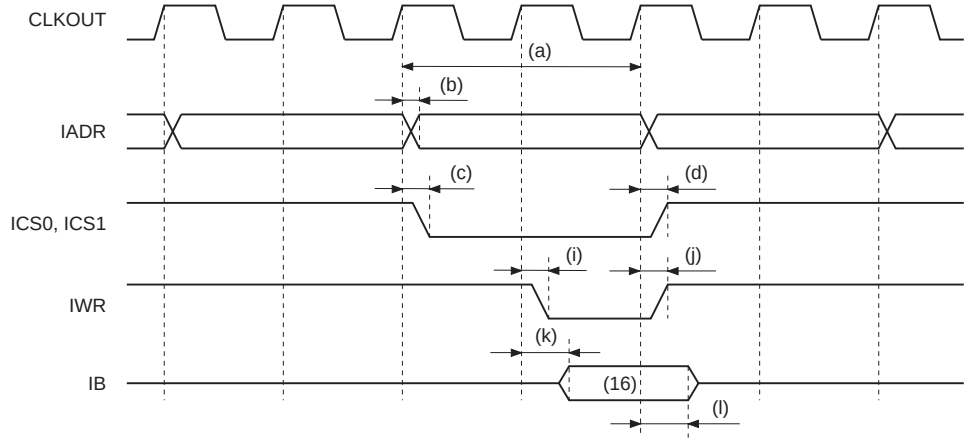
No.	Item	Min.	Typ.	Max.	Unit
(a)	Read cycle time (Fex: @9.207MHz)	—	108	—	ns
(b)	Address delay time	—	—	5	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	9	ns
(e)	Read signal fall delay time	1	—	3	ns
(f)	Read signal rise delay time	1	—	5	ns
(g)	Read data setup time	8	—	—	ns
(h)	Read data hold time	0	—	—	ns

External Data Access Timing (ICS0, ISC1)

(1) Read (half-word access)

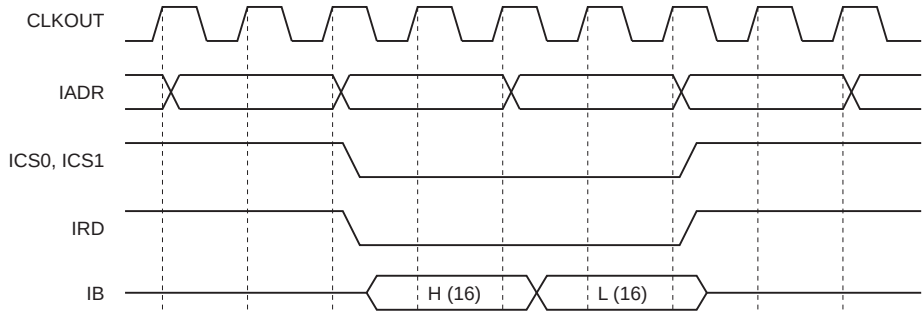


(2) Write (half-word access)

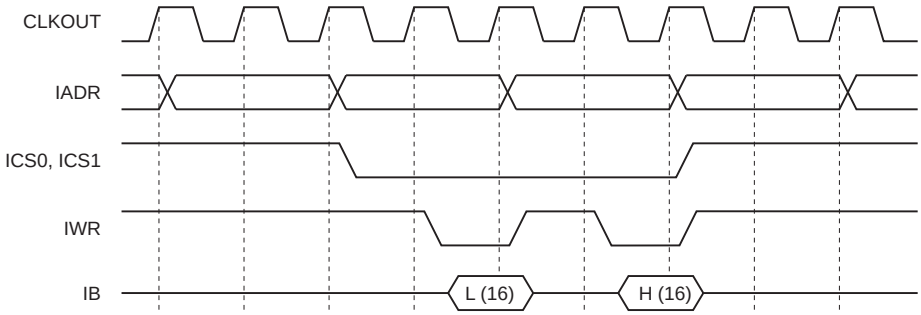


No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @9.207MHz)	—	108	—	ns
(b)	Address delay time	—	—	5	ns
(c)	Chip select fall delay time	2	—	10	ns
(d)	Chip select rise delay time	2	—	9	ns
(e)	Read signal fall delay time	1	—	3	ns
(f)	Read signal rise delay time	1	—	5	ns
(g)	Read data setup time	8	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	5	ns
(l)	Write data hold time	5	—	—	ns

(3) Read (word access)

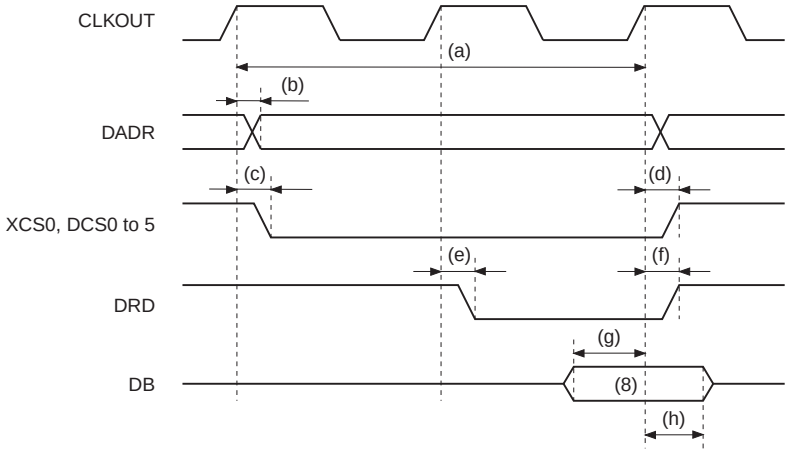


(4) Write (word access)

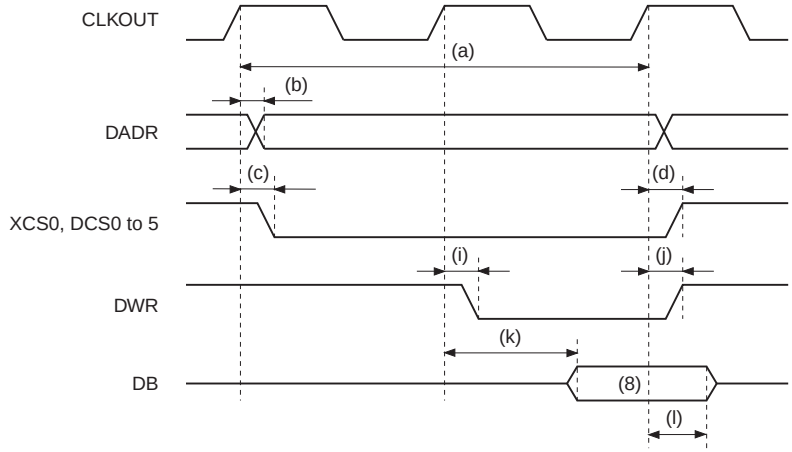


External Data Access Timing (XCS0, DCS0 to 5, no data wait)

(1) Read (byte access, no data wait)

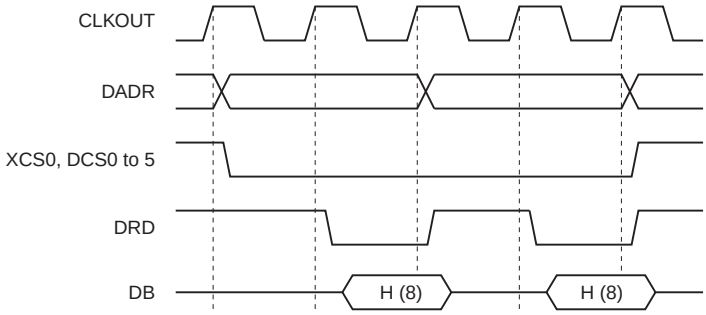


(2) Write (byte access, no data wait)

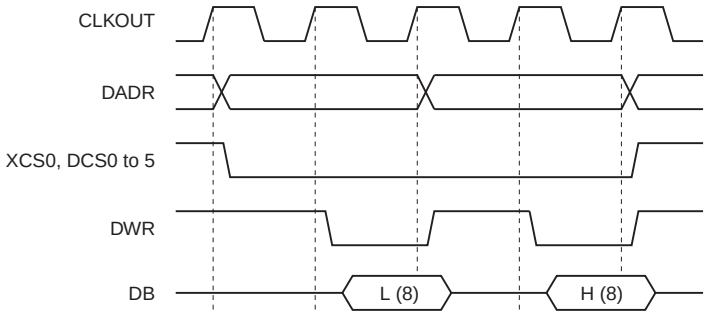


No.	Item	Min.	Typ.	Max.	Unit
(a)	Read/write cycle time (Fex: @9.207MHz)	—	108	—	ns
(b)	Address delay time	—	—	9	ns
(c)	Chip select fall delay time	4	—	13	ns
(d)	Chip select rise delay time	4	—	13	ns
(e)	Read signal fall delay time	2	—	8	ns
(f)	Read signal rise delay time	3	—	10	ns
(g)	Read data setup time	16	—	—	ns
(h)	Read data hold time	0	—	—	ns
(i)	Write signal fall delay time	0	—	1	ns
(j)	Write signal rise delay time	0	—	2	ns
(k)	Write data established time	—	—	7	ns
(l)	Write data hold time	5	—	—	ns

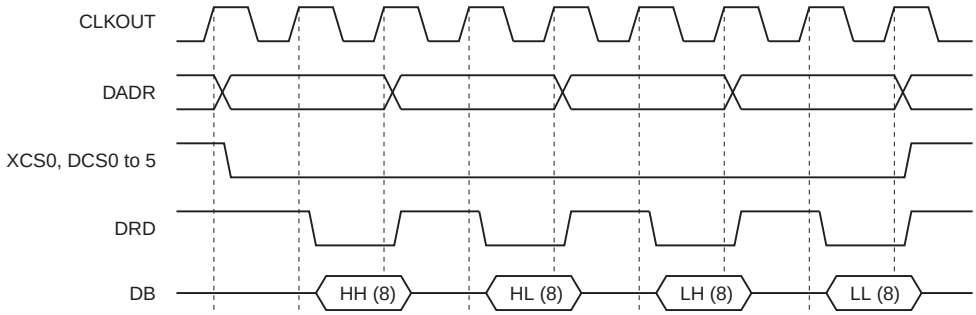
(3) Read (half-word access, no data wait)



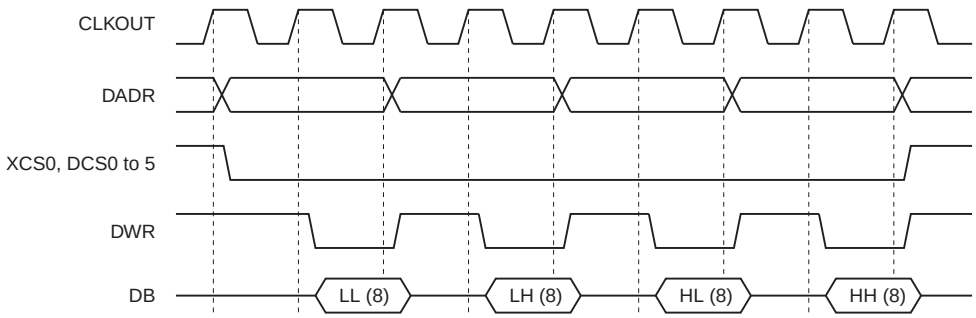
(4) Write (half-word access, no data wait)



(5) Read (word access, no data wait)

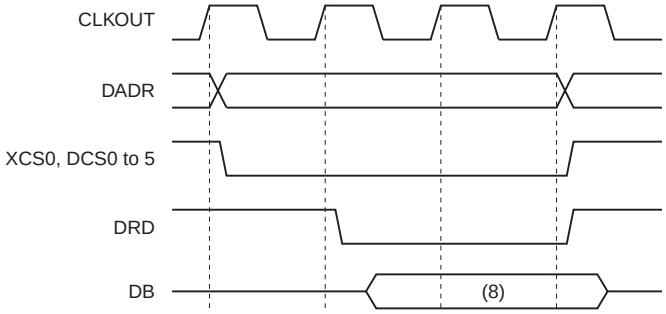


(6) Write (word access, no data wait)

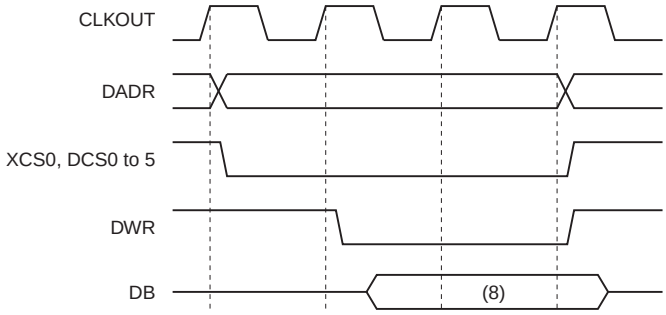


External Data Access Timing (XCS0, DCS0 to 5, with data wait)

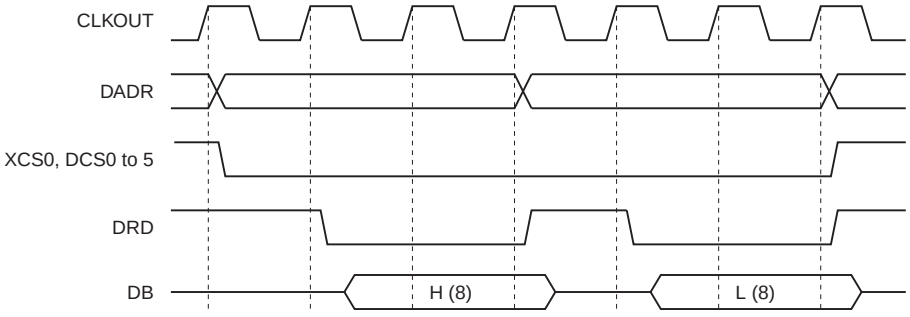
(1) Read (byte access, with data wait)



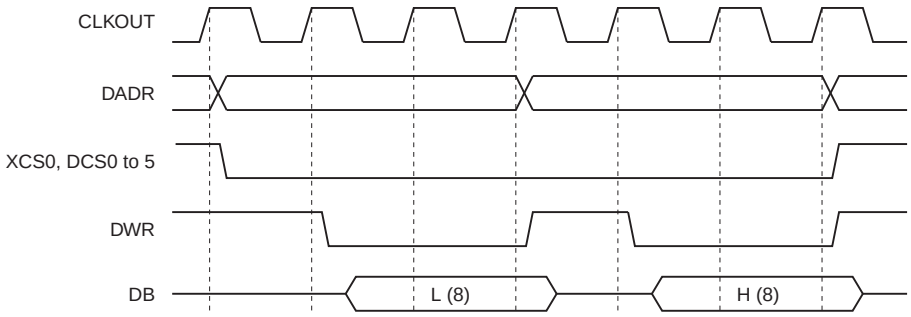
(2) Write (byte access, with data wait)



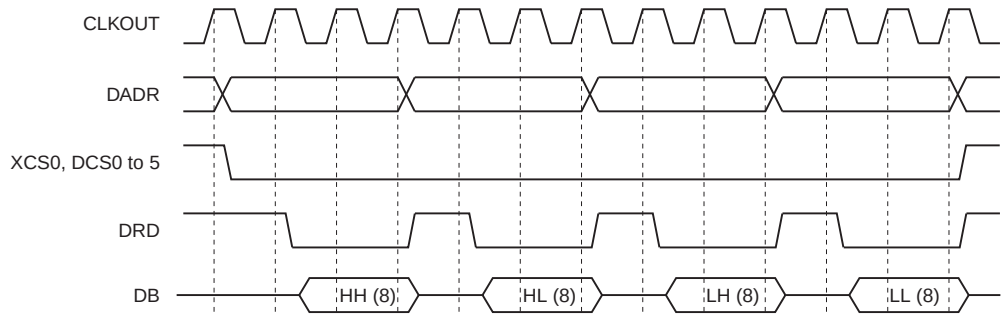
(3) Read (half-word access, with data wait)



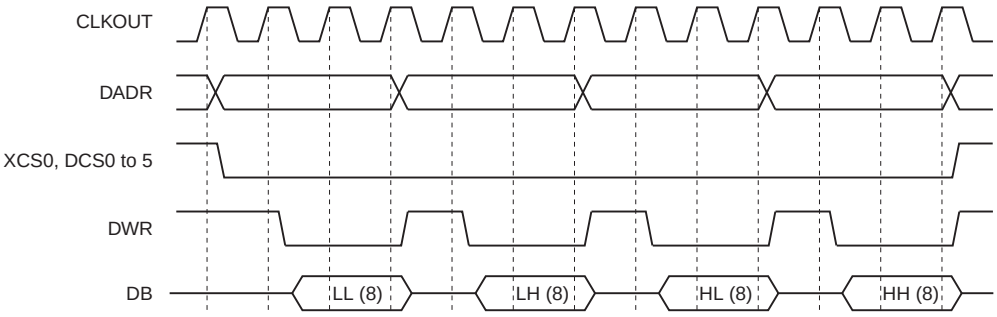
(4) Write (half-word access, with data wait)



(5) Read (word access, with data wait)



(6) Write (word access, with data wait)



Description of Application Circuit

See the Application Circuit when using the CXD2930BR to configure a GPS receiver.
Points for caution are as follows.

1. Unused pins
   Software processing is performed to prevent undesired current from flowing to unused pins in the circuit diagram, so leave these pins open.

2. TCXO input
   The TCXO frequency is 18.414MHz ± 3ppm. Signals that have not been binary-converted should be input with an amplitude of 0.8Vp-p or more via a DC filter capacitor (C19 in the circuit diagram). Input binary-converted signals directly to Pin 7 (TCXO) without passing through C19 or R1 in the circuit diagram.
   Make sure the input level at this time satisfies the Electrical Characteristics.

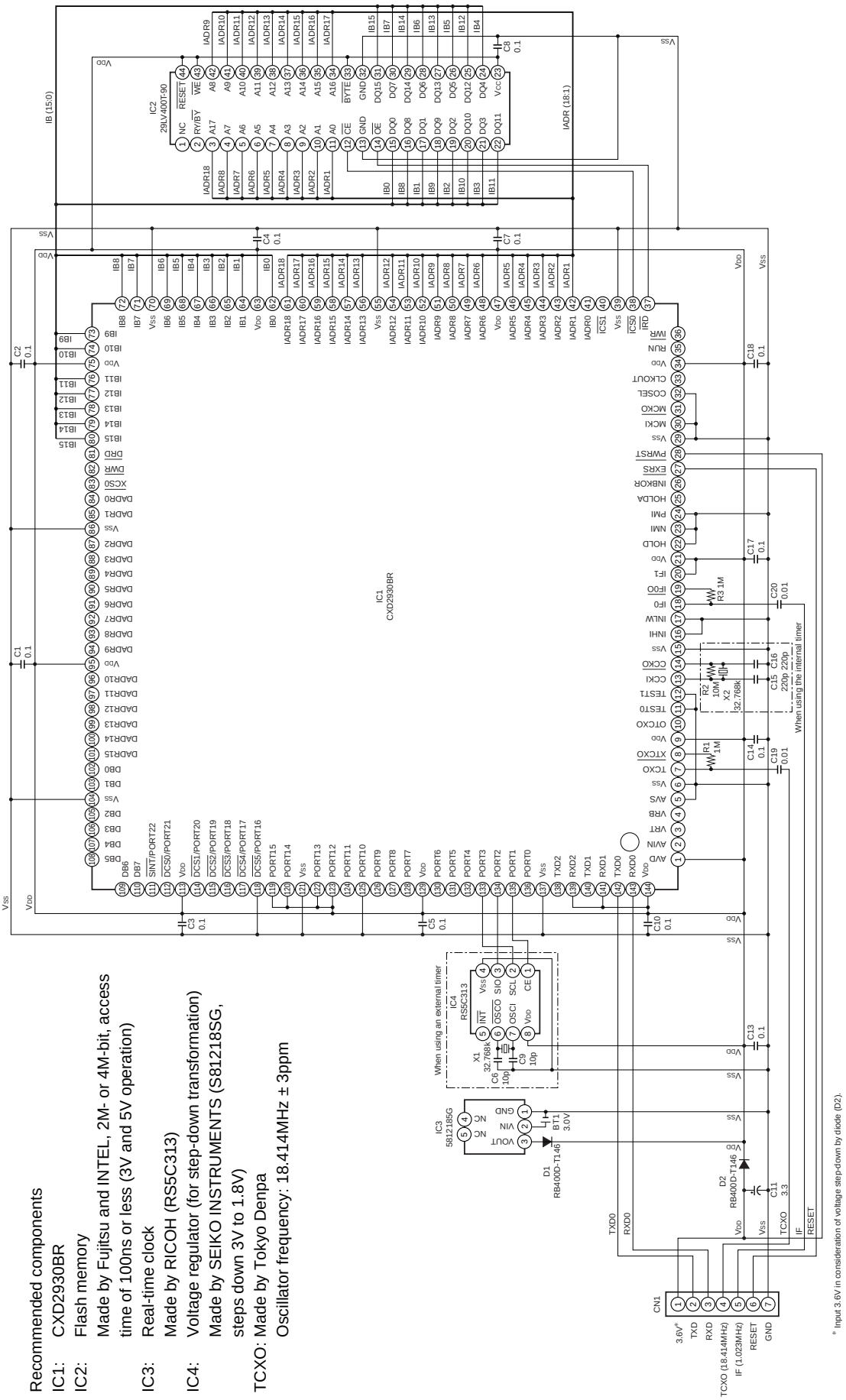
3. IF input
   The CXD2930BR interface is 1.023MHz, and does not accept other frequencies. Signals that have not been binary-converted should be input with an amplitude of 0.8Vp-p or more via a DC filter capacitor (C20). Input binary-converted signals directly to Pin 18 (IF0) without passing through C20 or R3 in the circuit diagram.
   Make sure the input level at this time satisfies the Electrical Characteristics.

4. TXD (SIO output)
   The TXD amplitude low level is 0.4V or less, and the high level is V_{DD} – 0.4V (V_{DD} = 3.0 to 3.6V) or more.
   When the LSI, etc., connected to TXD operates at 5V and has a CMOS input level, perform 3 to 5V conversion before inputting the signal.

5. Real-time clock
   The current software version uses an external real-time clock. Consult your Sony representative beforehand when using the internal real-time clock. When using an external real-time clock, connect Pin 13 (CCKI) to GND.

6. External program ROM
   Use a 2M- or 4M-bit external program ROM (IC2) with an access time of 100ns or less and which is capable of 16-bit read.

Application Circuit



Recommended components

IC1: CXD2930BR

IC2: Flash memory
Made by Fujitsu and INTEL, 2M- or 4M-bit, access time of 100ns or less (3V and 5V operation)

IC3: Real-time clock
Made by RICOH (RS5C313)

IC4: Voltage regulator (for step-down transformation)
Made by SEIKO INSTRUMENTS (S81218SG, steps down 3V to 1.8V)

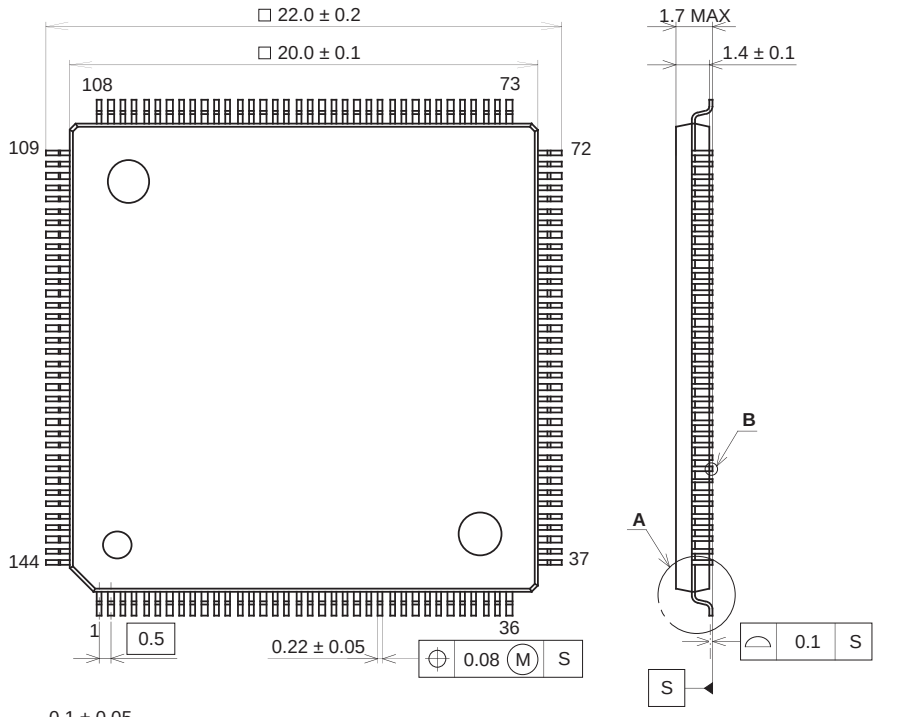
TCXO: Made by Tokyo Denpa
Oscillator frequency: 18.414MHz ± 3ppm

* Input 3.6V in consideration of voltage step-down by diode (D2).

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

144PIN LQFP (PLASTIC)



SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.3 g