SONY

CXG1040TN

High Isolation DPDT Switch

Description

The CXG1040TN is a DPDT (Dual Pole Dual Throw) antenna switch MMIC used in Personal Communication handsets such as PCS.

This IC is designed using the Sony's GaAs J-FET process and operates with CMOS input.

Features

- CMOS input control
- Insertion loss 0.5 dB (Typ.) at 2.0 GHz
- High isolation 25 dB (Typ.) at 2.0 GHz
- Small Package TSSOP-10pin

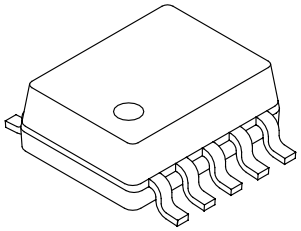
Applications

DPDT switch for digital cellular telephones such as PCS handsets.

Structure

GaAs J-FET MMIC

10 pin TSSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

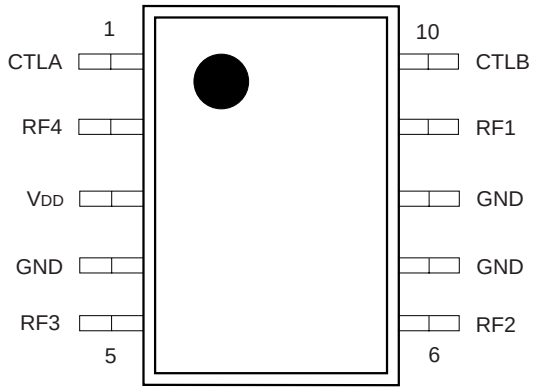
• Supply voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Input power	Pin	25	dBm
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E99144-TE

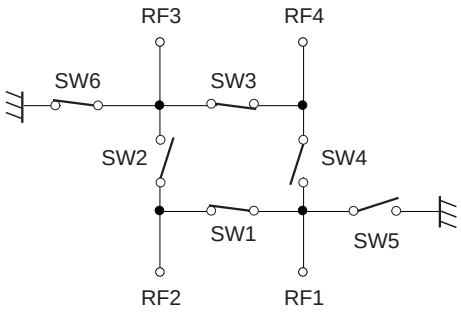
Pin Configuration

Unit : mm

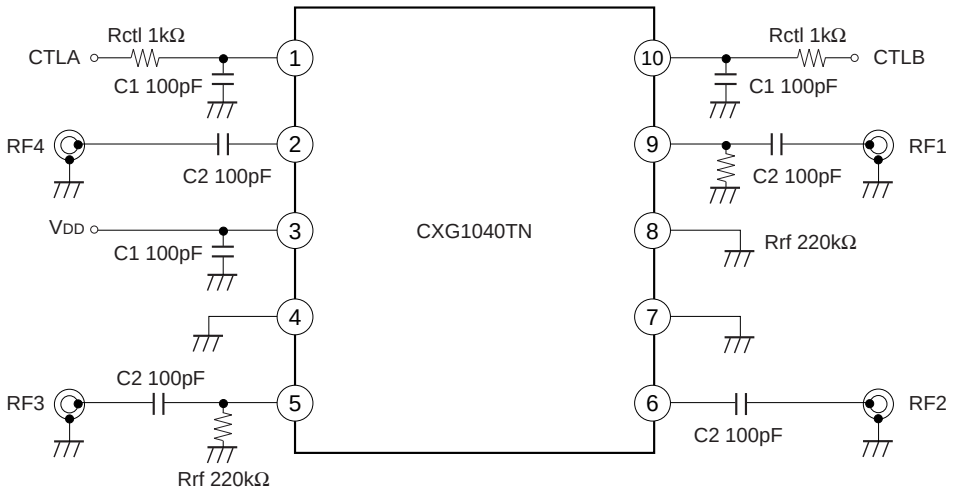


10pin TSSOP (PLASTIC)

Block Diagram



Recommended Circuit



When using the CXG1040TN, the following external components should be used:

- C1: This is used for signal line filtering 100 pF is recommended.
- C2: This is used for RF De-coupling and must be used in all applications. 100 pF is recommended.
- Rctl: This is used to give improved ESD performance.
- Rrf: This resistor is used to stabilize the dc operating point at high power levels. A value of 220 kΩ is recommended.

Truth Table

CTLA	CTLB		SW1	SW2	SW3	SW4	SW5	SW6
H	H	RF1 - RF2 ON	H	L	H	L	L	H
H	L	RF2 - RF3 ON	L	H	L	H	H	L
L	H	RF3 - RF4 ON	H	L	H	L	H	L
L	L	RF4 - RF1 ON	L	H	L	H	L	H

Operating Condition (Ta=–35 °C to +85 °C)

	Symbol	Min.	Typ.	Max.	Unit.
Control voltage (High)	Vctl (H)	2.5		3.6	V
Control voltage (Low)	Vctl (L)	0		0.5	V
Bias voltage	V_{DD}	2.7		4	V

Electrical Characteristics (1)

V_{DD}=3 V, Vctl (L)=0 V, Vctl (H)=2.8 V±3 %,

@2 GHz, Pin=10 dBm, Impedance at all ports : 50 Ω (Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Insertion loss	IL		0.5	0.8	dB
Isolation	Iso	20	25		dB
VSWR	VSWR		1.3	1.5	
Input power for 1 dB compression	P1dB	20	24		dBm
3rd order input intercept point *1	IP3	45			dBm
Switching speed	Tsw		1	5	µs
Bias current	I_{DD}		0.7	1.1	mA
Control current	Ictl		80	150	µA

*1 two-tone input power up to 10 dBm

Electrical Characteristics (2)

V_{DD}=3 V, Vctl (L)=0 V, Vctl (H)=2.8 V±3 %,

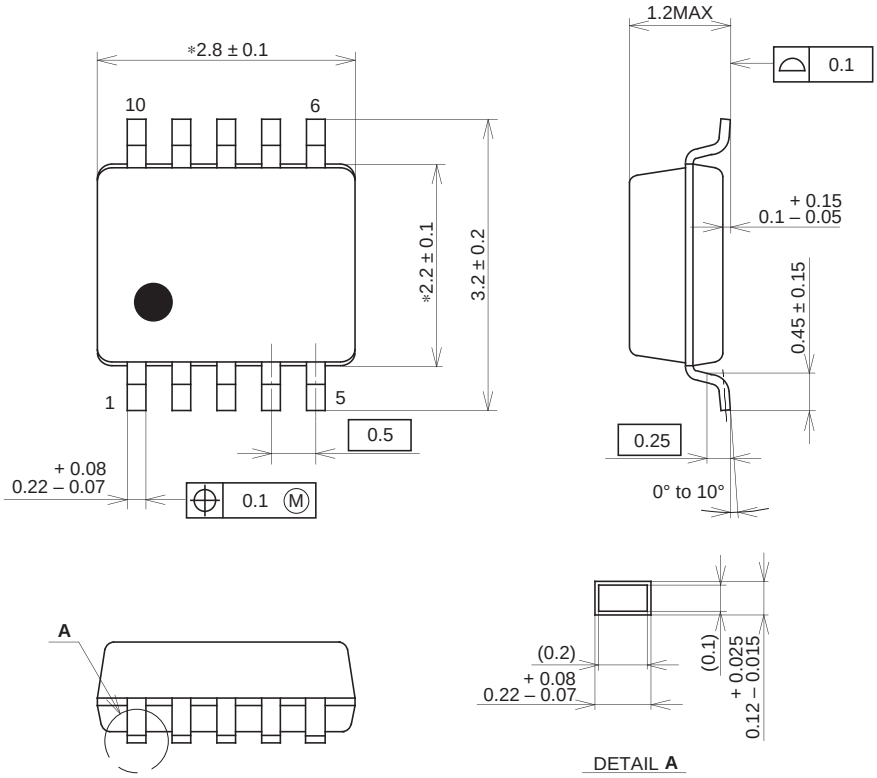
@2 GHz, Pin=10 dBm, Impedance at all ports : 50 Ω (Ta=–35 °C to +85 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Insertion loss	IL		0.5	1.0	dB
Isolation	Iso	20	25		dB
VSWR	VSWR		1.3	1.5	
Input power for 1 dB compression	P1dB	20	24		dBm
3rd order input intercept point *1	IP3	45			dBm
Switching speed	Tsw		1	5	µs
Bias current	I_{DD}		0.7	1.3	mA
Control current	Ictl		80	180	µA

*1 two-tone input power up to 10 dBm

Package Outline Unit : mm

10PIN TSSOP(PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	TSSOP-10P-L01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g