

**Power Amplifier/Antenna Switch + Low Noise Amplifier/Down Conversion Mixer for PHS**

**Description**

The CXG1053FN is an MMIC consisting of the power amplifier, antenna switch, low noise amplifier and down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

**Features**

- Operates at a single positive power supply:  $V_{DD} = 3V$
- Small mold package: 26-pin HSOF

**<Power amplifier/antenna switch transmitter block >**

- Low current consumption:  $I_{DD} = 150mA$   
( $P_{OUT} = 20.2dBm, f = 1.9GHz$ )
- High power gain:  $G_p = 39dB$  Typ.  
( $P_{OUT} = 20.2dBm, f = 1.9GHz$ )

**<Antenna switch receiver block/  
low noise amplifier>**

- Low current consumption:  $I_{DD} = 2.5mA$  Typ.  
(When no signal)
- Low noise:  $NF = 2.7dB$  Typ. ( $f = 1.9GHz$ )

**<Down conversion mixer>**

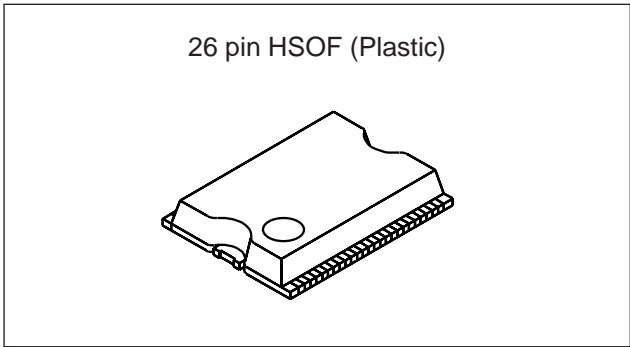
- High conversion gain:  $G_c = 9dB$  Typ. ( $f = 1.9GHz$ )
- Low distortion: Input  $IP3 = +1dBm$  Typ. ( $f = 1.9GHz$ )

**Applications**

Japan digital cordless telephones (PHS)

**Structure**

GaAs J-FET MMIC



**Absolute Maximum Ratings**

**<Power amplifier block>**

- Supply voltage  $V_{DD}$  6 V
- Voltage between gate and source  $V_{GSO}$  1.5 V
- Drain current  $I_{DD}$  550 mA
- Allowable power dissipation  $P_D$  3 W

**<Switch block>**

- Control voltage  $V_{CTL}$  6 V

**<Front-end block>**

- Supply voltage  $V_{DD}$  6 V
- Input power  $P_{RF}$  +10 dBm

**<Common to each block>**

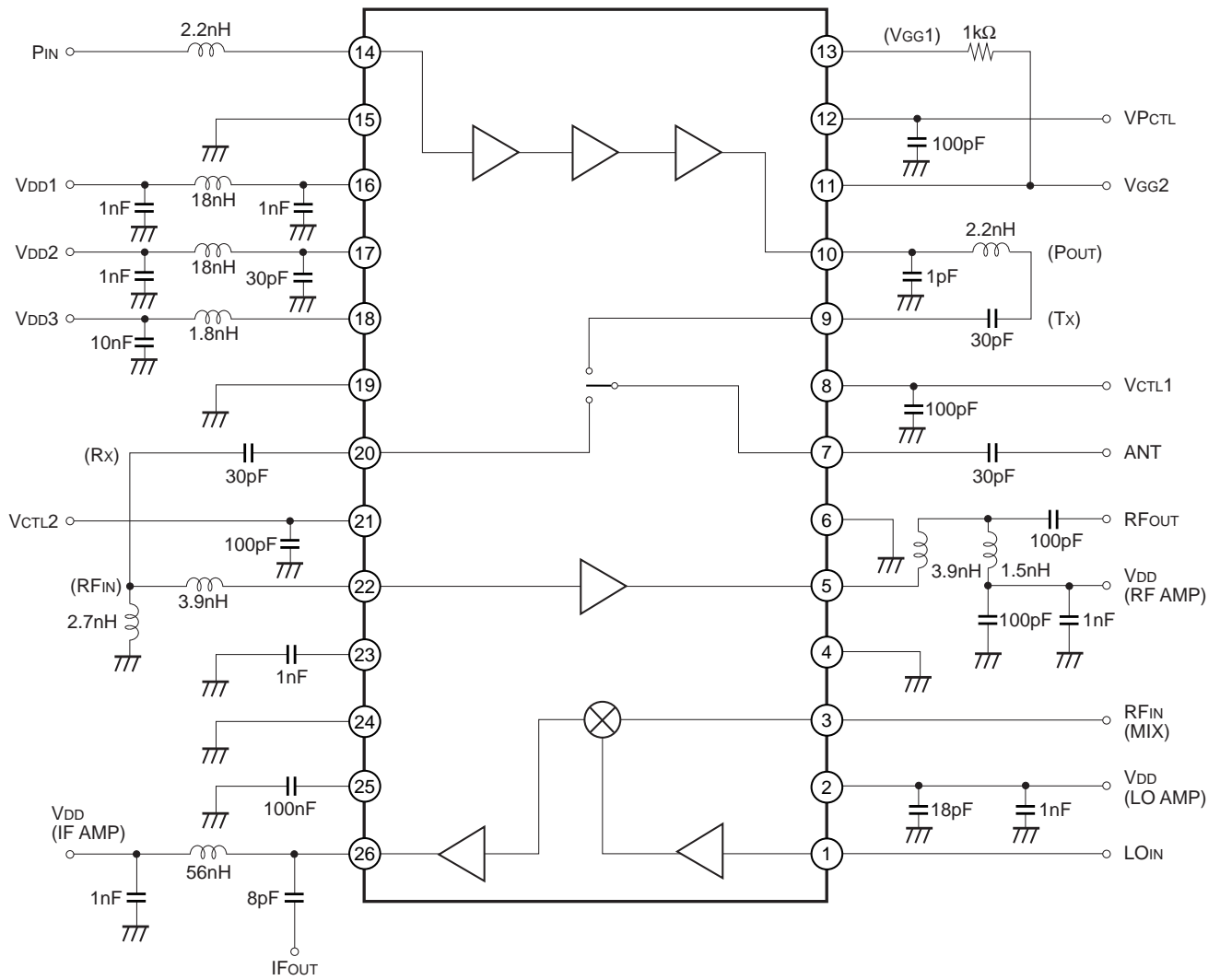
- Channel temperature  $T_{ch}$  150 °C
- Operating temperature  $T_{opr}$  -35 to +85 °C
- Storage temperature  $T_{stg}$  -65 to +150 °C

**Note on Handling**

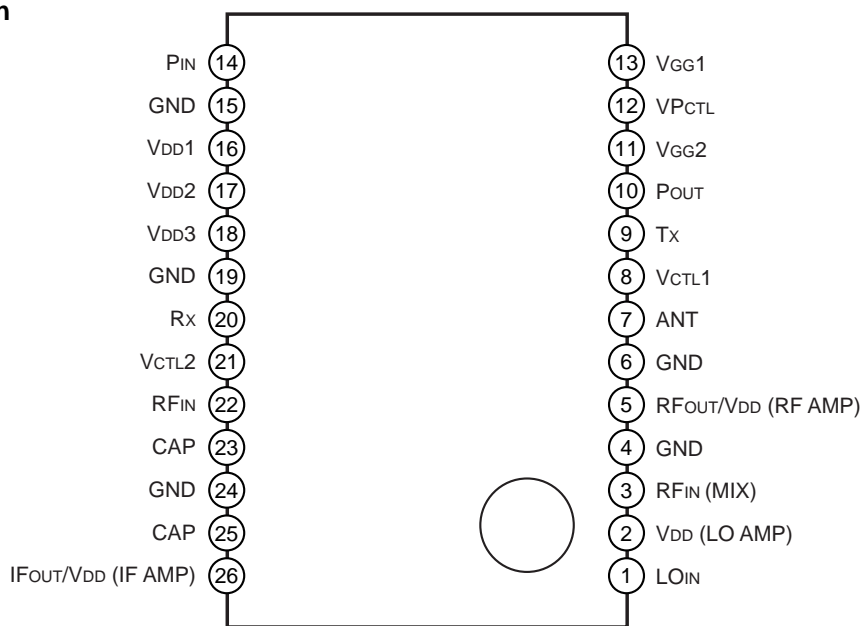
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Block Diagram and External Circuit



Pin Configuration



## Electrical Characteristics

### 1. Control Pin Logic for Antenna Switch

Conditions of control pin	ANT – Tx	ANT – Rx
$V_{CTL1} = 3V, V_{CTL2} = 0V$	ON	OFF
$V_{CTL1} = 0V, V_{CTL2} = 3V$	OFF	ON

### 2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are when the Sony's recommended evaluation board with the external circuit shown on page 7 is used. Therefore, the power amplifier output pin ( $P_{OUT}$ ) and the antenna switch transmission input pin (Tx) are connected via an external circuit. The specifications of the power amplifier block are set including the antenna switch transmitter block.

Unless otherwise specified:  $V_{DD} = 3V, V_{PCTL} = 2V, V_{CTL1} = 3V, V_{CTL2} = 0V, I_{DD} = 150mA,$   
 $P_{OUT} = 20.2dBm, f = 1.9GHz, T_a = 25^{\circ}C$

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	$I_{DD}$			150		mA
Gate voltage adjustment value	$V_{GG}$		0	0.25	0.6	V
Output power	$P_{OUT}$	Measured with the ANT pin	20.2			dBm
Power gain	$G_P$		36	39		dB
Adjacent channel leak power ratio (600 ± 100KHz)	ACPR600kHz	Measured with the ANT pin		-63	-55	dBc
Adjacent channel leak power ratio (900 ± 100KHz)	ACPR900kHz	Measured with the ANT pin		-70	-60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	KHz
2nd-order harmonic level	—	Measured with the ANT pin			-25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			-25	dBc

### 3. Antenna Switch Receiver Block + Front-end Block

These specifications are when the Sony's recommended evaluation board with the external circuit shown on page 7 is used. Therefore, the antenna switch reception pin (Rx) and the low noise amplifier input pin (RF<sub>IN\_LNA</sub>) are connected via an external circuit. The specifications of the low noise amplifier block are set including the antenna switch reception block.

#### (a) Antenna switch receiver block + low noise amplifier block

Unless otherwise specified: V<sub>DD</sub> = 3V, V<sub>CTL1</sub> = 0V, V<sub>CTL2</sub> = 3V, RF = 1.9GHz/−30dBm, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I <sub>DD_LNA</sub>	When no signal		2.5	3.5	mA
Power gain	G <sub>P</sub>		12.5	14.5	16.5	dB
Noise figure	NF			2.7	3.5	dB
Input IP3	IIP3	*1	−11	−8		dBm
Isolation	ISO		25	30		dB

\*1 Conversion from IM3 compression ratio during FR1 = 1.9000GHz/−30dBm and FR2 = 1.9006GHz/−30dBm input.

#### (b) Mixer Block

Unless otherwise specified: V<sub>DD</sub> = 3V, RF = 1.90GHz/−25dBm, LO = 1.66GHz/−12dBm, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
LO block current consumption	I <sub>DD_LO</sub>	When no signal		1.7	2.5	mA
IF block current consumption	I <sub>DD_IF</sub>	When no signal		3.3	4.5	mA
Conversion gain	G <sub>C</sub>		7	9	11	dB
Noise figure	NF			8.5	11.5	dB
Input IP3	IIP3	*2	−2	+1		dBm
LO to ANT leak	PLK	*3		−43	−38	dBm

\*2 Conversion from IM3 compression ratio during FR1 = 1.9000GHz/−25dBm and FR2 = 1.9006GHz/−25dBm input.

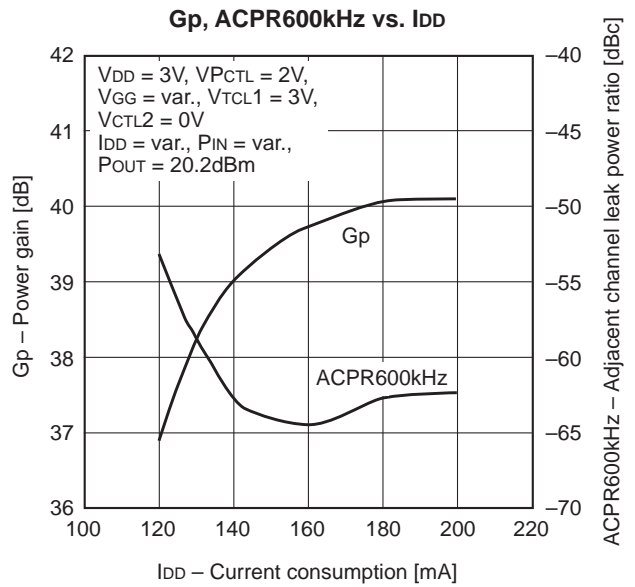
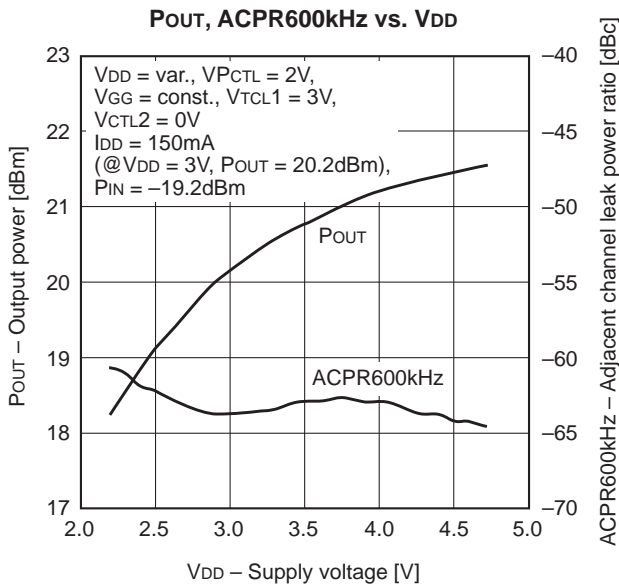
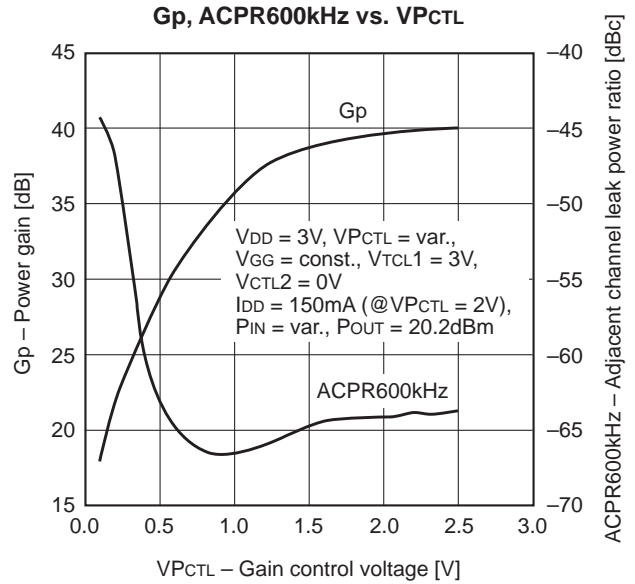
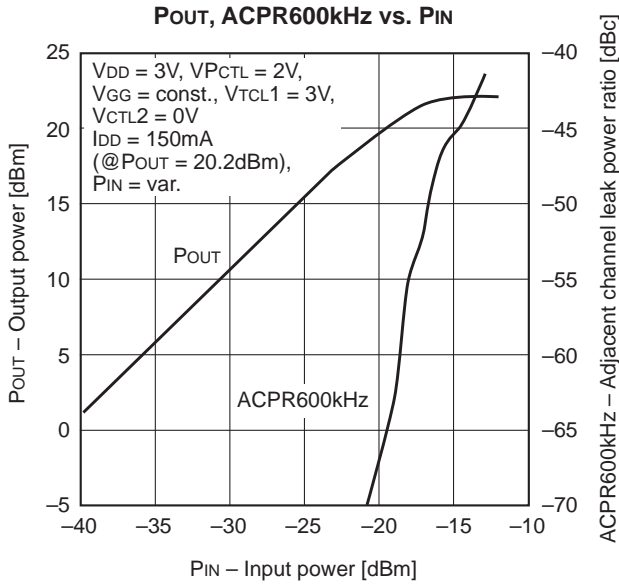
\*3 The RF<sub>OUT</sub> pin of the LNA and the RF<sub>IN</sub> pin of the MIX block is connected directly with the cable. And the power supply of the LNA is turned on.

#### (c) Total of (a) + (b)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I <sub>DD_total</sub>	When no signal		7.5	10	mA

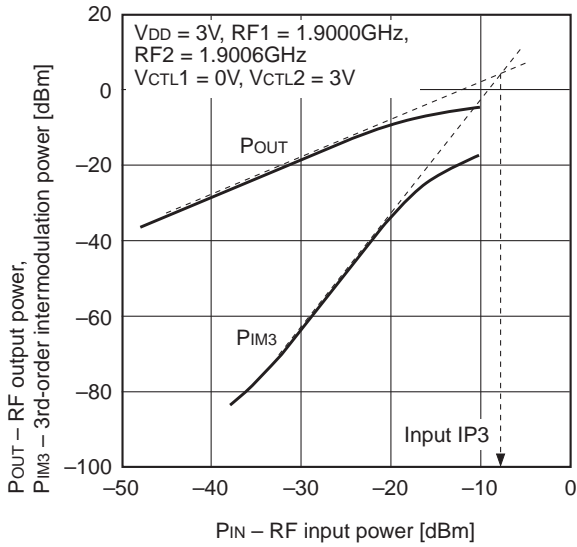
Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

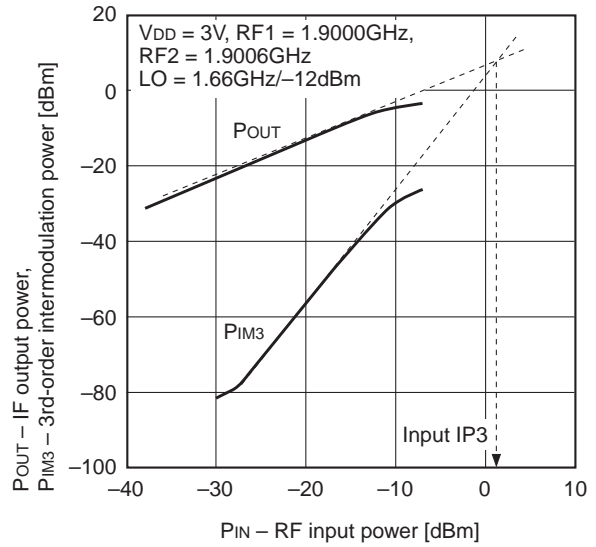


2. Antenna Switch Receiver Block + Low Noise Amplifier, Down Conversion Mixer (Ta = 25°C)

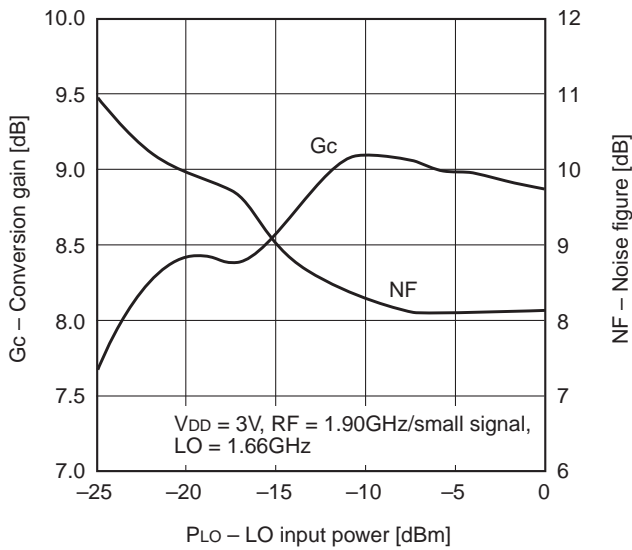
SW/LNA block: POUT, PIM3 vs. PIN



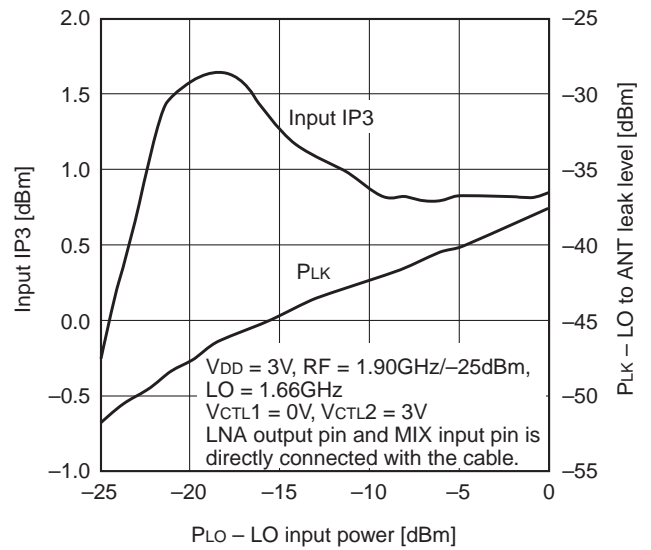
MIX block: POUT, PIM3 vs. PIN



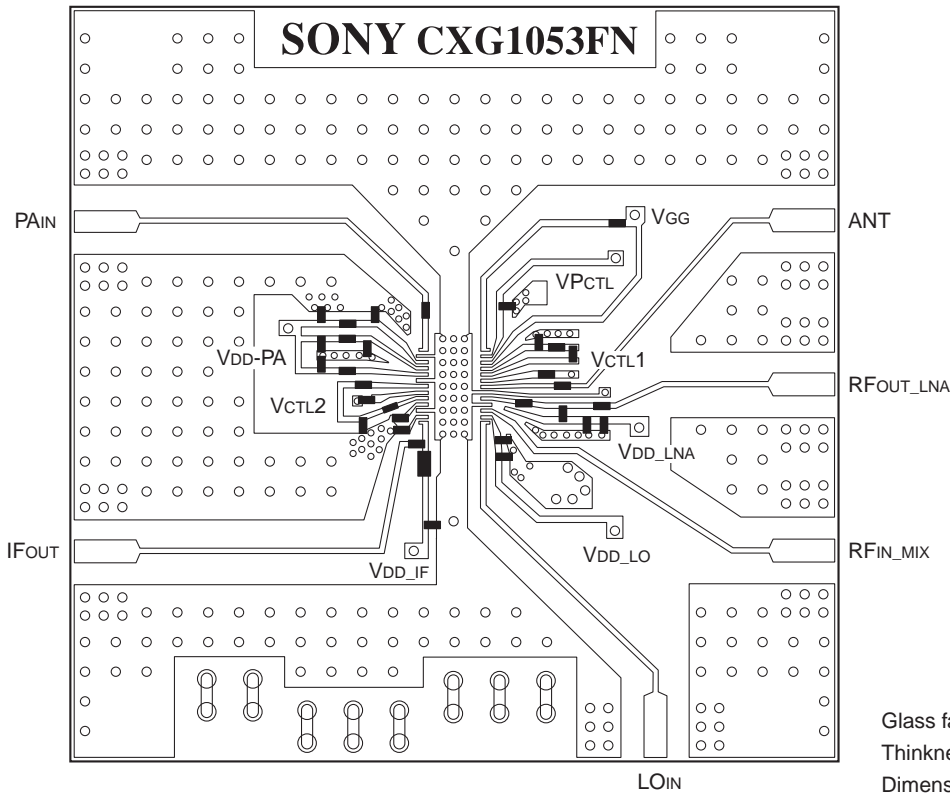
MIX block: Gc, NF vs. PLO



MIX block: Input IP3, PLK vs. PLO



Recommended Evaluation Board



Glass fabric-base epoxy board (4 layers)  
 Thickness between layers 1 and 2: 0.2mm  
 Dimensions: 50mm x 50mm

Enlarged Diagram of External Circuit Block

