## Laser Driver

Description

The CXB1558Q-Y is a high-speed monolithic Laser Driver/Current Switch with ECL input level. Open collector outputs are provided at the output pins (Q, $\overline{Q}$) and have the capability of driving modulation current of 60mApp at a max. data rate of 2.0Gbps (NRZ). DRIVADJ and SDRIV inputs control the modulation current amplitude, and BIASADJ, SBIAS inputs control the bias current. Modulation and bias current can be controlled by either voltage or current through these pins. This device includes D-FF for duty cycle correction and Laser Shutdown function.

32 pin QFP (Ceramic)
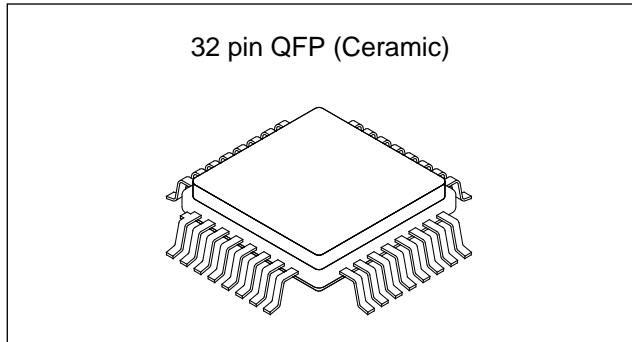
Features

- Maximum data rate (NRZ): 2.0Gbps (Typ.)
- Differential Data input: ECL
- D-FF for Duty Cycle Correction
- Laser Shutdown Input: TTL

Applications

- SONET/SDH: 155,622Mb/s,1.2Gb/s
- Fiber channel: 133,266,532Mb/s,1.062Gb/s
- FDDI: 125Mb/s   ESCON: 200Mb/s   HDTV: 1.5Gb/s

Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	−0.3 to +7.0	V	
• Input voltage	V_{IN}	V_{EE} to +0.5	V	
• Differential input voltage	$|V_{IN} - \overline{V_{IN}}|$	0 to 2.5	V	
• Differential clock voltage	$|V_{CLK} - \overline{V_{CLK}}|$	0 to 2.5	V	
• Output current (Continuous)	I_Q, I_{BIAS}	0 to 80	mA	
Input current (Continuous)	I_{DRVADJ}	0 to 8	mA	
	$I_{BIASADJ}$	0 to 8	mA	
• Storage temperature	Tstg	−65 to +150	°C	

Recommended Operating Conditions

• DC power supply voltage	$V_{CC} - V_{EE}$	4.75 to 5.46	V
• Operating case temperature	Tc	0 to +85	°C

Structure

Bipolar silicon monolithic IC

E94720-PK

Block Diagram and Pin Assignment

Pin labels (top, left to right): V_{CC2} (24), $\overline{LDOFF}$ (23), NC (22), CLK (21), $\overline{CLK}$ (20), V_{EE} (19), NC (18), NC (17)

Left side (top to bottom): $V_{EE}1$ (25), V_{BB} (26), $\overline{D}$ (27), D (28), $V_{CC}1$ (29), $\overline{P}$ (30), P (31), DRIVADJ (32)

Right side (top to bottom): NC (16), NC (15), NC (14), NC (13), NC (12), BIASADJ (11), $V_{EE}2$ (10), SBIAS (9)

Bottom (left to right): SDRIV (1), $V_{EE}2$ (2), $\overline{\overline{Q}}$ (3), $\overline{\overline{Q}}$ (4), $\overline{Q}$ (5), Q (6), BIASB (7), BIASA (8)

Internal blocks: VOLTAGE SOURCE, D-FF, INPUT SIGNAL MONITOR, MODULATION GENERATOR, BIAS GENERATOR

Truth table

$\overline{LDOFF}$	D	Q	P
H	L	H	H
H	H	L	L
L	L	H	H
L	H	H	L

* In a case of resistor load.

Pin Description

Pin No.	Symbol	Typical voltage (V)		Equivalent circuit	Description
		DC	AC		
1	SDRIV	0mA to 8mA*1 0mA to 6mA*2	—		Modulation generator current monitor.
32	DRIVADJ	V_{EE} to V_{EE} +2.5V			Modulation generator current adjustment.
2, 10	$V_{EE}2$	−5.2V			Negative power supply pin.
3	$\overline{Q}$	—	0mA to 60mA*1		Modulation generator current output.
4			0mA to 40mA*2		
5	Q	—	0mA to 60mA*1		
6			0mA to 40mA*2		
7	BIASB	0mA to 30mA	—		Bias generator current output.
8	BIASA				
9	SBIAS	0mA to 8mA	—		Bias generator current monitor.
11	BIASADJ	V_{EE} to V_{EE} +2.5V	—		Bias generator current adjustment.
20	$\overline{CLK}$	—	−1.84V to −0.81V		Clock signal input.
21	CLK				
19	V_{EE}	−5.2V	—		
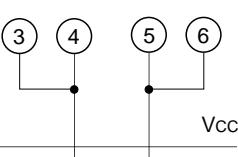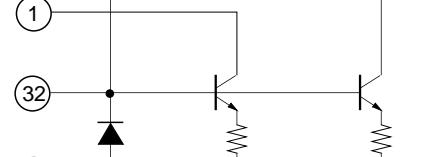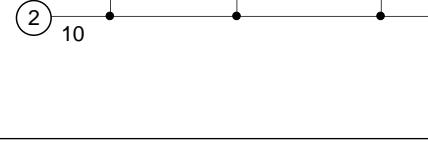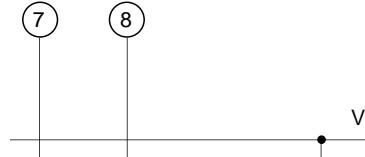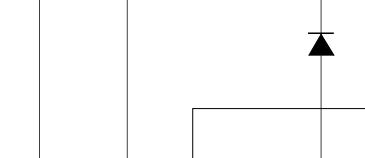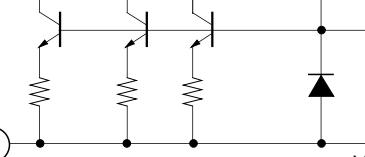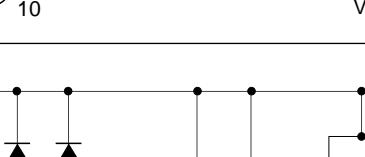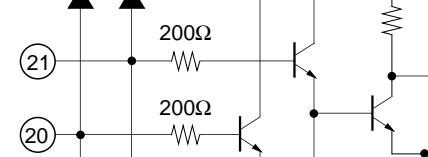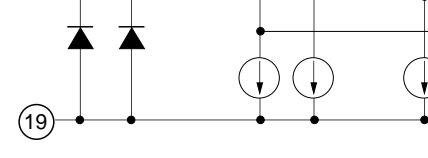
*1 V_{EE} = −5.46V to −4.94V

*2 V_{EE} = −4.94V to −4.75V

| Pin No.	Symbol	Typical voltage (V)		Equivalent circuit	Description
		DC	AC		
26	V$_{BB}$	−1.3V	—		Reference voltage (−1.3V) Use for the reference voltage in the case of single-phase input. Max. drive current ±200μA
25	V$_{EE}$1	−5.2V	—		Negative power supply pin.
27	$\overline{D}$	—	−1.84V to −0.81V		Data signal input.
28	D				
29	V$_{CC}$1	0V	—		Positive power supply pin.
30	$\overline{P}$	—	0mA to 2.7mA		Input signal monitor output.
31	P	—			
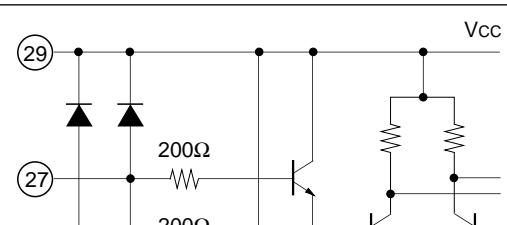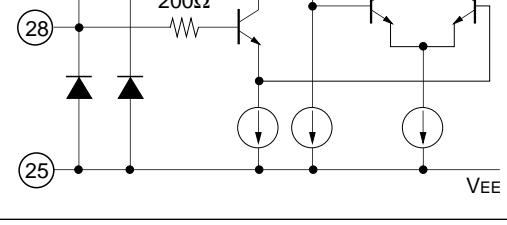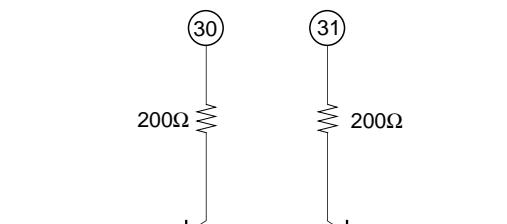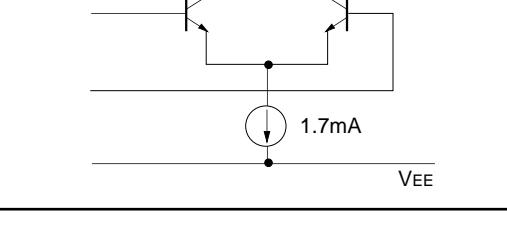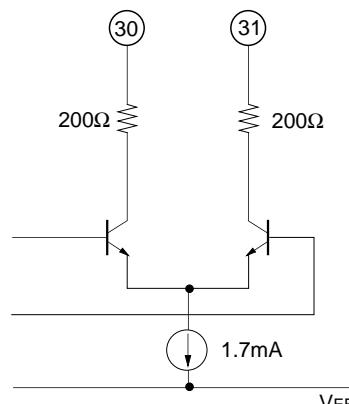
Electrical Characteristics

• DC Electrical Characteristics

($V_{CC}1 = V_{CC}2 = $ GND, $V_{EE}1 = V_{EE}2 = -5.46$ to -4.75V, Tc = 0 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}	I_Q = 0mA, I_{BIAS} = 0mA	−110	−78	—	mA
		I_Q = 60mA, I_{BIAS} = 60mA	−260	−213	—	
Max. Modulation current	I_Q	V_{EE} = −5.46 to −4.94V	60	—	—	
		V_{EE} = −4.94 to −4.75V	40	—	—	
Modulation output voltage range	V_Q	Tc = 25°C	−2.5	—	2.0	V
Max. Bias current	I_{BIAS}	I_{BIASA} + I_{BIASB}	60	—	—	mA
Bias output voltage range	V_{BIAS}		−2.7	—	0.0	V
Modulation current monitor output voltage range	V_{SQ}	at voltage control application	−2.7	—	0.0	
Bias current monitor output voltage range	V_{SBIAS}	at voltage control application	−2.7	—	0.0	
Input signal monitor current	I_P		1	1.7	2.7	mA
Input signal monitor output voltage range	V_P	Tc = 25°C	−2.5	—	2.0	V
ECL Input High voltage	V_{EDH}		−1.17	—	−0.81	
ECL Input Low voltage	V_{EDL}		−1.84	—	−1.48	
ECL Input High current	I_{EDH}		—	—	20	μA
TTL Input High voltage	V_{TDH}		V_{EE} + 2.0	—	Vcc	V
TTL Input Low voltage	V_{TDL}		V_{EE} − 0.5	—	V_{EE} + 0.8	
TTL Input High current	I_{TDH}		—	—	10	μA
TTL Input Low current	I_{TDL}		−320	—	—	
Reference bias voltage	V_{BB}		−1.38	−1.32	−1.26	V

Ratio of current setup

Item	Symbol	Condition	Min.	Typ.	Max.
Modulation current vs. Modulation monitor current	S1	at voltage control application	9.0	11.4	12.0
Modulation current vs. Modulation control current	S2	at current control application	6.5	8.6	10.5
Bias current vs. Bias monitor current	S3	at voltage control application	11.0	12.0	13.0
Bias current vs. Bias control current	S4	at current control application	7.4	9.8	12.0

• AC Electrical Characteristics

$(V_{CC}1 = V_{CC}2 = GND, V_{EE}1 = V_{EE}2 = -5.46$ to $-4.75V$, $Tc = 0$ to $+85°C$, $RI = 25\Omega$ to GND$)$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Max. Data rate	f_{DMAX}	NRZ	1.6	2.0	—	Gbps
Max. FF Operating Frequency	f_{FMAX}		1.6	2.0	—	GHz
Set Up Time	Ts		150	—	—	ps
Hold Time	T_H		10	—	—	
Shut Down Time	T_{SHUT}		—	—	30	µs
Rise time	T_{TLH}	20 to 80%	—	170	—	ps
Fall time	T_{THL}	$I_Q = 60mA$, $I_{BIAS} = 0$	—	150	—	

Application Circuit

Current Control Application
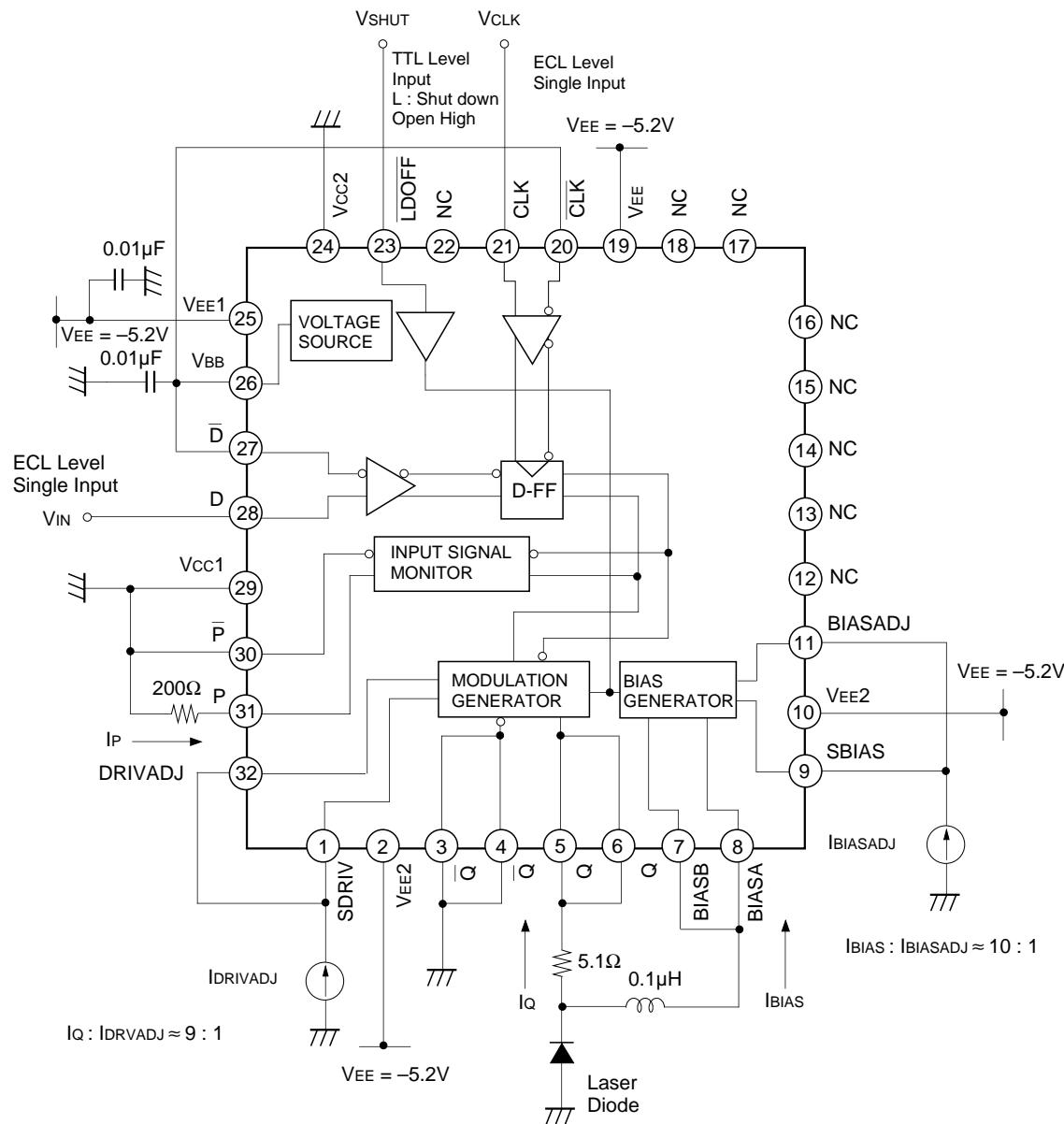
Measurement Circuit (DC)
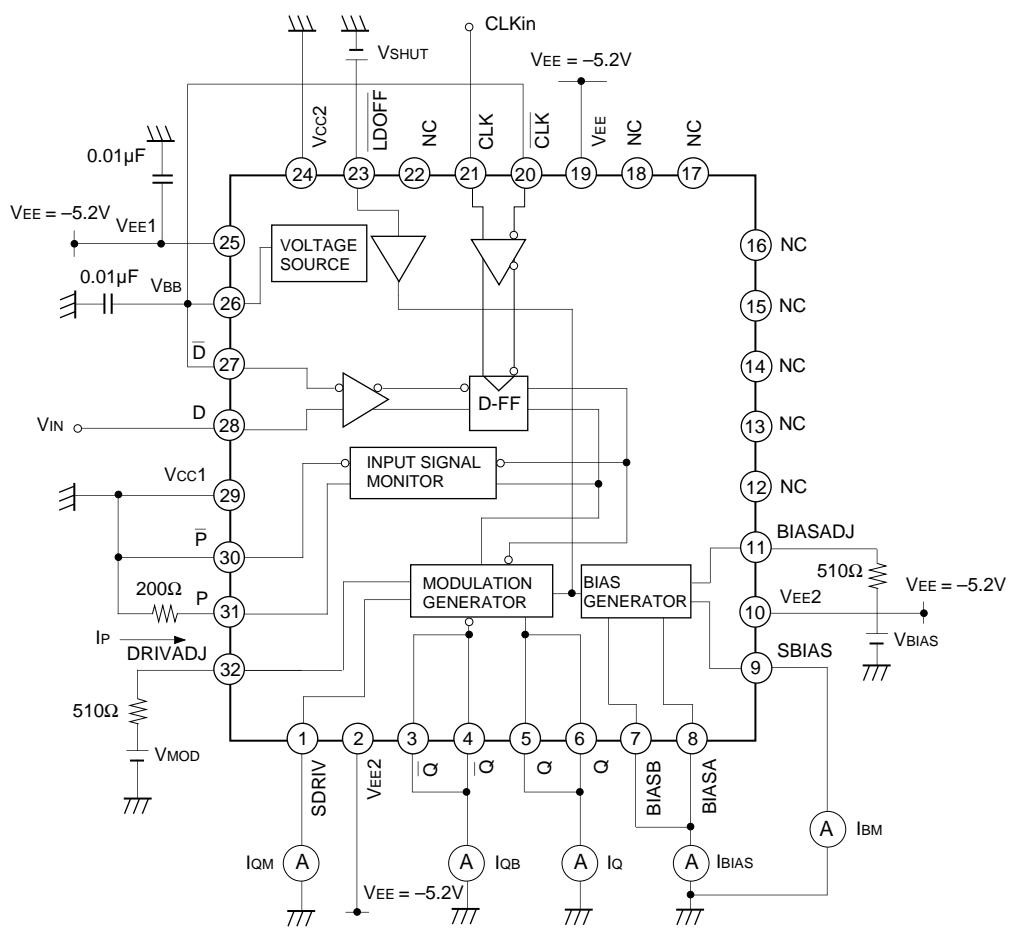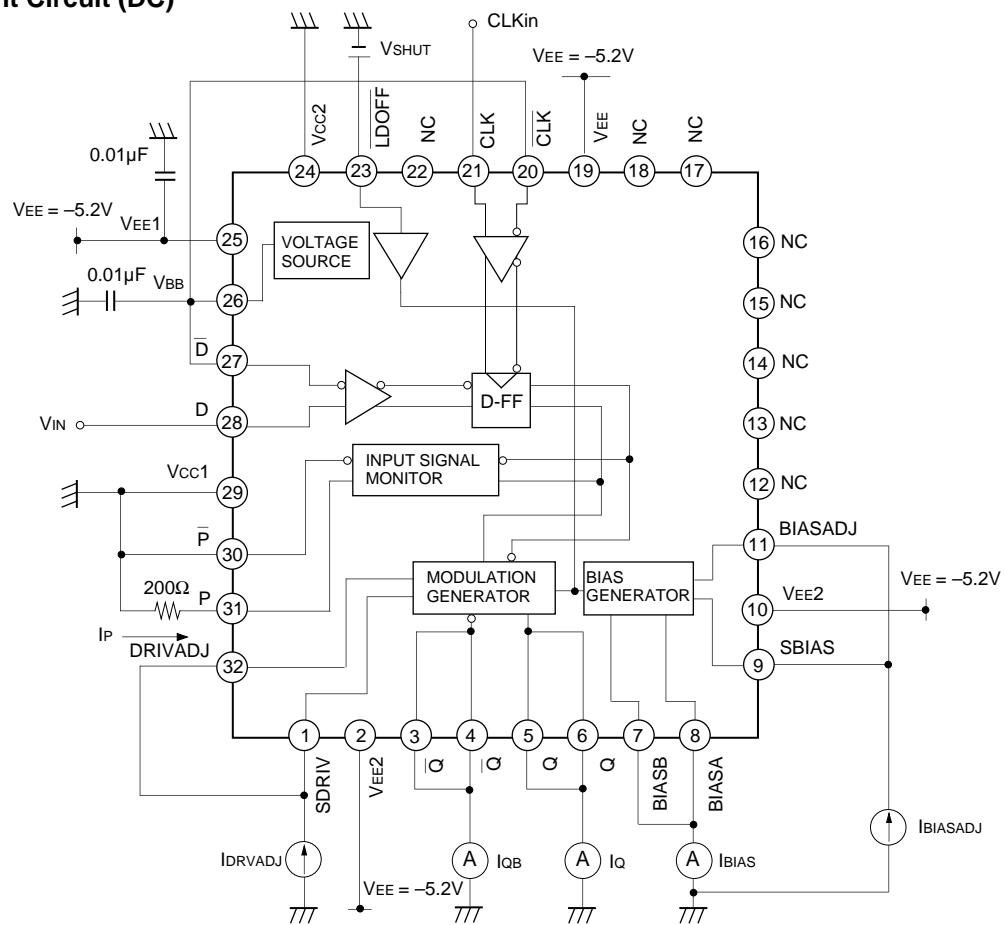
Measurement Circuit (AC)
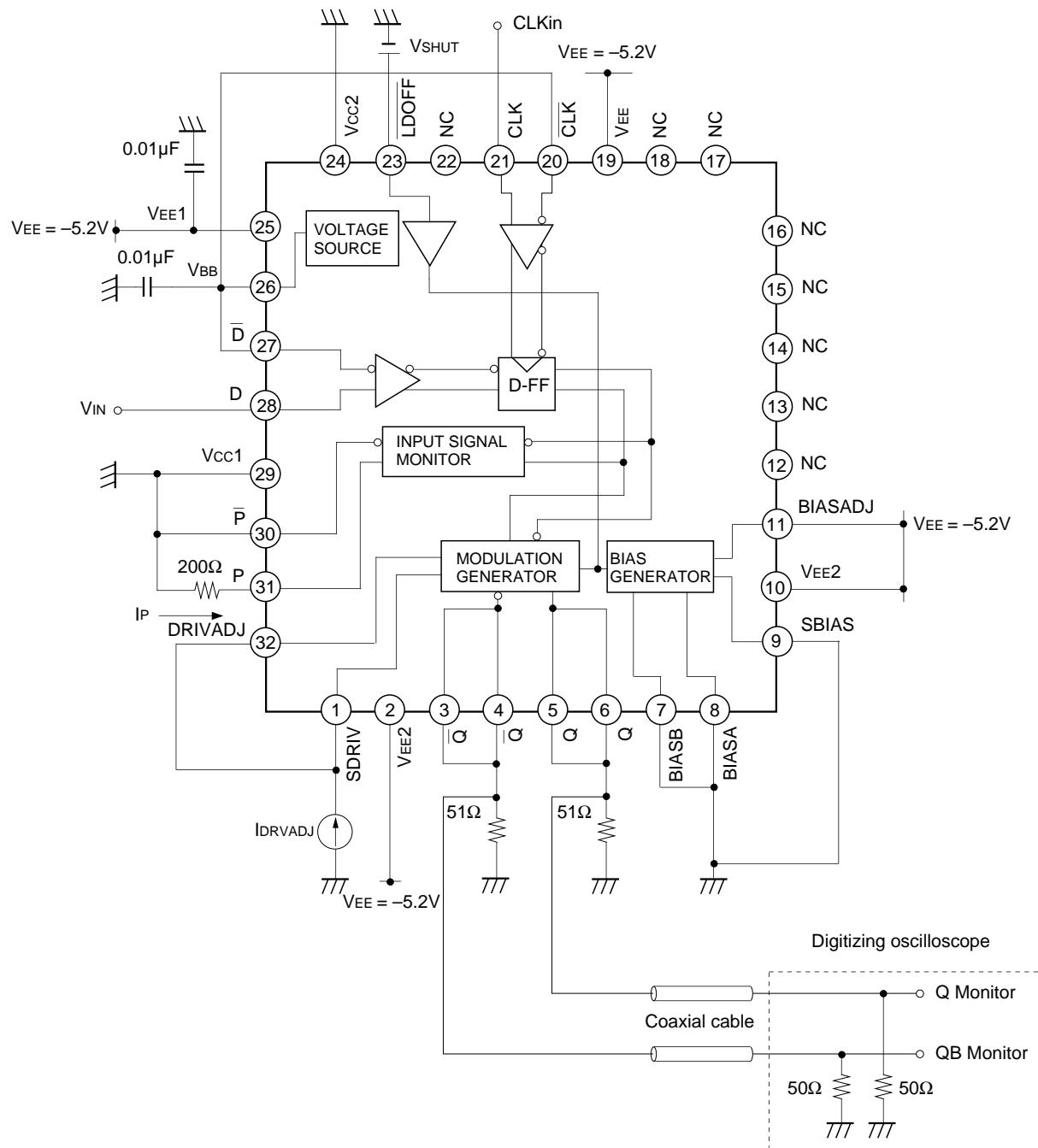
Voltage Control Application
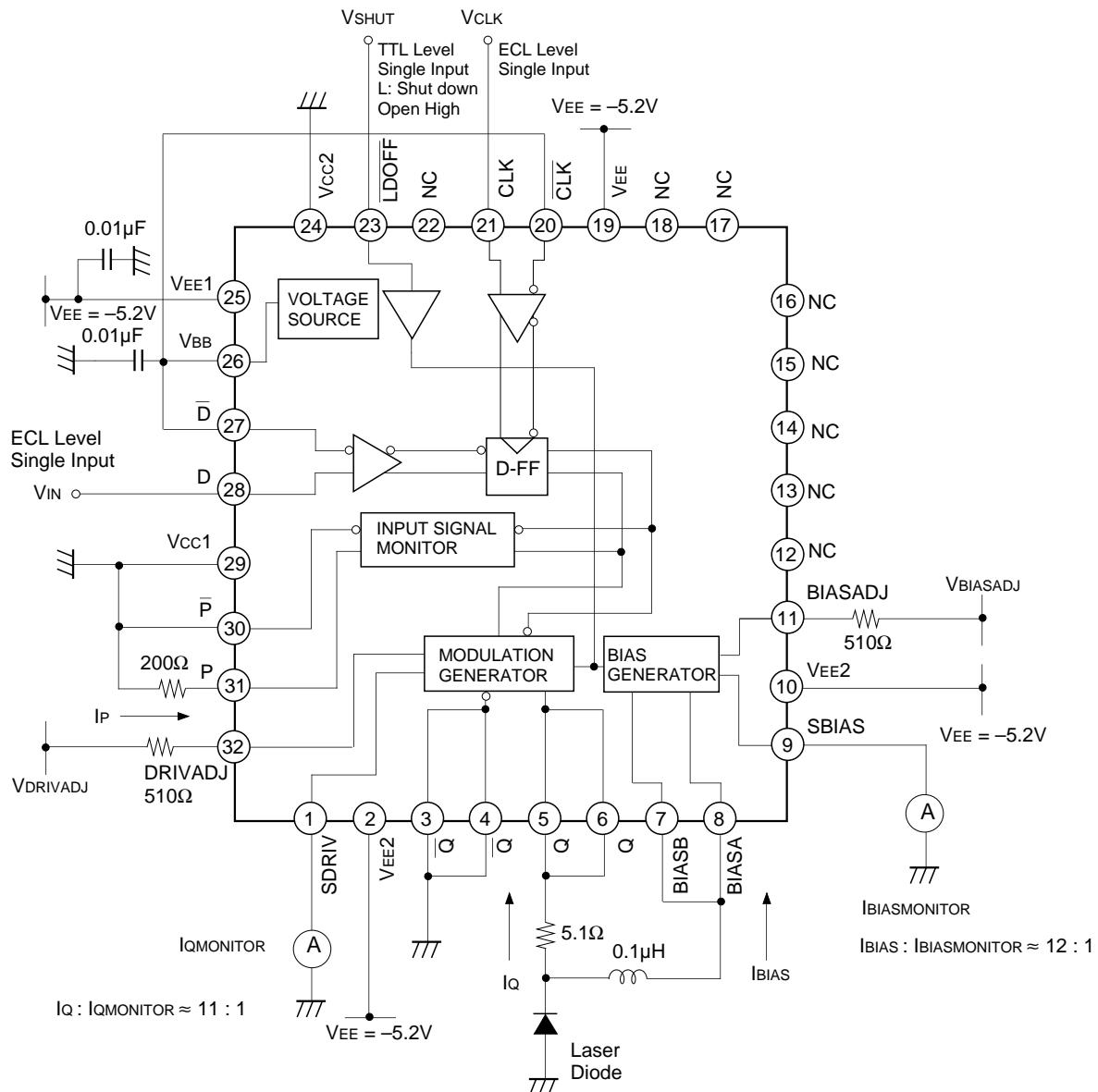

Cautions for Handling

1. The outputs (Q, $\overline{Q}$, BIASA, BIASB, SDRIV, SBIAS, P and $\overline{P}$) on this IC are the open collector type.
   Therefore, when these pins are not bing used, connect them to Vcc.
2. When the inputs (DRIVEADJ and BIASADJ) are not bing used, connect them to V_{EE}.
3. Do not apply voltage over V_{EE} + 2.5V to DRIVADJ pin and BIASADJ pin.
4. In voltage control Application, do not apply voltage over the output voltage range to SDRIV pin and SBIAS pin. (see DC Characteristics of Laser Part and Voltage Control Application Circuit.)
5. Maximum drive current of V_{BB} pin is ±200μA.
6. Maximum input differential voltage is 2.5V. (| D − $\overline{D}$ | , | CLK − $\overline{CLK}$ |)
7. As the electronic breakdown level is weak, take care to handle.

Example of Representative Characteristics

### Modulation current vs. Modulation control current
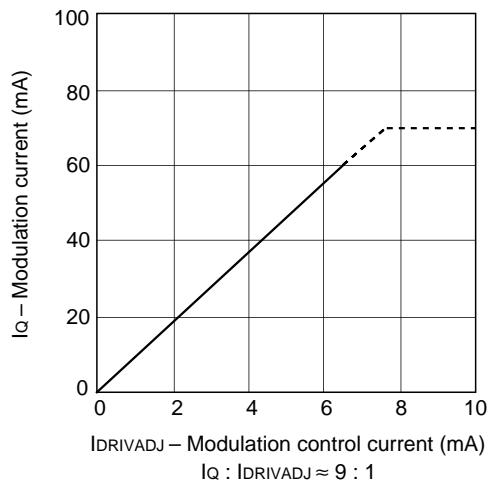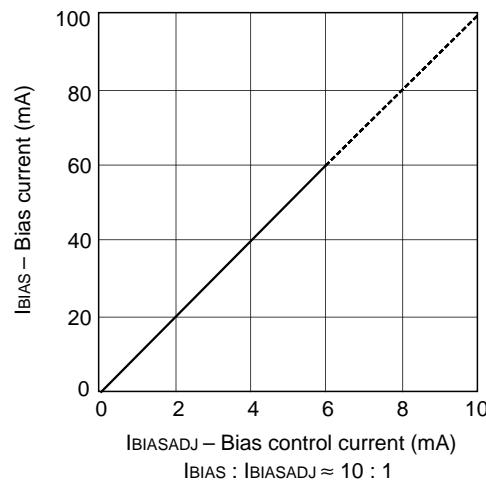
I_Q – Modulation current (mA)

$I_{DRIVADJ}$ – Modulation control current (mA)

$I_Q : I_{DRIVADJ} \approx 9 : 1$

Bias current vs. Bias control current

I_{BIAS} – Bias current (mA)

$I_{BIASADJ}$ – Bias control current (mA)

$I_{BIAS} : I_{BIASADJ} \approx 10 : 1$

Modulation current vs. Modulation control voltage

I_Q – Modulation current (mA)

V_{DRVADJ} – Modulation control voltage (V)

$I_Q \approx 0.1 \times (V_{mod} - 0.8)$ [A]

Bias current vs. Bias control voltage

I_{BIAS} – Bias current (mA)

V_{BIAS} – Bias control voltage [V]

$I_{BIAS} \approx 0.11 \times (V_{BIAS} - 0.8)$ [A]
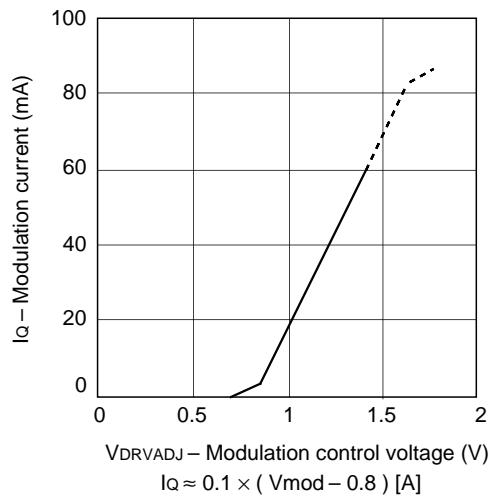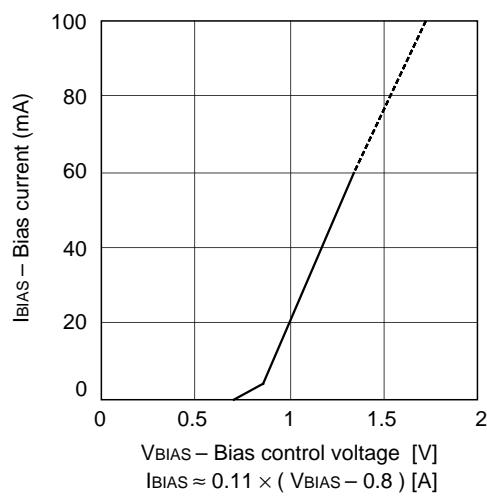
Package Outline   Unit: mm

32PIN QFP (CERAMIC)

□ 14.73 ± 0.3

24   17

25   16

32   9

1   8

1.016   0.48 ± 0.1

4.92 MAX

0.15 ± 0.05

10.63 MAX

0.76

0° to 10°

0.635 ± 0.125

(0.825)

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g
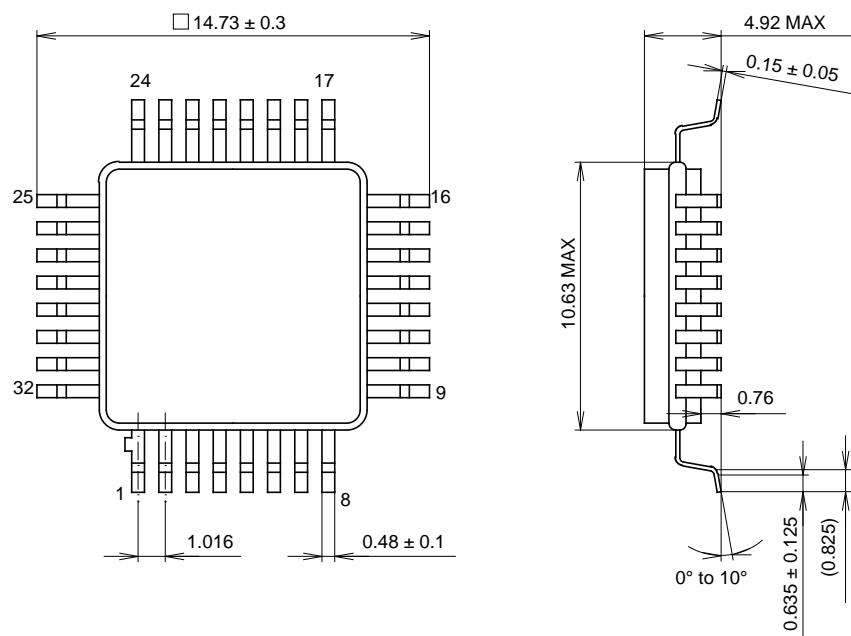
SONY CODE	QFP-32C-L01
EIAJ CODE	XQFP023-G-0000-A
JEDEC CODE	————