SONY

CXB1818Q

Laser Diode Driver

Description

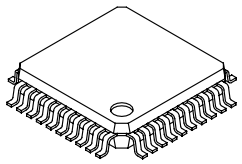
The CXB1818Q is a high-speed monolithic Laser Diode Driver/Current Switch with ECL/PECL input level. Open collector outputs are provided at the output pins (Q, QBX) and have the capacity of driving modulation current of 50mAp-p at a maximum data rate of 622Mbps. Along with the modulation current generator there is the laser diode bias current generator which has capacity of sourcing up to 60mA (Bias). The laser diode bias current can be controlled by either a voltage or current into the bias adjust pin (BiasAdj) and the bias set pin (SBias), depending on how these pins are configured. Control of the bias current is achieved through the APC (Automatic Power Control) circuit. In order to avoid having a large current go through the laser diode, this IC also provides an Activity detector function for laser protection. The Activity detector circuit detects data edge transitions and if no data transition occurs after a certain period, then both the modulation and bias currents are shutdown. The bias currents are shut it down by in order to pull down the output voltage of APC OP.Amp.

When the automatic shutdown is conducted, it is possible to select whether the laser diode alarm output is activated or not. Additionally, this IC has the DFF for the input signal correction and the internal Duty Cycle correction circuit that can control the falling edge of the input pulse up to a maximum of 1.0ns(Min.).

Features

- Maximum data rate (NRZ): 622Mbps
- Alarm and Shutdown function
- DFF for input signal correction
- Input signal Duty cycle correction
- Automatic Power Control (APC) for bias current
- Activity detector function for laser protection
- Alarm signal mask function during shutdown
- Differential PECL inputs or AC coupled inputs

40 pin QFP (Plastic)



Applications

- SONET/SDH: 622Mbps
- Fibre channel: 531Mbps

Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +6.0	V
• Input voltage	V_{IN}	V_{EE} to V_{CC}	V
• Differential input voltage	$\lvert V_D - V_{DB} \rvert$	0 to 2.5	V
• Bias output current		0 to 80	mA
• SBias input/output current		0 to 5	mA
• Bias control current	IBset (Ibiasadj)	0 to 5	mA
• Bbias control voltage	VBset (Vbiasadj)	0 to 3	V
• Modulation output current		70	mA
• Modulation adjust current	IQset (Idrvadj)	0 to 15	mA
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

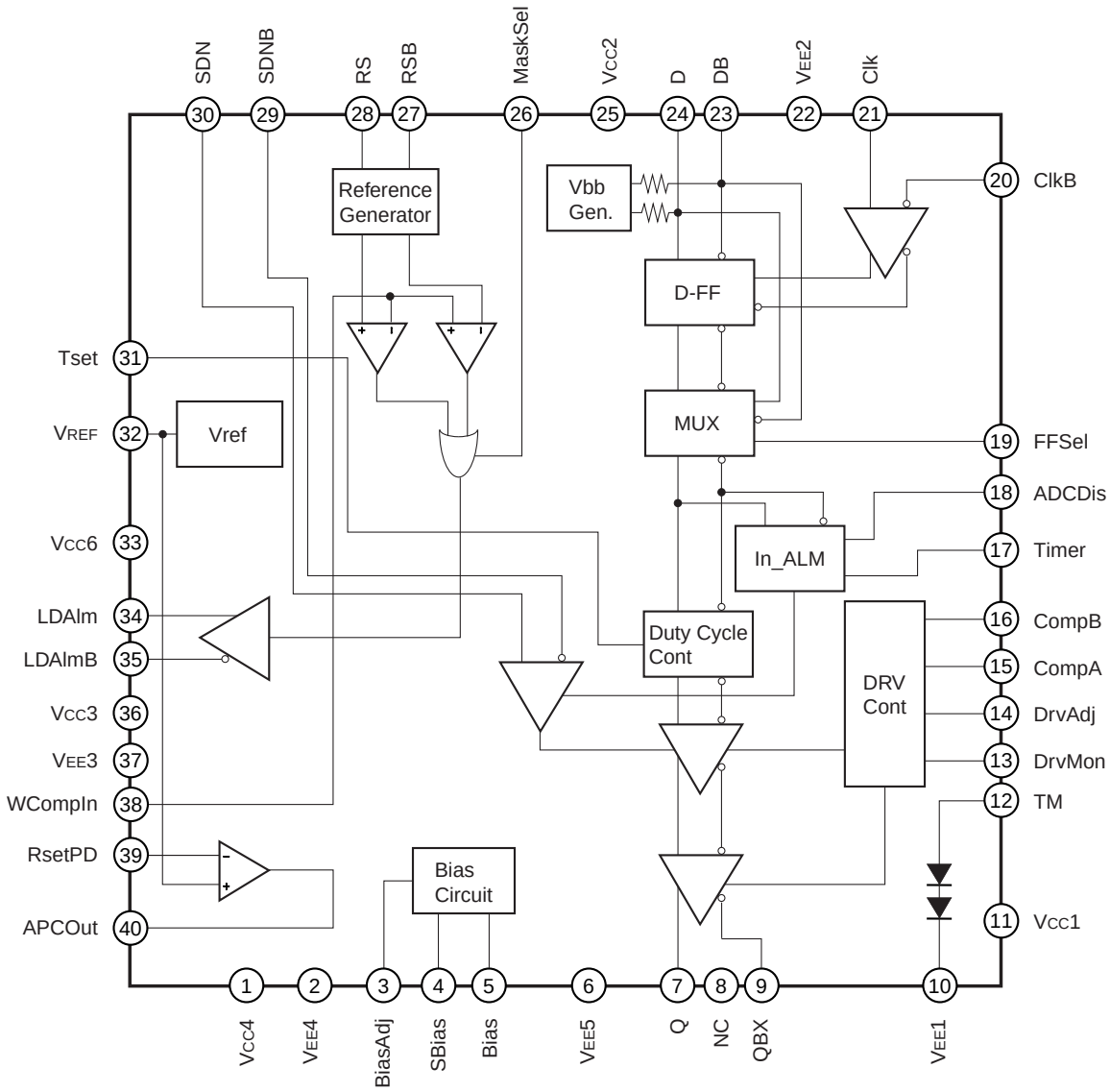
• DC supply voltage	$V_{CC} - V_{EE}$	3.14 to 3.46	V
• Operating ambient temperature	Ta	–40 to +85	°C

Structure

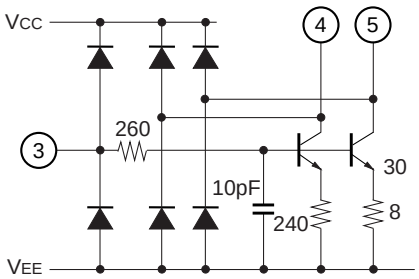
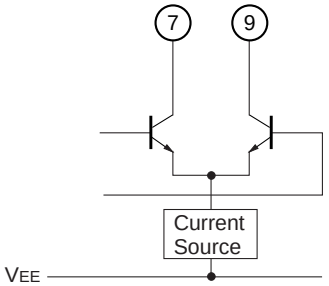
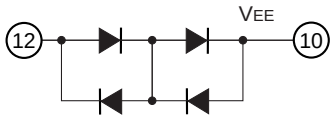
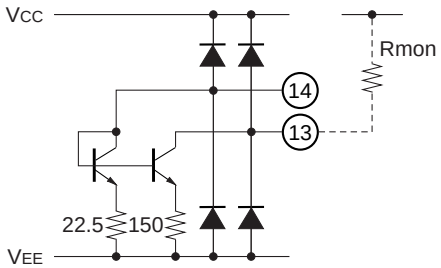
Bipolar silicon monolithic IC

E99227-PS

Block Diagram and Pin Configuration

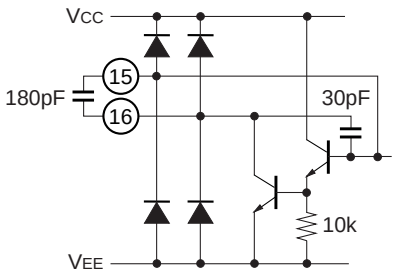
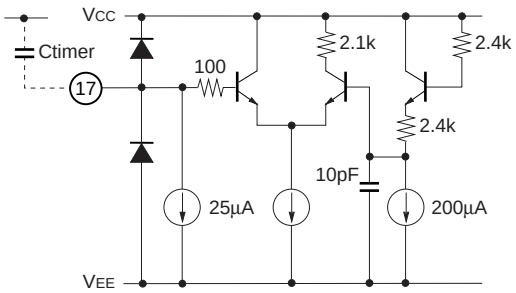
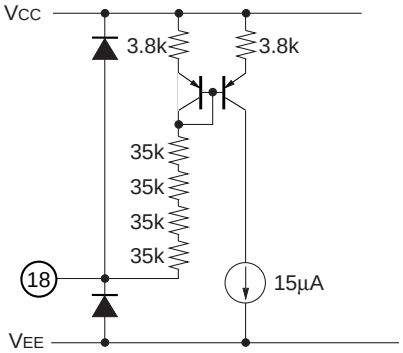
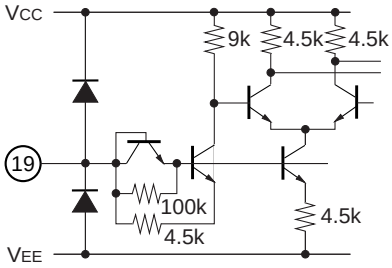


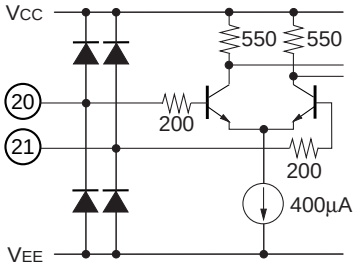
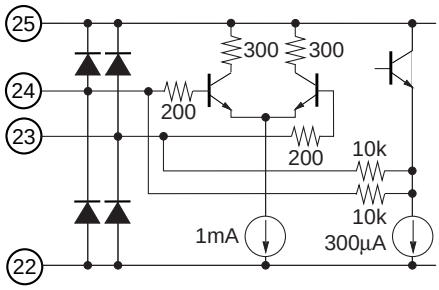
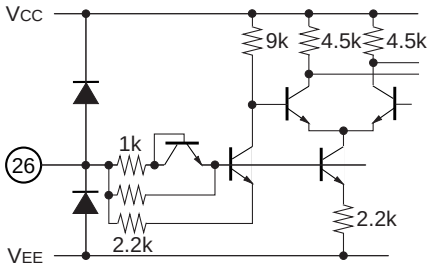
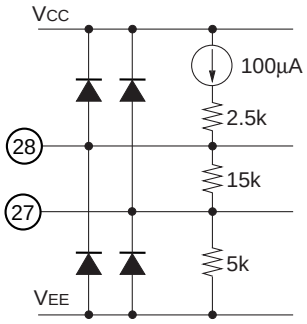
Pin Description

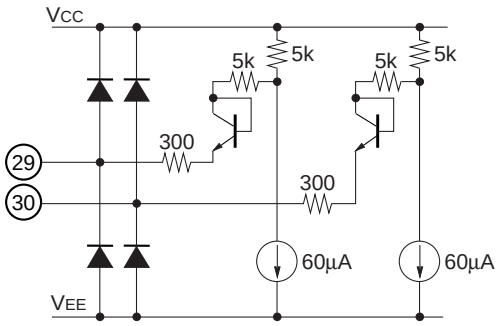
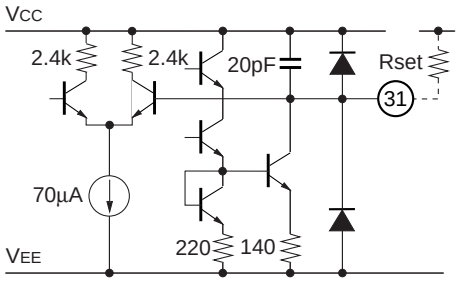
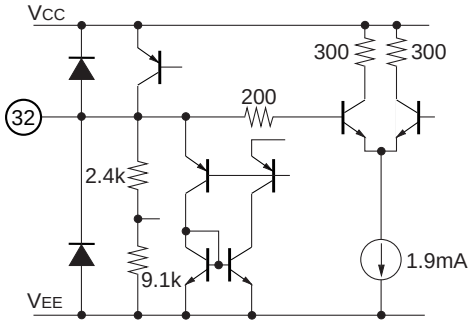
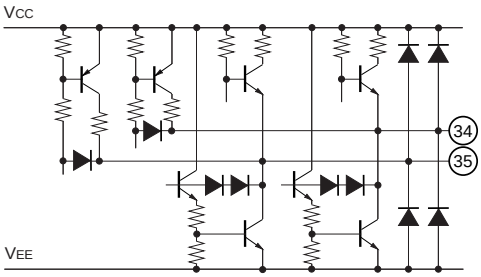
Pin No.	Symbol	Typical pin voltage [V]		Equivalent circuit	Description
		DC	AC		
1	$V_{CC}4$	3.3			Positive power supply for APC circuit.
2	$V_{EE}4$	0			Negative power supply for APC circuit.
3	BiasAdj	1.5 to 0			Bias current setting.
4	SBias	0mA to 2.5mA			Bias current setting or monitor.
5	Bias	0mA to 60mA			Bias current output. Open collector output.
6	$V_{EE}5$	0			Negative power supply for bias circuit.
7	Q	1.3 to 3.3	6mA to 30mA*1 6mA to 50mA*2		Modulation current output. Open collector output.
9	QBX	1.3 to 3.3	6mA to 30mA*1 6mA to 50mA*2		Complementary current output. Q and QBX are not symmetrical output. Use Q output for laser diode.
8	NC	—	—		No connected.
10	$V_{EE}1$	0			Negative power supply for driver circuit.
11	$V_{CC}1$	3.3			Positive power supply for driver circuit.
12	TM	1.5			Chip temperature monitor.
13	DrvMon		0mA to 1.4mA		Modulation current (IQ) monitor. IQ is monitored by connecting a resistor (Rmon) to this pin.
14	DrvAdj	0mA to 9mA			Modulation current (IQ) setting.

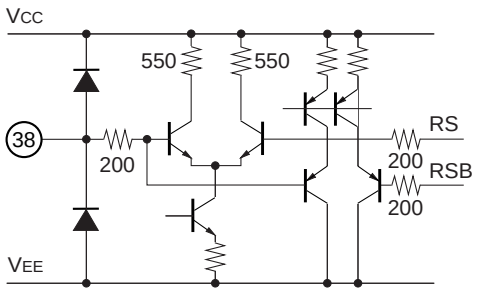
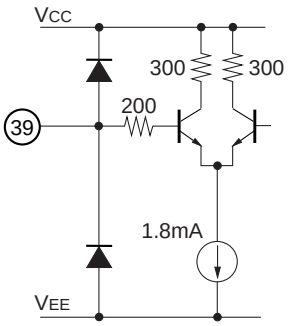
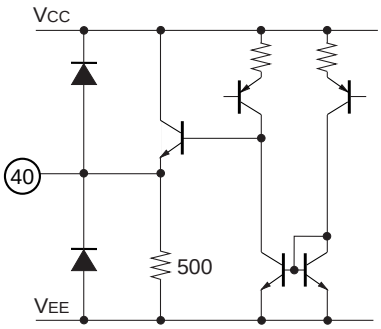
*1 Ta = –40 to 0°C

*2 Ta = 0 to +85°C

Pin No.	Symbol	Typical pin voltage [V]		Equivalent circuit	Description
		DC	AC		
15	CompA				Modulation current driver compensation. Normally, connects 180pF capacitor between CompA and CompB pins.
16	CompB				
17	Timer				Capacitor connection for activity detector (IN_ALM) operation. This pin sets the period of inactive time for activity detector. Inactive time is controlled by connecting a capacitor to this pin.
18	ADCDis	VEE to Vcc (open)			Activity detector circuit control. High (connected to Vcc or open): Activity detector is disable. Low (connected to VEE): Activity detector is enable.
19	FFSel	VEE or open			Input data D-FF selection control. High (open): FF not used (Through mode) Low (connect to VEE): FF used (FF mode)

Pin No.	Symbol	Typical pin voltage [V]		Equivalent circuit	Description
		DC	AC		
20	ClkB		1.6 to 2.4		Differential PECL clock input.
21	Clk		1.6 to 2.4		
22	VEE2	0			Negative power supply for data input circuit.
23	DB		1.6 to 2.4		Differential PECL data input.
24	D		1.6 to 2.4		
25	VCC2	3.3			Positive power supply for data input circuit.
26	MaskSel	VEE or open			Alarm signal control for optical power output forced shutdown. High (open): Alarm signal is High for shutdown. Low (connect to VEE): Alarm signal stays Low for shutdown.
27	RSB	0.5			Window comparator top/bottom threshold voltage for LD_ALARM. The alarm (fault) assert voltage can be set by the external resistor. Default voltages are RS equal to 2.0V and RSB equal to 0.5V. (Option)
28	RS	2.0			

Pin No.	Symbol	Typical pin voltage [V]		Equivalent circuit	Description
		DC	AC		
29	SDNB		0 to 3.3		Complementary TTL input to disable the output current. (Shutdown input) When left open, High.
30	SDN		0 to 3.3		
31	Tset				Output duty cycle control. This pin controls the falling edge of the input High pulse. Variable delay limit of that is from 0 to 1.0ns. Duty cycle is controlled by connecting a resistor value between VCC and this pin.
32	VREF	1.7			Temperature compensated reference voltage for APC. Approximately 1.7V (Constant for VEE reference)
33	VCC6	3.3			Positive power supply for alarm output circuit.
34	LDAlm		0.2 to 3.0		Activates when the fault is detected in the laser monitor diode circuit. (Pseudo LVTTL output)
35	LDAlmB		0.2 to 3.0		

Pin No.	Symbol	Typical pin voltage [V]		Equivalent circuit	Description
		DC	AC		
36	$V_{CC}3$	3.3			Positive power supply for signal detection circuit.
37	$V_{EE}3$	0			Negative power supply for signal detection circuit.
38	WCompIn				APC alarm signal control.
39	RsetPD				Monitor PD connection.
40	APCOut				APC operational amplifier output. This signal controls the bias adjust pins. (BiasAdj and SBias)

Electrical Characteristics

DC Electrical Characteristics

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC supply voltage	Vdc	V_{CC} – V_{EE}	3.14	3.3	3.46	V
Supply current	I_{EE}	I_Q = 0mA, I_{BIAS} = 0mA	–80	–57	—	mA
Modulation output current range	I_Q1	Ta = –40 to 0°C	6	—	30	mA
	I_Q2	Ta = 0 to +85°C	6	—	50	
Modulation output voltage range	V_Q		V_{CC} – 2	—	V_{CC}	V
Ratio of IQ vs. IQset	IQ vs IQset		4	6	9	—
Bias output current range	I_B		0	—	60	mA
Bias output voltage range	V_B		V_{CC} – 2	—	V_{CC}	V
Ratio of IB vs. IBset	IB vs IBset		14	22	28	—
ECL input High voltage	V_{EIH}		V_{CC} – 1.17	—	V_{CC} – 0.81	V
ECL input Low voltage	V_{EIL}		V_{CC} – 1.84	—	V_{CC} – 1.48	
SDN, SDNB input High voltage	V_{TIH}		2	—	V_{CC}	
SDN, SDNB input Low voltage	V_{TIL}		0	—	0.8	
LDA, LDAB output High voltage	V_{TOH}	Iin = –0.4mA	2.4	—	—	
LDA, LDAB output Low voltage	V_{TOL}	Iin = 2.0mA	—	—	0.5	
Reference bias voltage for OP Amp	V_{REF}		1.5	1.7	1.9	
Operating current range of V_{REF}	V_{REFdrv}		–500	—	+500	µA

AC Electrical Characteristics

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum data rate	fdmax		622			Mbps
Rise time (20 to 80%)	tr	I_Q = 20mA, R_L = 25Ω		200		ps
Fall time (20 to 80%)	tf	I_Q = 20mA, R_L = 25Ω		200		
Max. variable High pulse width by duty cycle control	tdelay	Data rate = 622Mbps	1.0			ns
Max. setting time of IN_Alarm	ts_alm		20			µs
Shutdown time	tsut_off				10	
Shutdown recovery time	tsut_on				100	
Maximum set up time	T_S		200			ps
Maximum hold time	T_H		200			

DC and AC Electrical Characteristics for OpAmp of APC Circuit

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}		1.2	—	2.8	V
Output voltage range	V_O		0.6	—	2	V
Input bias current	I_B		—	7	—	µA
Input offset voltage	V_{OFF}		—	2.5	—	mV
Input offset current	I_{OFF}		—	0.7	—	µA
Input impedance	Z_{IN}		—	12	—	kΩ
Output drive current	I_O		–5.0	—	1.0	mA
Through rate	SR		—	1.9	—	V/µs
Open loop gain	Av		—	55	—	dB
Unity gain band width	funit		—	20	—	MHz

Description of Each Function Block

1. Data Buffer, Clock Buffer

Data Buffer and Clock Buffer are comprised of the data buffer, clock buffer, DFF, MUX and delay generator. ECL/PECL data is input to the data buffer at a maximum data rate of 622Mbps. The input data DFF selection pin (Pin 19 FFSel) can select whether the input data is used in through mode or the signal which is corrected by the clock signal in the DFF is used. When the FFSel is open, the data becomes through mode, when the FFsel is connected VEE,the data becomes DFF mode.

And, this data is input to the delay circuit. The delay circuit adds a delay to the falling edge of the pulse up to a maximum of 1.0ns for the D input signal High pulse (Q output current pulse). The delay is set by an external resistor between the delay set pin (Pin 31 Tset) and V_{CC}. The relation between the High pulse width and the set resistance (Rset) is shown in Fig. 1.

The Vbb generator provides a reference bias current to the data buffer for AC coupling inputs.

2. Modulation Current Generator

This circuit modulates the laser diode and the modulation current can be set by feeding the current to the modulation current set pin (Pin 14 DrvAdj). The relation between the modulation current (I_Q) and the modulation set current (IQset) is shown in Fig. 2. There is also a modulation current monitor pin (Pin 13 DrvMon) that allows the IC user to monitor the modulation current by putting an external fixed resistor between V_{CC} and DrvMon pins, and the modulation current can be monitored by measuring the voltage of DrvMon pin. The relation between the modulation current (IQ) and the DrvMon current (Idrvmon) is shown in Fig. 7.

3. Laser Diode Bias Current Generator

This circuit is a very large current source capable of sourcing up to 60mA of bias current to the laser diode. The circuit is a 22 to 1 (for current – current setting) current mirror that can be controlled externally two ways.

The first method is to short BiasAdj (Pin 3) and SBias (Pin 4) together and inject a control current (IBset) into the two pins. Bias (Pin 5) is connected to the laser diode. Laser diode bias current vs. control current (IBset) characteristics is shown in Fig. 3.

The second method is to tie SBias (Pin 4) to V_{CC} and tune BiasAdj (Pin 3) with a voltage source. Varying the voltage at the BiasAdj pin will vary the current through the laser diode. Laser diode bias current vs. control voltage characteristics is shown in Fig. 4.

4. APC (Automatic Power Control) Circuit

The APC circuit is comprised of the window comparator, APC OpAmp, and laser diode alarm circuit.

The APC OpAmp is normally configured as an inverting integrator. The inverting input is connected to the photodiode that monitors the optical power output from the laser diode. The photodiode converts the optical power received from the laser diode to a current. The output of the OpAmp then drives the laser diode current bias adjust pin (BiasAdj), and the laser diode current bias set pin (SBias) is shorted to V_{CC} via a resistor. With the OpAmp configured as an inverting integrator, the OpAmp can tune the laser diode current inversely to the current in the photodiode. That is to say that if a Low current is detected by the photodiode the integrator output goes up causing more bias current to flow through the laser diode. If the photodiode current is High, the output of the OpAmp will go Low causing less bias current to flow through the laser diode.

When the output of the APC OpAmp (Pin 40 APCOut) is connected to the window comparator input pin (Pin 38 WCompIn), the function of the window comparator detects the voltage which is outside of the reference voltage range for each comparator (RS, RSB). When this happens, the comparator outputs cause the laser diode alarm output (LDAlm) to go High alerting the system that the laser diode current is in the outside of the range.

The laser diode alarm output state can be controlled by the alarm signal control pin (Pin 26 MaskSel) for the optical power output forced shutdown. When the automatic shutdown is conducted and MaskSel pin is left open, the laser diode alarm output goes High. The laser diode alarm output is kept Low (disable) by connecting MaskSel pin to V_{EE}.

5. Shutdown and Input Alarm Circuits

These circuits disable both the modulation current and the bias current under various conditions. The function block diagram for all of the shutdown mechanisms for the circuit is shown in Fig. 5.

The Shutdown circuit has complementary TTL input to disable the output current. Shown below is the desired truth table for the shutdown function.

SDN	SDNB	Output current
Low	Low	Off
Low	High	On
High	Low	Off
High	High	Off

The Activity detector (In_ALM) circuit is designed to detect the input data edge transition. If there is no input data transition over a certain period determined by the user (T_{ACT}), the Shutdown circuit is enabled, causing the modulation current and bias current to be shutdown. The Inactive time (T_{ACT}) is set by the external capacitor value between Timer (Pin 17) and V_{CC}. The relation between the Inactive time and Ctimer is shown in Fig.6.

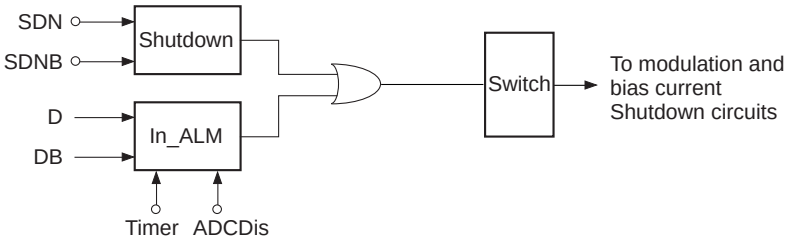


Fig.5. Shutdown and In_ALM Functional Block Diagram

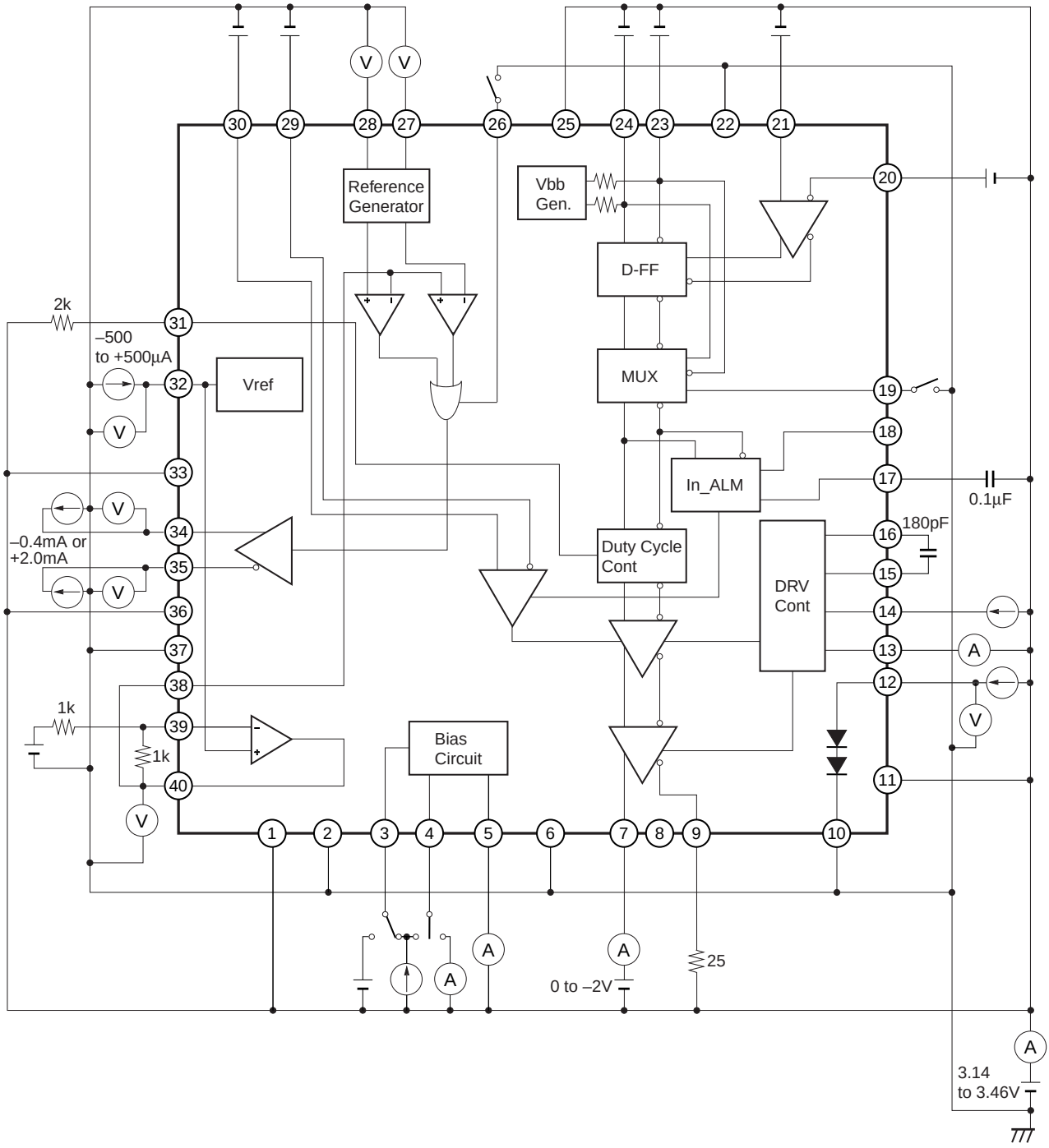
6. Others

Pay attention to handling this IC because its electrostatic discharge strength is weak.

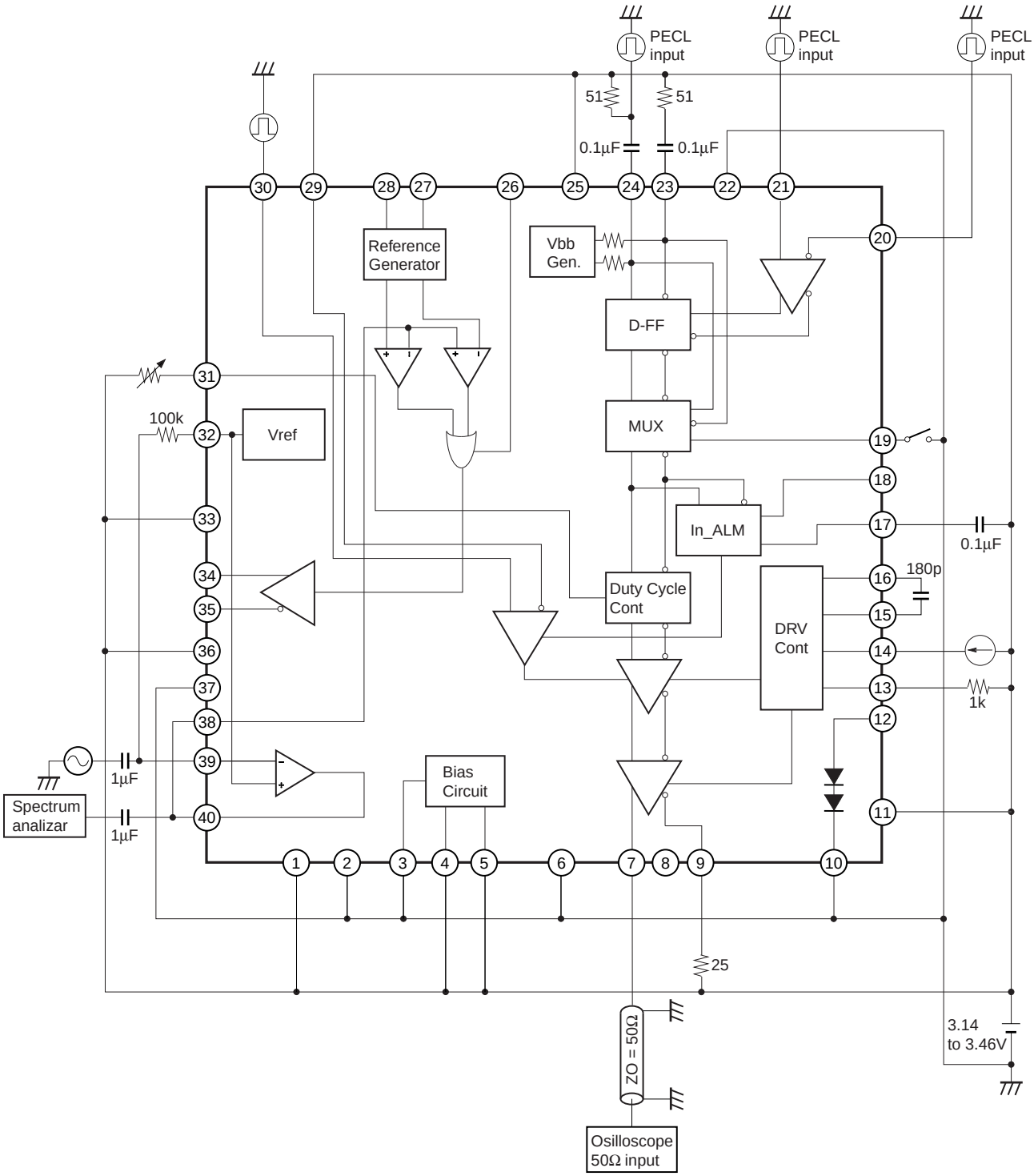
The Tset pin (Pin 31) should be connected to V_{CC} through a resistor.

Do not leave this pin open or connect to V_{CC} directly.

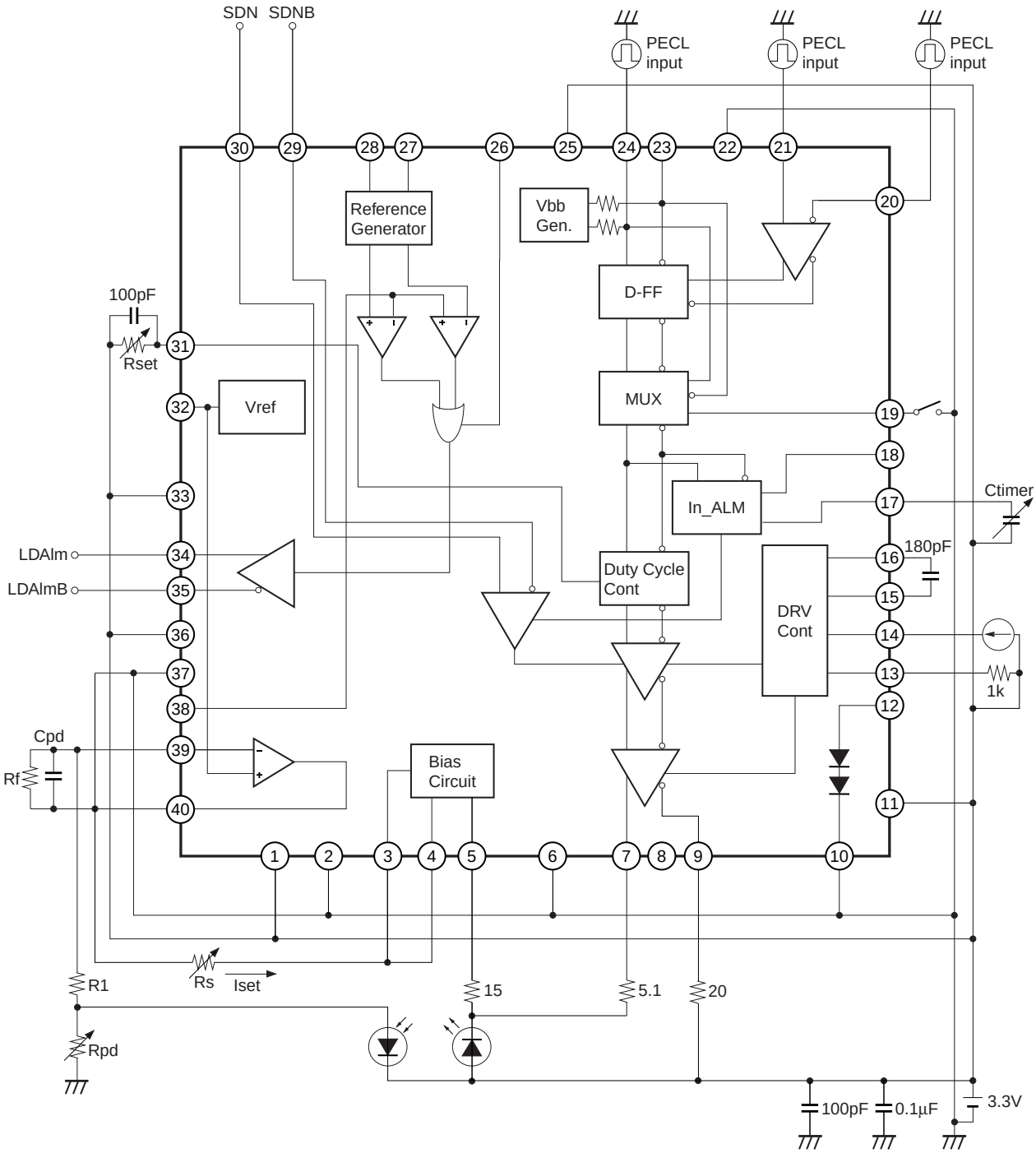
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit (at V_{CC} = 3.3V, V_{EE} = 0V)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

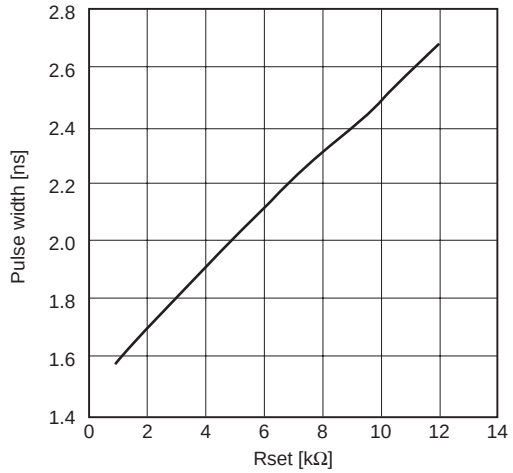


Fig. 1. Pulse width vs. Rset characteristics when 1.6ns input data pulse (622Mbps) is applied

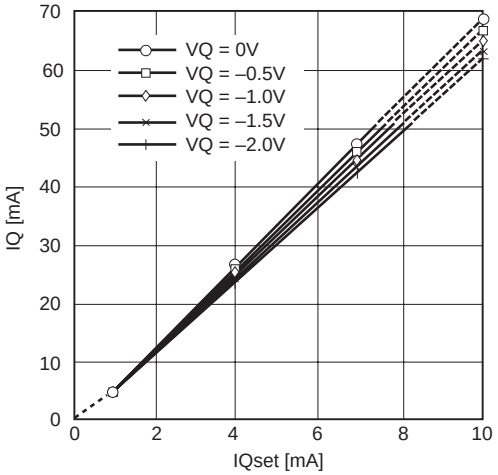


Fig. 2. Modulation current (I_Q) vs. IQset characteristics

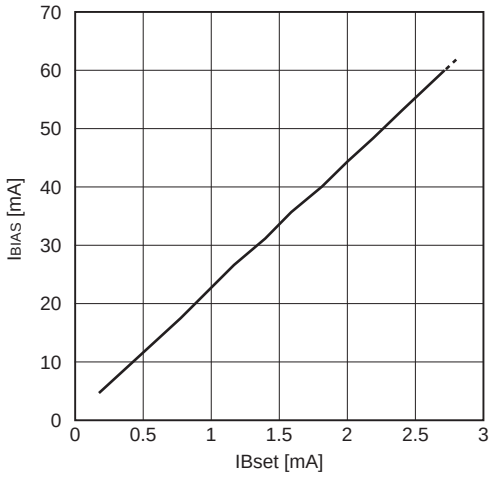


Fig. 3. Bias current (I_{BIAS}) vs. Bias adjust current (IBset) characteristics

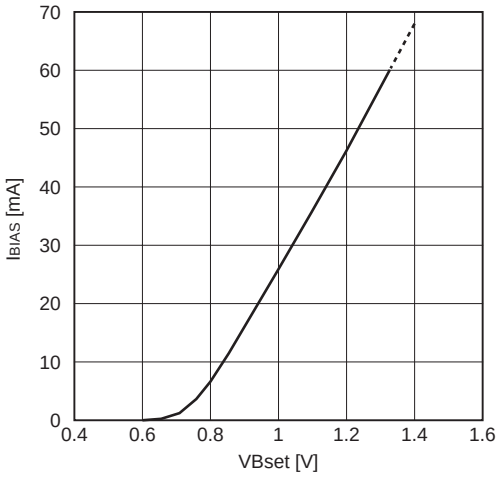


Fig. 4. Bias current (I_{BIAS}) vs. Bias adjust voltage (VBset) characteristics

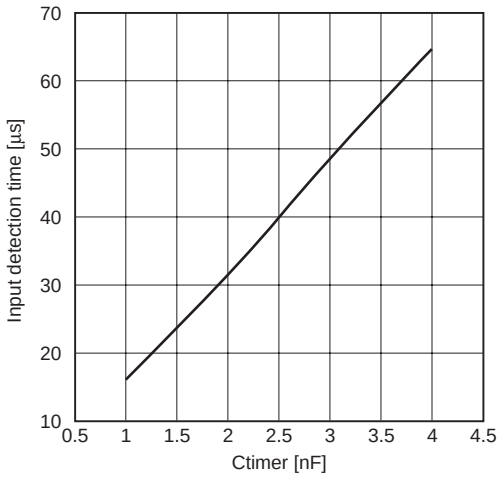


Fig. 6. Input detection time vs. Ctimer characteristics

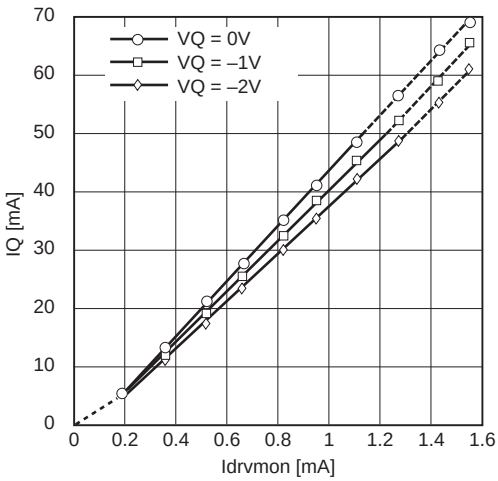
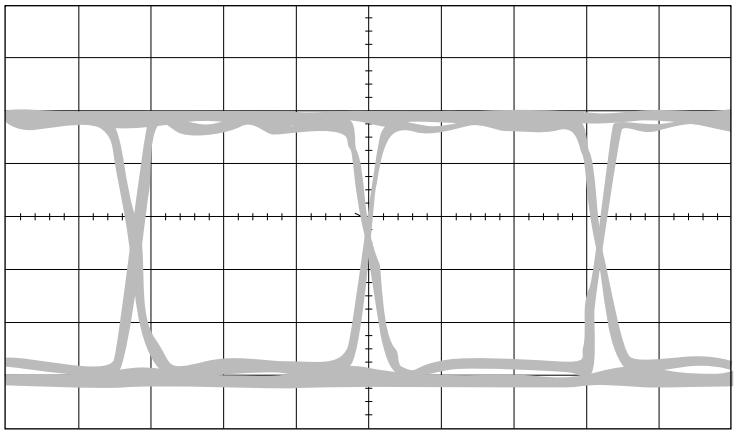


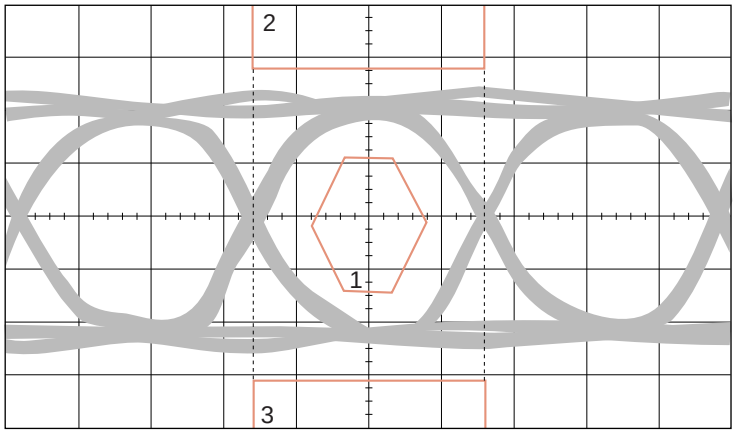
Fig. 7. Modulation current (IQ) vs. DrvMon current characteristics



V_{CC} = 0V
V_{EE} = –3.3V
RL = 25Ω
Ta = 27°C
IQ = 30mA
Single-phase input
Pattern = PRBS2^{23} – 1
Data Rate 622Mbps

Ch.1: 150mV/div
Time Base: 500ps/div

Fig. 8. Electrical Output Waveform

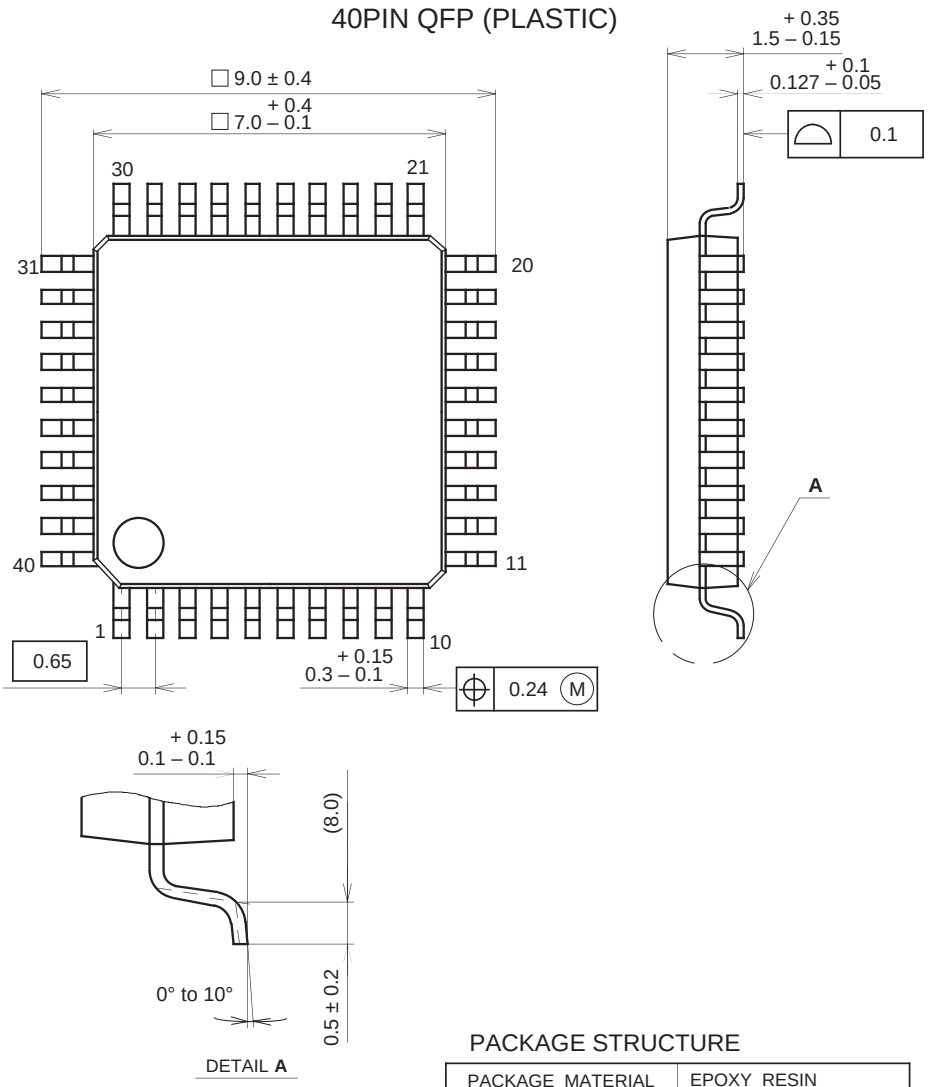


V_{CC} = 0V
V_{EE} = –3.3V
FP – LD (λ = 1330nm)
Ta = 27°C
Single-phase input
Pattern = PRBS2^{23} – 1
Data Rate 622Mbps
Filter (Cut Off 450MHz)
Mask: STM4/OC12

Ch.2: 5.0mV/div
Time Base: 500ps/div

Fig. 9. Optical Power Output Waveform

Package Outline Unit: mm



SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).