SONY

CX20206

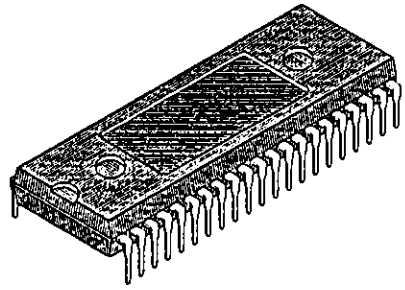
8 bit 35 MSPS RGB 3-Channel D/A Converter

For the availability of this product, please contact the sales office.

Description

CX20206 is an 8 bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

42 pin SDIP (Plastic)



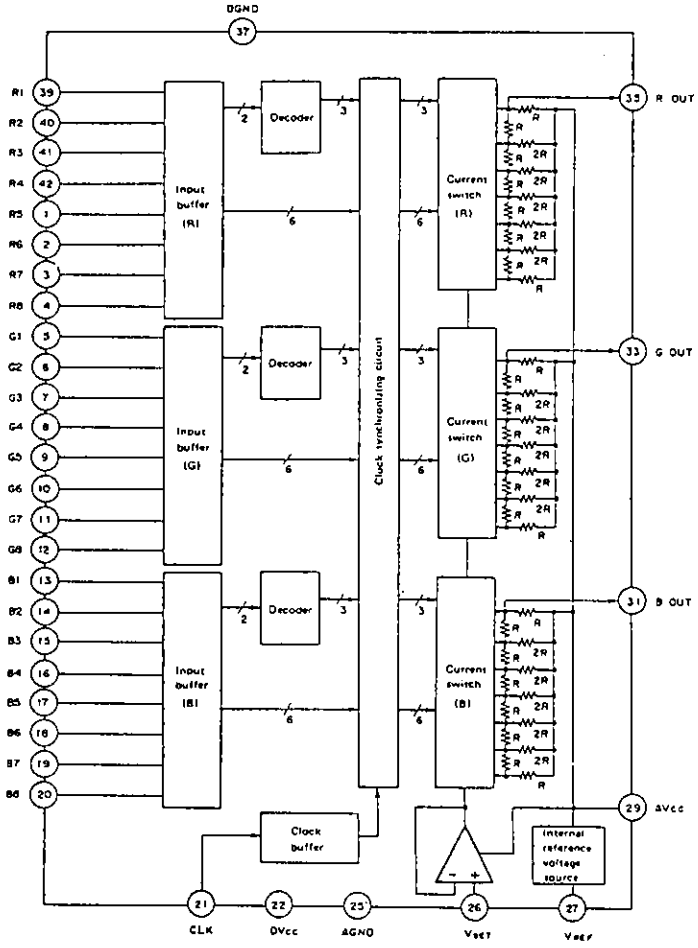
Features

- Resolution: 8 bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

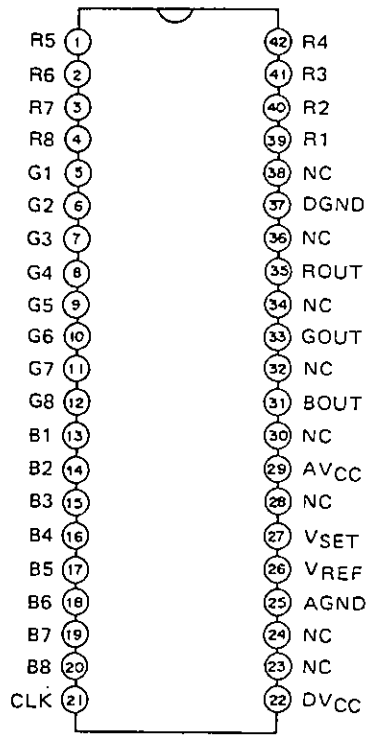
Structure

Bipolar silicon monolithic IC

Block Diagram



Pin Configuration (Top View)



E89638-ST

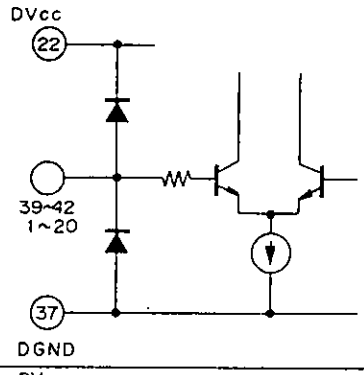
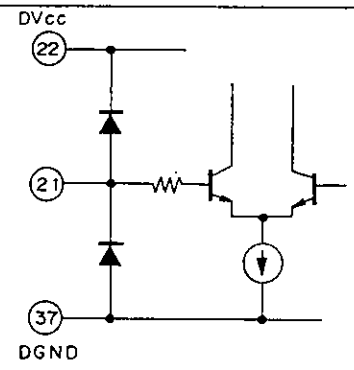
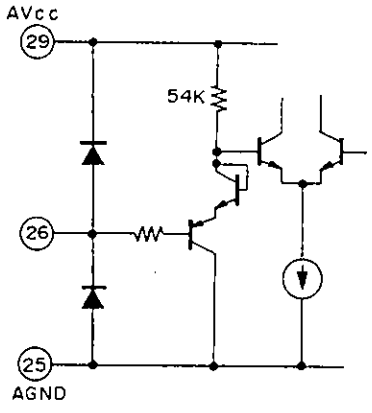
Absolute Maximum Ratings (Ta=25°C)

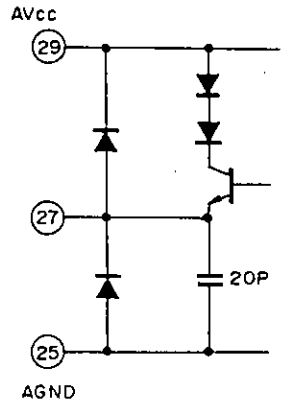
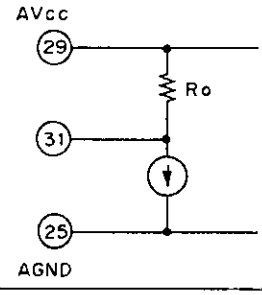
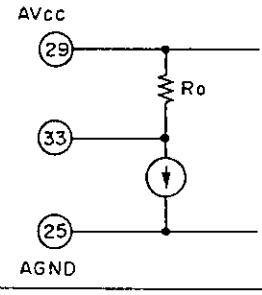
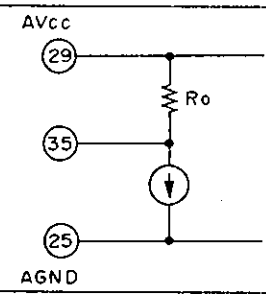
• Supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.5	W

Recommended Operating Conditions

• Supply voltage	AVcc, DVcc	4.5 to 5.5	V
	AVcc–DVcc	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	VIH, V_{CLKH}	2.0 to DVcc	V
L level	VIL, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 0.9	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 1 to 20	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock input pin.
22	DVcc		Digital Vcc.
23 24	NC		Vacant pin (non-connection)
25	AGND		Analog GND.
26	VSET		Bias input pin. Normally, apply 0.8V. See "Note on use".

No.	Symbol	Equivalent circuit	Description
27	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
28	NC		Vacant pin (non-connection)
29	AVcc		Analog Vcc
30	NC		Vacant pin but connect to AVcc*
31	BOUT		Analog output pin for BLUE.
32	NC		Vacant pin but connect to AVcc*
33	GOUT		Analog output pin for GREEN.
34	NC		Vacant pin but connect to AVcc*
35	ROUT		Analog output pin for RED.
36	NC		Vacant pin but connect to AVcc*
37	DGND		Digital GND
38	NC		Vacant pin (non-connection)

*: Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics

(Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item			Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	V_{SET}−AGND=0.8V R_L>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			f_{MAX}	V_{SET}−AGND=0.8V R_L>10kΩ C_L<20pF	35			MSPS
Full-scale output voltage(note 1)			V_{OFS}		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio(note 2)			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			R_O		270	340	420	Ω
Consumption current			I_D	V_{SET}−AGND=0.8V R_L>10kΩ I_{REF}=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	$I_{IH(U)}$	V_I=DVcc		1.2	20	μA
		Lower 6 bits	$I_{IH(L)}$			0.6	10	μA
	L level	Upper 2 bits	$I_{IL(U)}$	V_I=DGND	−10	0	10	μA
		Lower 6 bits	$I_{IL(L)}$		−10	0	10	μA
Clock input current		H level	I_{CLKH}	V_{CLK}=DVcc		3	30	μA
		L level	I_{CLKL}	V_{CLK}=DGND	−10	0	10	μA
V_{SET} input current			I_{SET}	V_{SET}−AGND=0.8V	−5	−0.3	0	μA
Internal reference voltage			V_{REF}	I_{REF}=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

(Note 1) $A_{VCC}-V_O$

(Note 2) Maximum value among

$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|,\ 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|,\ \text{or}\ 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

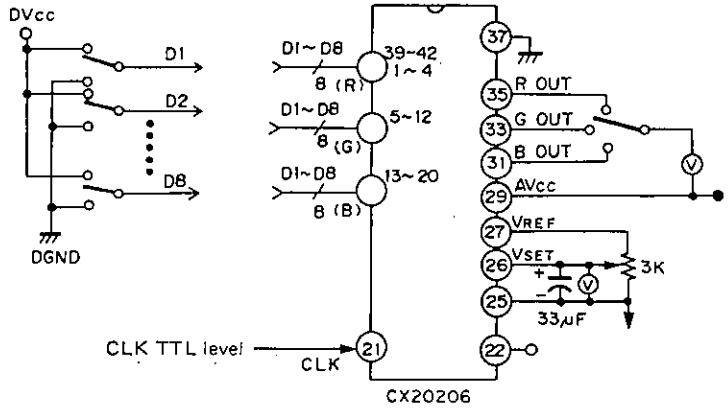
Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	Vcc+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

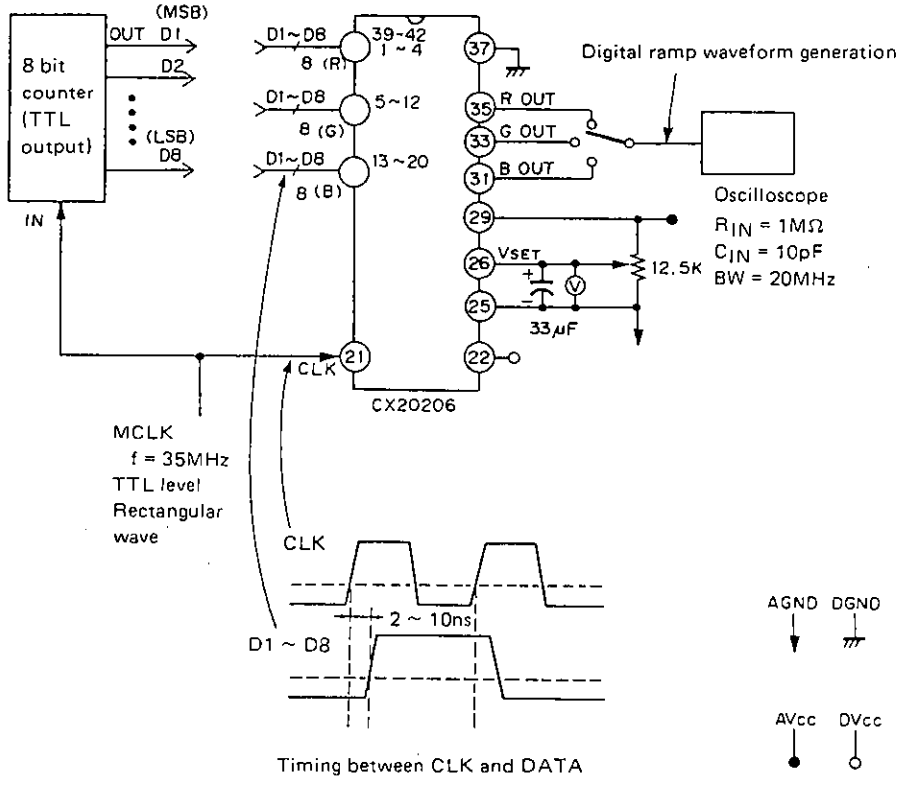
In case the output voltage full-scale is 1.00V. (1 LSB=3.92 mV)

Electrical Characteristics Measuring Circuit

Differential linearity and integral linearity measuring circuits



Maximum conversion speed measuring circuit



Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage measuring circuits

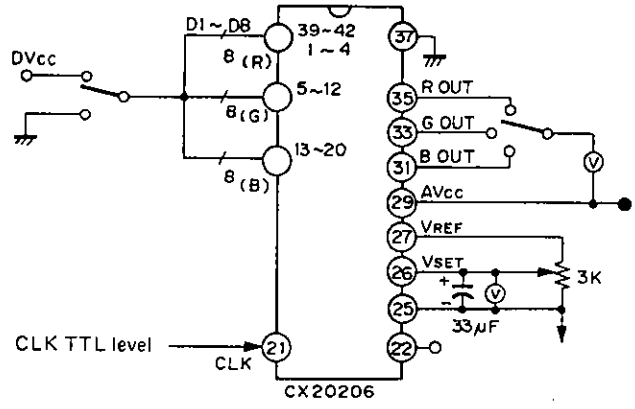
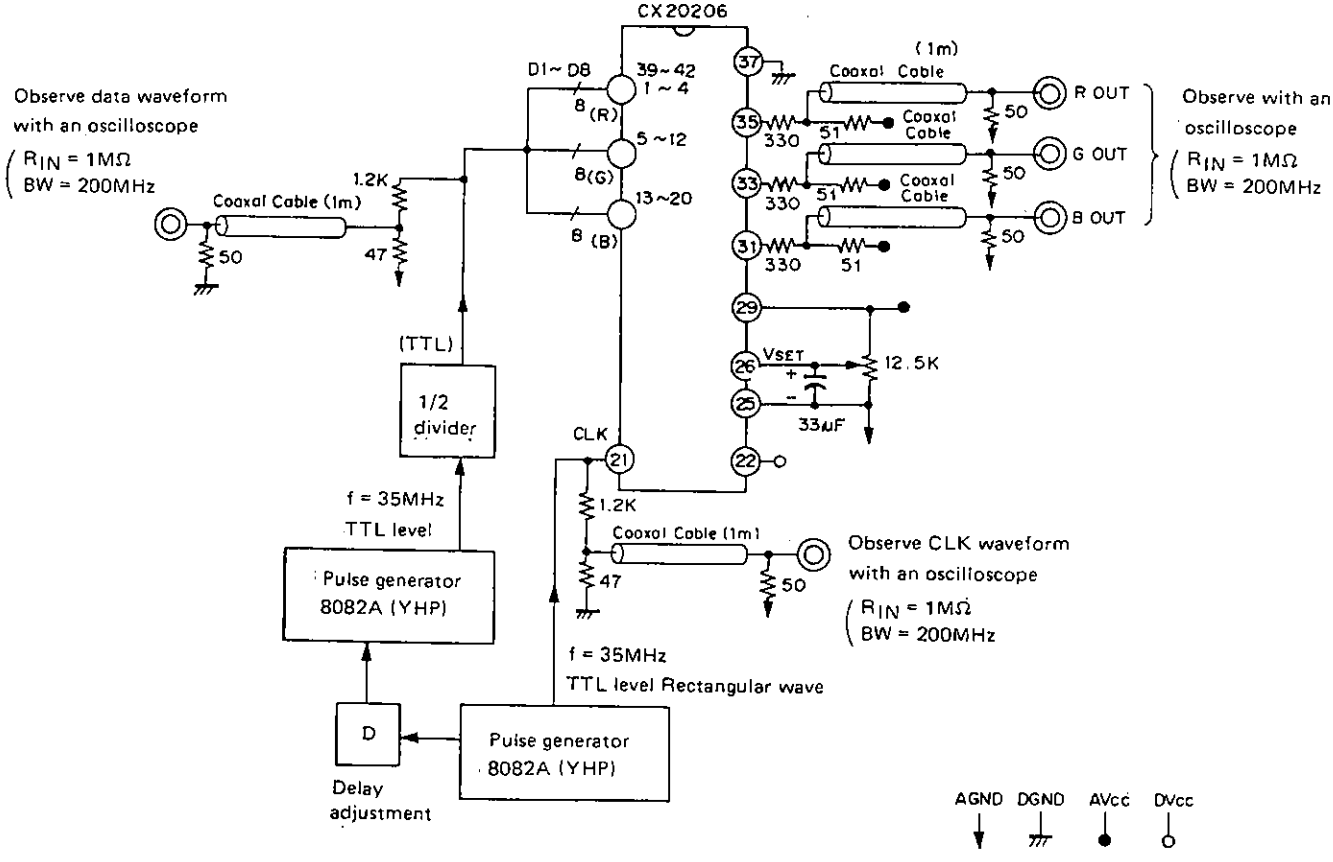


Fig. 1

Set-up time, hold time, and rise and fall time measuring circuits



Standard Circuit Design Data (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p R_L>10kΩ C_L<20pF f_{DATA}=7MHz f_{CLK}=14MHz See Fig.2		−40	−33	dB
Glitch energy	GE	V_{SET}−AGND=0.8V R_L>10kΩ f_{CLK}=1MHz Digital ramp output See Fig.3(note 1)		160		pV-s
Rise time(note 2)	tr	V_{SET}−AGND=0.8V See Fig. 1.		5.5		ns
Fall time(note 2)	tf			5.0		ns
Settling time	tset			16		ns

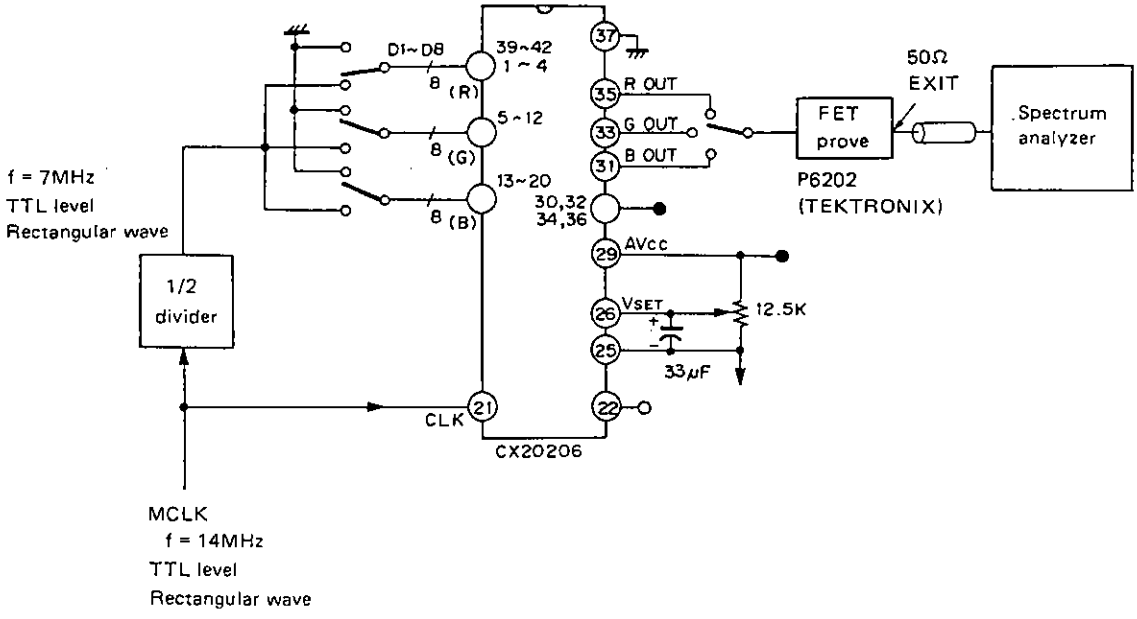
(Note 1) Observe the glitch which is generated when the digital input varies as follows:

0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

(Note 2) The time required for the D/A OUT to arrive at 90% of its final value from 10%.

Standard Circuit Design Data Measuring Circuit

Fig. 2 Crosstalk among R, G and B measuring circuit

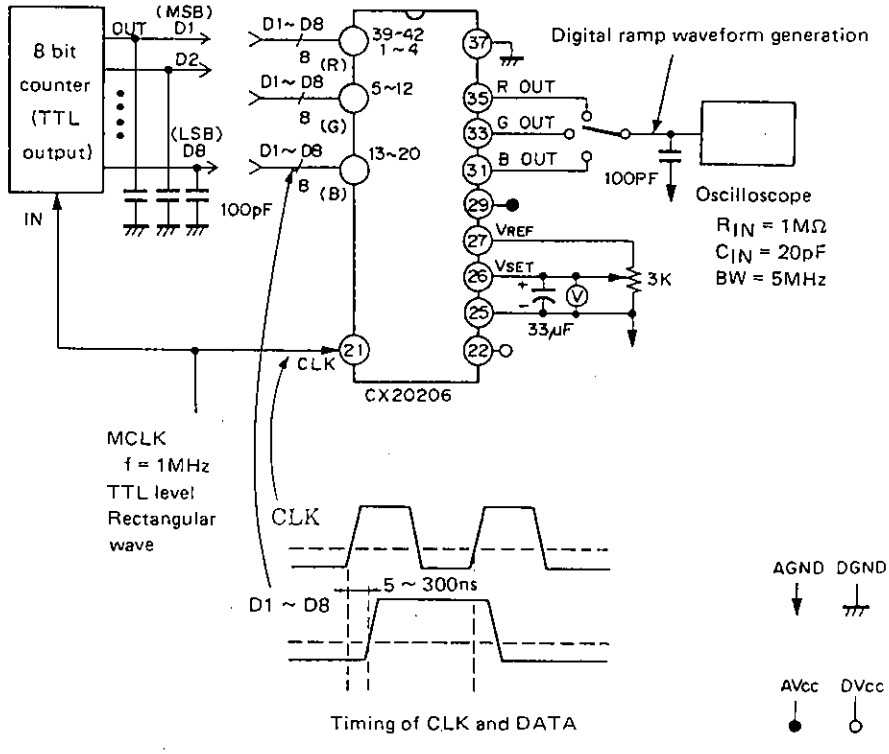


[Measuring method]

In case the measuring crosstalk of G → R

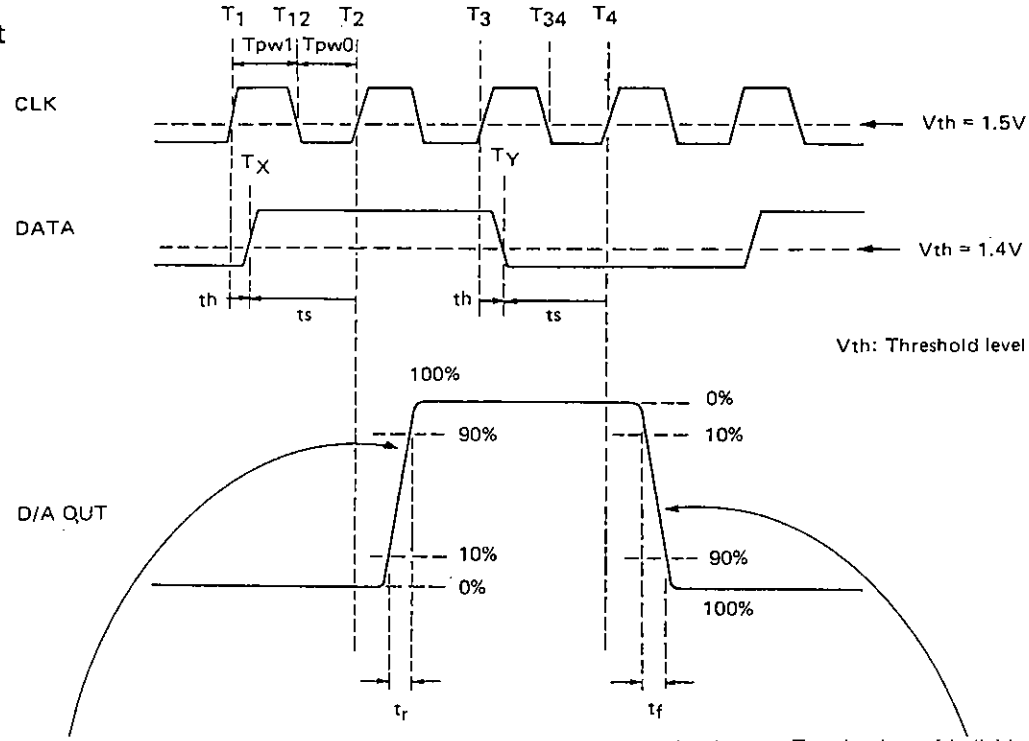
1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Fig. 3 Glitch energy measuring circuit



Operation Description

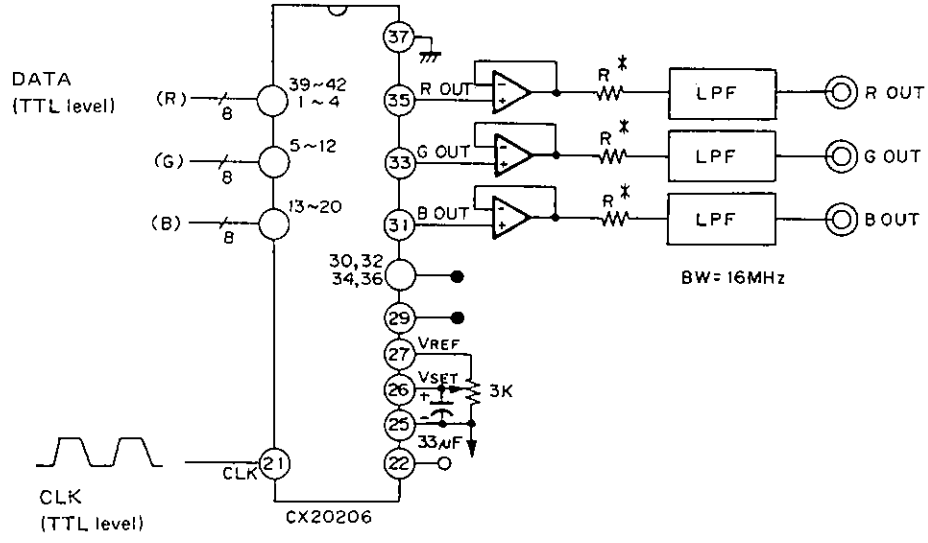
Timing chart



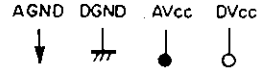
At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_4)).

Applied Circuit Example



R* is matching resistance for LPF



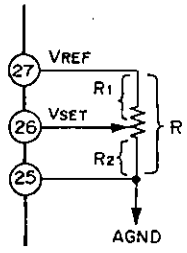
Note on Use

(1) Setting of pin 26 (V_{SET})

The full-scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.

When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of 1 Vp-p can be obtained.

(Example of use)

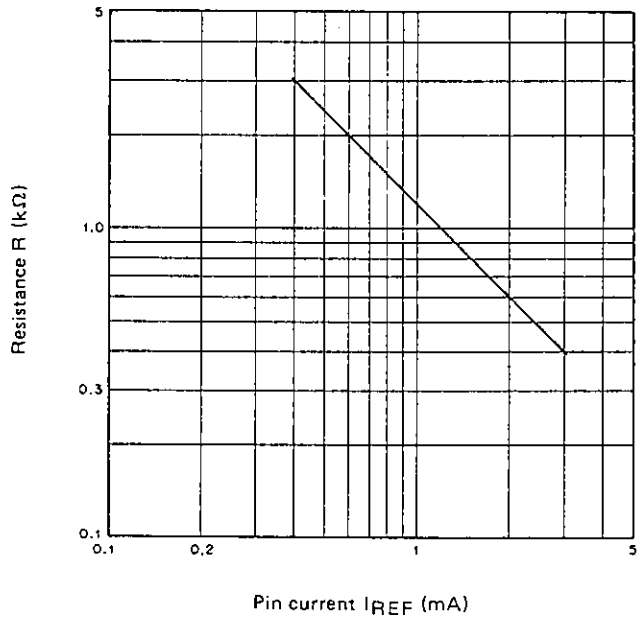


(Adjustment method)

1 The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
$R = V_{REF}/I_{REF}$

2 Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
(At this point, it becomes R1:R2=1:2)

Fig. 4 Resistance vs. V_{REF} pin current



(2) Phase relationship between data and clock

In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.

Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the load of D/A output pin

Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

$R_L > 10\ k\Omega$

$C_L < 20\ pF$

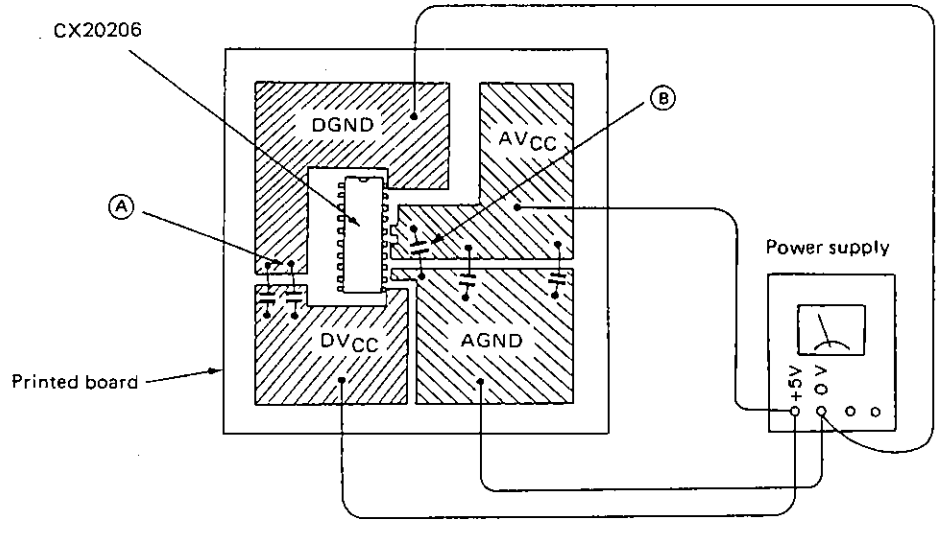
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

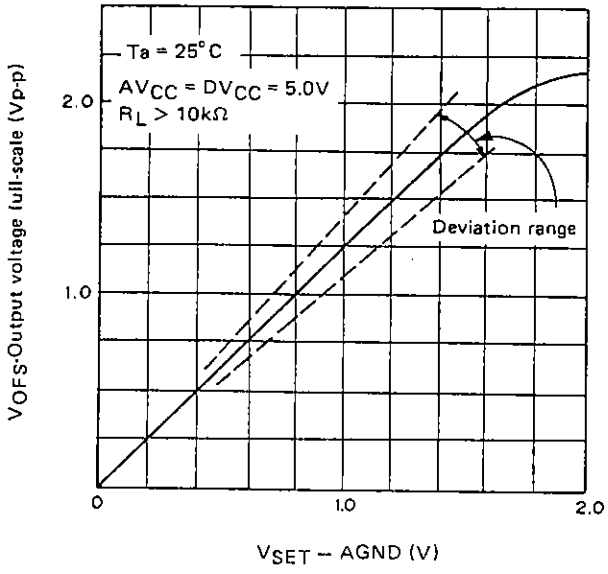
(4) Noise reduction measures

As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.

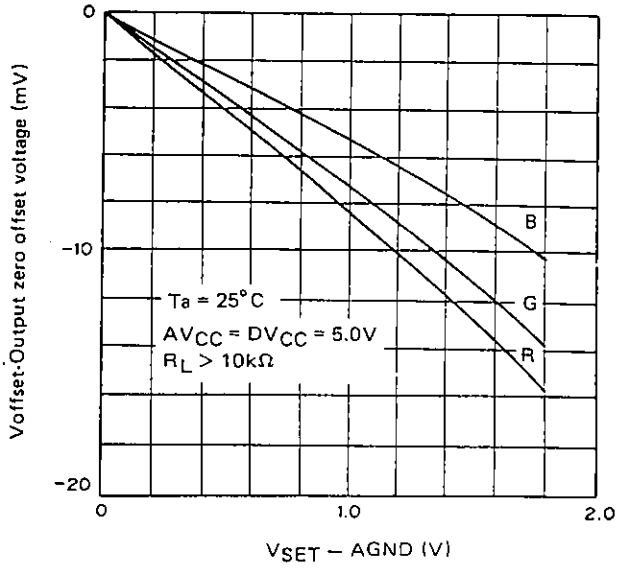
- When mounting onto the printed board, allow as much space as possible to the ground surface and the Vcc surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AVcc and DVcc. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AVcc and DVcc be conducted separately, and then making AGND and DGND as also AVcc and DVcc in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the Vcc surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the Vcc surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 25 (AGND) and pin 26 (V_{SET}).



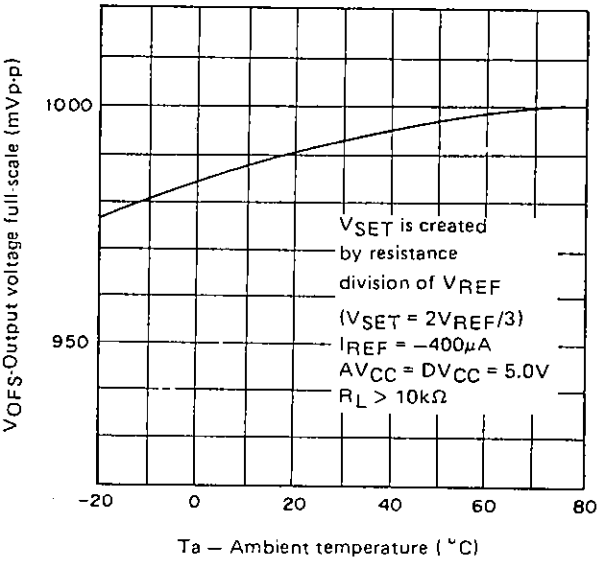
Output voltage full-scale vs. V_{SET}—AGND



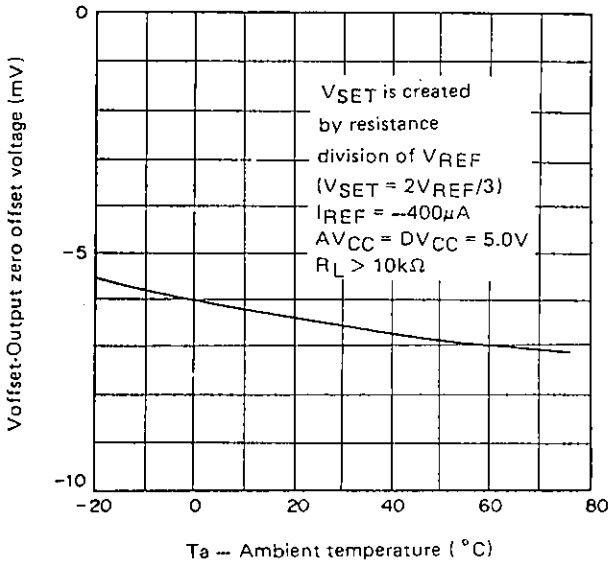
Output zero offset voltage vs. V_{SET}—AGND



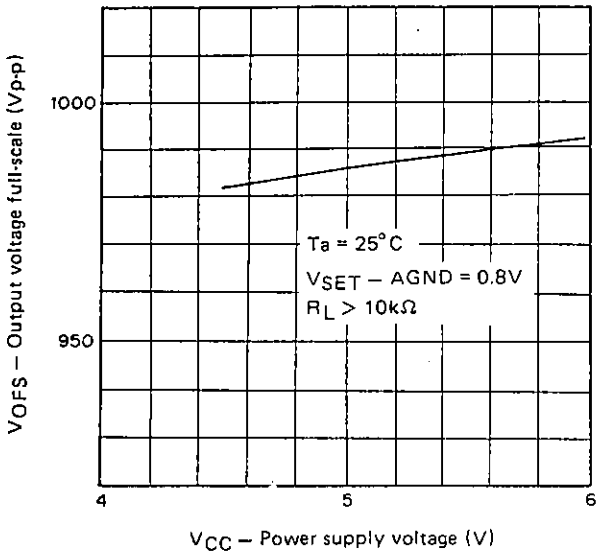
Output voltage full-scale vs. Ambient temperature



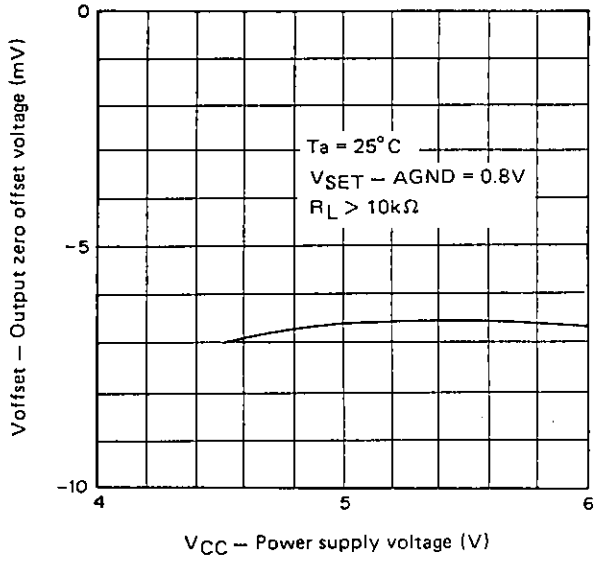
Output zero offset voltage vs. Ambient temperature



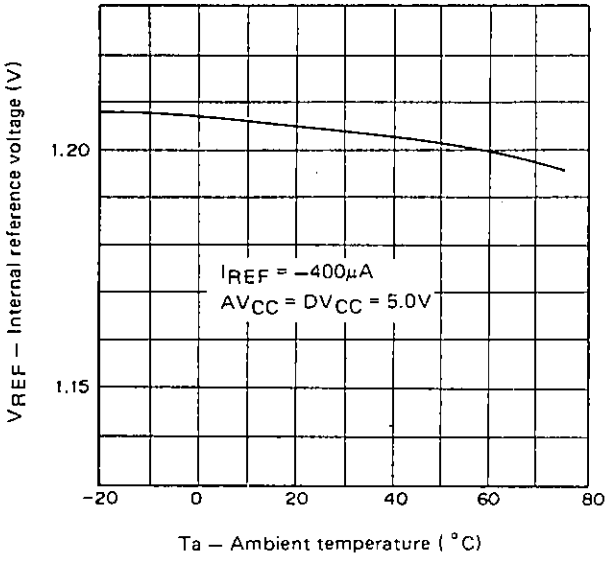
Output voltage full-scale vs. Power supply voltage



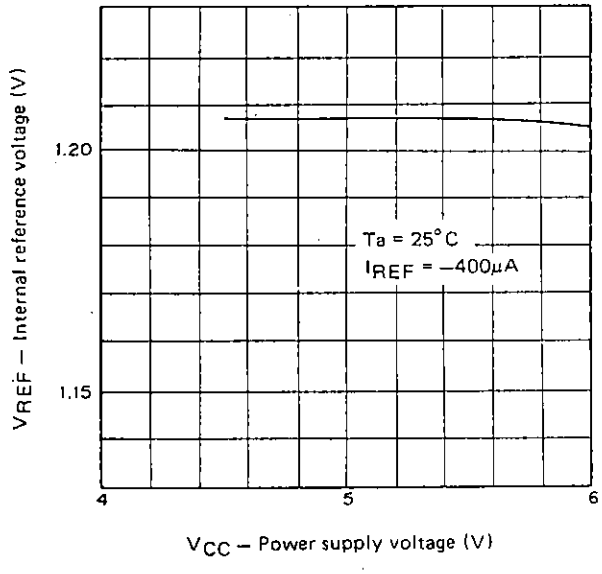
Output zero offset voltage vs. Power supply voltage



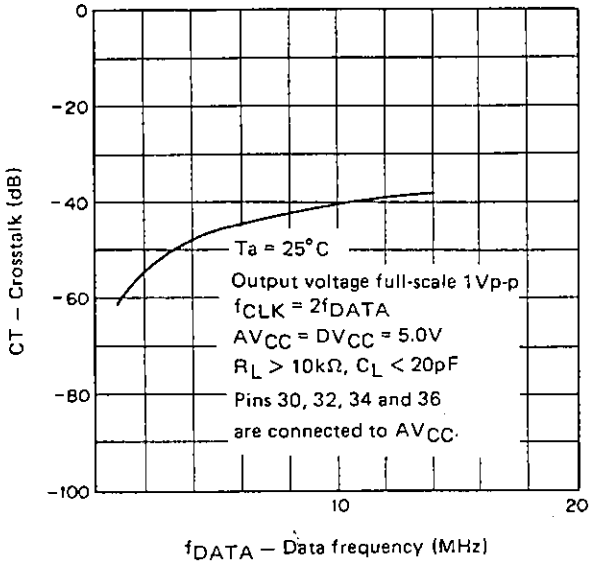
Internal reference voltage vs. Ambient temperature



Internal reference voltage vs. Power supply voltage



Crosstalk among R, G and B vs. Data frequency



Package Outline Unit: mm

42 pin SDIP (Plastic) 600 mil 4.4g