SONY

CXA1047M

Recording Y/C Amplifier

For the availability of this product, please contact the sales office.

Description

CXA1047M is a bipolar IC developed to process the recording signals (luminance/chroma signals) of 8 mm video's.

Features

- Recording Y(Luminance)/C(Chroma) signals can be processed by 1 chip IC.
- Built-in, DDS (Date Display System) and timing phase detector, circuits.
- Low power consumption 95 mW (Typ.) (during recording)
- Single supply voltage 5 V

Functions

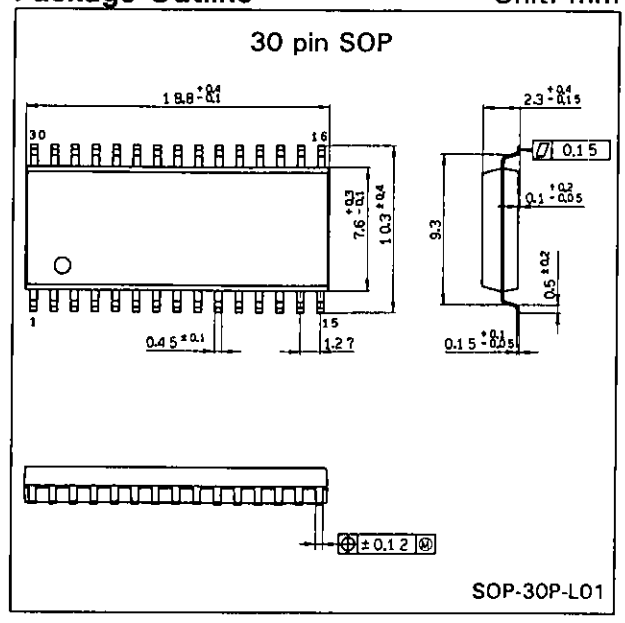
Y clamp circuit, KNEE circuit, camera white clip, Y emphasis circuit, white clip circuit, dark clip circuit, FM modulater, chroma emphasis circuit, chroma AGC, MUTE circuit, DDS circuit. Timing phase detector circuit, 4.2 V regulator.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

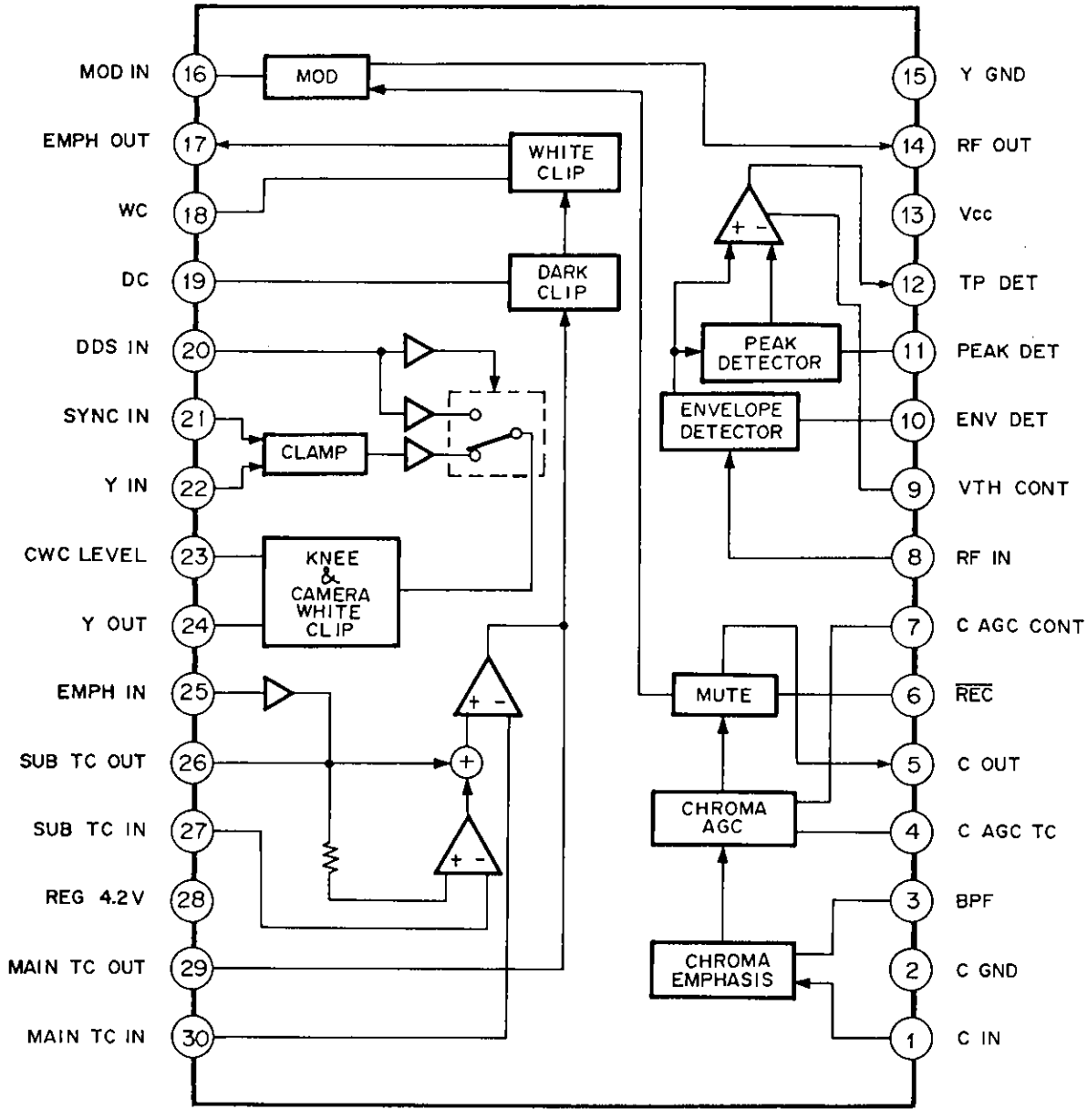
• Supply voltage	V_{CC}	7.0	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	600	mW

Recommended Operating Condition

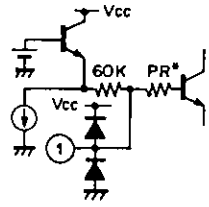
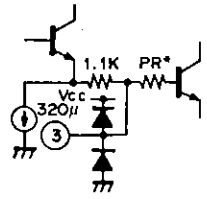
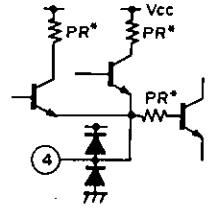
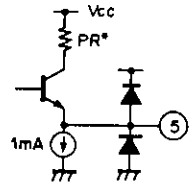
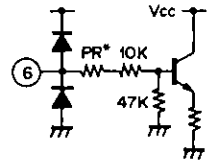
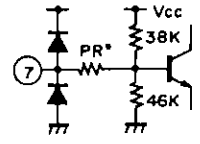
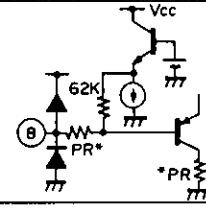
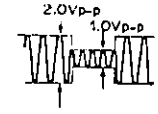
• Supply voltage	V_{CC}	4.5 to 5.5	V

70607-TO

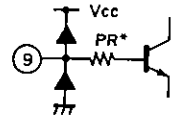
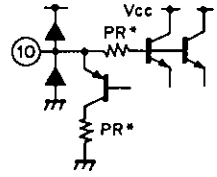
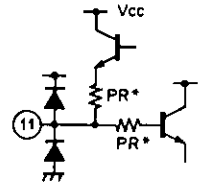
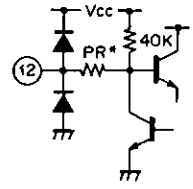
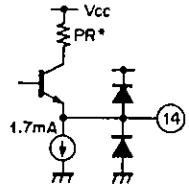
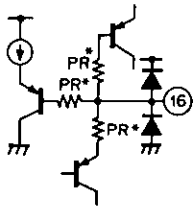
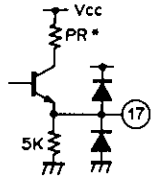
Block Diagram



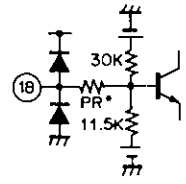
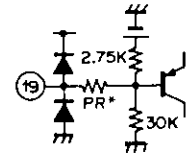
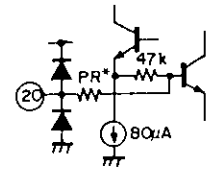
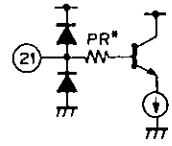
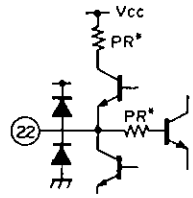
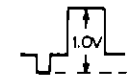
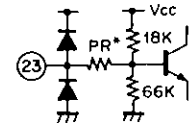
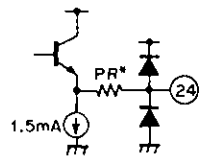
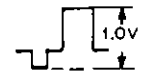
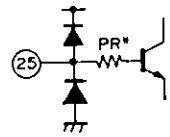
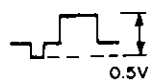
Pin Description and Equivalent Circuit

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
1	C IN		2.8 V	420 mVp-p (Ref. level)	Down converted chroma (743 kHz) signal input pin.
2	C GND	–	–	–	GND for chroma emphasis, chroma AGC and 4.2 V Reg.
3	BPF		2.35 V	–	BPF connecting pin for chroma emphasis.
4	C AGC TC		1.3 V	–	Time constant connecting pin for chroma AGC.
5	C OUT		2.4 V	420 mVp-p	Chroma signal output pin.
6	$\overline{\text{REC}}$		–	–	Control pin for REC/PB mode Vcc to 3.0 V: PB 1.0 V to GND: REC
7	C AGC CONT		2.3 V	–	Chroma AGC level adjustment pin. By applying an external DC, AGC setting level can be varied.
8	RF IN		3.7 V		Playback RF signal input pin for Timing phase detector. (Track adjustment, f3 detection)

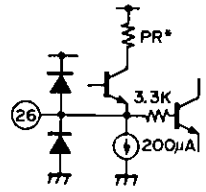
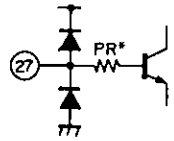
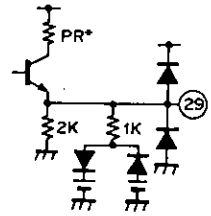
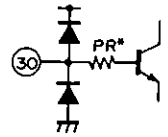
Note) PR indicates Protective Resistance (about 140Ω).

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
9	V TH CONT		1.3 V	–	Sets the peak level (V_{TH}) of the peak detection circuit. By applying an external DC, V_{TH} can be varied.
10	ENV DET		4.4 V	–	Connects the time constant for the detection of the playback RF signal envelope.
11	PEAK DET		3.7 V	–	Connects the time constant for the peak detection of the playback RF signal envelope.
12	TP DET		–	–	Peak detection output pin for the playback RF signal envelope.
13	V_{CC}	–	–	–	Supply pin
14	RF OUT		3.3 V	500 mVp-p	FM MOD output pin
15	Y GN	–	–	–	GND for Y system amplifier, Y emphasis and DDS, timing phase detector circuits.
16	MOD IN		2.1 V	–	FM MOD input pin (Current input). Imaginary-shorted to 2.1 V ($V_{REG}/2$)
17	EMPH OUT		2.1 V	250 mVp-p	Output pin of Y signal emphasis circuit.

Note) PR indicates Protective Resistance (about 140Ω).

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
18	WC		2.7 V	–	Sets the white clip level of Y signal. By applying an external DC, the white clip level can be varied.
19	DC		1.9 V	–	Sets the dark clip level of Y signal. By applying an external DC, the dark clip level can be varied.
20	DDS IN		2.4 V	–	DDS signal input pin. An input level above 40 mVo-p is necessary.
21	SYNC IN		–	–	Composite sync input pin. H level: 3.5 V to V_{CC} L level: GND to 1.0 V
22	Y IN		2.1V	 (100% white)	Input pin for Y signal from the camera system.
23	CWC LEVEL		3.3 V	–	Sets the white clip level of the Y signal from the camera system. By applying an external DC, the white clip level can be varied.
24	Y OUT		2.1 V	 (100% white)	Output pin of Y signal (including DDS signal).
25	EMPH IN		–		Input pin of the Y signal emphasis circuit.

Note) PR indicates Protective Resistance (about 140Ω).

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
26	SUB TC OUT		2.1 V	500 mVp-p	The time constant for the sub emphasis circuit of the Y signal emphasis circuit is connected.
27	SUB TC IN		–	–	The time constant for the sub emphasis circuit is connected. It is also the input pin of the sub emphasis limiter.
28	REG 4.2 V	–	4.2 V	–	Regulator (4.2 V) output pin.
29	MAIN TO OUT		2.1 V	250 mVp-p	The time constant for the main emphasis circuit of the Y signal emphasis circuit is connected. It is also the output pin of the Y signal emphasis circuit.
30	MAIN TC IN		–	–	The time constant for the main emphasis circuit is connected. It is also the input pin of the main emphasis amplifier.

Note) PR indicates Protective Resistance (about 140Ω).

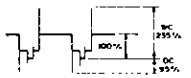
Electrical Characteristics

(Ta = 25°C, Vcc = 5.0 V)

Test No.	Test item	Symbol	SW Conditions K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	Bias conditions Adjust	Signal source	Test point	Output waveform and testing method	Min.	Typ.	Max.	Unit
1	Quiescent Current	$I_{CC(REC)}$	OFF	b	b	OFF	b	OFF	a	a	b	OFF	OFF	a	a	a	c	c	d	a	b			AM-1	DC current test	13	19	25	mA
2	Y output DC	V_{Y-DC}																b						F	Pin 24 DC test	1.80	2.00	2.20	V
3	Empha. OUT-MOD IN DC off-set (1)	V_{17}																c						D	Pin 17 DC test	1.95	2.10	2.25	V
4	Empha. OUT-MOD IN DC off-set (2)	V_{17-16}																						H	Pin 17 DC-pin 16 DC	−40	0	40	mV
5	SYNC Input level (Low)	SYNC(L)													b	b		b						F	Pin 24 DC test	1.75	2.0	2.25	V
6	SYNC Input level (High)	SYNC(H)													c									F		2.95	3.2	3.45	V
7	REG 4.2 V DC test	V_{REG}													a	a		c						G	Pin 28 DC test	4.05	4.20	4.40	V
8	FM MOD carrier set	A_{fo}																	b			V_{16} (2.0V to 2.8V)		C	At V16, adjust pin 14 output to 4.2 MHz.	4.15	4.2	4.25	MHz
9	FM MOD output level	V_{MOD}																						C	Pin 14 output level	440	500	560	mVp-p
10	REC MUTE level (High)	$V_{MUTE(Y)}$			a														d					C	Pin 14 output level. 20 log (T10/T9)			−38	dB
11	FM MOD Second harmonicdistortion	D2(MOD)			b														b					C	Pin 14 Second harmonic distortion (8.4 MHz) 20 log (TH/T9)		−40	−37	dB
12	FM MOD deviation	DEV(MOD)																	a					C	Pin 14 frequency variation when pin 25 DC is varied.	1.05	1.20	1.50	MHz
13	FM MOD Linearity	L(MOD)								b									b			V_{15} (3.0V to 4.5V)		C AM-2	Pin 14 frequency is set at V15. See details in Note 1.	0.90	1.00	1.10	MHz
14	HHS	F_{HHS}							b	a													SG3	C	MOD output frequency variation when a 30 Hz pulse is applied to MOD input.	6.5	7.8	9.1	kHz
15	CWC characteristics (1)	CWC(1)							a						d	d		b	d				SG5 SG6	F	Level difference between output and Input when 1 Vp-p (100% white) is input.	−110		0	mV
16	CWC characteristics (2)	CWC(2)																						F	Output level when 1.3 Vp-p (130% white) is input.	0.95	1.10	1.25	Vp-p
17	CWC level adjustment (1)	CWC(A1)															a							F	Output level when pin 23 DC is varied with 1.3 Vp-p (130% white) input.	0.70	0.85	1.05	Vp-p

Note 1) Assume current (AM-2) at 4.2 MHz to be I1 and current at 5.4 MHz to be I2. Assume frequency to be f with current I2 + (I2 - I1), to calculate

$$\frac{f - 5.4\ MHz}{1.2}$$ (V15 in the range of 3.0 to 4.5V)

Test No.	Test item	Symbol	SW Conditions K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	Bias conditions Adjust	Signal source	Test point	Output waveform and testing method	Min.	Typ.	Max.	Unit
18	CWC level adjustment (2)	CWC(A2)	OFF	b	b	OFF	b	OFF	a	a	b	OFF	OFF	a	d	d	b	b	d	a	b		SG5 SG6	F	Output level when pin 23 is varied with 1.3 Vp-p (130% white)	1.10	1.25	1.40	Vp-p
19	White clip adjustment	A_{WC}										ON	ON				c	a				V_6 (2.4V to 2.9V)		D	Input level: 1 Vp-p (100% white) 	220	235	250	%
20	Dark clip adjustment	A_{DC}																				V_7 (1.7V to 2.1V)		D		80	95	110	%
21	Y frequency characteristics	Y_{fc}										OFF	OFF		c	c		b					SG7	F	Pin 24 output level is taken as A and B respectively when f=100 kHz and 5 MHz. 20 log (B/A)	−2.5	0		dB
22	Y-pre Emphasis (1)	Y-EM (1)									a	ON	ON		a	a		c	c			V_{14} (2.35V to 2.55V)	SG8	E	−3 dB (354 mVp-p), 2 MHz input Take the output as reference with −3 dB, 10 kHz input	11.8	13.8	15.8	dB
23	Y-pre Emphasis (2)	Y-EM (2)																						E	−10 dB (158 mVp-p), 2 MHz input Take the output as reference with −10 dB, 10 kHz input.	15.0	17.0	19.0	dB
24	Y-pre Emphasis (3)	Y-EM (3)																						E	−20 dB (=50 mVp-p), 500 kHz input Take the output as reference with −20 dB, 10 kHz input	15.1	16.6	18.1	dB
25	Y-pre Emphasis (4)	Y-EM (4)																						E	−20 dB, 2 MHz input Take the output as reference with −20 dB, 10 kHz input	19.5	22.5	25.5	dB
26	Chroma Emphasis (1)	C-EM (1)	ON	a							b	OFF	OFF										SG1	A	0 dB (=420 mVp-p), 743 kHz input, pin 5 output 20 log (T26/420 mV)	0.0	2.0	4.0	dB
27	$\overline{\text{REC}}$ input MUTE level	$V_{MUTE(C)}$			a																			A	0 dB (=420 mVp-p), 743 kHz input pin 5 output 20 log (T27/T26)			−38	dB
28	Chroma Emphasis (2)	C-EM (2)			b																			A	With pin 1, 0 dB, f=843 kHz input; The output level of pin 5 is compared with test item (No. 26) taken as reference.	−0.1	0.3	0.7	dB
29	Chroma Emphasis (3)	C-EM (3)																						A	With pin 1, 0 dB, f=1234 kHz, input: The output level of pin 5 is compared with test item No. 26 taken as reference	−1.4	0.6	2.6	dB
30	Chroma Emphasis (4)	C-EM (4)																						A	With pin 1 −10 dB, f=743 kHz, input: The output level of pin 5 is compared with test item (No. 26) taken as reference.	−11.0	−10.0	−9.0	dB
31	Chroma Emphasis (5)	C-EM (5)																						A	With pin 1 −10 dB, f=843 kHz input: The output level of pin 5 is compared with test item (No. 30) taken as reference.	1.0	1.4	1.8	dB

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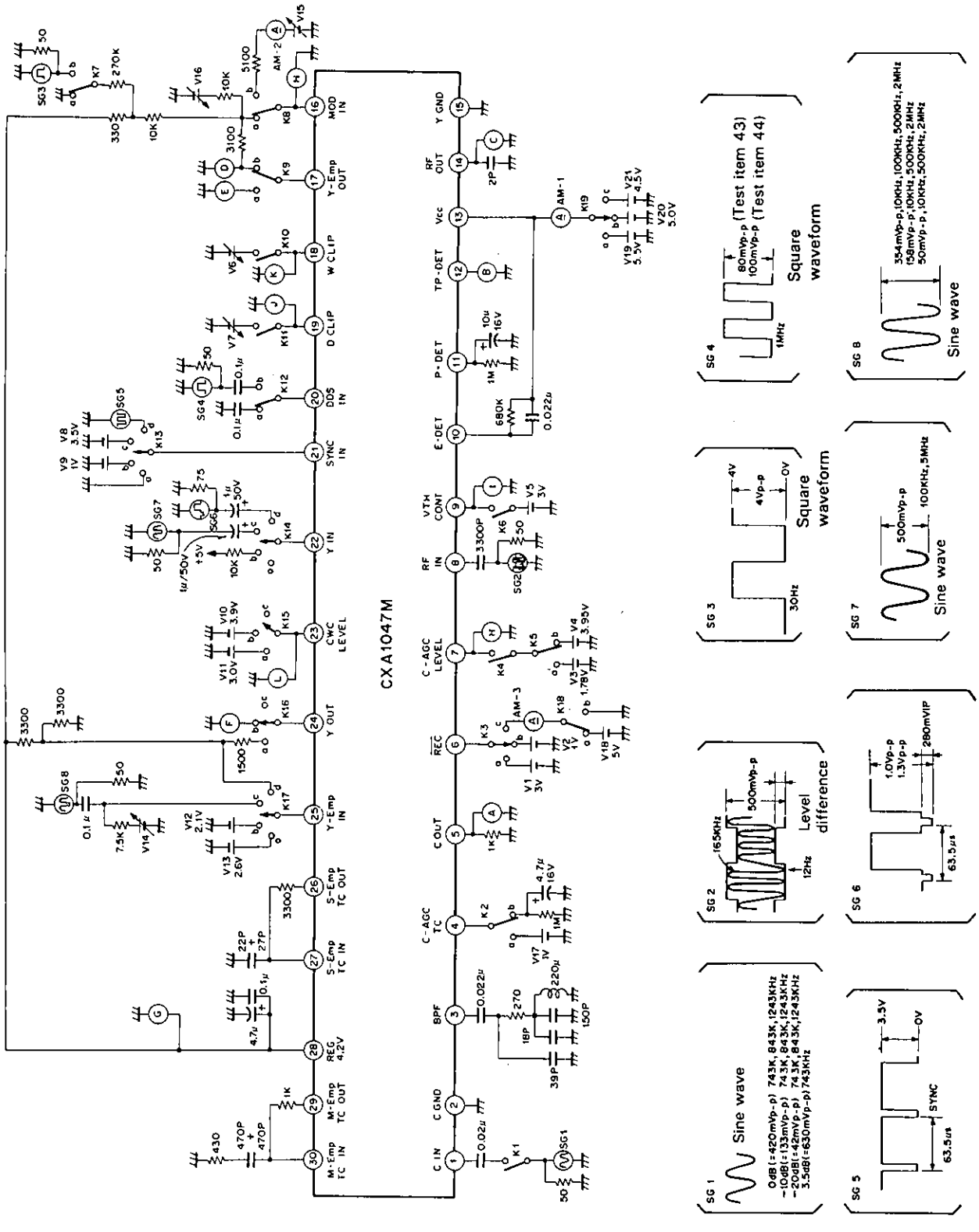
Test No.	Test item	Symbol	SW · Conditions																			Bias conditions		Test point	Output waveform and testing method	Min.	Typ.	Max.	Unit
			K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18	K19	Adjust	Signal source						
32	Chroma Emphasis (6)	C-EM (6)	ON	a	b	OFF	b	OFF	a	a	a	OFF	OFF	a	a	a	c	c	c	a	b		SG1	A	With pin 1 −10 dB, f=1243 kHz input: The output level of pin 5 is compared with test item (No. 30) taken as reference	1.4	3.4	5.4	dB
33	Chroma Emphasis (7)	C-EM (7)																						A	With pin 1 −20 dB (=42 mVp-p), f=743 kHz input: The output level of pin 5 is compared with test item (No. 26) taken as reference	−21.0	−20.0	−19.0	dB
34	Chroma Emphasis (8)	C-EM (8)																						A	With pin 1 −20 dB, f=1243 kHz input: The output level of pin 5 is compared with test item (No. 33) taken as reference	4.1	6.1	8.1	dB
35	Chroma AGC Characteristics (1)	C-AGC (1)		b																				A	The output of pin 5, when CR time constant is connected to pin 4 and 420 mVp-p f=743 kHz is input to pin 1	360	410	460	mVp-p
36	Chroma AGC Characteristics (2)	C-AGC (2)																						A	The output of pin 5, when under test conditions of test item No. 35, 630 mVp-p f=1243 kHz is input to pin 1	370	420	470	mVp-p
37	Chroma AGC level adjustment (1)	C-AGC (A1)				ON	a																	A	The output of pin 5, when under test conditions of test item No. 35	420	500	580	mVp-p
38	Chroma AGC level adjustment (2)	C-AGC (A2)					b																	A	The output of pin 5, when under test conditions of test item No. 35. 3.95 V DC is applied to pin 7.	260	310	360	mVp-p
39	DDS switching voltage	$V_{TH(DDS)}$	OFF			OFF								b				b					SG4	F	The output level of pin 24 when a square waveform of 1 MHz, 80 mVp-p is input to pin 20.	240	280	330	mVp-p
40	DDS output level	$V_{O(DDS)}$																						F	A square waveform of 1 MHz 100 mVp-p is input to pin 20. The output level of pin 24 is tested, and (pin 24 output level)—(100 mV/2) is taken as data.	200	250	300	mVp-p
41	Timing phase detector characteristics	TA-C												a				c					SG2	B	An quasi-RF signal level (difference 50 mV) is input to pin 8. The High, Low DC level of the square waveform output of pin 12 at that time.	4.5		0.5	(Low) V (High)
42	Timing phase detector level adjustment	TA-A						ON																B	The level difference of the RF signal when a square waveform appears at pin 12. 3 VDC is applied to pin 9 and a quasi-RF signal is input to pin 8.	50	80	110	mVp-p

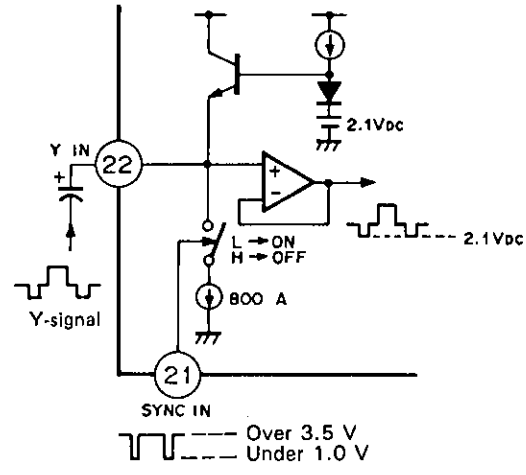
Electrical Characteristics Test Circuit



Description of Functions

1. Y clamp circuit

The Y signal sync tip level is clamped at 2.1 VDC. At that time it is necessary to input COMP sync to the sync IN of pin 21.



Y clamp circuit

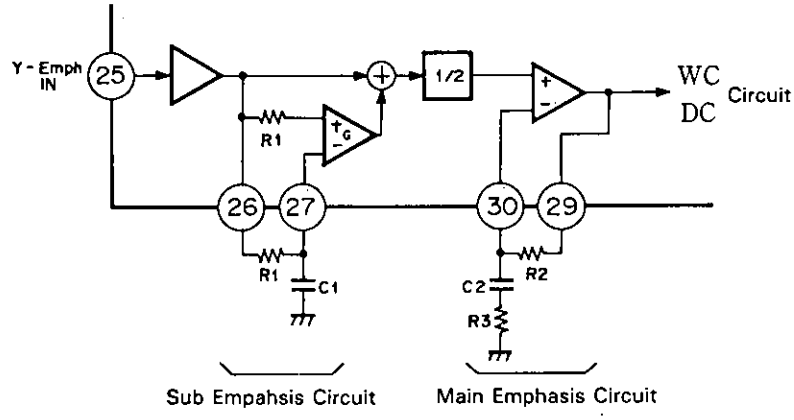
COMP sync L level: 0 V to 1.0 V
H level: 3.5 V to Vcc

2. KNEE and CWC (Camera White Clip) Circuit

When the reference level (from the Y signal sync tip level to the white peak) is set to 1.0 V (100% white), a signal of 1.3 V maximum (130%) is input. There to prevent over modulation, it is necessary to control the white peak level at the CWC circuit. Also, to preserve the high luminance tone, soft limiter characteristics are maintained at the KNEE circuit.

3. Y Emphasis circuit

Here is shown the structure of Y-Emphasis circuit for CXA1047M.

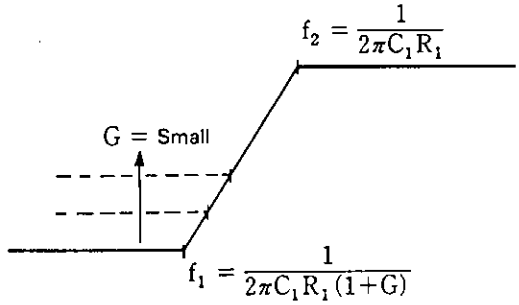


Y-Emphasis circuit

Sub Emphasis Transfer Function H(S)SUB is as follows:

$$H(S)_{SUB} = 1 + (1 - \frac{1}{1+SC_1R_1}) G = \frac{1+SC_1R_1(1+G)}{1+SC_1R_1}$$

Here, in amplifier G, by providing non linear characteristics where the gain varies according to the input level, the sub emphasis transfer function H(S)SUB achieves non linear emphasis characteristics. Sub emphasis characteristics are shown in the figure below.



Sub emphasis characteristics

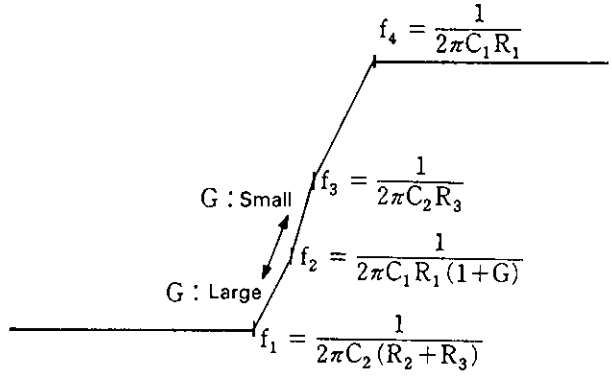
Main emphasis transfer function H(S)MAIN is as follows:

$$H(S)_{MAIN} = \frac{1+SC_2(R_2+R_3)}{1+SC_2R_3}$$

Accordingly the total Y-emphasis characteristics become:

$$H(S)_{EMP} = \frac{\{1+SC_1R_1(1+G)\}\{1+SC_2(R_2+R_3)\}}{(1+SC_1R_1)(1+SC_2R_3)}$$

The frequency response of Y-emphasis is shown in the figure below.



Y-Emphasis characteristics

When $C_2(R_2+R_3) > C_1R_1(1+G) > C_2R_3 > C_1R_1$

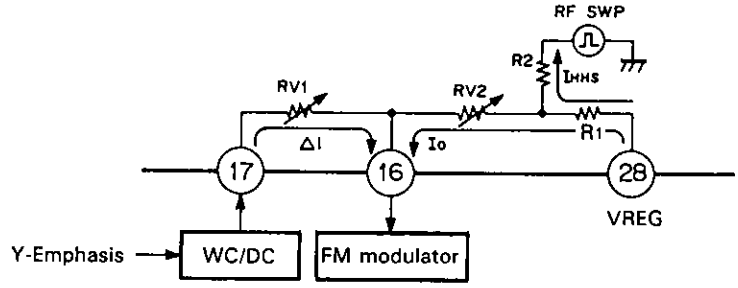
The Y-emphasis circuit reference input level is set to 500 mVp-p and at that time the output level is 250 mVp-p.

4. White Clip Circuit (WC) and Dark Clip Circuit (DC)

The output signal of the Y-emphasis circuit features a spike wave at the signal's rising or falling edge.
There may generate over modulation.
In the WC and DC circuits, a diode limiter is used to determine the DC clip level of the Y-emphasis output signal. Also by applying an external DC, the clip level can be varied.

5. FM Modulator

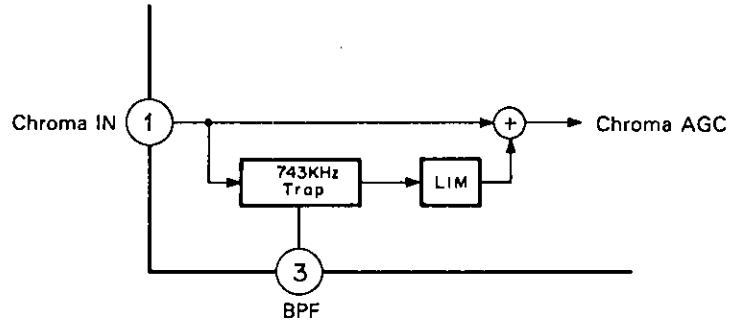
The CXA1047M FM modulator consists of a current controlled oscillator.
The modulator input (pin 16) is imaginary-shorted to VREG/2 (≒2.1 V) under a low input impedance.
The bias current for carrier (fo), the modulation signal current and HHS (1/2 fh shift) current are added to input.



FM modulator

At the figure, (FM modulator) the carrier bias current Io can be adjusted through RV_2,. Also, the level (deviation) of signal current Δi can be set with RV_1. The HHS current (I_{HHS}) is determined through R_1 R_2, and RF SWP level.
The FM modulator control sensitivity of CXA1047M amounts to about 15 kHz/μA.

6. Chroma Emphasis



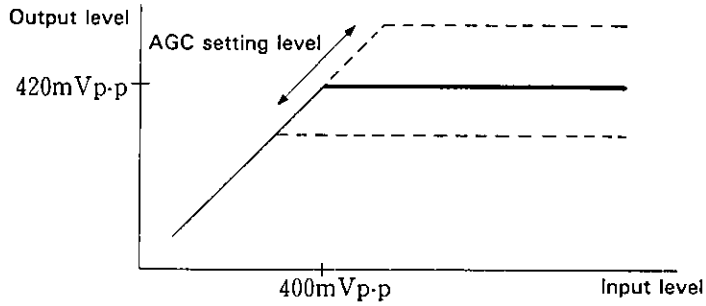
Chroma Emphasis

The down converted chroma signal is applied to the chroma Emphasis input, and the amount of emphasis diminishes around f_{SC} (color sub carrier frequency: 743.444 kHz) as it is distanced from f_{SC}, the amount of emphasis grows.

The above figure shows the structure of the chroma emphasis. By using the 743 kHz Trap, the amount of emphasis around f_{SC} is controlled, and LIM (limiter) realizes the non linear characteristics.

7. Chroma AGC

Chroma AGC Input/Output characteristics are shown in the Figure below.



Chroma AGC Characteristics

By applying DC to pin 7, AGC setting level can be varied.

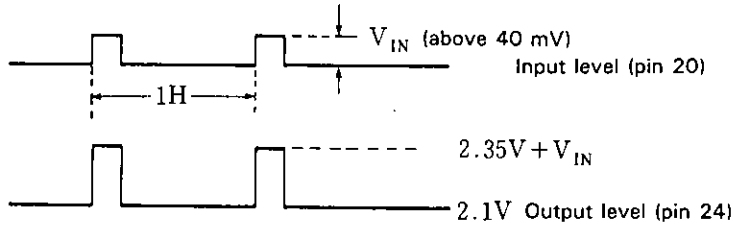
For the AGC setting level, assuming DC of pin 7 is V7, the following relation is obtained.

AGC setting level (output, p-p) $\fallingdotseq V7\frac{30}{170}$

8. DDS (Date Display System) Circuit

The DDS circuit serves to input the date and other information.

When DDS signal is input, Y signal and DDS signal are switched and DDS signal is output at Y OUT. The Y/DDS signal switching is executed at the DDS signal itself, and a signal level above 40 mVp-p is necessary. The relation between the DDS input level and output level is shown in the figure below.

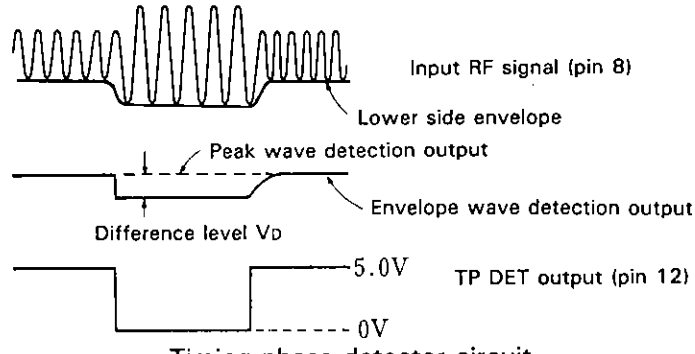


DDS I/O level

9. Timing Phase Detector Circuit

The timing phase detector circuit executes envelope wave detection and peak wave detection for

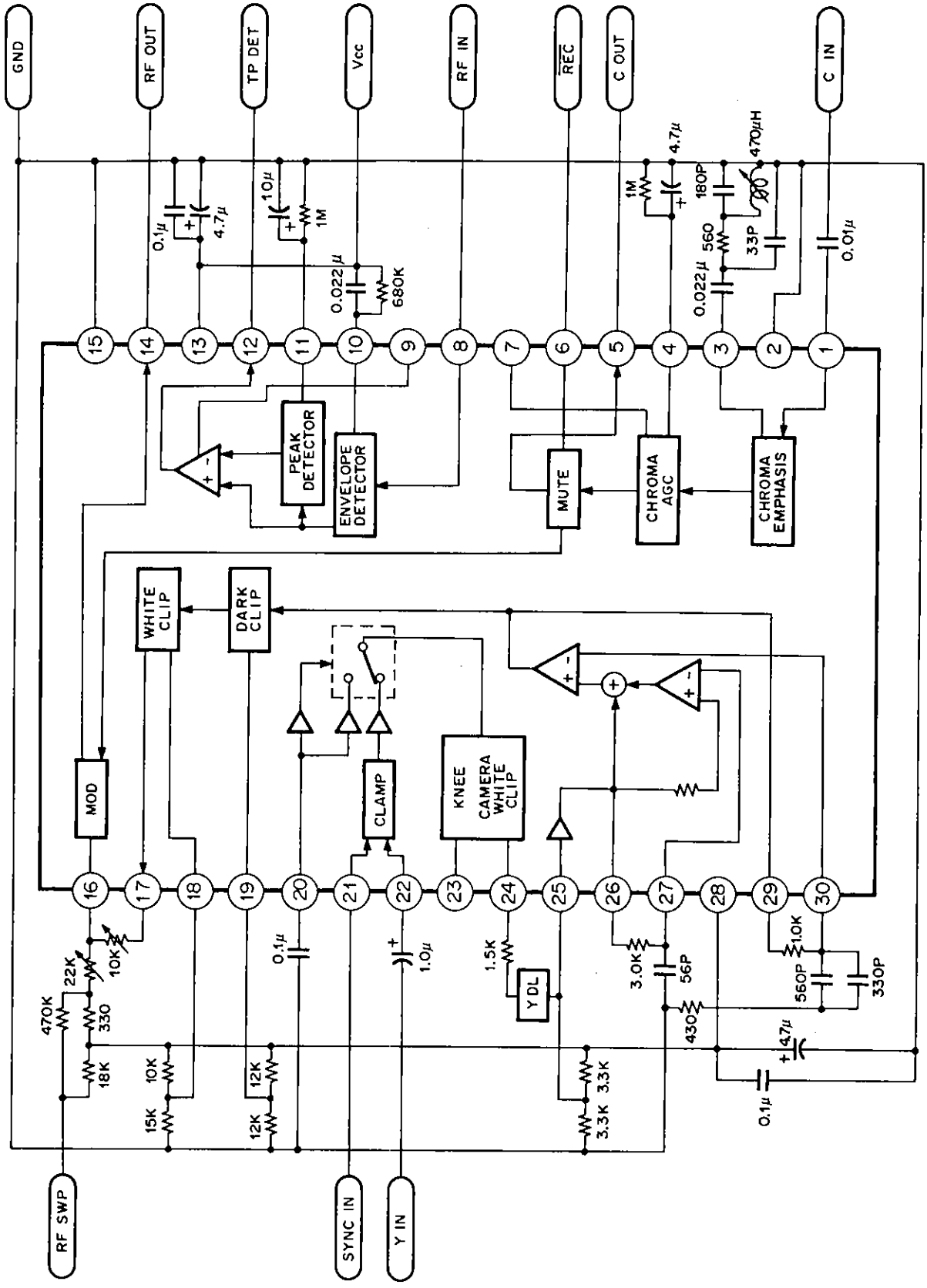
1) Timing phase detection for the track adjustment using slow playback.
2) Phase adjustment of ATF PILOT signal.



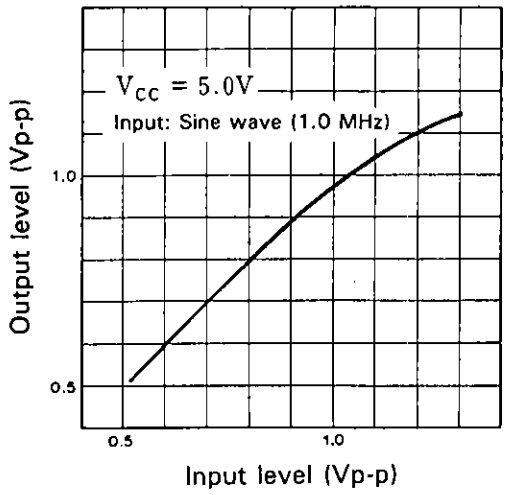
Timing phase detector circuit

The envelope wave detection circuit detects the lower side envelope of input RF signal. The peak detection circuit detects the level difference VD of the envelope wave detection output. By applying DC to pin 9 the difference detection level (VTH) can be varied. However when pin 9 is open (it is internally biased to 1.3 V), VTH becomes 50 mV, and with a signal where the difference exceeds 50 mV, TP DET output is obtained.

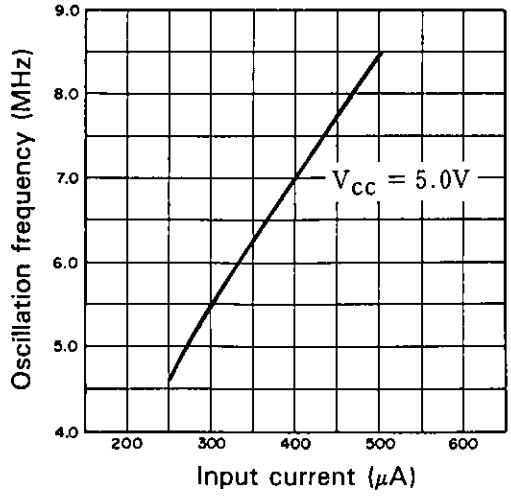
Application Circuit



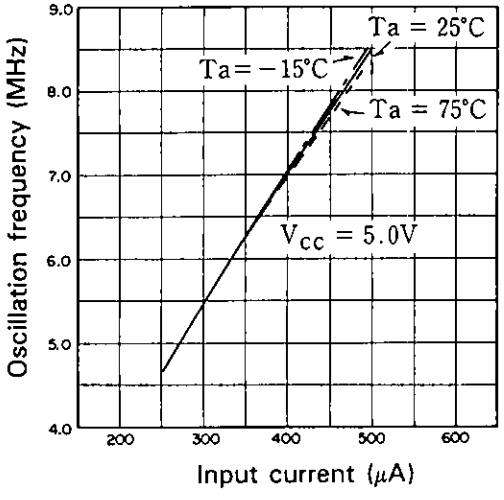
KNEE and CWC characteristics



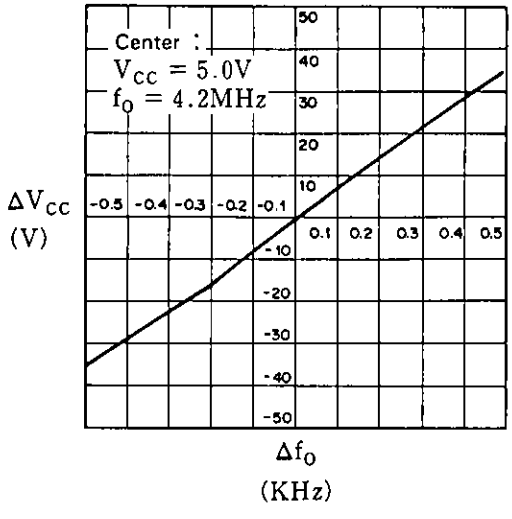
FM MOD Oscillation frequency characteristics



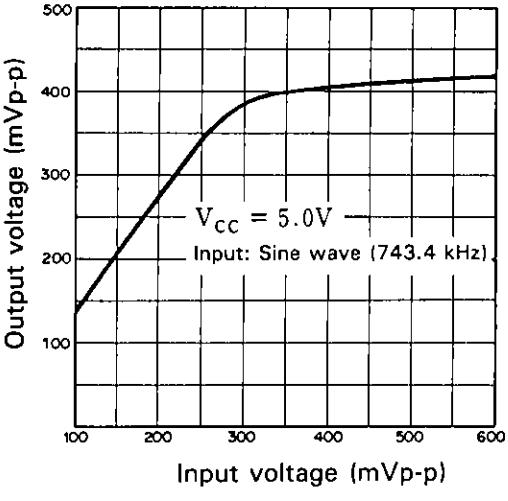
FM MOD Oscillation frequency temperature characteristics



FM MOD Oscillation frequency supply voltage characteristics



Chroma AGC I/O characteristics (Including chroma emphasis)



Y-Emphasis characteristics