SONY

CXA1585Q

RGB Decoder

For the availability of this product, please contact the sales office.

Description

The CXA1585Q is an IC which converts Y/C separation signals into RGB signals, and can be used with both NTSC and PAL systems.

Features

- Filter for sharpness
- APL circuit
- Low carrier leak
  (3.58MHz component, 5mVp-p or less Typ.)
- Compatible with both NTSC and PAL systems
- Low power consumption (120mV, Vcc=5V)

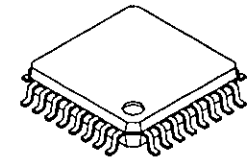
Applications

General-purpose RGB decoders, color liquid crystal viewfinders, liquid crystal TVs, etc.

Structure

Bipolar silicon monolithic IC

32 pin QFP (Plastic)



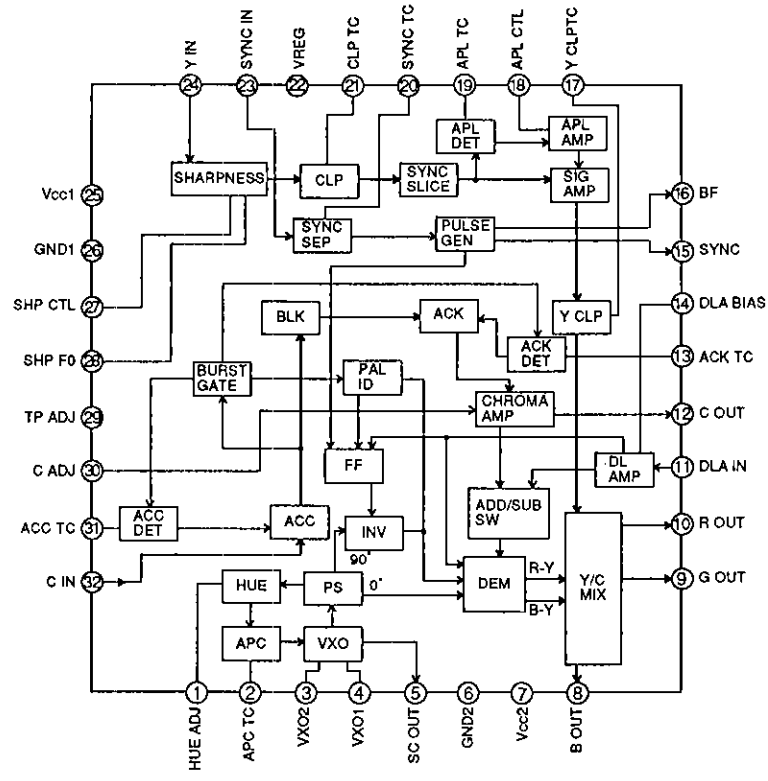
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	PD	500	mW

Recommended Operating Conditions

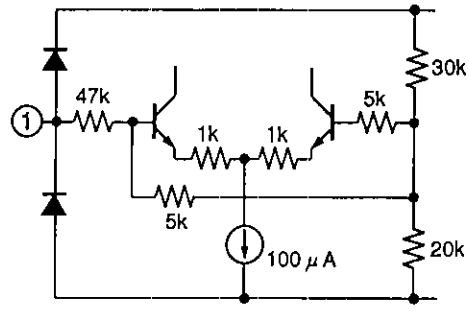
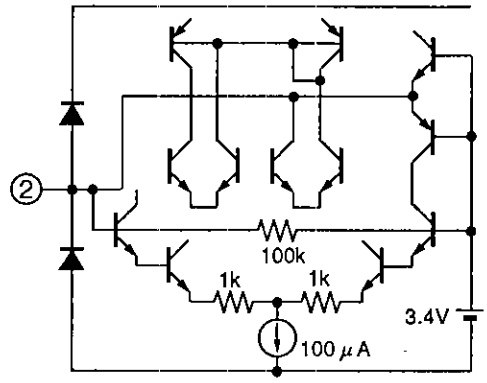
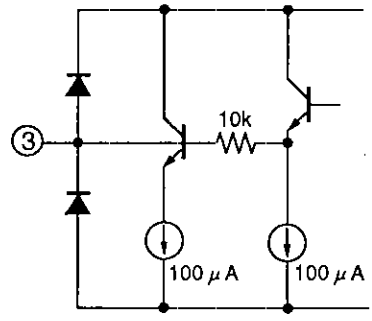
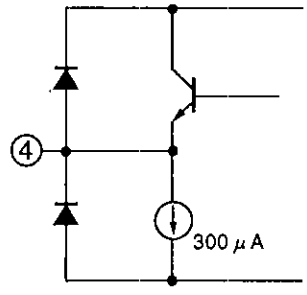
• Supply voltage	4.6 to 5.25 (Typ. 5V)	V

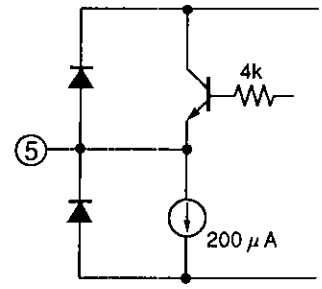
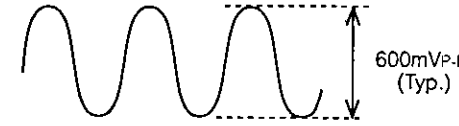
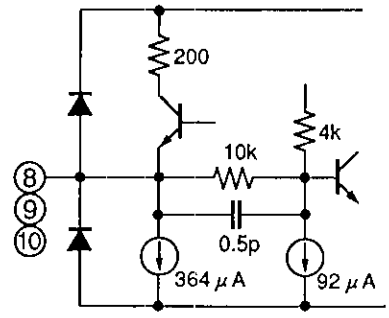
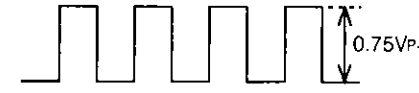
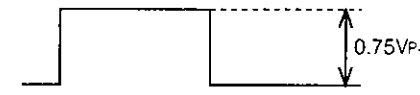
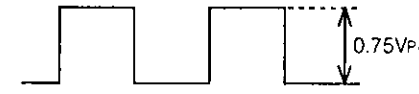
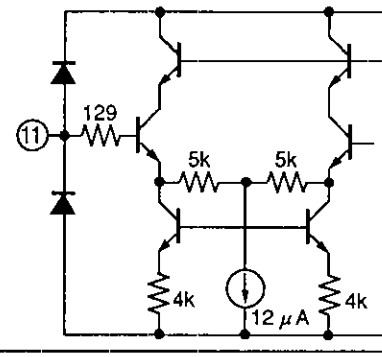
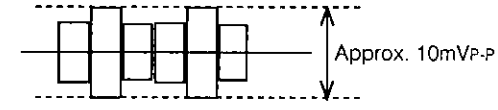
Block Diagram

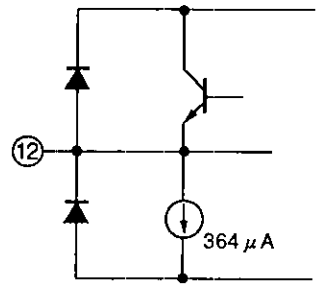
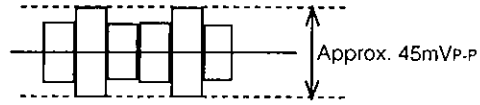
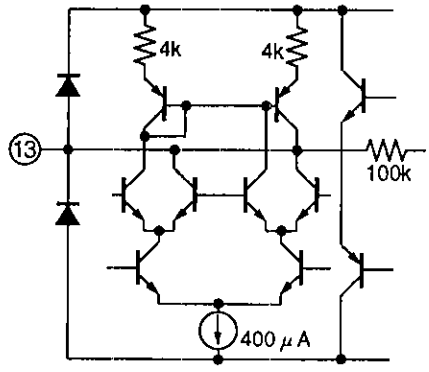
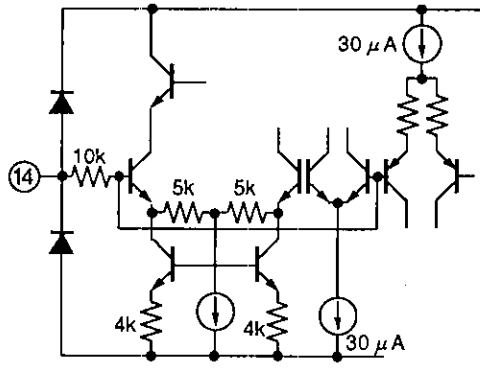
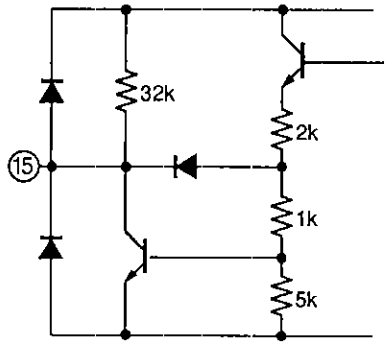
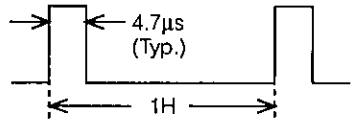


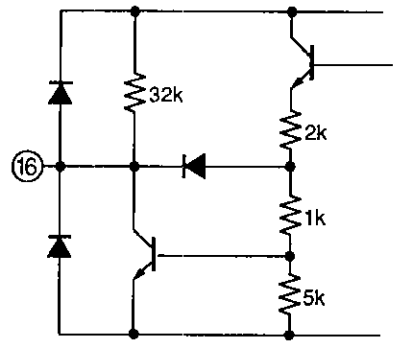
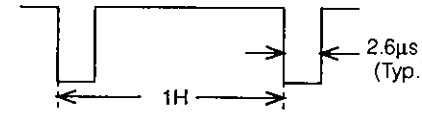
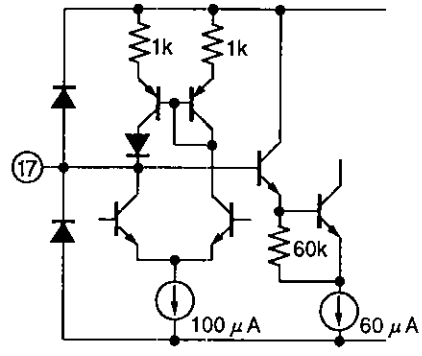
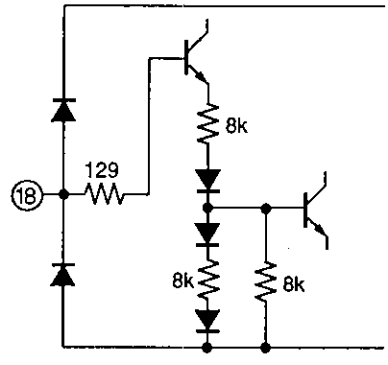
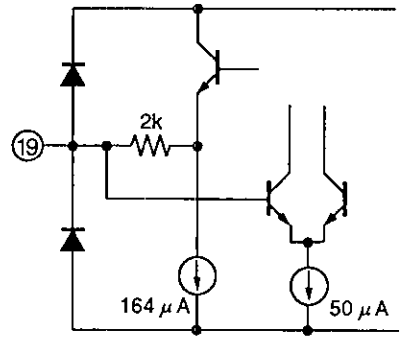
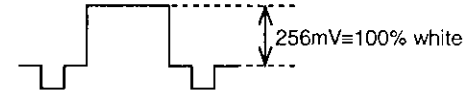
E92515B46-TE

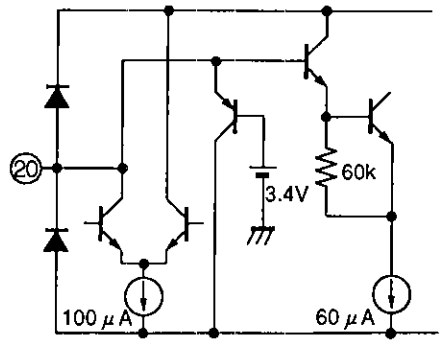
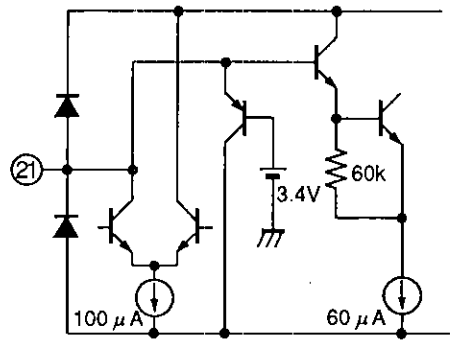
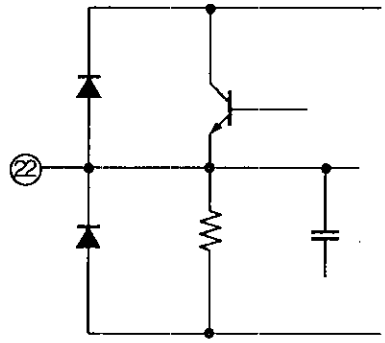
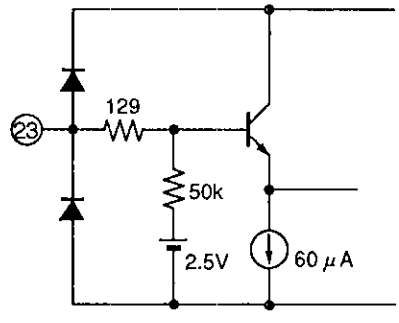
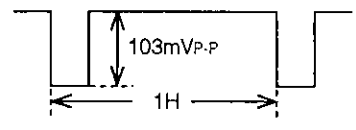
Pin Description

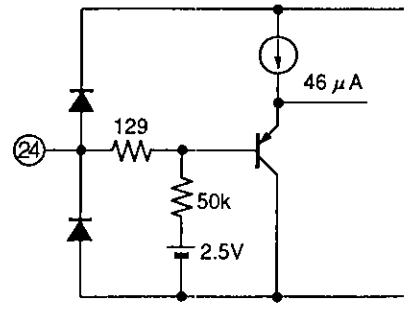
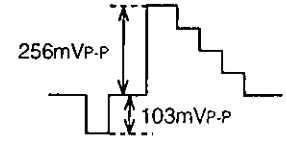
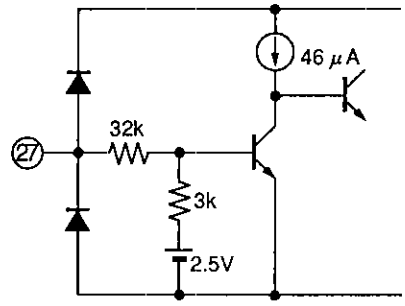
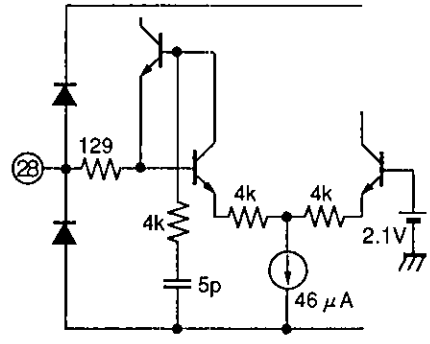
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	HUE ADJ	2.0V		Hue adjustment. The hue can be adjusted by ±10° or more by applying a voltage ranging from 0.5 to 3.5 V to this pin.
2	APC TC	3.4V		APC (color sync) time constant and free-running frequency adjustment. The VXO free-running frequency can be adjusted by varying the DC voltage applied to this pin for no signal.
3	VXO2	3.1V		Crystal oscillator
4	VXO1	3.2V		Crystal oscillator

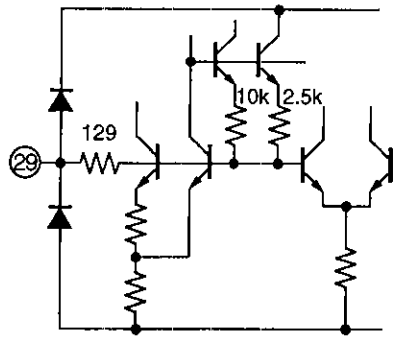
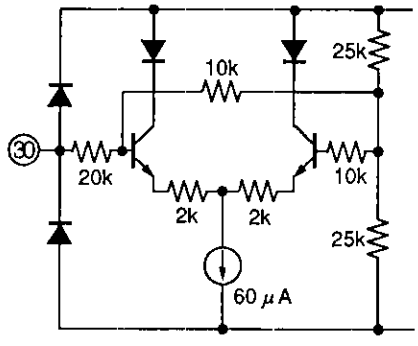
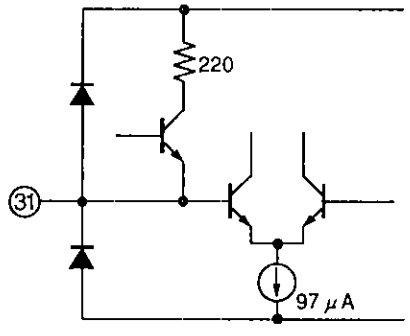
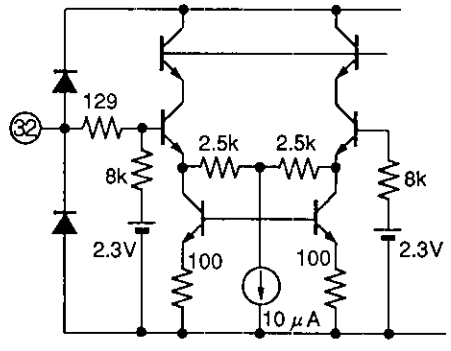
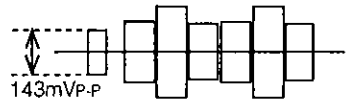
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	SC OUT	1.6V		Subcarrier output 
6	GND2	0V		GND for chroma
7	Vcc2	5V		Vcc for chroma
8	B OUT	2.0V		B output * With 75% color bar reference level input 
9	G OUT			G output 
10	R OUT			R output 
11	DLA IN	0V (NTSC) 2.3V (PAL)		Delay line amplifier input. Connects to GND for NTSC mode; connects the 1H delay line output for PAL mode. 

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	C OUT	3.15V		Chroma output for PAL. Connects to Vcc for NTSC mode; connects to the 1H delay line input for PAL mode. 
13	ACK TC	3.1V		ACK (automatic color killer) time constant
14	DLA BIAS	0V (NTSC) 2.3V (PAL)		NTSC/PAL mode switching and delay line amplifier gain control NTSC mode: $V_{14} \leq 0.8V$ PAL mode: $2.0V \leq V_{14} \leq 2.6V$ Variable range: ±2dB or more
15	SYNC	H 4V or more L 0.5V or less		Composite sync output. This polarity is positive. (Typ.) 

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	BF	H 4V or more L 0.5V or less		Burst flag output. This polarity is negative. (Typ.) 
17	Y CLP TC	3.1V		Pedestal clamp time constant
18	APL CTL	3.0V		APL sensitivity control. The control range is 3 to 5V. When APL control is not performed, connects this pin to GND.
19	APL TC	2.5V		Time constant for detecting APL (average picture level) of luminance signal APL 0% V_{19}=2.0V (Typ.) APL 100% V_{19}=3.2V (Typ.) 

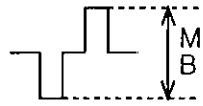
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
20	SYNC TC	3.1V		Sync tip clamp time constant for sync separation
21	CLP TC	3.1V		Pedestal clamp time constant
22	VREG	4.2V		4.2V regulator output. Decoupling capacitance is provided. It cannot be used as an external power supply.
23	SYNC IN	2.5V		Signal input pin for sync separation. Standard sync level is 103mVp-p. Normally shorted with Y IN (Pin 24) for use. 

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	Y IN	2.5V		Y signal input. Standard input level SYNC=103mVp-p 100% white=256mVp-p Do not supply the burst signal. 
25	Vcc1	5V		Vcc for Y
26	GND1	0V		GND for Y
27	SHP CTL	2.5V		Sharpness gain control Variable range: –4.5dB to +4.5dB (1.5V≤V27≤3.5V) Adjusts the sharpness level by the voltage supplied to this pin.
28	SHP Fo	2.1V		Sharpness filter frequency adjustment. Adjusts the filter fo by varying the current took out from this pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
29	TPADJ	1.23V		Sets the timing of the pulses used in the IC. Connects a 27kW resistor between this pin and GND. * Use a metal film resistor with an accuracy of ±1%.
30	C ADJ	2.5V		Chroma amplifier gain adjustment. Adjusts the gain of chroma amplifier by the voltage (1.5 to 3V) supplied to this pin. Gain variable range: –20 to +8dB
31	ACC TC	2.2V		ACC (automatic color control) time constant
32	C IN	2.3V		Chroma signal input. The standard input level is 143mVp-p of burst amplitude. 

Electrical Characteristics (Ta=25°C, Vcc=5V Refer to the Electrical Characteristics Test Circuit)

Item	Symbol	Conditions	Input signals Y IN 24pin	Input signals C IN 32pin	Test point (pin)	Min.	Typ.	Max.	Unit
Power consumption	Icc1	Sum of currents flowing to Vcc1 and Vcc2	SIG1	—	7, 25	17.0	24.0	32.0	mA
Gain for Y	Vo	F=300kHz, VA=160mVp-p, VL=160mV Measure gain between input (=VL) and output.	SIG2	—	8	10.0	11.5	13.0	dB
Cut-off frequency for Y	VFC	F=3.5MHz, VA=160mVp-p, VL=160mV Gain difference between 300kHz and 3.5MHz	SIG2	—	8	–3.0			dB
Sharpness characteristics Max.	VSHP (Max.)	F=1.5MHz, VA=50mVp-p, VL=160mV Ratio of 300kHz and 1.5MHz when SHP CTL (Pin 27) is 3.5V.	SIG2	—	8	4.5			dB
Sharpness characteristics Min.	VSHP (Min.)	F=1.5MHz, VA=160mVp-p, VL=160mV Ratio of 300kHz and 1.5MHz when SHP CTL (Pin 27) is 1.5V.	SIG2	—	8			–4.5	dB
AGC characteristics APL 100%	VAGC1	F=300kHz, VA=160mVp-p, VL=256mV Measures gain between input (=VL) and output.	SIG2	—	8	3.6	4.9	6.2	dB
AGC characteristics APL 50%	VAGC2	F=300kHz, VA=160mVp-p, VL=128mV APL CTL(18pin)=3.0V Measures gain between input (=VL) and output.	SIG2	—	8	3.9	5.5	7.0	dB
AGC characteristics APL 35%	VAGC3	F=300kHz, VA=160mVp-p, VL=90mV APL CTL(18pin)=3.0V Measures gain between input (=VL) and output.	SIG2	—	8	6.3	8.0	9.7	dB
AGC OUT APL 100%	VAGC4	VL=256mV Measures DC voltage at APL TC (Pin 19).	SIG3	—	19	3.0	3.2	3.5	V
AGC OUT APL 0%	VAGC5	VL=0mV Measures DC voltage at APL TC (Pin 19).	SIG3	—	19	1.9	2.0	2.2	V
RGB output pedestal level	VDC	Measures pedestal voltage at Pins 8, 9 and 10.	SIG1	—	8 9 10	1.4	2.0	2.4	V

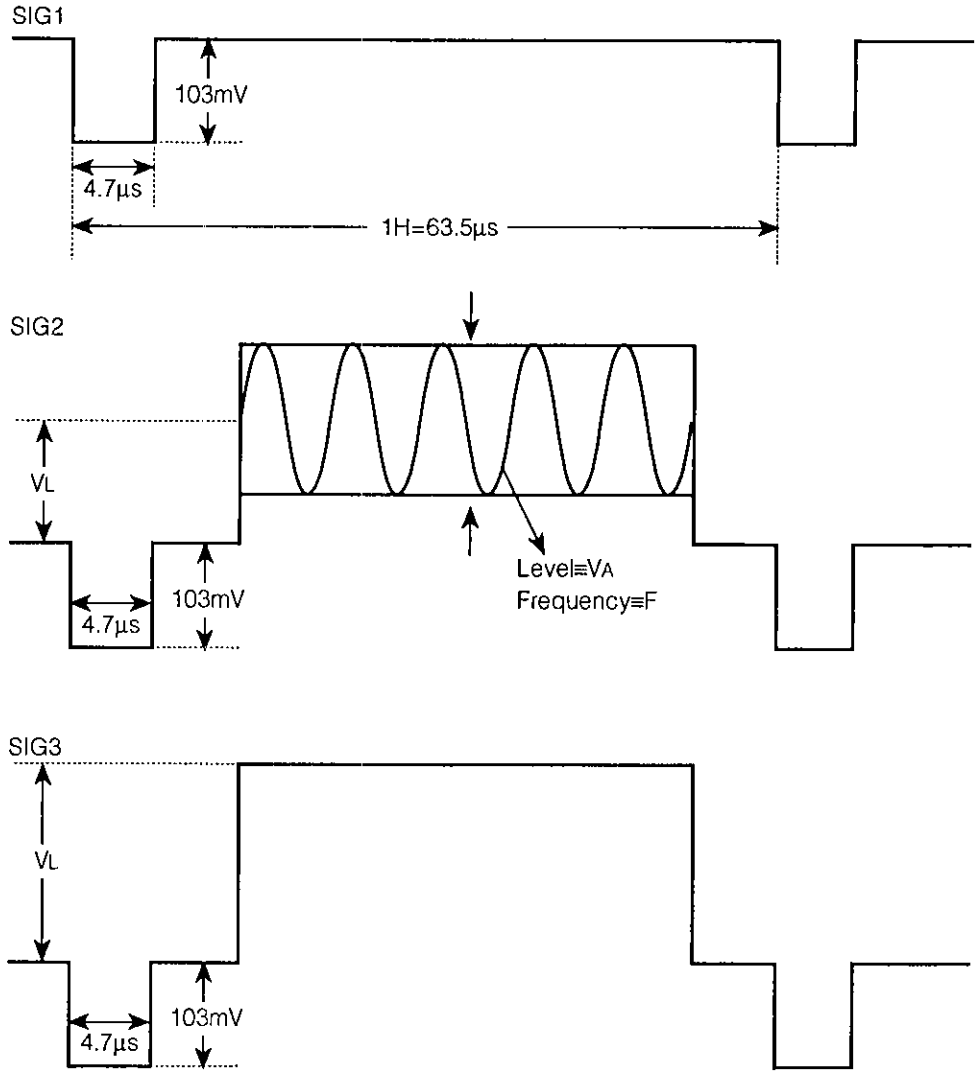
Item	Symbol	Conditions	Input signals Y IN 24pin	Input signals C IN 32pin	Test point (pin)	Min.	Typ.	Max.	Unit
APC pull-in upper range	Fpu	Inputs fsc+250Hz sine wave and confirms that it is locked with SC OUT (Pin 5).	SIG1	SIG5 /SIG8	5	250			Hz
APC pull-in lower range	Fpd	Inputs fsc–250Hz sine wave and confirms that it is locked with SC OUT (Pin 5).	SIG1	SIG5 /SIG8	5			–250	Hz
ACC cover upper range	Acc1	$Acc1=\frac{\text{C OUT (6dB : VA=286mVp-p)}}{\text{C OUT (0dB : VA=143mVp-p)}}$	SIG1	SIG4 /SIG7	12		0.5	3.0	dB
ACC cover lower range	Acc2	$Acc2=\frac{\text{C OUT (–14dB : VA=28.6mVp-p)}}{\text{C OUT (0dB : VA=143mVp-p)}}$	SIG1	SIG4 /SIG7	12	–3.0	–1.5		dB
Output D range	VDL	C ADJ (30pin)=3.0V 	SIG1	SIG6 /SIG9	8	1.0			V
Carrier leak	CL	Input signal: SYNC only Measures 3.58MHz component of output.	SIG1	—	8		5	20	mV
NTSC ACK operation	ACK	With VA=143mVp-p as 0dB, measures input level (VA) when C OUT chroma signal is no longer output, and calculates the ratio of this to when the level is 143mVp-p.	SIG1	SIG4 /SIG7	12	–50		–30	dB
C.SYNC High level	VOH		SIG1	—	15	4.0			V
C.SYNC Low level	VOL		SIG1	—	15			0.5	V
Burst flag High level	VOH		SIG1	—	16	4.0			V
Burst flag Low level	VOH		SIG1	—	16			0.5	V
Subcarrier output voltage	VO(SC)	Amplitude when frequency at Pin 5 is adjusted to 3.579545MHz ±20Hz.	SIG1	—	5	500	600		mV

Vcc1=5V, Vcc2=5V, Ta=25°C

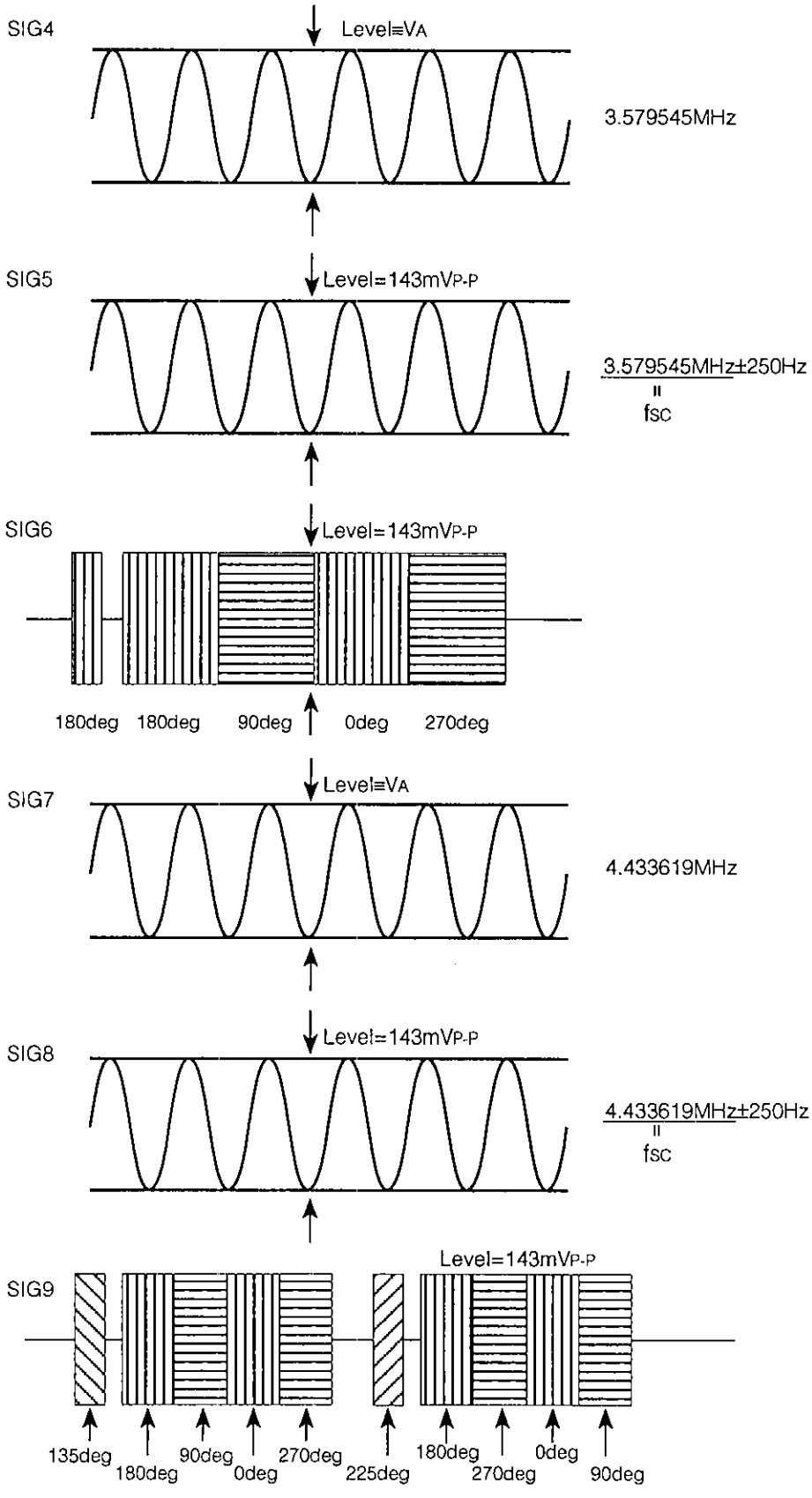
* Default conditions for pin settings SHP F0=39kΩ, SHP CTL=2.5V, APL CTL=0V

Input signals (electrical characteristic input signals)

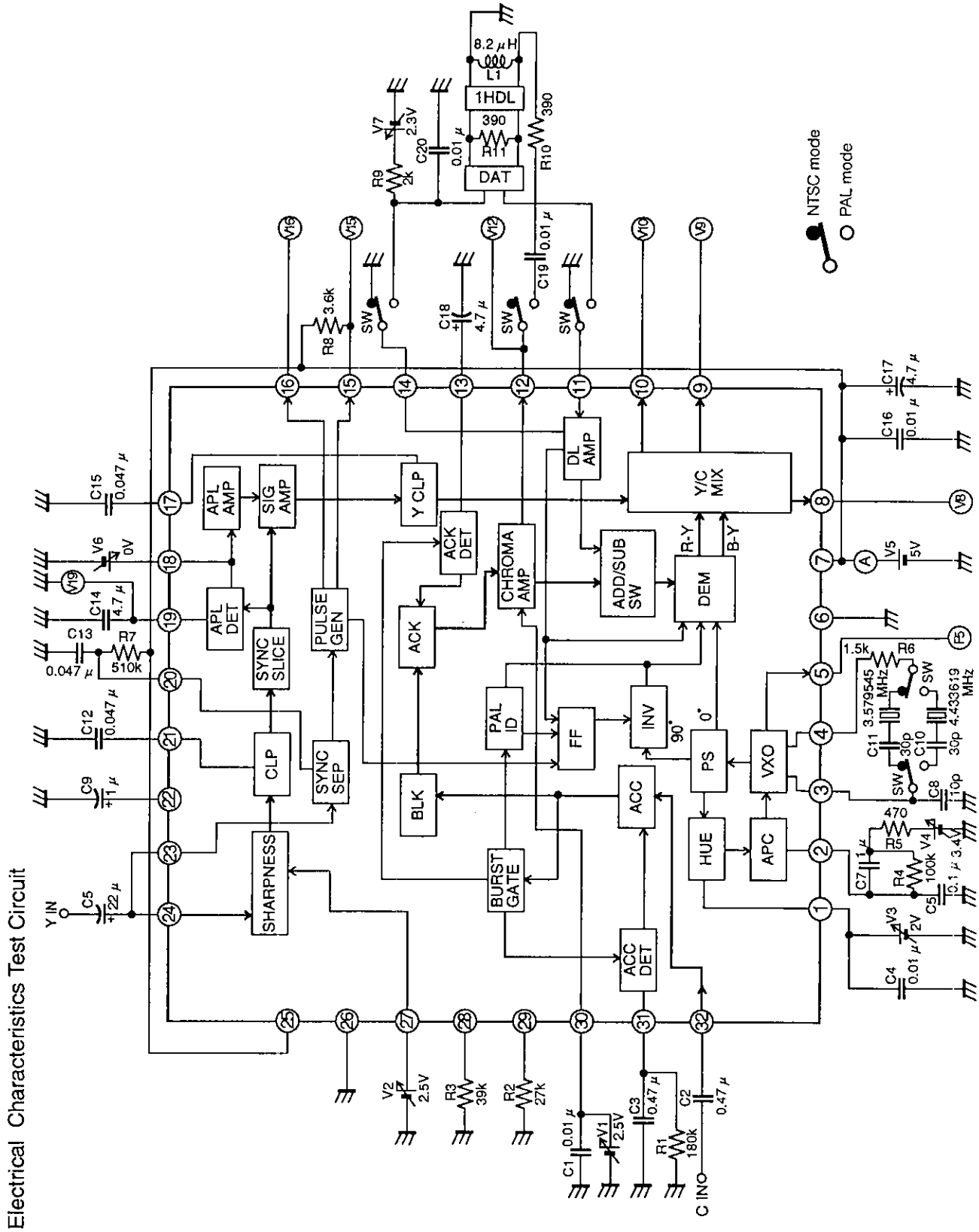
Y input



C input


SIG4
Level≒VA
3.579545MHz
SIG5
Level=143mVP-P
3.579545MHz±250Hz
=
fsc
SIG6
Level=143mVP-P
180deg 180deg 90deg 0deg 270deg
SIG7
Level≒VA
4.433619MHz
SIG8
Level=143mVP-P
4.433619MHz±250Hz
=
fsc
Level=143mVP-P
SIG9
135deg 180deg 90deg 0deg 270deg 225deg 180deg 270deg 0deg 90deg

Electrical Characteristics Test Circuit



Description of Operation

(1) Luminance signal regeneration system

<1> Sharpness filter

The video (luminance and sync) signals input from Pin 24 (VIDEO IN) are boosted near 1.5MHz by the sharpness filter. The 1.5MHz component can be varied from –4.5 to +4.5dB (as compared to the 300kHz) according to the voltage of Pin 27 (SHP CTL). Approximately 0dB (as compared to the 300kHz) when Pin 27 (SHP CTL) is 2.5 V.

Keep Pin 27 open when sharpness is not operated. Since the DC bias in the IC is 2.5V, the frequency response characteristics are almost the same as the characteristics applied 2.5V to Pin 27 externally.

<2> APL circuit

The Y AMP gain is controlled by the APL (average picture level) function, and the gain is reduced as the APL increases.

The APL circuit is operated when the voltage at Pin 18 (APL CTL) is between 3.0V and 5.0V. It is OFF when APL CTL is 0V.

(2) Chrominance signal regeneration system

<1> ACC circuit

The chroma signal input from Pin 32 (C IN) is controlled so that the burst signal is detected by ACC DET, feedback is applied to ACC AMP in accordance with the detective output, and the burst level is controlled to be constant.

The chroma signal level (Pin 12) is approximately 45mVp-p for ACC operations.

<2> APC circuit

Only the burst signal among the signals whose level has been made constant by ACC AMP enters the APC circuit at the burst gate circuit. 0°, 90° and 180° signals are generated in the phase circuit for the VXO output, and their composite waves (90° carrier) enter the APC circuit passing through the hue circuit.

Here their phase is compared with that of the burst signal and feedback is applied to VXO to obtain a phase difference of 90°. The 0° and 90° carriers created in this way are supplied to B-Y, R-Y and DEM. This means that the demodulation axis can be changed by rotating the phase of the composite waves by the DC voltage at Pin 1 (HUE ADJ).

<3> DEM circuit (NTSC)

The chroma signal whose level has been made constant by ACC AMP is amplified by CHROMA AMP, demodulated by B-Y DEM and R-Y DEM, applied to the Y/C MIX circuit with G-Y created by the resistance matrix, mixed with the luminance signal and then output as the R, G and B primary colors.

<4> DEM circuit (PAL)

The processing is the same as for NTSC until CHROMA AMP. The chroma signal output to Pin 12 (C OUT) enters DL AMP from Pin 11 (DLA IN) via 1HDL (1H delay line), its level is controlled, and the signal is applied to the ADD/SUB circuit. The original signal is added or subtracted in this circuit: the addition signal is applied to B-Y DEM and the subtraction signal to R-Y DEM, and they are demodulated by the 90° carrier whose phase is inverted every 1H and the 0° carrier.

The signals are then mixed with the luminance signal and output as the R, G and B primary colors.

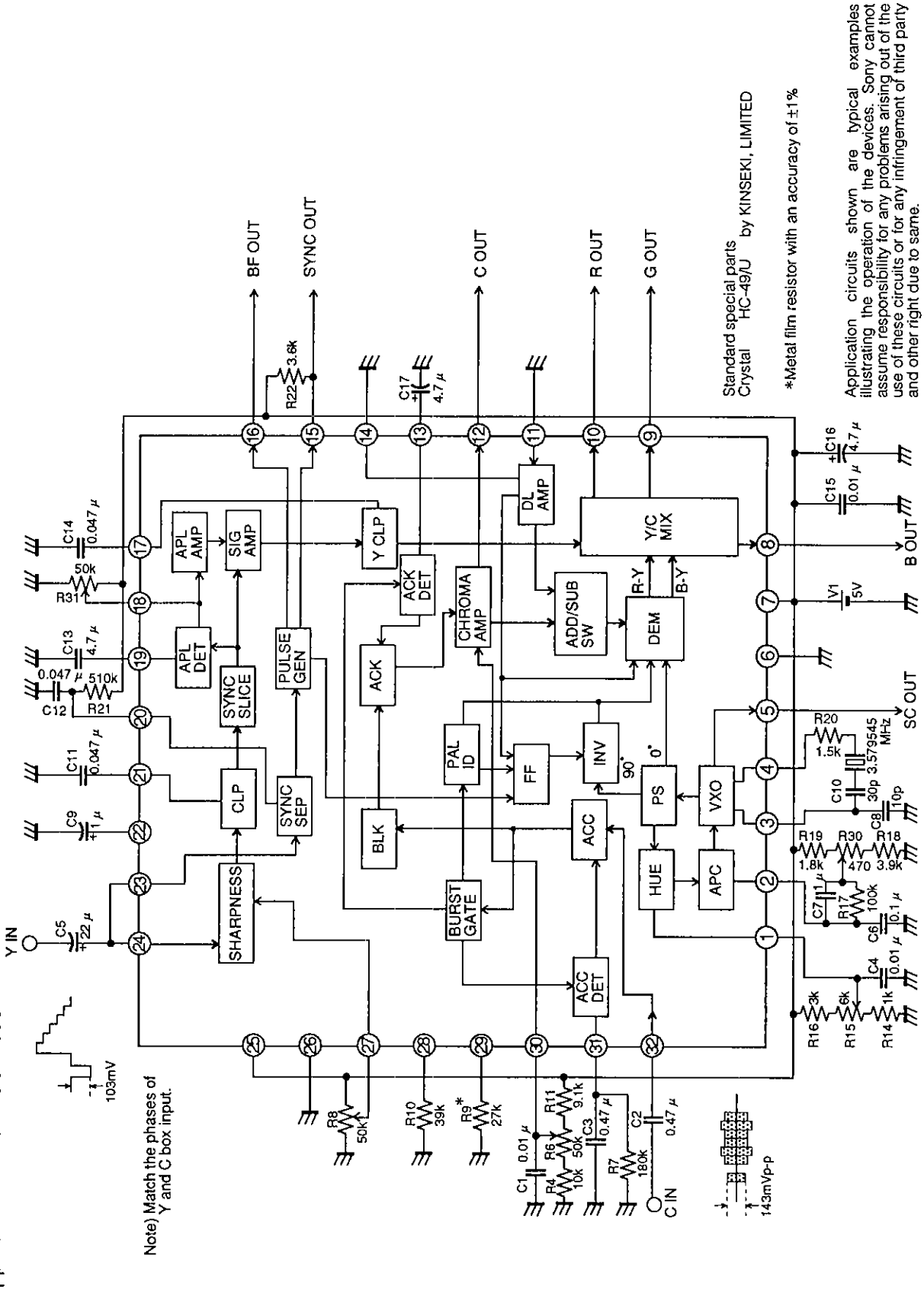
<5> PAL ID

In PAL mode, the phase of the 90° carrier is inverted in synchronization with H.SYNC.
Sync detection is conducted to establish whether this matches the input burst. When there is an error, it is corrected by applying feedback to FF (flip-flop).

(3) Sync separation system

The sync tip of the video signals input from Pin 23 (SYNC IN) is clamped and the sync signals are separated. On the basis of the SYNC pulse created here, BF (burst flag), BLK pulse and other timing pulses are generated and supplied to the circuits. The SYNC and BF (burst flag) pulses are output to Pins 15 and 16 via a buffer.

Application Circuit NTSC mode



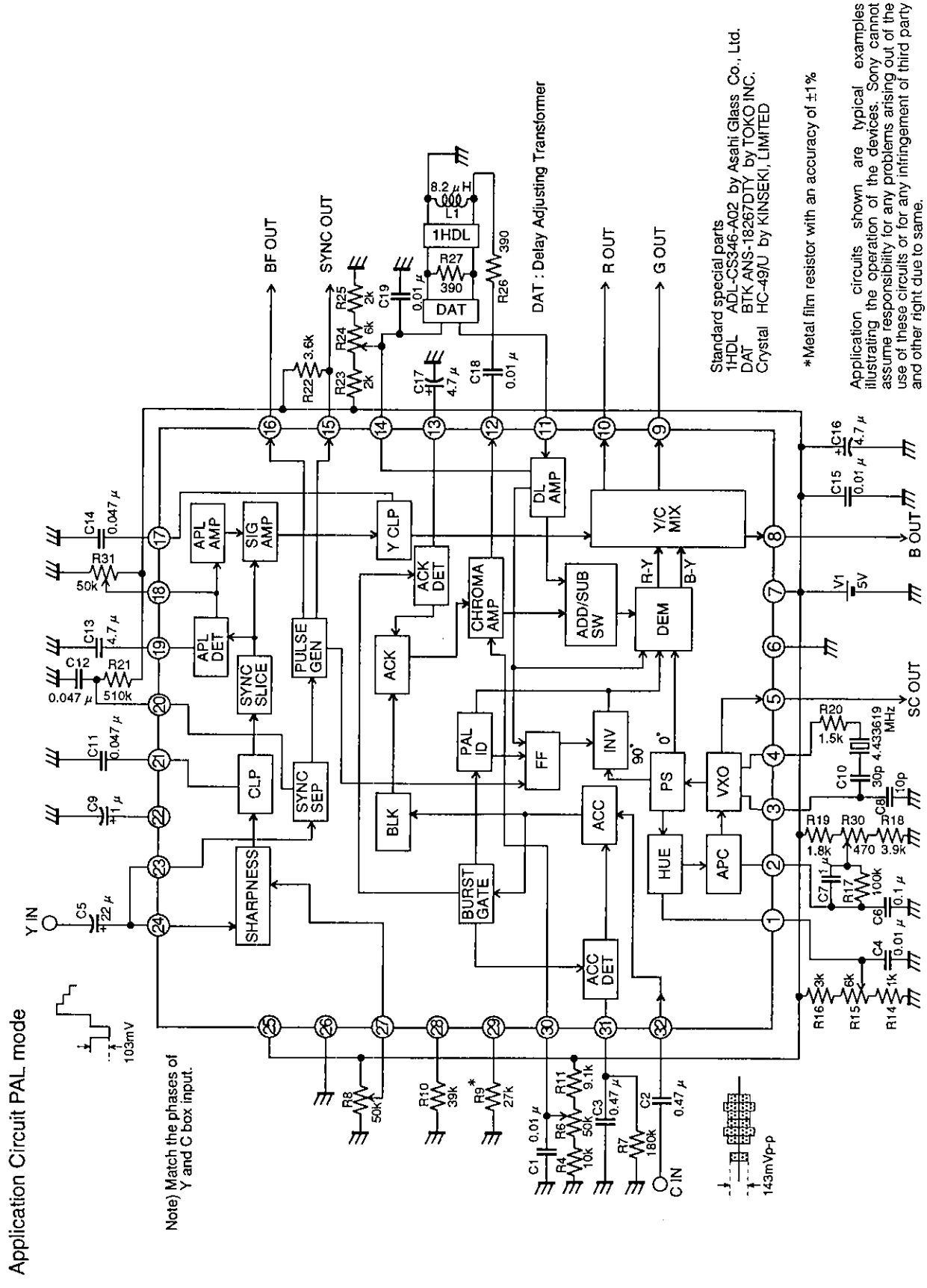
Note) Match the phases of Y and C box input.

Standard special parts
Crystal HC-49/U by KINSEKI, LIMITED

*Metal film resistor with an accuracy of ±1%

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Application Circuit PAL mode



Adjustment Procedure

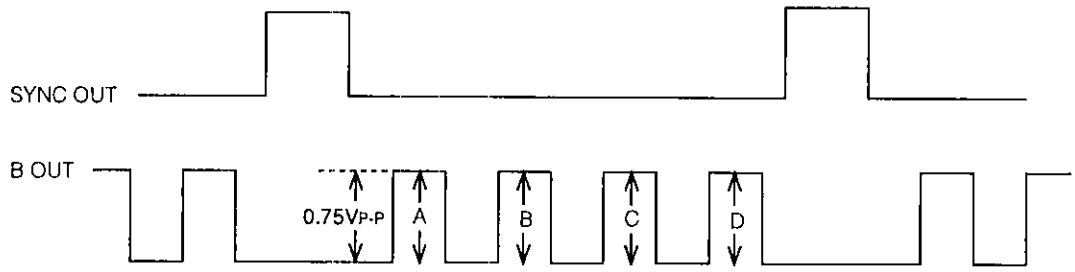
NTSC mode

Input signal: 75% color bar

1) Free-running f0 adjustment
   Adjust (R30) the DC voltage at Pin 2 (APC TC) so that the oscillation frequency (subcarrier) fsc=3.579545MHz at Pin 5 (SC OUT) is within ±20Hz under inputting sync condition.

2) Input level adjustment
   Adjust (R13) the input level so that the white peak (75% white) is set to 0.75Vp-p at the B output.
   Connect Pin 18 (APL CTL) to GND at this time.

3) HUE ADJ, C ADJ adjustment
   Adjust (R15, R6) HUE ADJ (Pin 1) and C ADJ (Pin 30) so that the colors (A, B, C and D in the figure below) of the B output amplitude are set to the same amplitude.



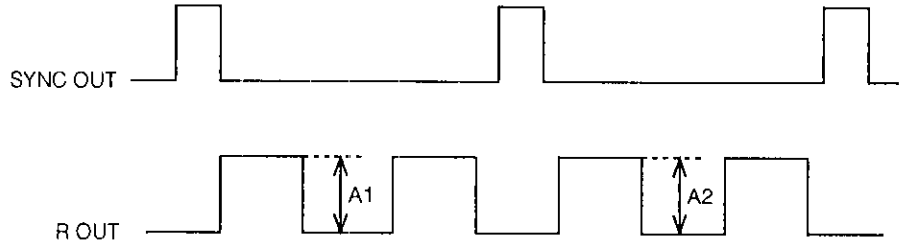
PAL mode

Input signal: 75% color bar

1) Free-running f0 adjustment
   Adjust (R30) the DC voltage at Pin 2 (APC TC) so that the oscillation frequency (subcarrier) fsc=4.433619MHz at Pin 5 (SC OUT) is within ±20Hz under inputting sync condition.

2) Input level adjustment (same as for NTSC)

3) DL AMP and DAT (delay adjusting transformer) adjustment
   Adjust (R24, DAT) Pin 14 (DLA BIAS) and DAT alternately so that the R output amplitudes (A1 and A2) are equal for the H periods before and after.



4) C ADJ adjustment
   Adjust (R6) C ADJ so that the colors of the R output amplitude are set to 0.75Vp-p.

Applications

1) The input dynamic range is 0.36Vp-p (max.). The breakdown is given as follows.

Y IN (Pin 24)	Sync signal :	0.103Vp-p
	Luminance signal :	0.256Vp-p (100% white)
C IN (Pin 32)	Burst signal:	0.143Vp-p

Note that when the input signal exceeds the value of 0.36Vp-p from sync tip to white peak, the output may be clipped and flattened.
This applies the case for the APL circuit OFF (Pin 18 APL CTL=0V).

2) The center frequency for the sharpness varies according to the resistor connected to Pin 28. The variation is –40 kHz/kW, and the standard value is approximately 1.5MHz for 39kW.

3) The voltage of Pin 19 (APL TC) is the following values according to the APL (average picture level).
APL 0% (all black) : 2.0V
APL 100% (all white) : 3.2V

4) Pin 23 (SYNC IN) is normally connected to Pin 24 (Y IN) for use. To cope with weak electric fields, however, its level can be increased or a low-pass filter inserted to provide a separate input.

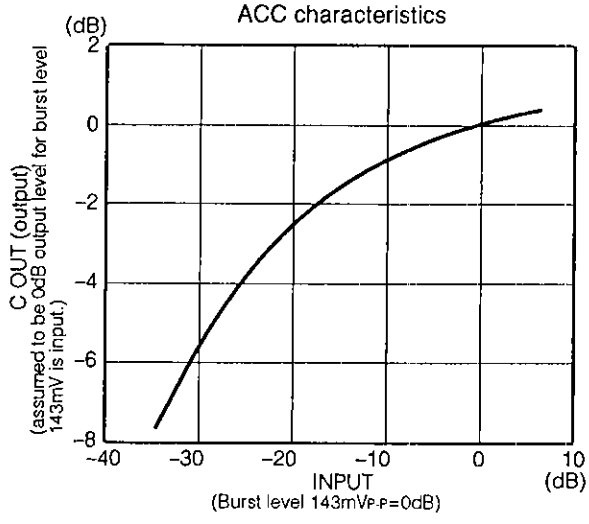
5) The amount of delay for luminance and chroma signals in the IC is the same.

6) Demodulation axis and detective output ratio
The standard values are given below as referenced to the B-Y axis.

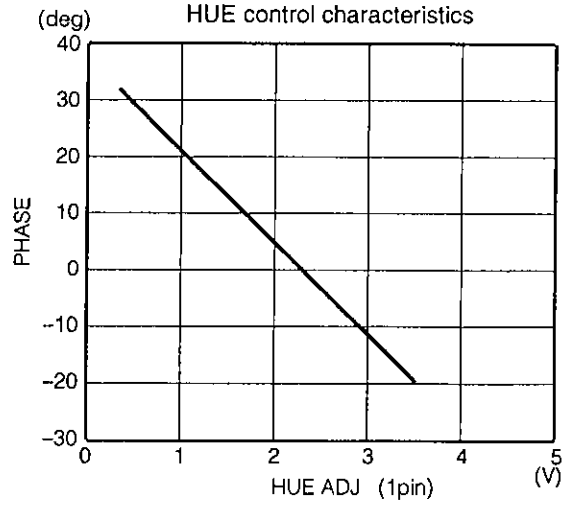
	Demodulation axis	Detective output ratio
R-Y axis	88°	0.57
G-Y axis	235°	0.37

7) Notes on Operation
Be sure to wire X'tal (crystal oscillator) as close to the IC and as short as possible since F0 varies depending on floating capacitance and other factors. Also, take particular care with the routing of the Vcc and GND leads. Use a decoupling capacitor for Vcc and others with a superior performance and attach it as close to the IC as possible.

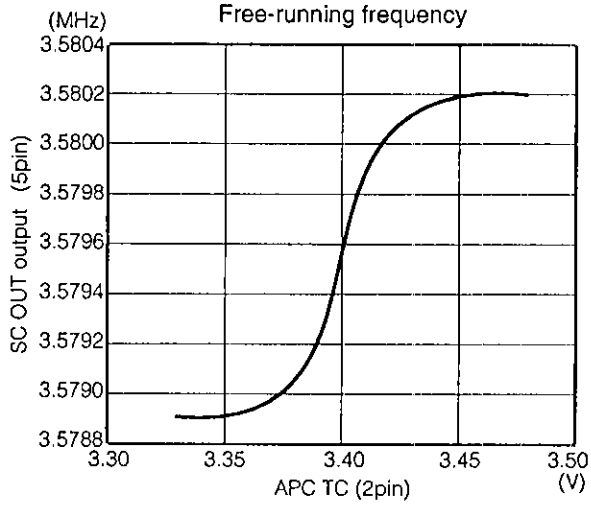
ACC characteristics



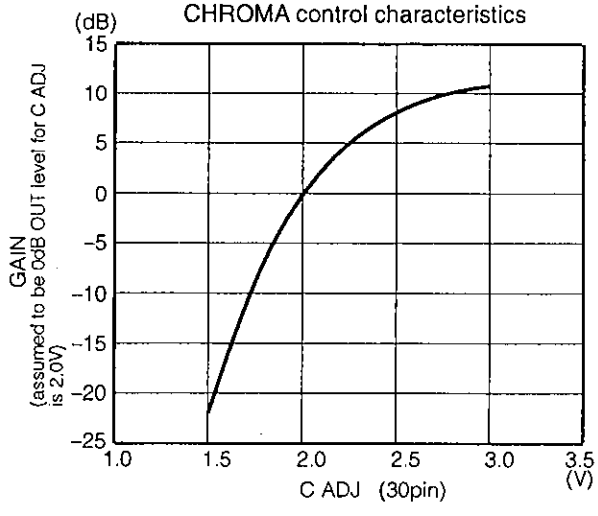
HUE control characteristics



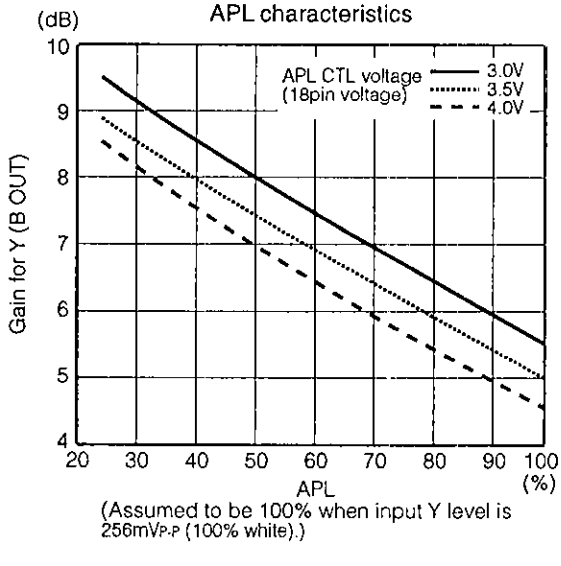
Free-running frequency



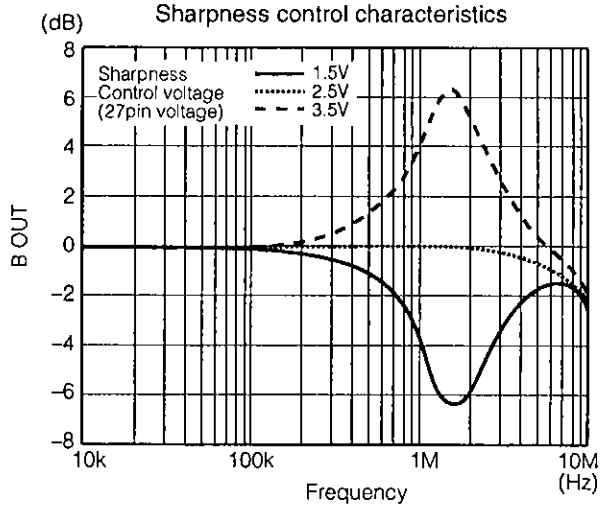
CHROMA control characteristics



APL characteristics

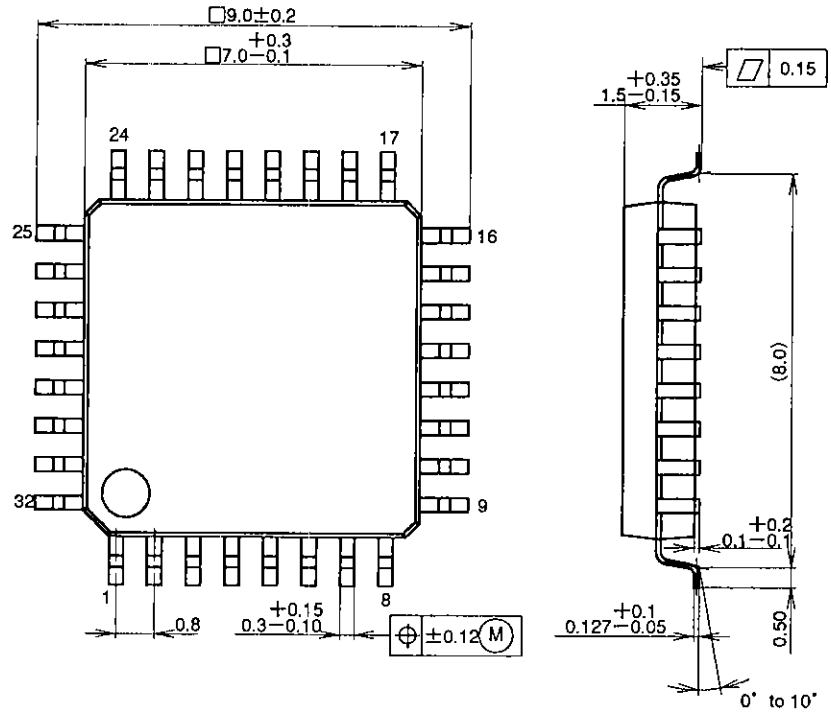


Sharpness control characteristics



Package Outline Unit : mm

32PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-32P-L01
EIAJ CODE	*QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42ALLOY
PACKAGE WEIGHT	0.2g