SONY

CXA1844Q

10-bit 33MSPS A/D Converter

For the availability of this product, please contact the sales office.

Description

The CXA1844Q is a 10-bit 33MSPS 2-step parallel type A/D converter for video signal processing.

This A/D converter operates on ± 5V power supplies. The analog signal can be converted to the digital signal by using this IC in conjunction with the Sample-and-hold IC (CXA1843Q).

48 pin QFP (Plastic)

Features

- Maximum operating speed : 33MSPS (Min.)
- Resolution : 10-bit
- Low power dissipation : 320mW (Typ.)
- Wide-band analog input : 15MHz
- Low input capacitance : 50 pF (Typ.)
- Built-in digital correction
  (Compensation within ± 16 LSB)
- TTL input (Except CLK which is ECL LIKE)
- TTL output
- Output code : binary/2S complement/
  1S complement

Function

10-bit 33MSPS 2-step parallel type A/D converter

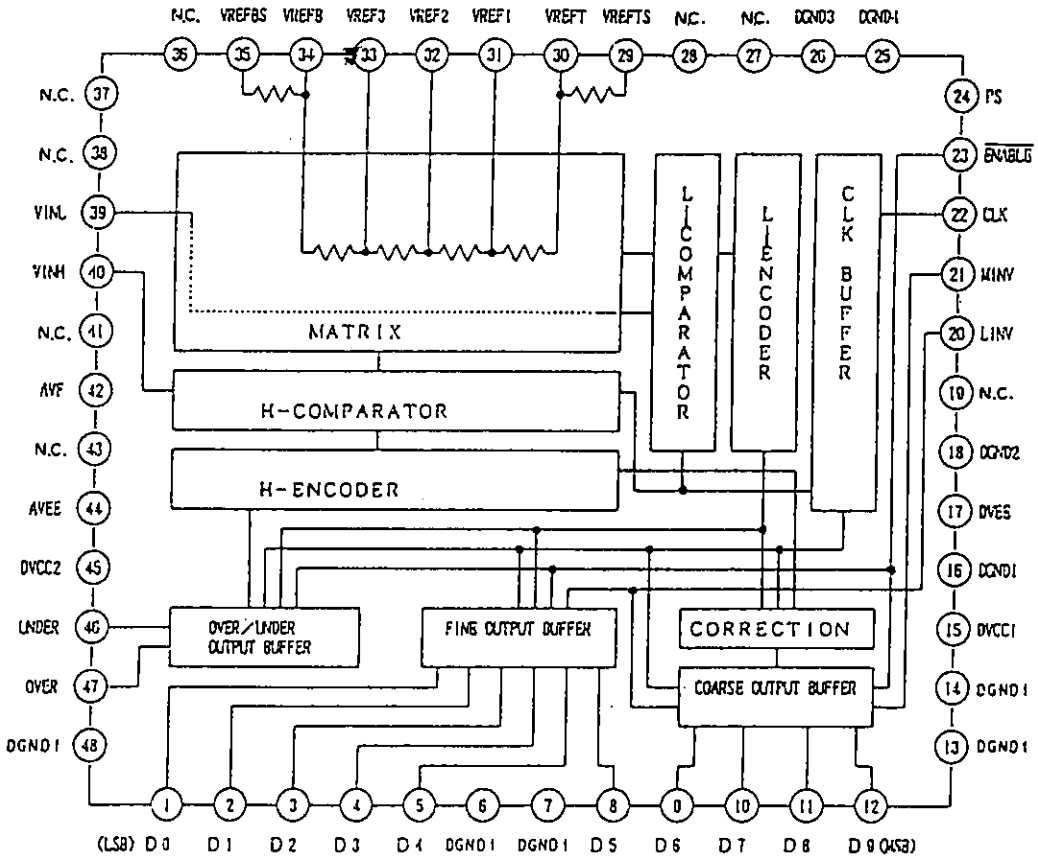
Structure

Bipolar silicon monolithic IC

Applications

High resolution video signal processing

Block Diagram



E93737 A77

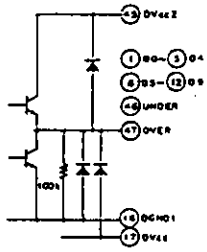
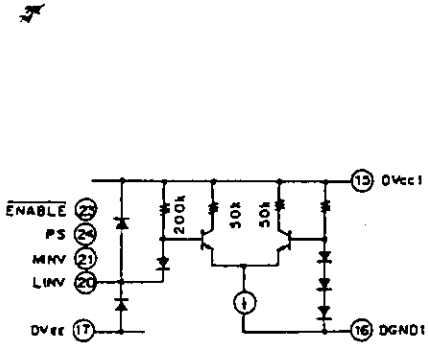
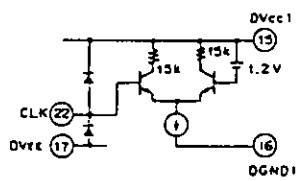
Absolute Maximum Ratings (Ta=25°C)

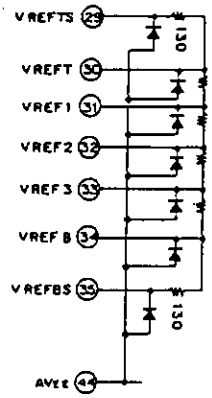
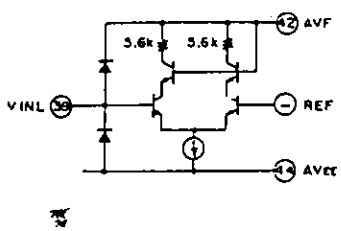
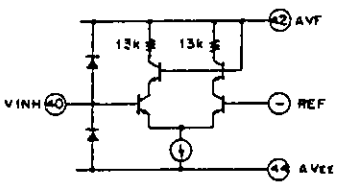
• Supply voltage	DVcc1	0 to +6	V
	DVcc2	0 to +6	V
	AVEE	−6 to 0	V
	DVEE	−6 to 0	V
• Analog input voltage	VINH	AVEE to AVF+0.3	V
	VINL	AVEE to AVF+0.3	V
• Reference voltage	VREFT	AVEE to AVF+0.3	V
	VREFB	AVEE to AVF+0.3	V
• Digital input voltage	CLK	DGND1−0.5 to DVcc1	V
	MINV	DGND1−0.5 to DVcc1	V
	LINV	DGND1−0.5 to DVcc1	V
	PS	DGND1−0.5 to DVcc1	V
	$\overline{\text{ENABLE}}$	DGND1−0.5 to DVcc1	V
• Digital output voltage	Vo	DGND1−0.5 to +3.6	V
	(Vo: The voltage is applied to the output pin for high impedance output.)		
• Storage temperature	Tstg	−65 to 150	°C
• Allowable power dissipation	PD	0.62	W

Recommended Operating Conditions

		Min.	Typ.	Max.	Unit
• Supply voltage	DVcc1	+4.75	+5	+5.25	V
	DVcc2	+4.75	+5	+5.25	V
	DGND1		0		V
	DGND2		0		V
	DGND3		0		V
	DGND4		0		V
	AVF	+0.5	+0.7	+0.9	V
	AVEE	−5.25	−5	−4.75	V
	DVEE	−5.25	−5	−4.75	V
• Analog input voltage	VINH	−2		0	V
	VINL	−2		0	V
• Reference voltage	VREFT	−0.1	0	+0.1	V
	VREFB	−2.1	−2	−1.9	V
• Digital input voltage	(CLK)				
	VIH1	DVcc1−0.9	DVcc1−0.75		V
	VIL1		DVcc1−1.5	DVcc1−1.35	V
	(MINV, LINV, PS, $\overline{\text{ENABLE}}$)				
	VIH2	+2			V
	VIL2			+0.8	V
• Clock width	tPWH	14			ns
	tPWL	13			ns
• Operating temperature	Topr	−20		+75	°C

Pin Description

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1 to 5 8 to 12	D0 to D9	O	TTL		Digital output D0 (LSB) to D9 (MSB)
46	UNDER	O			Underflow output
47	OVER	O			Overflow output
15	DVcc1	—	+5V Typ.		Digital power supply
45	DVcc2				
6, 7 13, 14 16, 48	DGND1	—	GND		Digital ground
18	DGND2				
26	DGND3				
25	DGND4				
17	DVEE	—	−5V Typ.		Digital negative power supply
44	AVEE	—			Analog negative power supply
20	LINV	I	TTL		This input can invert output form of D0 to D8. In open condition, this pin turns to high level input. (For details, refer to the Output Formula Chart.)
21	MINV	I	TTL		This input can invert output form of D9 (MSB). In open condition, this pin turns to high level input. (For details, refer to the Output Formula Chart.)
23	$\overline{\text{ENABLE}}$	I	TTL		3-state control. Turns to enable when low is input. In open condition, this pin turns to high level input.
24	PS	I	TTL		Power save input. Power save condition is entered when high level is input. In open condition, this pin turns to high level input.
22	CLK	I	ECL LIKE		Clock input

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
29	VREFTS	—	GND		Reference voltage sense (Top)
30	VREFT	I			Reference voltage force (Top)
31	VREF1	—	–0.5V		
32	VREF2	—	–1.0V		
33	VREF3	—	–1.5V		
34	VREFB	I	–2V		Reference voltage force (Bottom)
35	VREFBS	—			Reference voltage sense (Bottom)
39	VINL	I	–2V to 0V		Analog input (Lower comparator input)
40	VINH	I	–2V to 0V		Analog input (Upper comparator input)
42	AVF	—	+0.7V		Analog power supply
19, 27	N.C.	—	—		Open. Not connected to internal circuit, but connection to DGND (digital ground) is recommended.
28, 36 37, 38 41, 43	N.C.	—	—		Open. Not connected to internal circuit, but connection to AGND (analog ground) is recommended.

Electrical Characteristics

(Ta=25°C, DVcc1, 2=+5V, DGND1 to 4=0V, AVF=0.7V, AVEE, DVEE=–5V, VREFB=–2V, VREFT=0V)

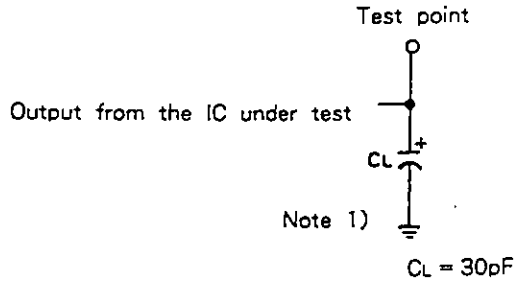
Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Resolution	n		10	10	10	bit
DC characteristics						
Integral linearity error	EIL	VIN=–2 to 0V	–1.5		+1.5	LSB
Differential linearity error	EDL	VIN=–2 to 0V	–1		+1	LSB
Analog input						
Analog input current	IIN	VIN=0	0	25	120	µA
Analog input capacitance	CIN	VIN=–1V+0.07Vrms		50		pF
Analog input band width	BW	–1dB	15			MHz
Reference voltage input						
Reference current	IREF	VREFB=–2V	–16	–10	–7	mA
Reference resistance	RREF		120	200	280	Ω
Offset voltage	EOT		5	10	25	mV
	EOB		5	10	25	mV
Reference voltage	VREF1			–0.5		V
	VREF2			–1.0		V
	VREF3			–1.5		V
Digital input						
Digital input voltage	VIH1	*1	DVcc1–0.9			V
	VIL1	*1			DVcc1–1.35	V
	VIH2	*2	2			V
	VIL2	*2			0.8	V
Digital input current	IIH1	*1, DVcc1=Max., VIH=DVcc1–0.8V	–10		+15	µA
	IIL1	*1, DVcc1=Max., VIL=DVcc1–1.6V	–15		+10	µA
	IIH2	*2, DVcc1=Max., VIH=2.7V	–15		+15	µA
	IIL2	*2, DVcc1=Max., VIL=0.5V	–25		0	µA
Digital input characteristics				2		pF

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Switching characteristics						
Maximum operating speed	Fc		33			MSPS
Clock pulse width	t_{PWH}	*3	14			ns
	t_{PWL}		13			ns
Sampling delay	t_{SH}		−2	1	2	ns
	t_{SL}		−3	−2.5	1	ns
Output delay time	t_{DLH}	*3 C_L=30pF *5	4		18	ns
	t_{DHL}		4		18	ns
3-state output disable time	t_{PHZ}	*4 *6			150	ns
	t_{PLZ}				100	ns
3-state output enable time	t_{PZH}				300	ns
	t_{PZL}				150	ns
Digital output						
Digital output voltage	V_{OH}	I_{OH}=−500 μA, DV_{CC2}=Min.	2.7	3.4		V
	V_{OL}	I_{OL}=1mA, DV_{CC2}=Min.			0.5	V
Leak current during output off	I_{OZ}	DV_{CC2}=Max., Vo=3.6V (Max.)	−20		150	μA
Dynamic characteristics						
Differential gain error	DG	NTSC 40IRE mod ramp, Fc=14.3MSPS		0.5		%
Differential phase error	DP			0.3		deg
SNR	SNR	Fc=33MSPS F_{IN}=1kHz		57		dB
		Fc=33MSPS F_{IN}=1MHz		53		dB
		Fc=33MSPS F_{IN}=8MHz		50		dB

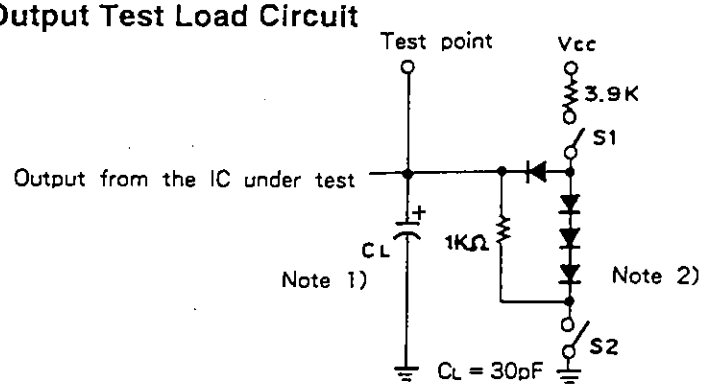
Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Power supply						
DVcc1 current	I_{DVCC1}	DVcc1=5V	9	20	30	mA
		*7 During power save	7.5	14.5	21.5	mA
DVcc2 current	I_{DVCC2}	DVcc2=5V	0.001	0.3	1	mA
		*7 During power save	0	0	0.1	mA
AVEE current + DVEE current	I_{VEE}	AVEE=–5V, DVEE=–5V	–57.5	–38	–20.8	mA
		*7 During power save	–4.4	–2.8	–1.6	mA
AVF current	I_{AVF}	AVF=0.7V	3.5	6.8	10.5	mA
		*7 During power save	30	55	85	µA
Power dissipation Pd=A+B+C A=(I_{DVCC1}+I_{DVCC2}+|I_{VEE}|) × 5V B=I_{AVF} × 0.7V C=|I_{REF}| × 2V	Pd		178	316	482	mW
		*7 During power save	59	107	163	mW

*1 CLK input
*2 MINV, LINV, $\overline{\text{ENABLE}}$, and PS inputs
*3 Refer to Timing Diagram (1)
*4 Refer to Timing Diagram (2)
*5 The load is a bi-state totem-pole output delay time test load circuit.
*6 The load is a 3-state output test load circuit.
*7 When PS and $\overline{\text{ENABLE}}$ inputs are in high level.

Bi-state Totem-pole Output Delay Time Test Load Circuit



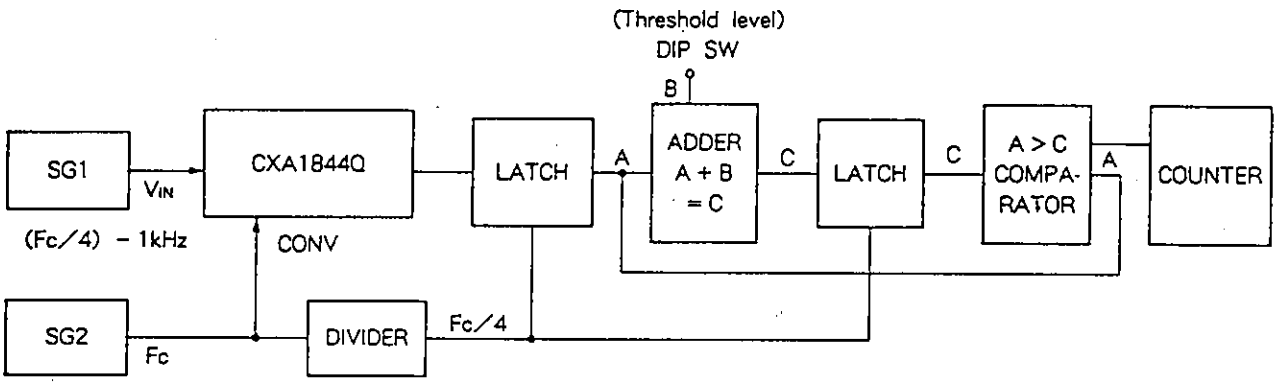
3-state Output Test Load Circuit



Test condition	S1	S2
t_{PZL}	Close	Open
t_{PZH}	Open	Close
t_{PLZ} t_{PHZ}	Close	Close

Note 1) C_L includes probe capacitance and parasitic capacitance in Test Board.
Note 2) All diodes are IS2076.

Error Rate Test Circuit



Notes on Operation

1. Analog ground (Analog ground on PCB)
   Keep analog ground surface on PCB as wide as possible with impedance and resistance as low as possible.

2. Digital ground (DGND1, DGND2, DGND3, DGND4)
   Upon mounting to PCB keep ground surface as wide as possible with impedance and resistance as low as possible.
   Moreover, a common analog and digital ground immediately near ADC will help obtain characteristics smoothly.

3. Digital positive power supply (DVcc1, DVcc2)
   Connect to the digital ground with a ceramic capacitor over 0.1 µF and as close to the pins as possible.
   Insert a ceramic capacitor between DVcc2 and DGND1 of TTL output power supply as shortly as possible because noise tends to occur.

4. Analog positive power supply (AVF)
   As shown in the Standard Circuit, make the positive power supply about +0.7V by connecting to the analog ground with a diode and +5V with a pull-up resister respectively.
   Connect to the analog ground on PCB with a ceramic capacitor over 0.1 µF as close to the pin as possible.

5. Analog negative power supply (AV_{EE})
   Connect to the analog ground on PCB with a ceramic capacitor over 0.1 µF as close to the pin as possible.

6. Digital negative power supply (DV_{EE})
   Connect to the digital ground with a ceramic capacitor over 0.1 µF as close to the pin as possible.
   When V_{EE} is divided into digital and analog, there is continuity because of about 4Ω resistance between the two inside the IC. Accordingly, if an excessive potential difference (more than 100mV) is applied continuously, this may destroy the IC. To prevent the IC destruction, connect AV_{EE} and DV_{EE} with a inductance having good high frequency characteristics. Prevent noise mixing and the generation of potential difference between analog and digital.

7. Reference voltage (VREFTS, VREFT, VREF1, VREF2, VREF3, VREFB, VREFBS)
   These pins provide reference voltage to upper and lower comparators. Voltage between VREFT and VREFB corresponds to input dynamic range.
   There is a 200Ω resistance between VREFT and VREFB. By applying 2V to both pins a current of about 10 mA flows. When the reference voltage is destabilized by the clock, ADC characteristics are adversely affected. Connect VREFT and VREFB to the analog ground on PCB by means of a tantalum capacitor over 10 µF and a ceramic capacitor over 0.1 µF respectively. Also, connect each of VREF1, VREF2 and VREF3 to the analog ground on PCB using a ceramic capacitor over 0.1 µF. This will provide stability to the characteristics of high frequency. Strictly speaking on reference voltage VREFT side and VREFB side there is a respective about 10mV offset.
   When there is no problem with the usage of those offset voltages, voltage is applied directly to VREFT, VREFB. In case the reference voltage is to be strictly applied, adjust to obtain an offset voltage of 0V, keeping VREFTS and VREFBS as sense pins and VREFT and VREFB as force pins to form a feedback loop circuit.
   For details, see the Standard Circuit.

8. Analog input (VINH, VINL)
VINH is the input pin for the upper comparator while VINL is the input pin for the lower comparator.
Keep the input signal level within the level between VREFT and VREFB.
As this IC's analog input capacitance stands at about 50pF, it is necessary to drive with an buffer amplifier having sufficient driving capability. Also, when driving is done with the buffer amplifier of a low output impedance, as A/D converter input capacitance is large, ringing is generated and settling time grows longer. Here a small resistance of about 5 to 30Ω is connected in series between the buffer amplifier and each of A/D converter's VINH and VINL, as a dumping resistance. This eliminates ringing and shortens settling time. Also keep wiring between buffer amplifier and A/D converter as short as possible.

9. Clock input (CLK)
ECL LIKE input. Adds the signal of Vcc1 (5V) –0.8V at high level and Vcc1 (5V) –1.6V at low level. Clock line wiring should be the shortest possible while distanced from other signal lines to avoid affecting them.
This IC is 2-step parallel type A/D converter. Accordingly an external sample-and-hold circuit (SH) is necessary. However the timing between this SH circuit output waveform (A/D converter analog input waveform) and the A/D converter clock timing requires attention. In the relation between A/D converter clock and the A/D converter analog input signal, with the timing T_H of the rising edge of A/D converter clock, the upper comparator compares the input signal and the reference voltage to latch the results. After that, with the timing T_L of the falling edge of A/D converter clock, the lower comparator compares the input signal and reference signal to latch the results. (Strictly speaking, the sampling delay t_{SH} is in T_H and the sampling delay t_{SL} is in T_L.)
In this A/D converter, the lower comparator features a length of ±32mV (±16 LSB) redundance in relation to the upper comparator. At the timing when the lower comparator compares input signal and reference signal to latch at the timing T_L, it is necessary to have the SH output settling performed. But at the timing when the upper comparator compares input signal and reference voltage to latch at the timing T_H, as long as the SH output is within the ±32mV range to the final settling value, digital correction applies, A/D conversion precisely occurs. As seen from the above, A/D converter clock rise and fall timing versus SH output waveform should be duly considered. For the clock high level time t_{PWH} and low level time t_{PWL}, set to a value in excess of the time indicated for the respective operating conditions.
Output data is synchronously with the clock rising edge.
For details on timing, refer to the Timing Chart.

10. MINV input (MINV)
Digital output polarity inversion control pin of D9 (MSB).
TTL input. At open, turns to high level input.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

11. LINV input (LINV)
Digital output polarity inversion control pin of D8 to D0 (LSB).
TTL input. At open, turns to high level input.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

12. Output enable ($\overline{\text{ENABLE}}$)
3-state control pin of digital output (D0 to D9, UNDER , OVER)
TTL input. At open, turns to high level input. At that time digital output turns all to high impedance.

13. Power save input (PS)
Power save control pin of internal circuit.
TTL input. At open, turns to high level input.
To set to power save mode, turn both PS and $\overline{\text{ENABLE}}$ to high level input.

14. Digital output (D0 to D9)
Output pin of D9 (MSB) to D0 (LSB).
TTL output.
Output data polarity inversion is executed by means of MINV and LINV signals. Can output in binary, 1S complement and 2S complement.
Also, by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.
However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart. For the timing, refer to the Timing Chart.

15. Overflow output (OVER)
When the input signal exceeds VREFT, overflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.
However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.
For the timing, refer to the Timing Chart.

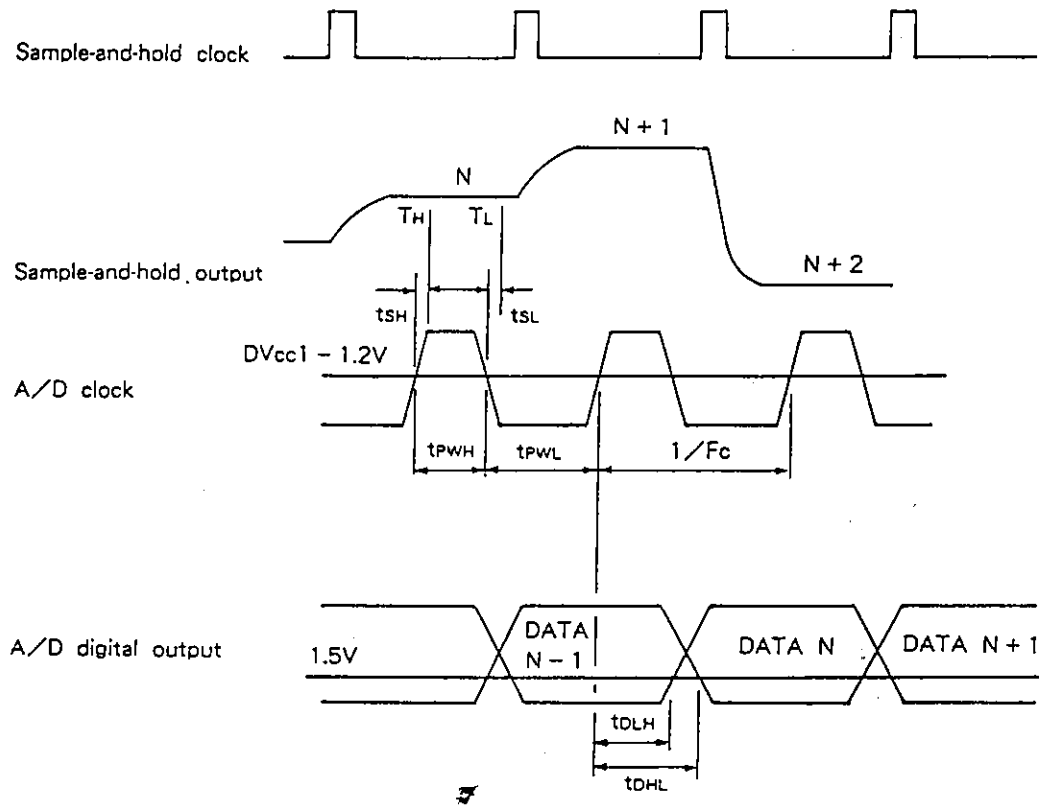
16. Underflow output (UNDER)
When the input signal turns below VREFB, underflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning $\overline{\text{ENABLE}}$ signal to high level, the output can be turned into high impedance output.
However, when the output level is for high impedance output or is in power save mode, the voltage of 3.6V or more must not be applied to prevent the distruction of IC.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.
For the timing, refer to the Timing Chart.

Output Formula Chart

$\overline{\text{ENABLE}}$		0	0	0	0	1 (OPEN)
MINV		1 (OPEN)	1 (OPEN)	0	0	—
LINV		1 (OPEN)	0	1 (OPEN)	0	—
OUTPUT		0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	
0V	0	1 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 0	1 1 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 0	Z
⋮	1	0 0 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 1 1 1 1 1 1 1 1 1 0 0	Z
⋮	2	0 0 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 1 1 1 1 1 1 1 1 0 1 0	Z
⋮	3	0 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 1 1 1 1 1 1 1 1 0 0 0	Z
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	512	0 1 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 0	Z
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	1019	0 1 1 1 1 1 1 1 0 1 1 0	0 1 0 0 0 0 0 0 1 0 0 0	0 0 1 1 1 1 1 1 1 0 1 1 0	0 0 0 0 0 0 0 0 1 0 0 0	Z
⋮	1020	0 1 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 0 0 0 0 0 0 0 0 1 1 0	Z
⋮	1021	0 1 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 0 0 0 0 0 0 0 0 1 0 0	Z
⋮	1022	0 1 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0 1 0	Z
–2V	1023	0 1 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0 0 0 0 1	0 0 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 1	Z

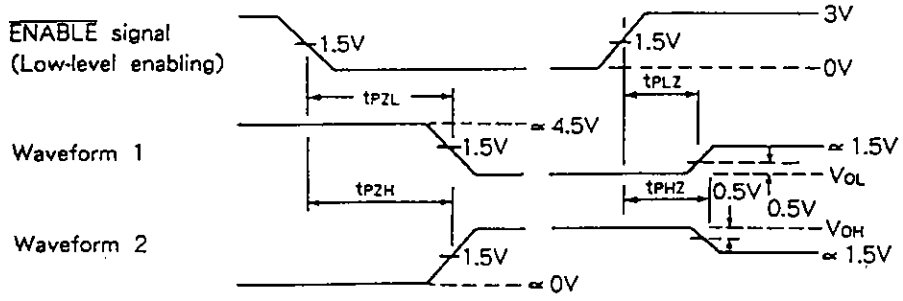
0: VOLTAGE LEVEL-LOW OF: OVER FLOW
1: VOLTAGE LEVEL-HIGH UF: UNDER FLOW
Z: HIGH IMPEDANCE

Timing Chart (1)



T_H is the timing of latching result for the comparator of V_{IN} and V_{REF} in the upper comparators.
T_L is the timing of latching result for the comparator of V_{IN} and V_{REF} in the lower comparators.

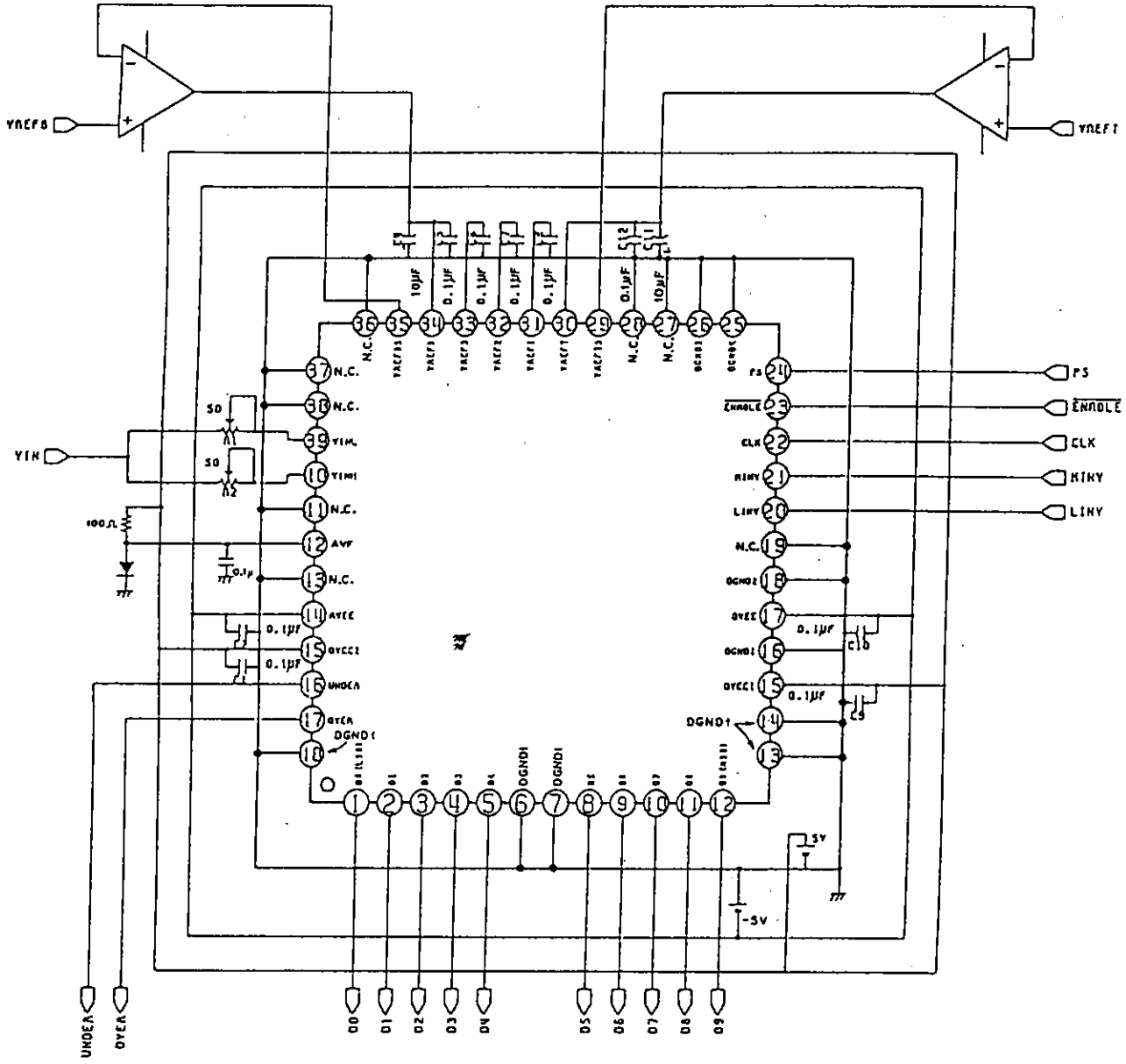
Timing Chart (2)



Output waveform of 3-state enable and disable time *.
(* Enable time=t_{PZL}/t_{PZH}, disable time=t_{PLZ}/t_{PHZ})

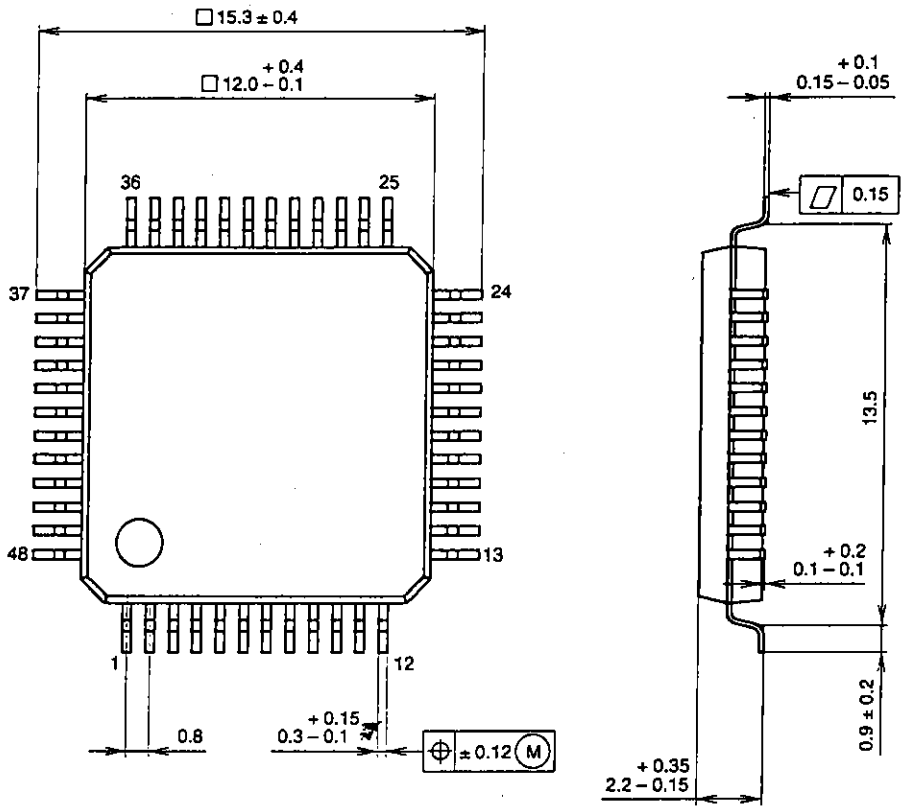
Notes) Waveform 1 indicates the output waveform when internal conditions are set to obtain a low level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.
Waveform 2 indicates the output waveform when internal conditions are set to obtain a high level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.

Standard Circuit



Package Outline Unit: mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).