

Electronic volume control

Description

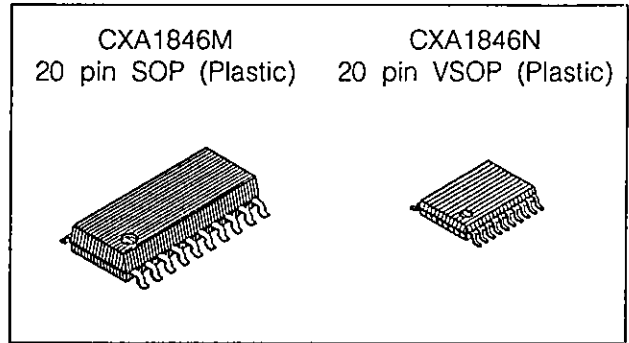
The CXA1846M/N is an electrical volume control IC for use in car radios/stereos and radio-cassette recorders featuring serial data control.

Features

- Volume adjustment (0dB to -87dB, -∞dB)
- Balance
- Serial data control (DATA, CLK, CE)
- Single 8V power supply
- Zero-cross detection circuit

Structure

Bipolar silicon monolithic IC



Absolute Maximum Ratings (Ta=25°C)

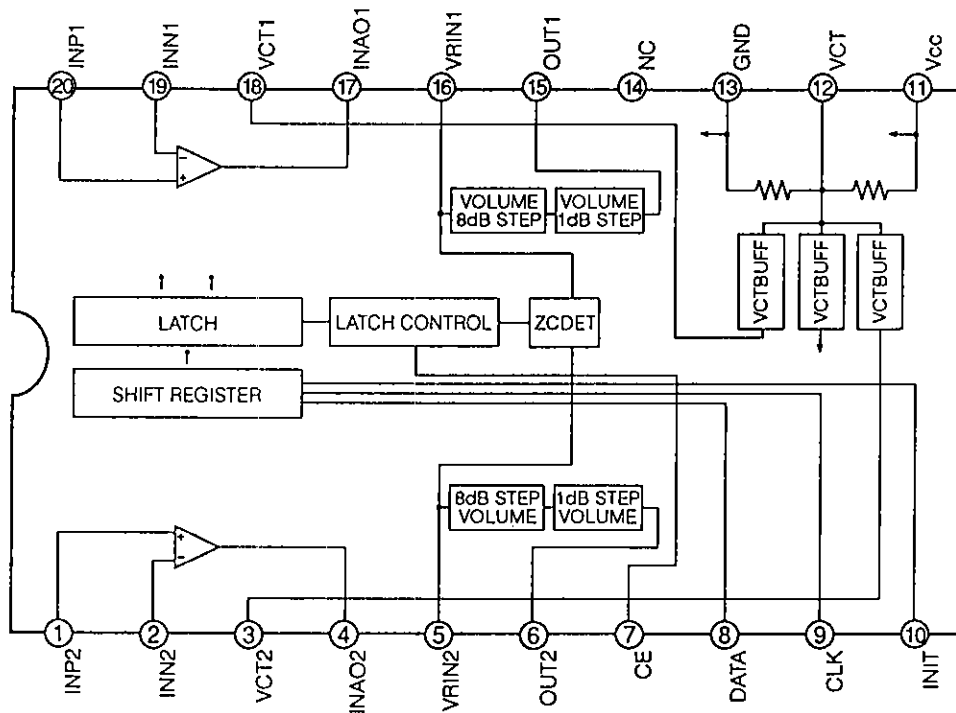
- Supply voltage Vcc 13 V
- Operating temperature Topr -40 to +85 °C
- Storage temperature Tstg -65 to +150 °C
- Allowable power dissipation

Pd	SOP	500 (75°C)	mW
	VSOP	220 (75°C)	mW

Recommended Supply Voltage Range

- Supply voltage Vcc 6 to 12 V

Block Diagram and Pin Configuration



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Pin Description

Pin No.	Symbol	I/O resistance voltage	Equivalent circuit	Description
1 20	INP2 INP1	50kΩ VCT		Input operational amplifier positive phase input
2 19	INN2 INN1	— VCT		Input operational amplifier reversed phase input
3 18	VCT2 VCT1	— VCT		VCT buffer output
4 17	INAO2 INAO1	— VCT		Input operational amplifier
5 16	VRIN2 VRIN1	8.2kΩ VCT		Volume input

Pin No.	Symbol	I/O resistance voltage	Equivalent circuit	Description
6 15	OUT2 OUT1	— VCT		Volume output
7	CE	∞ —		Latch enable
8	DATA	∞ —		Serial data input
9	CLK	∞ —		Serial clock
10	INIT	— —		System reset
11	Vcc	—		+power supply
12	VCT	— VCT		Mid-point potential
13	GND	— —		GND

Electrical Characteristics (Unless otherwise specified Vcc=8V, Ta=25°C)

Item	Symbol	Measurement Condition	Min.	Typ.	Max.	Unit	
Circuit current	Icc	No signal	5	8	12	mA	
Total harmonic distortion	THD	1kHz, 5dBm	—	0.003	0.01	%	
Output noise voltage	Vn	Input shorted	—	5	7	μVrms	
Maximum output voltage	Vom	1kHz	8	—	—	dBm	
Separation	CS	1kHz	85	90	—	dB	
Maximum attenuation	ATTm		85	90	—	dB	
Input voltage	High	Vsh	Data, INIT	3	—	6	V
	Low	Vsl	CLK, CE	0	—	1.5	V
Input voltage range	Vin		1	—	Vcc-1	V	
Maximum output current	I _{max}	Input buffer amplifier output current	—	—	1	mA	

RESET

The IC is reset by reducing the voltage at the INIT pin to 1V or less when CLK is high. Reset can not be performed when CLK is low. The table below shows the status when the IC has been reset.

MODE	Setting
VRC1	-∞
VRF1	-7dB
VRC2	-∞
VRF2	-7dB

Data Allocation

Fast bit

D1	NOP	MSB	
D2	VRC1		
D3			
D4			
D5			
D6	VRF1		
D7			
D8			
D9	NOP		
D10	VRC2		
D11			
D12			
D13			
D14	VRF2		LSB
D15			
D16			

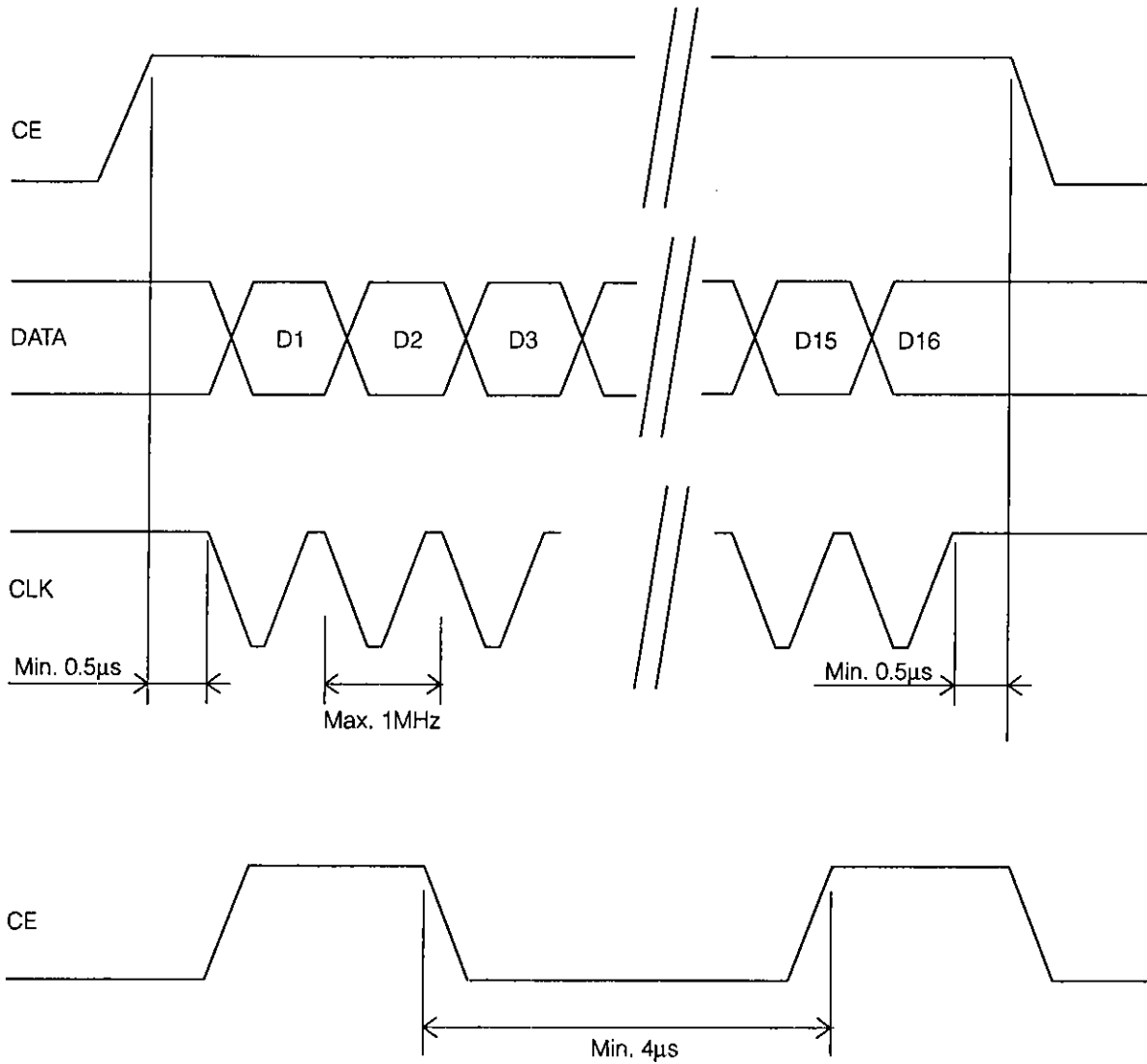
VRC1/VRC2

Setting	D2/D10	D3/D11	D4/D12	D5/D13
0	1	1	1	1
-8	1	1	1	0
-16	1	1	0	1
-24	1	1	0	0
-32	1	0	1	1
-40	1	0	1	0
-48	1	0	0	1
-56	1	0	0	0
-64	0	1	1	1
-72	0	1	1	0
-80	0	1	0	1
-∞	0	1	0	0
-∞	0	0	0	0

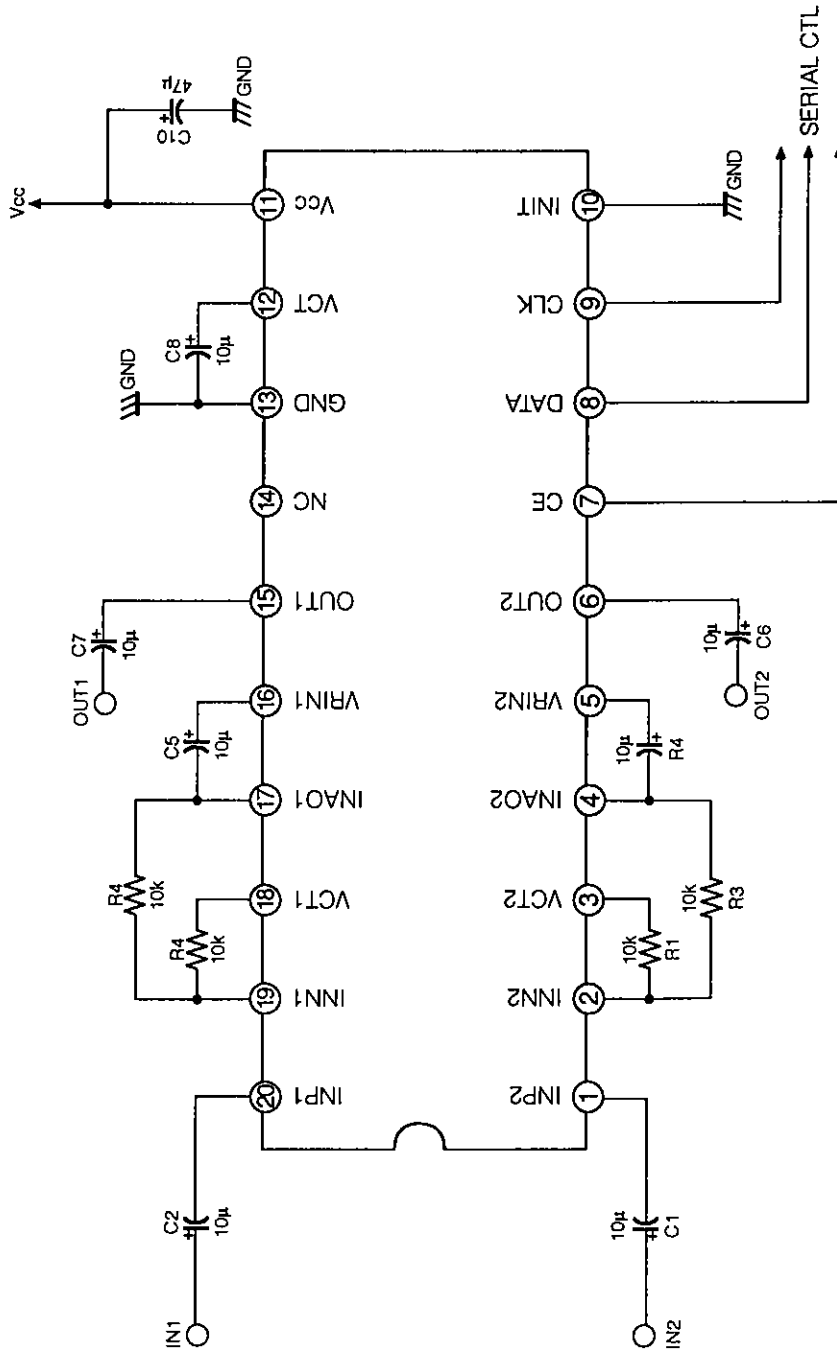
VRF1/VRF2

Setting	D6/D14	D7/D15	D8/D16
0	1	1	1
-1	1	1	0
-2	1	0	1
-3	1	0	0
-4	0	1	1
-5	0	1	0
-6	0	0	1
-7	0	0	0

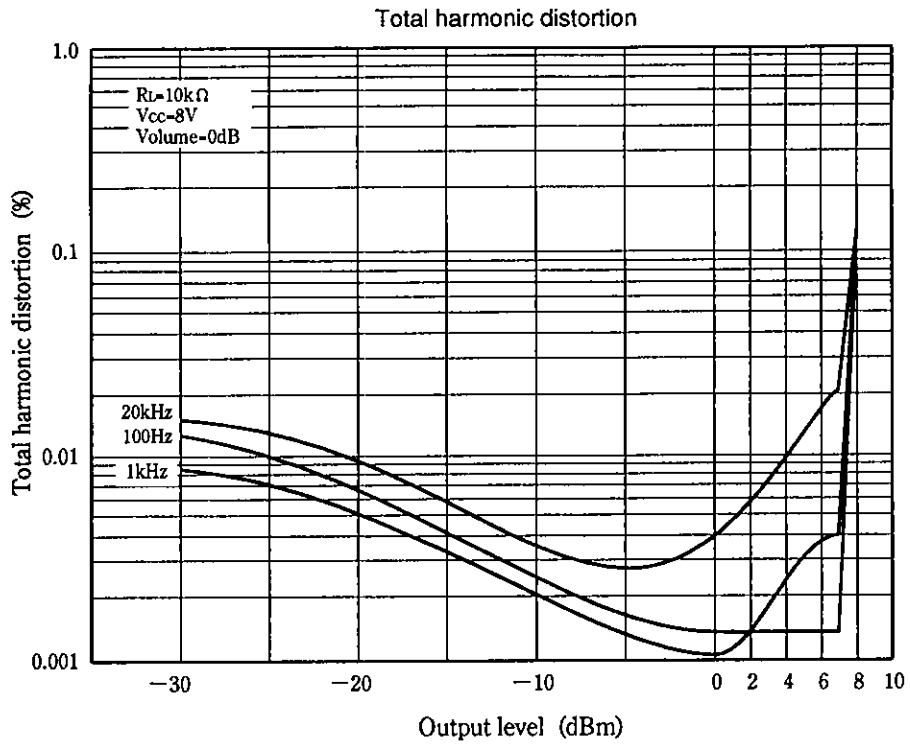
Data Timing



Application Circuit



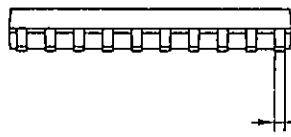
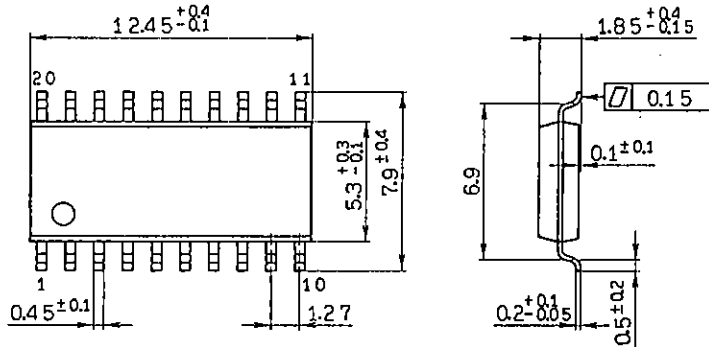
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.



Package Outline Unit : mm

CXA1846M

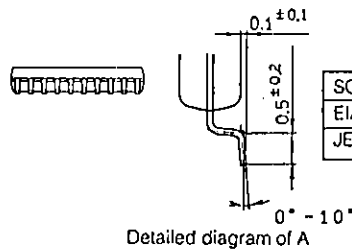
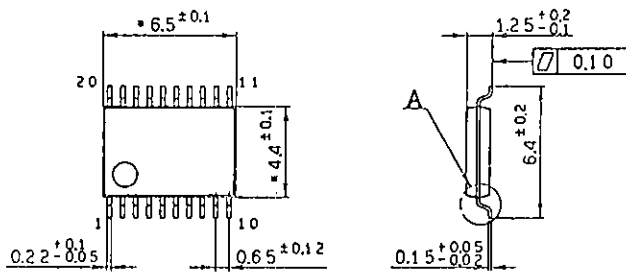
20pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-20P-L01
EIAJ NAME	*SOP020-P-0300-A
JEDEC CODE	—

CXA1846N

20pin VSOP (Plastic) 225mil



SONY NAME	VSOP-20P-L01
EIAJ NAME	SSOP020-P-0225-similar A
JEDEC CODE	—

Note) Dimensions marked with * do not include resin residue.