SONY

CXA1870S

Color TV Y/C/Jungle

For the availability of this product, please contact the sales office.

Description

The CXA1870S is a bipolar IC which integrates the NTSC color TV luminance signal processing, chroma signal processing, sync signal processing, and RGB signal processing onto a single chip.

Features

- I^2C bus compatible. Various types of adjustments and user controls performed with two bus lines SCL and SDA.
- H and V oscillation frequencies made non-adjusting with a countdown system.
- Non-adjusting Y system filters (chroma trap, delay line)
- Built-in V picture distortion correction circuit
- Built-in delay line aperture compensation
- Auto cut-off function for automatic CRT cut-off adjustment and compensation for changes with time
- Multiple inputs

Composite video: 2 systems
(Built-in 2-input, 1-output video switch)
Y/C separation input: 1 system
On screen display input: 1 system

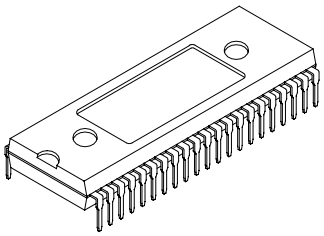
Applications

- Color TV

Structure

Bipolar silicon monolithic IC

42 pin SDIP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

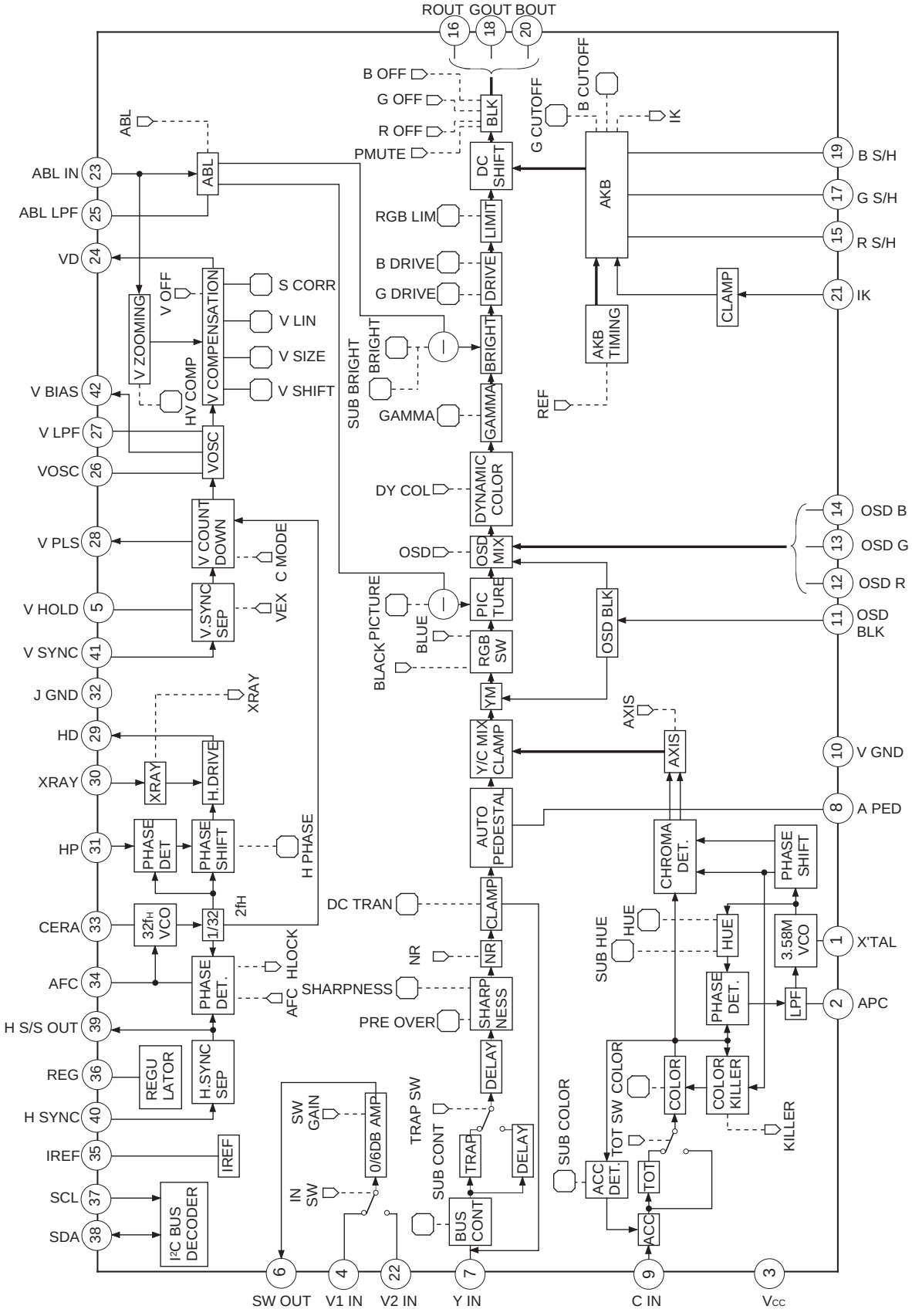
• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.73	W

Recommended Operating Conditions

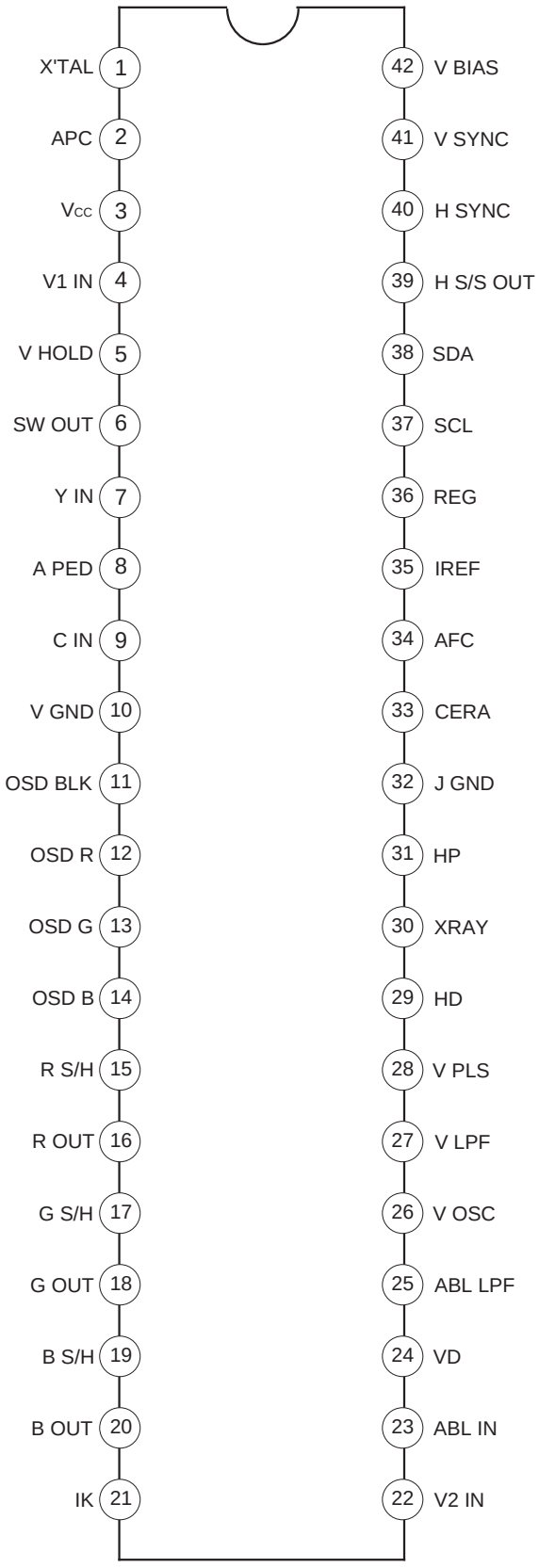
Supply voltage	V_{CC}	9±0.5	V

E95431-TE

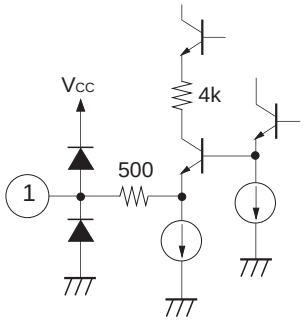
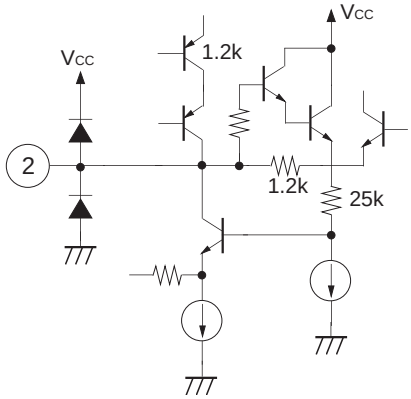
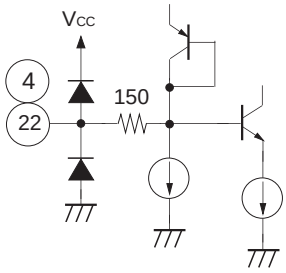
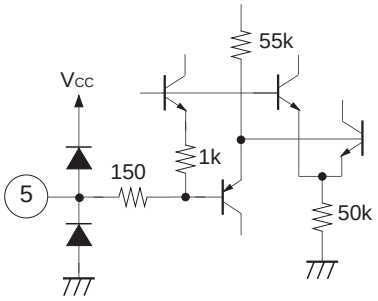
Block Diagram

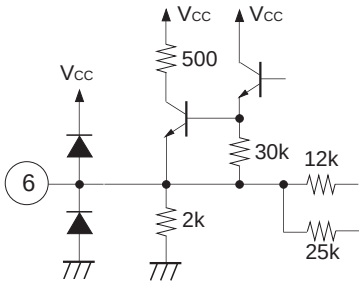
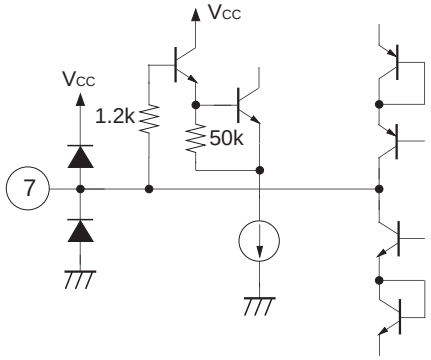
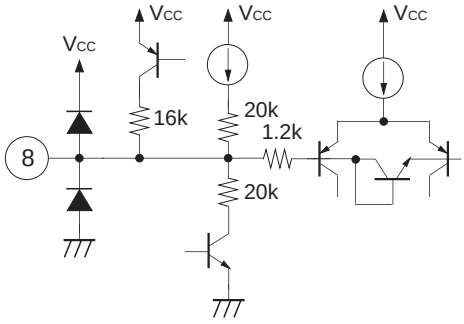
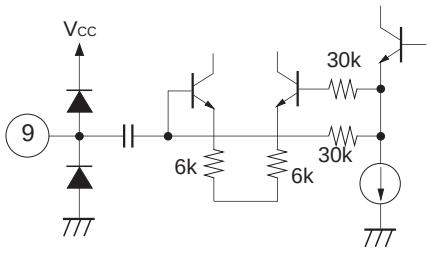


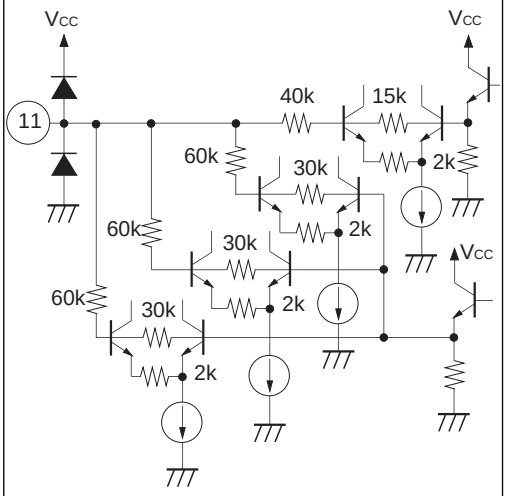
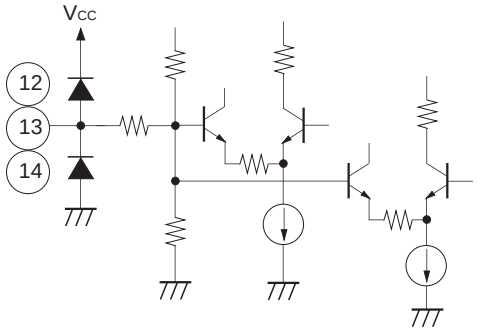
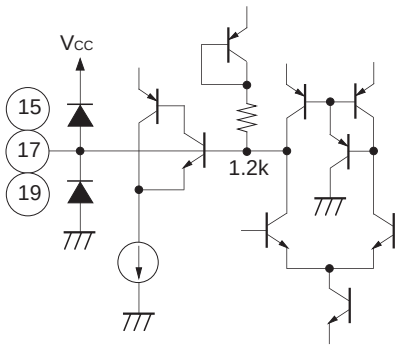
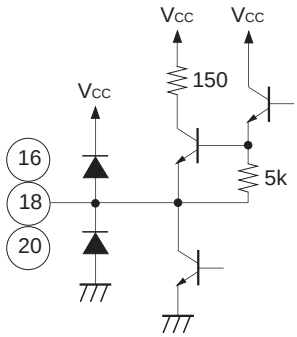
Pin Configuration

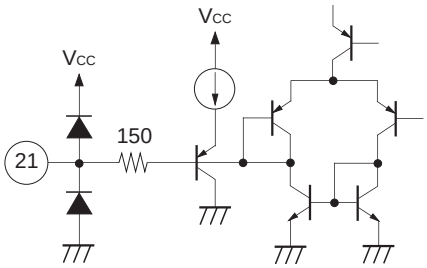
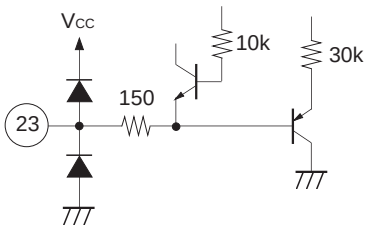
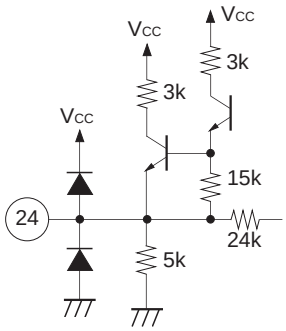
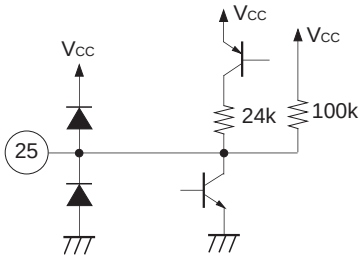
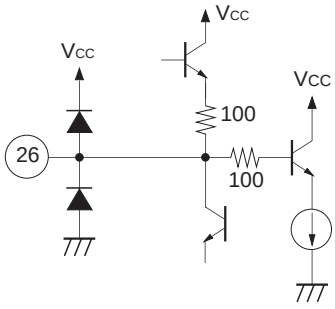


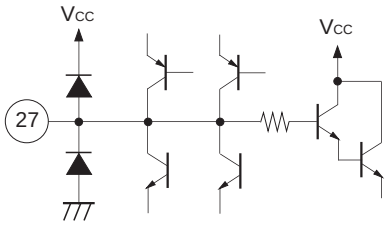
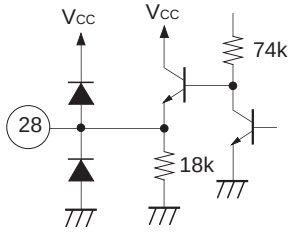
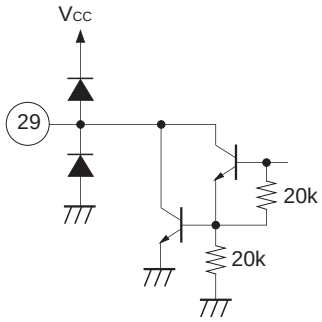
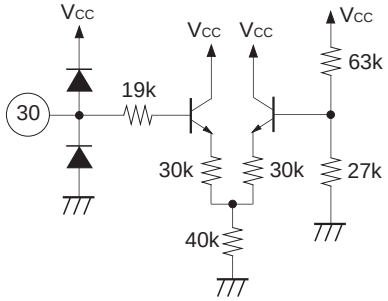
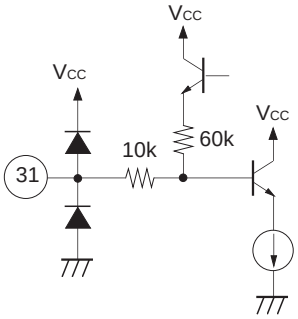
Pin Description

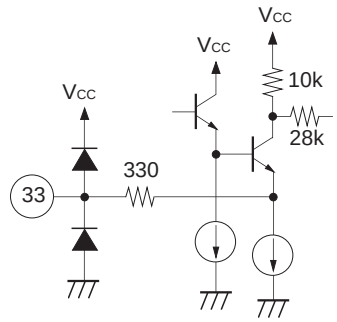
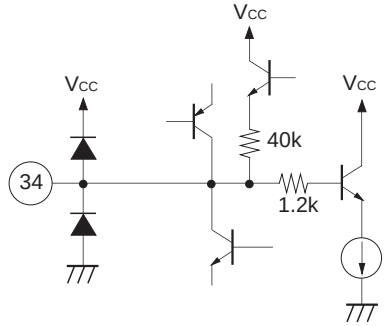
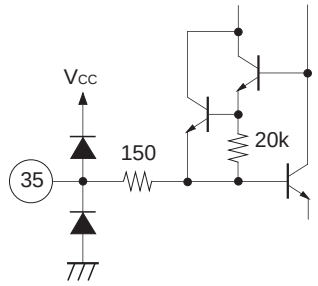
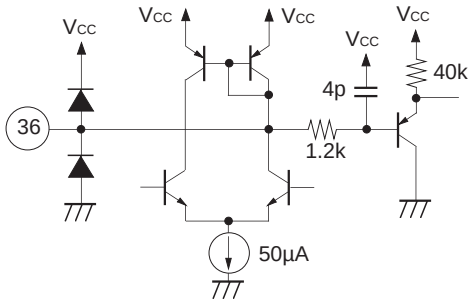
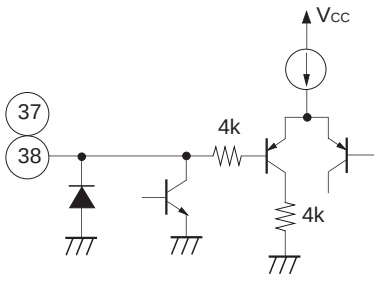
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	X'TAL	2.6 V		Connect a 3.58 MHz crystal oscillator.
2	APC	5 V		APC lag-lead filter CR connection pin.
3	Vcc	9 V		Power supply pin.
4 22	V1 IN V2 IN	2 V		Video switch input pins. Sync tip clamping is performed, so input via capacitors.
5	V HOLD	0.7 V		Peak hold pin for V sync separation. Connect a capacitor.

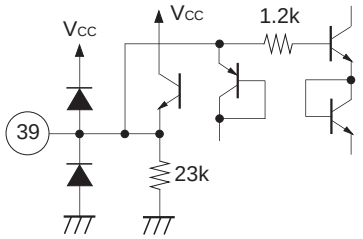
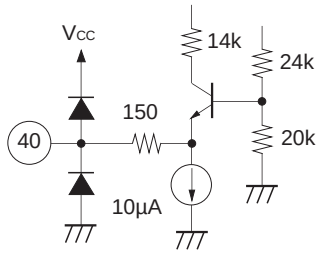
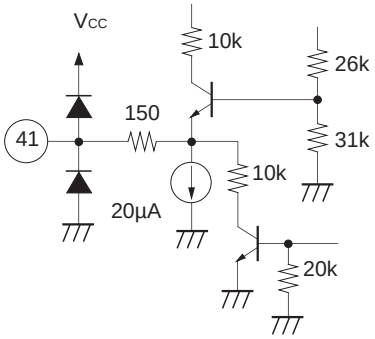
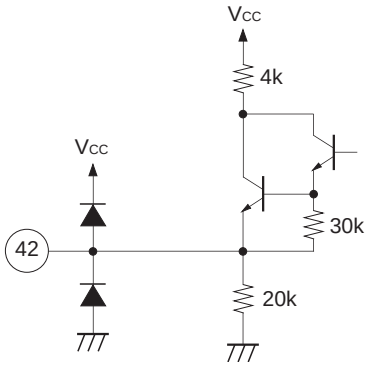
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	SW OUT	—		Video switch output pin.
7	Y IN	3.5 V		Y signal input pin. Input via a capacitor. Standard input level: 2 Vp-p
8	A PED	3.5 V		Auto pedestal (black elongation) black peak hold pin. Connect a capacitor.
9	C IN	—		Chroma signal input pin. Standard input level (burst level): 570 mVp-p
10	V GND	—		Video system (Y/C/RGB) GND pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	OSD BLK	—		Blanking signal input pin for OSD RGB input. 0 to 1 V: Blanking not performed. 2 to 3 V: Signal from Y IN/C IN lowered by –6 dB. 4 to 6 V: R, G and B outputs become lower than black level.
12 13 14	OSD R OSD G OSD B	—		Digital R, G and B signal input pins for on screen display. 0 to 1 V: No OSD display. 2 to 3 V: OSD level = 46 IRE (33 IRE) 4 to 6 V: OSD level = 92 IRE (65 IRE) Figures in parentheses are for when the I²C OSD register is set to 0.
15 17 19	R S/H G S/H B S/H	—		Sample-and-hold pins for R, G and B AKB (Auto Kinetic Bias). Connect to GND via capacitors.
16 18 20	R OUT G OUT B OUT	—		R, G and B output pins.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	IK	—		Inputs the signal obtained by converting the CRT beam current (Ik) into voltage. Connect to an emitter follower via a capacitor.
23	ABL IN	—		ABL voltage input pin.
24	VD	—		Vertical deflection sawtooth wave output pin.
25	ABL LPF	—		ABL signal LPF pin. Connect a capacitor.
26	V OSC	—		Connect a capacitor to generate the V sawtooth wave.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	V LPF	5 V		Connect a capacitor to hold the AGC voltage which maintains the V sawtooth wave at a constant amplitude.
28	V PLS	—		V pulse output pin. A negative polarity pulse 3 to 3.5 H width is output from this pin. High level: 4.5 V Low level: 0 V
29	HD	—		H drive output pin. This pin is output at the open collector.
30	XRAY	—		X-ray protection circuit input pin. When a pulse with a width of 7 V or more is input, HD output becomes low and R, G and B outputs are blanked. This status is maintained until the power supply is turned off. Vilmax = 2.4 V Vihmin = 3.0 V
31	HP	3.3 V (at no signal)		H pulse input pin. Inputs a 3 to 5 Vp-p signal via a capacitor.
32	J GND	—		Jungle system (H/V) GND pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
33	CERA	2.3 V		Connect a 32 fh (503.5 kHz) ceramic oscillator.
34	AFC	3.2 V		AFC lag-lead filter CR connection pin.
35	IREF	2.6 V		Connect a 15 kΩ resistor between this pin and GND.
36	REG	7 V		Regulator pin for voltage generated internally from Vcc. Connect a capacitor for stabilization.
37 38	SCL SDA	—		I²C bus SCL (Serial Clock) and SDA (Serial Data) pins. Vilmax = 1.5 V Vihmin = 3 V Volmax = 0.4 V

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
39	H S/S OUT	—		H sync separation pulse output. A positive polarity pulse is output from this pin. High level: 4.6 V Low level: 0 V
40	H SYNC	2.6 V		H sync separation input pin. Inputs a 2 Vp-p video signal via a capacitor and resistor.
41	V SYNC	3.4 V		V sync separation input pin. Inputs a 2 Vp-p video signal via a capacitor and resistor.
42	V BIAS	3.8 V		The V oscillator reference voltage is output from this pin.

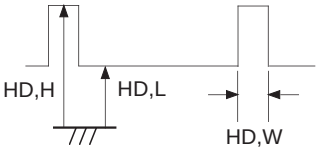
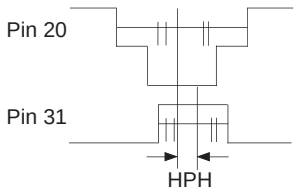
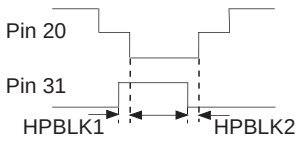
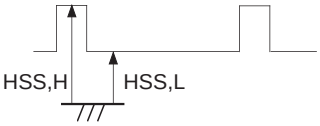
Electrical Characteristics

Setting conditions

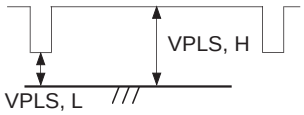
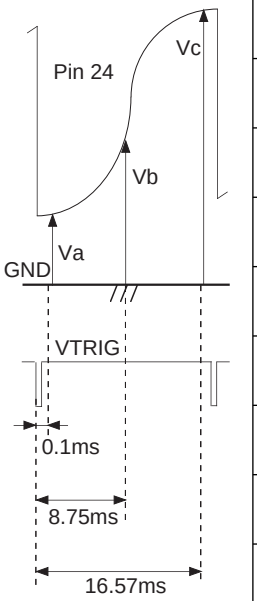
- Ta = 25 °C V_{CC} = 9 V
- I^2C bus register should be set to "I^2C Bus Register Initial Settings".

No.	Item	Symbol	Measurement conditions	Measurement pin	Measurement method	Min.	Typ.	Max.	Unit
1	Current consumption 1	ICC1		3	Measure the V_{CC} pin inflow current.	53	80	110	mA

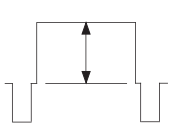
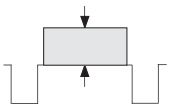
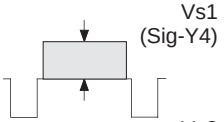
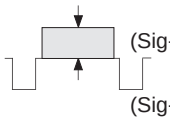
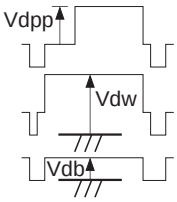
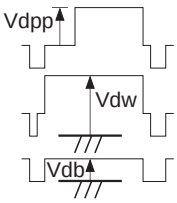
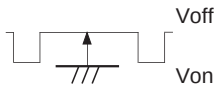
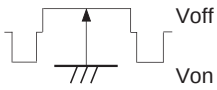
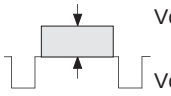
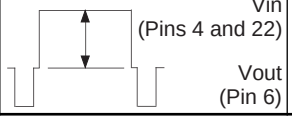
H system items

No.	Item	Symbol	Measurement conditions	Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
2	Horizontal free running frequency	Hfree		29			15.60	15.78	15.96	kHz
3	Horizontal sync pull-in range	ΔH	Video In: Sig-H2,H3 AFC: 0		Check that I2C register HLOCK is 1.		–400	—	400	µs
4	AFC gain 1	AFCmax	Video In: Sig-H6 AFC: 0 Video In: Sig-H7 AFC: 0	31	t1: Video In: Time from fall of Sig-H6 to rise of Pin 31. t2: Video In: Time from fall of Sig-H7 to rise of Pin 31.	AFCmax=t1-t2	0.12	0.3	0.48	µs
5	AFC gain 2	AFCcen	Video In: Sig-H6 AFC: 1 Video In: Sig-H7 AFC: 1	31		AFCcen=t1-t2	—	0.5	—	µs
6	AFC gain 3	AFCmin	Video In: Sig-H6 AFC: 2 Video In: Sig-H7 AFC: 2	31		AFCmin=t1-t2	0.75	1.2	1.75	µs
7	HD output pulse width	HD, W	Video In: Sig-H1	29			24	26	28	µs
8	HD output high level	HD, H	Video In: Sig-H1				8.7	9	—	V
9	HD output low level	HD, L	Video In: Sig-H1				0.5	0.8	1.1	V
10	Horizontal phase operating range 1	HPHmax	Video In: Sig-Y11 HPHASE: F	20 31			–4.3	–3.3	–2.3	µs
11	Horizontal phase operating range 2	HPHcen	Video In: Sig-Y11 HPHASE: 7				–1.5	–0.5	0.5	µs
12	Horizontal phase operating range 3	HPHmin	Video In: Sig-Y11 HPHASE: 0				1.3	2.3	3.3	µs
13	HP blanking delay time 1	HPBLK1	Video In: Sig-Y11	20 31			—	100	—	ns
14	HP blanking delay time 2	HPBLK2					—	100	—	ns
15	HSS OUT high level	HSS, H		39			4	4.6	5	V
16	HSS OUT low level	HSS, L					0	0.1	0.5	V
17	Overvoltage protection circuit VHT	XVTH		30	Check that HD appears at 2.4 V and disappears at 2.8 V.		2.4	2.6	2.8	V

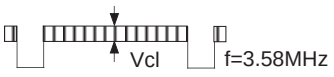
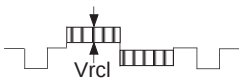
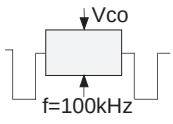
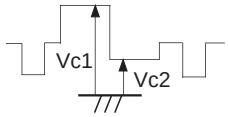
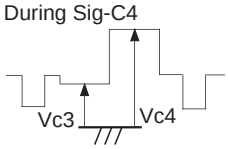
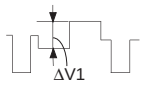
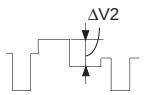
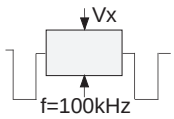
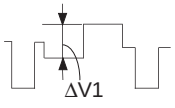
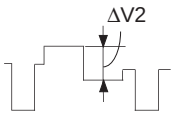
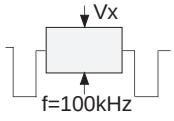
V system items

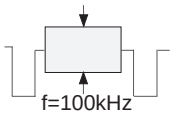
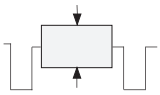
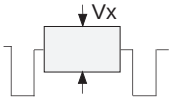
No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
18	VBias	V_{Bias}			42	Measure the pin voltage.			3.8		V
19	V PLS high level	VPLS, H	Video In: Sig-V1		28			4	4.5	5	V
20	V PLS low level	VPLS, L						0	0.1	0.5	V
21	VD output center voltage	VDcen	V SHIFT: F	Video In: Sig-V1	24		Vb	2.75	2.9	3.05	V
22	V SHIFT variable range 1	VSHIFT–	V SHIFT: 0				Vb-VDcen	–140	–125	–115	mV
23	V SHIFT variable range 2	VSHIFT+	V SHIFT: 1F				Vb-VDcen	110	120	140	mV
24	V SIZE variable range 1	VSIZE–	V SIZE: 0				Vc-Va	0.9	1.1	1.2	V
25	V SIZE variable range 2	VSIZE+	V SIZE: 3F				Vc-Va	1.5	1.65	1.8	V
26	S CORR variable range 1		S CORR: 0				Vsa=Va Vsc=Vc	45	65	85	mV
		Δ Sa	S CORR: F				Va-Vsa				
27	S CORR variable range 2	Δ Sc					Vc-Vsc	–55	–35	–15	mV
28	V LIN variable range 1		V LIN: 0				Vla=Va Vlc=Vc	90	120	140	mV
		Δ La	V LIN: F				Va-Vla				
29	V LIN variable range 2	Δ Lc					Vc-Vlc	60	90	110	mV
30	V zooming 1		HV COMP: 0, Pin 23: 6 V				Vsmin= Vc-Va	0	3	15	mV
			HV COMP: 7, Pin 23: 6 V				Vsmax= Vc-Va				
		ΔVZ1	HV COMP: 0, Pin 23: 0 V				Vsmin- (Vc-Va)				
31	V zooming 2	ΔVZ2	HV COMP: 7, Pin 23: 0 V				Vsmax- (Vc-Va)	60	80	100	mV

Y system items

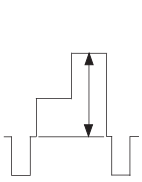
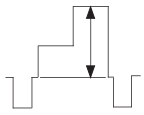
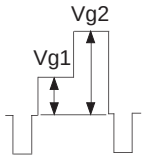
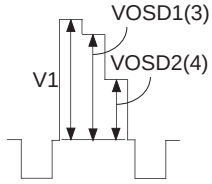
No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
32	R output level	VR	Video In: Sig-Y1		16			—	2.5	—	V
33	Sub-contrast variable range 1	Gsc, max	SUBCONT: F	Video In: Sig-Y1			$20\log \frac{Vsc1}{VR}$	2.2	2.7	3.2	dB
34	Sub-contrast variable range 2	Gsc, min	SUBCONT: 0				$20\log \frac{Vsc2}{VR}$	–3.8	–33	–2.8	dB
35	Trap attenuation	ATTtrap	TRAP SW: 0 TRAP SW: 1	Video In: Sig-Y2	16		$20\log \frac{Vtr2}{Vtr1}$	—	–30	–20	dB
36	Sharpness characteristics 1	Gsh, max	SHARP NESS: F	Video In: Sig-Y4	16		$20\log \frac{Vs2}{Vs1}$	5.5	7.0	8.5	dB
37	Sharpness characteristics 2	Gsh, cen	SHARP NESS: 7					1.5	2.5	4.5	dB
38	Sharpness characteristics 3	Gsh, min	SHARP NESS: 0	Video In: Sig-Y5				–7.5	–5.5	–4.5	dB
39	RGB output frequency response	Gfreq	Video In: Sig- Y4, Y6		16 18 20		$20\log \frac{Vf2}{Vf1}$	–6	–3.5	0	dB
40	DC transmission rate 1	Gdt1	DC TRAN: 0	Video In: Sig-Y3 Video In: Sig-Y1 Video In: Sig-H1	16		$\frac{Vdw-Vdb}{Vdpp}$	96	99	100	%
41	DC transmission rate 2	Gdt2	DC TRAN: 7	Video In: Sig-Y3 Video In: Sig-Y1 Video In: Sig-H1			$\frac{Vdw-Vdb}{Vdpp}$	73	78	85	%
42	Auto pedestal operation 1	Vdp1	Pin 8: 3 V Pin 8: 5 V	Video In: Sig-H1	16		Voff-Von	280	340	400	mV
43	Auto pedestal operation 2	Vdp2	Pin 8: 3 V Pin 8: OPEN	Video In: Sig-Y10	16		Voff-Von	120	170	220	mV
44	NR operation	Gnr	NR: 1 NR: 0	Video In: Sig-Y7	16		$20\log \frac{Von}{Voff}$	–5.5	–4	–2.5	dB
45	SW gain 1	Gsw1	SW GAIN: 1	Video In: Sig-Y1	4, 22 6		$20\log \frac{Vout}{Vin}$	5.5	6	6.5	dB
46	SW gain 2	Gsw2	SW GAIN: 0					–0.5	0	0.5	dB

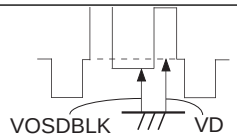
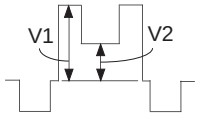
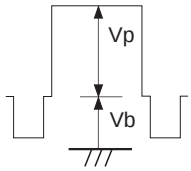
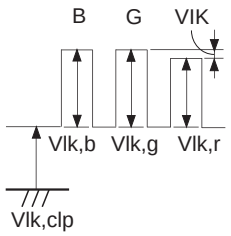
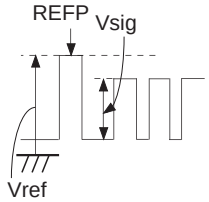
C system items

No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
47	APC pull-in range 1	Δ f, apc1	Video-In: Sig-H1 C In: Sig-C1, C2		20	Check that the burst frequency is changed to 3579545 ±400 Hz and pulled in.		–400	—	400	Hz
48	Carrier leak	Vcl	Video-In: Sig-H1 COLOR: 3F SUBCOLOR: F		20			—	—	50	mV
49	Residual carrier level	Vrcl	Video-In: Sig-H1 C In: Sig-C3 COLOR: 3F SUBCOLOR: F			 3.58 MHz component and 7.16 MHz component		—	—	200	mV
50	Color output level	Vco, cen		Video In : Sig-H1, C In :Sig-C5	20		Vco0	0.6	0.9	1.2	V
51	Color variable range 1	Gco, max	COLOR: 3F				$20\log\frac{Vco1}{Vco0}$	5.4	6.0	6.6	dB
52	Color variable range 2	Gco, min	COLOR: 0				$20\log\frac{Vco2}{Vco0}$	—	–50	–40	dB
53	Sub-color variable range 1	Gsc, max	SUB COLOR : F				$20\log\frac{Vsc1}{Vco0}$	2.1	2.7	3.3	dB
54	Sub-color variable range 2	Gcs, min	SUB COLOR : 0				$20\log\frac{Vsc2}{Vco0}$	–5.4	–3.7	–2.0	dB
55	Hue variable range 1	ø cen		Video In: Sig-H1, C In : Sig-C3, -C4	20	During Sig-C3  During Sig-C4 		–10	0	10	deg
56	Hue variable range 2	ø max	HUE: 3F				$\tan^{-1}\frac{Vc1-Vc2}{Vc4-Vc3}$	–56	–46	–36	deg
57	Hue variable range 3	ø min	HUE: 0					20	30	40	deg
58	Sub-hue variable range 1	ø s, max	SUB HUE: F					–24	–18	–12	deg
59	Sub-hue variable range 2	ø s, min	SUB HUE:0					7	13	19	deg
60	Detective axis R1	ø r1	AXIS: 0	Video In : Sig-H1, C In : Sig-C4 -C3	16		$90° + \tan^{-1}\frac{Vr2}{Vr1}$	89	96	103	deg
61	Detective axis G1	ø g1			18		$270° - \tan^{-1}\frac{Vg2}{Vg1}$	233	240	247	deg
62	Detective output ratio R1	Gr1	AXIS: 0	Video In :Sig-H1, C In : Sig-C5	16		$\frac{Vx}{Gcomax}\frac{VBW}{VRW}$	0.7	0.8	0.9	—
63	Detective output ratio G1	Gg1			18	Vgg	$\frac{Vx}{Gcomax}\frac{VBW}{VGW}$	0.26	0.3	0.34	—
64	Detective axis R2	ø r2	AXIS: 1	Video In :Sig-H1, C In : Sig-C4, -C3	16		$90° + \tan^{-1}\frac{Vr2}{Vr1}$	105	112	119	deg
65	Detective axis G2	ø g2			18		$270° - \tan^{-1}\frac{Vg2}{Vg1}$	245	252	259	deg
66	Detective output ratio R2	Gr2	AXIS: 1	Video In :Sig-H1, C In : Sig-C5	16		$\frac{Vx}{Gcomax}\frac{VBW}{VRW}$	0.7	0.8	0.9	—
67	Detective output ratio G2	Gg2			18	Vgg	$\frac{Vx}{Gcomax}\frac{VBW}{VGW}$	0.26	0.3	0.34	—

No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
68	ACC characteristics 1	Gacc1	Video In: Sig-H1	C In: Sig-C6	20		$20\log\frac{Vacl}{Vco0}$	–1.0	0.1	1.0	dB
69	ACC characteristics 2	Gacc2		C In: Sig-C7			$20\log\frac{Vac2}{Vco0}$	–3	–1	0	dB
70	Killer point	KP	Video In: Sig-H1 C In:Sig-C8, -C9		20		Check that output disappears at -38 dB and appears at -30 dB.	–38	–34	–30	dB
71	Chroma frequency response 1-1	Gcf1–	TOT SW: 1	C In: Sig-C5 -C11	20		$20\log\frac{Vx}{Vref}$ Vref= Vx (Sig-C5)	—	–3	—	dB
72	Chroma frequency response 1-2	Gcf1+	VIdeo-In: Sig-H1	C In: Sig-C10				—	–1	—	dB
73	Chroma frequency response 2-1	Gcf2–	TOT SW: 0	C In: Sig-C5 -C11				–2.3	—	0.2	dB
74	Chroma frequency response 2-2	Gcf2+	VIdeo-In: Sig-H1	C In: Sig-C10				–2.7	—	0.2	dB

RGB system items

No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
75	Drive variable range 1	Gdr1	G DRIVE : 1F B DRIVE : 1F	Video In : Sig-H1, Y In : Sig-R1	16, 18 20		$20\log\frac{Vdr1}{Vr0}$	0.7	1.5	2.2	dB
76	Drive variable range 2	Gdr2	G DRIVE : 0 B DRIVE : 0		18 20		$20\log\frac{Vdr2}{Vr0}$	–5.2	–4.5	–3.3	dB
77	Picture variable range	Gpic	PICTURE : 0		16 18 20		$20\log\frac{Vr1}{Vr0}$	–15.7	–14.7	–13.7	dB
78	Dynamic color operation R	Gdy, r	DY COL : 0	Video In : Sig-H1	16		$\frac{Vdyr}{Vr0}\times 100$	94.5	97	98.5	%
79	Dynamic color operation B	Gdy, b		Y In : Sig-R1	20		$\frac{Vdyb}{Vb0}\times 100$	104	106	108	%
80	Gamma characteristics 1 (50 IRE)	GAM1	GAMMA : 0/7	Video In : Sig-H1, Y In : Sig-R1	16 18 20		$\frac{Vg1\ (GAMMA: 7) - Vg1\ (GAMMA: 0)}{Vg2\ (GAMMA: 0)}$	10	18	26	IRE
81	Gamma characteristics 2 (100 IRE)	GAM2					$\frac{Vg2\ (GAMMA: 7) - Vg2\ (GAMMA: 0)}{Vg2\ (GAMMA: 0)}$	–8	0	8	IRE
82	OSD level 1	Vosd1	OSD : 0	Video In : Sig-Y1 OSD BLK : Sig-R3	16 18 20		$\frac{VOSD}{V1}\times 100$ V1=100IRE	55	65	75	IRE
83	OSD level 2	Vosd2						23	33	43	IRE
84	OSD level 3	Vosd3	OSD : 1					82	92	102	IRE
85	OSD level 4	Vosd4						36	46	56	IRE

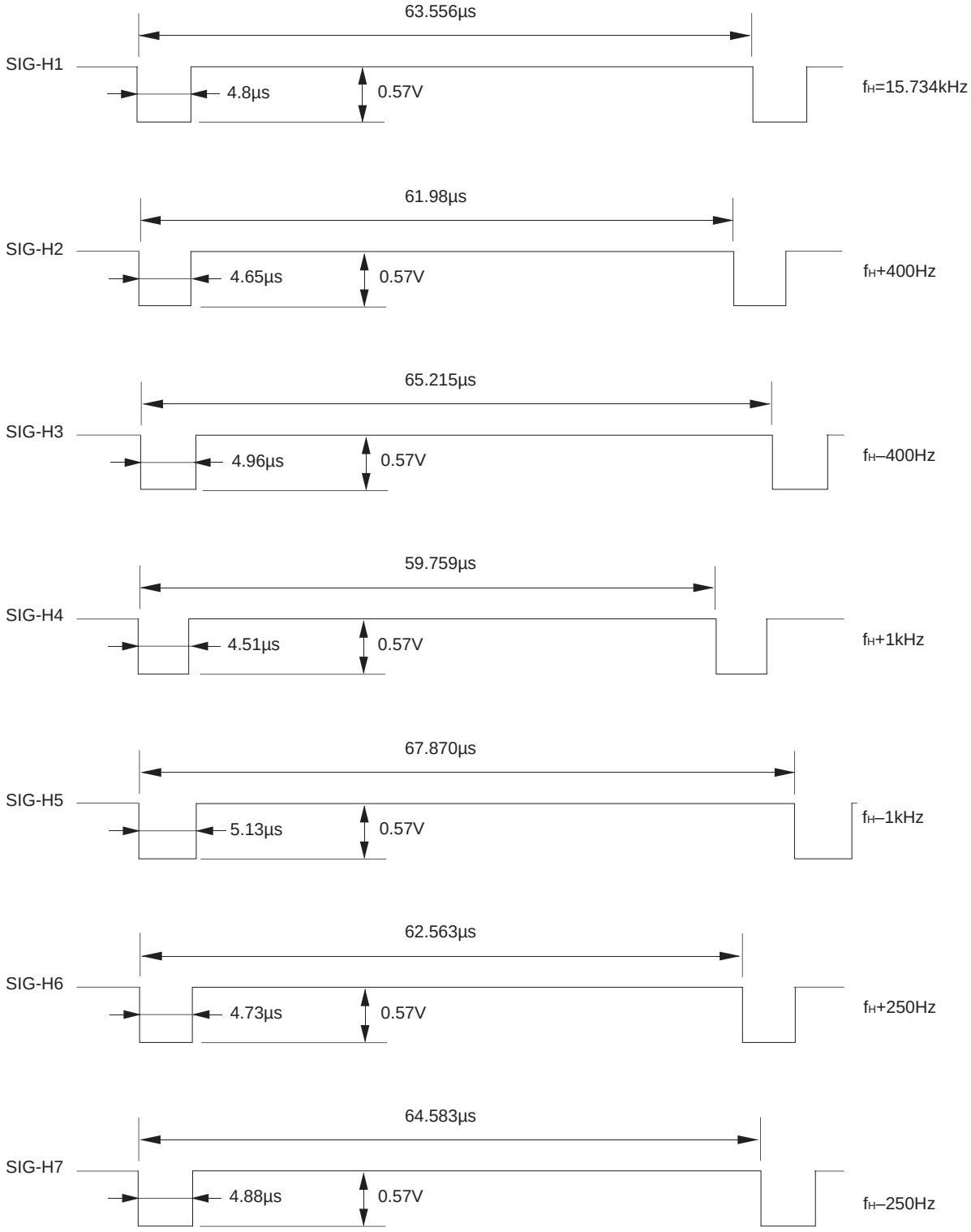
No.	Item	Symbol	Measurement conditions		Measurement pin	Measurement method		Min.	Typ.	Max.	Unit
86	OSD BLK black variation	Δ Vosd	OSD BLK: Sig-R2 (5V)	Video In: Sig-Y1	16 18 20		VD– VOSDBLK	–150	190	410	mV
87	OSD BLK attenuation	Gosd	OSD BLK: Sig-R2 (3V)	Video In: Sig-Y1	16 18 20		$20\log \frac{V2}{V1}$	–7	–6	–5	dB
88	ABL threshold	Vth, abl	Video In: Sig-Y1		16	Vary the voltage applied to Pin 23 and measure the voltage at which picture ABL operates.		1.1	1.2	1.3	V
89	ABL gain 1	Gabl1	ABL: 3	Video In: Sig-Y1	16		$20\log \frac{Vp, 5V}{Vp, 9V}$	–3.4	–2.4	–1.4	dB
90	ABL black level 1	Vabl1					Vb, 5V- Vb, 9V	100	200	300	mV
91	ABL gain 2	Gabl2	ABL: 0	Pin 25: 9 V/5 V			$20\log \frac{Vp, 5V}{Vp, 9V}$	–8.8	–6.8	–4.8	dB
92	ABL black level 2	Vabl2					Vb, 5V- Vb, 9V	–100	0	100	mV
93	Blanking level	Vblk	Video In: Sig-Y1		16, 18, 20	Measure the R, G and B blanking levels.		0	0.2	0.4	V
94	Ik clamp level	Vlk, clp		Video In: Sig-V1	21			1.25	1.35	1.45	V
95	Ik R level	Vlk, r						0.76	0.86	0.96	V
96	Ik variable range 1	Vlk, max	G CUTOFF: F B CUTOFF: F				Vlkg, b-Vlk, r	0.2	0.35	0.4	V
97	Ik variable range 2	Vlk, min	G CUTOFF: 0 B CUTOFF: 0					–0.64	–0.54	–0.44	V
98	RGB output DC range 1	Vref, max	Vsh: 4.6V (Pins 15, 17 and 19)	Video In: Sig-V1	16 18 20		Vref	3.2	3.5	4.0	V
99	RGB output DC range 2	Vref, min	Vsh: 8V (Pins 15, 17 and 19)					0.45	0.85	1.25	V
100	Bright center -R	Vbcen, r	BRIGHT: 1F		16		Vsig-Vref	–0.5	–0.4	–0.3	V
101	Bright center -G, B	Vbcen, gb			18 20			–0.46	–0.36	–0.26	V
102	Bright variable range 1-R	Vbrt1, r	BRIGHT: 3F		16		Vsig (BRIGHT: 1F) –Vsig	0.3	0.35	0.4	V
103	Bright variable range 1-G, B	Vbrt1, gb			18 20			0.27	0.32	0.37	V
104	Bright variable range 2-R	Vbrt2, r	BRIGHT: 0		16			–0.38	–0.33	–0.28	V
105	Bright variable range 2-G, B	Vbrt2, bg			18 20			–0.36	–0.31	–0.26	V
106	Sub-bright variable range 1-R	Vsbrt1, r	SUB BRIGHT: 3F		16			0.3	0.35	0.4	V
107	Sub-bright variable range 1-G, B	Vsbrt1, gb			18 20			0.27	0.32	0.37	V
108	Sub-bright variable range 2-R	Vsbrt2, r	SUB BRIGHT: 0		16			–0.38	–0.33	–0.28	V
109	Sub-bright variable range 2-G, B	Vsbrt2, gb			18 20			–0.36	–0.34	–0.26	V

I²C bus system items

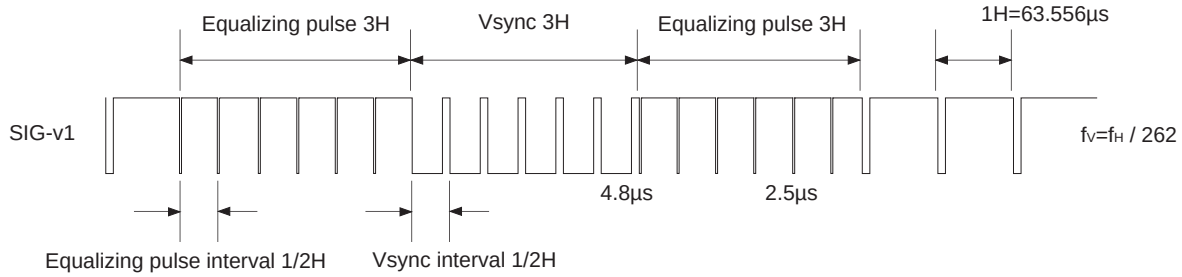
No.	Item	Symbol	Min.	Typ.	Max.	Unit
110	High level input voltage	Vih	3.0	—	5.0	V
111	Low level input voltage	Vil	0	—	1.5	V
112	High level input current	Iih	—	—	10	µA
113	Low level input current	Iil	—	—	10	µA
114	Low level output voltage During current inflow of 3 mA to SDA (Pin 38)	Vol	0	—	0.4	V
115	SDA inflow current	Iol	3	—	—	mA
116	Input capacitance	Ci	—	—	10	pF
117	SCL clock frequency	fscl	0	—	100	kHz
118	Time the bus must be free before a new transmission can start	tbuf	4.7	—	—	µs
119	Hold time start condition	thd;sta	4.0	—	—	µs
120	The Low period of the clock	tlow	4.7	—	—	µs
121	The High period of the clock	thigh	4.0	—	—	µs
122	Set up time for start condition	tsu;sta	4.7	—	—	µs
123	Hold time data	thd;dat	5	—	—	µs
124	Set-up time data	tsu;dat	250	—	—	ns
125	Rise time of both SDA and SCL lines	tr	—	—	300	ns
126	Fall time of both SDA and SCL lines	tf	—	—	300	ns
127	Set-up time for stop condition	tsu;sto	4.7	—	—	µs

Signals Used for Measurements

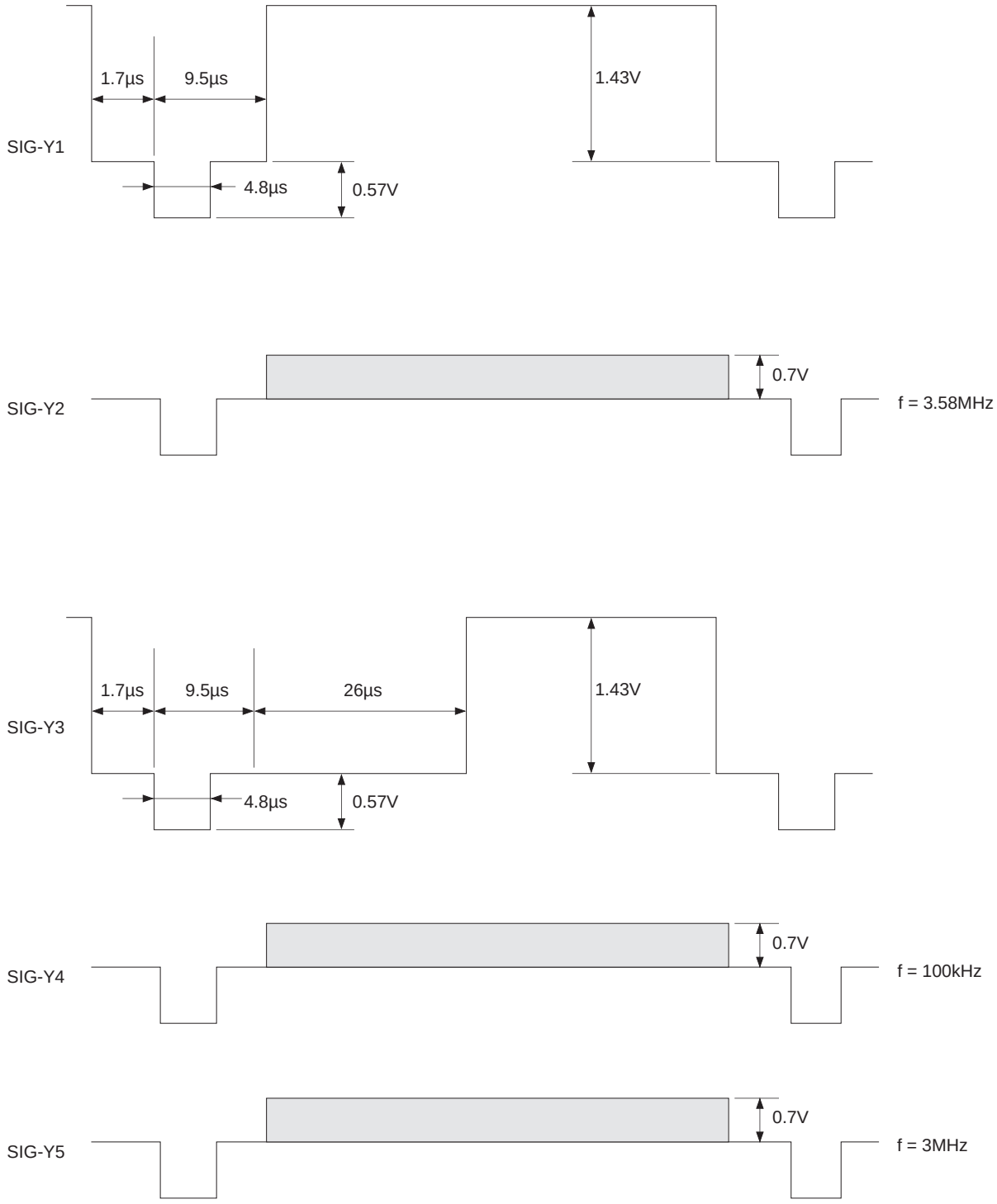
H system

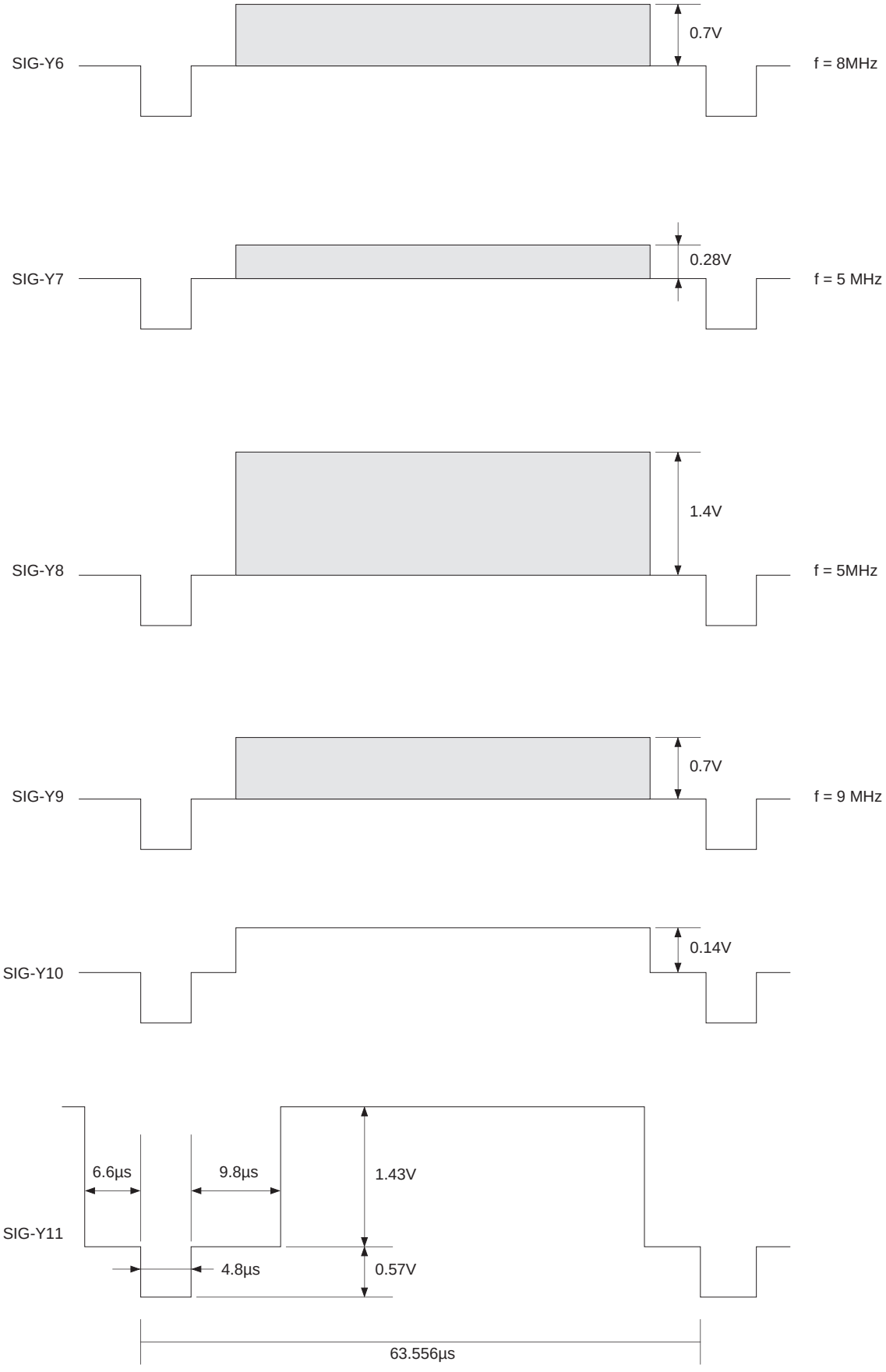


V system

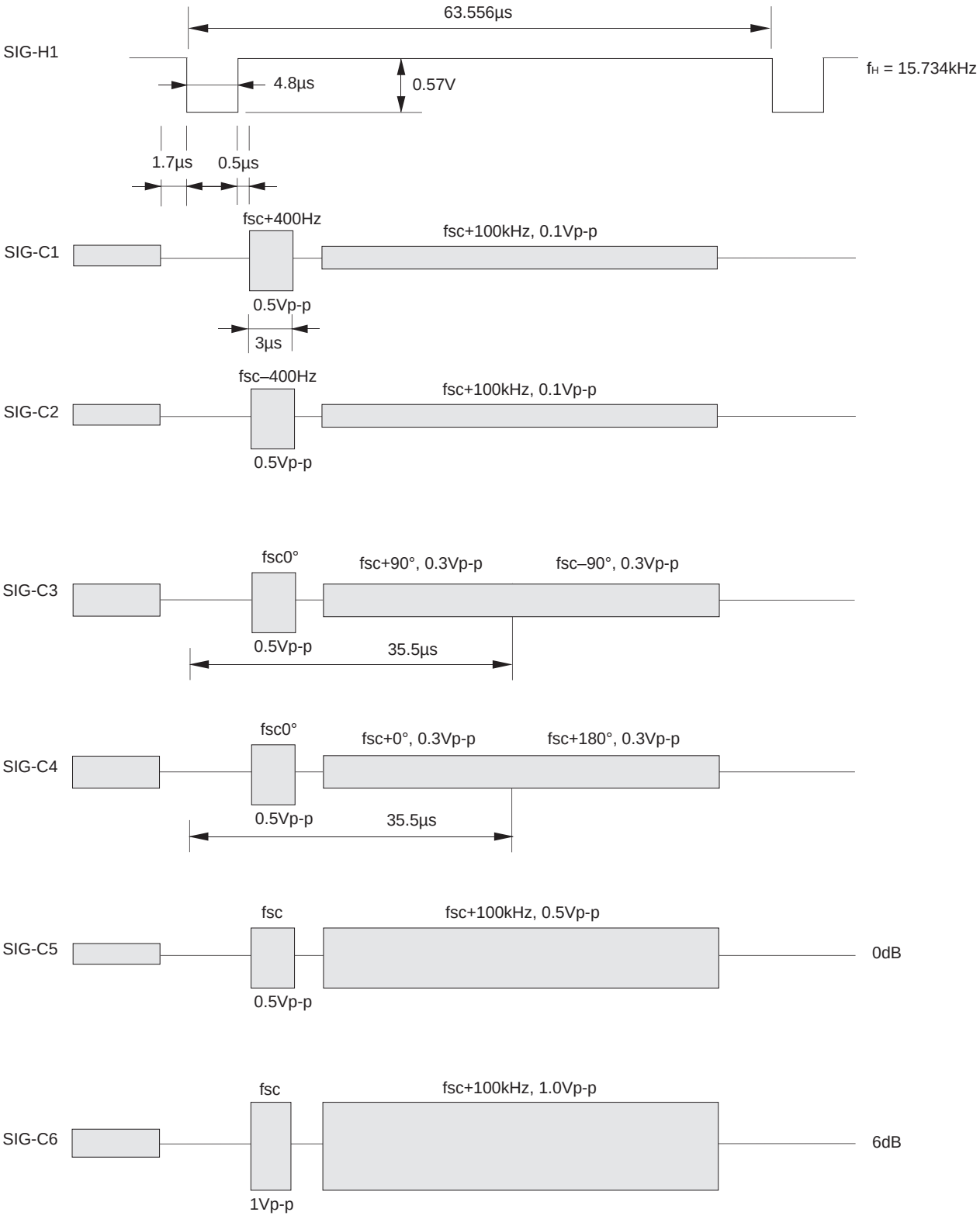

Equalizing pulse 3H
Vsync 3H
Equalizing pulse 3H
1H=63.556µs
SIG-v1
fV=fH / 262
4.8µs
2.5µs
Equalizing pulse interval 1/2H
Vsync interval 1/2H

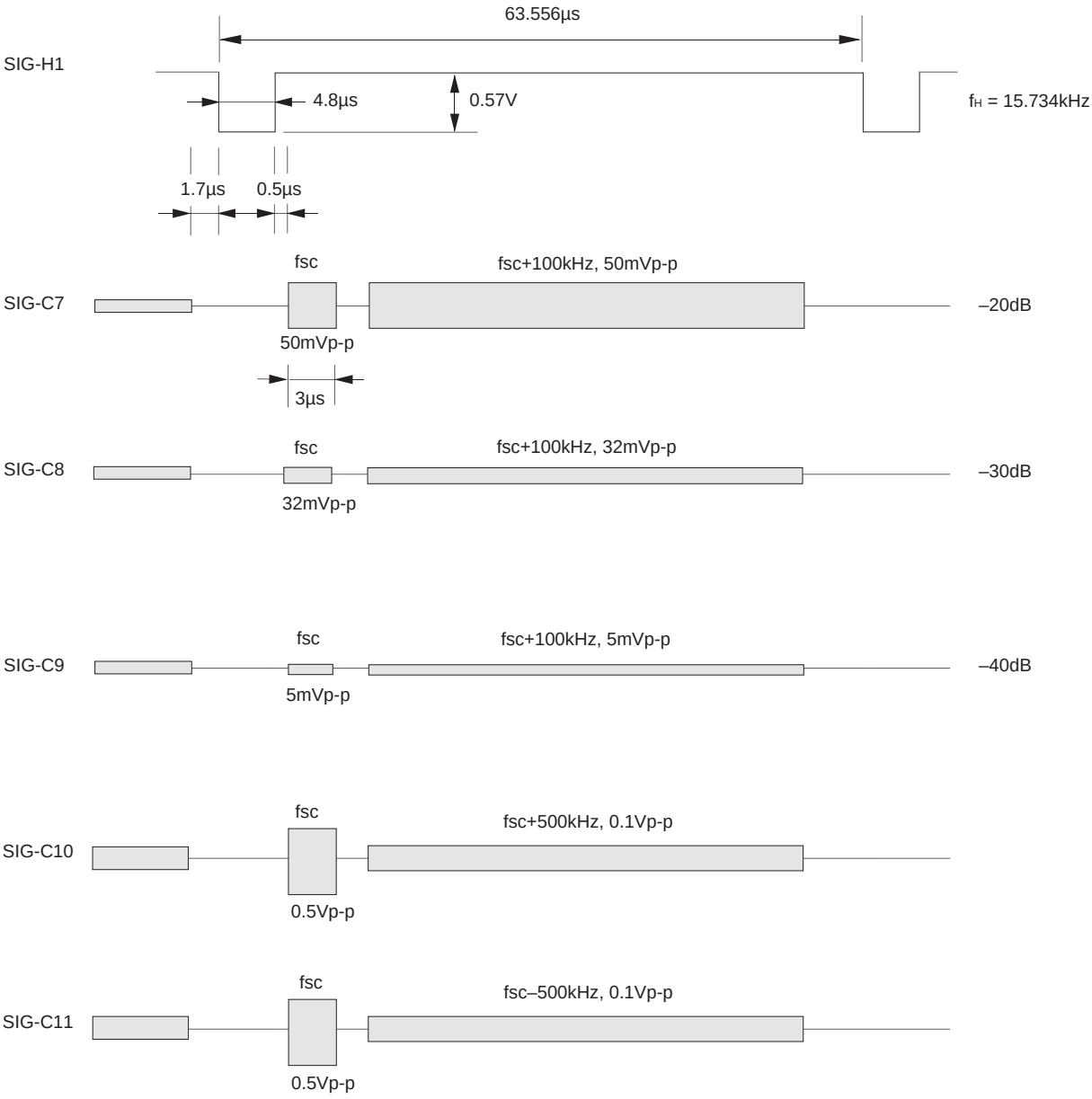
Y system


1.7µs
9.5µs
1.43V
SIG-Y1
4.8µs
0.57V
0.7V
SIG-Y2
f = 3.58MHz
1.7µs
9.5µs
26µs
1.43V
SIG-Y3
4.8µs
0.57V
0.7V
SIG-Y4
f = 100kHz
0.7V
SIG-Y5
f = 3MHz

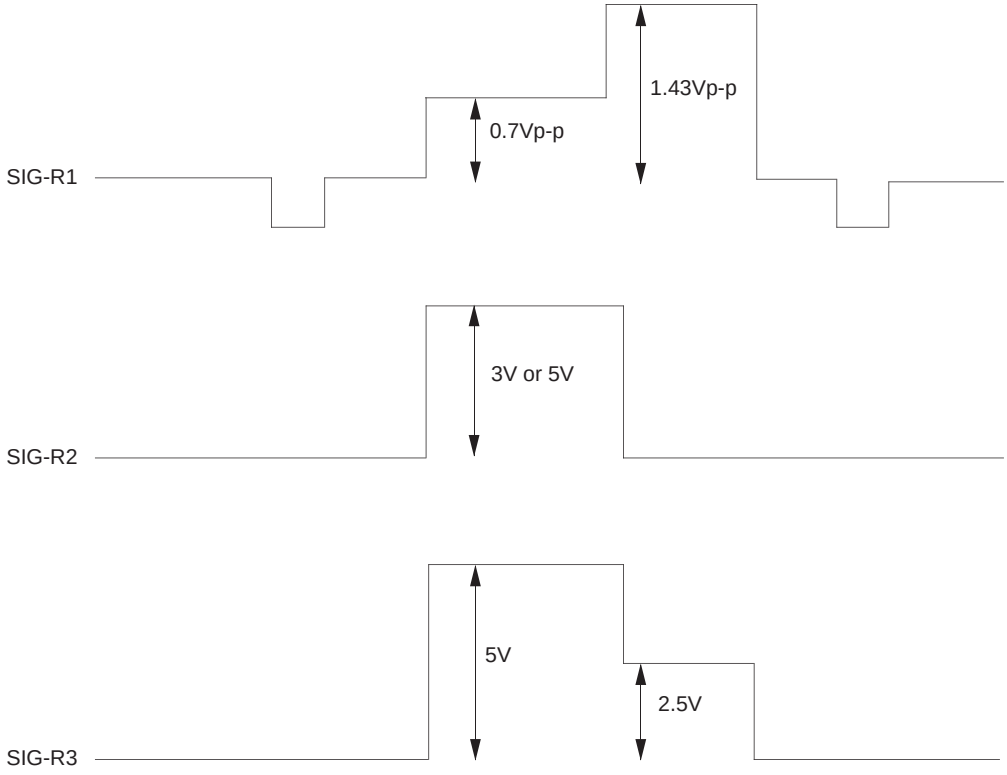

SIG-Y6
0.7V
f = 8MHz
SIG-Y7
0.28V
f = 5 MHz
SIG-Y8
1.4V
f = 5MHz
SIG-Y9
0.7V
f = 9 MHz
SIG-Y10
0.14V
SIG-Y11
6.6µs
9.8µs
1.43V
4.8µs
0.57V
63.556µs

C system


63.556µs
SIG-H1
fH = 15.734kHz
4.8µs
0.57V
1.7µs
0.5µs
fsc+400Hz
fsc+100kHz, 0.1Vp-p
SIG-C1
0.5Vp-p
3µs
fsc–400Hz
fsc+100kHz, 0.1Vp-p
SIG-C2
0.5Vp-p
fsc0°
fsc+90°, 0.3Vp-p
fsc–90°, 0.3Vp-p
SIG-C3
0.5Vp-p
35.5µs
fsc0°
fsc+0°, 0.3Vp-p
fsc+180°, 0.3Vp-p
SIG-C4
0.5Vp-p
35.5µs
fsc
fsc+100kHz, 0.5Vp-p
SIG-C5
0dB
0.5Vp-p
fsc
fsc+100kHz, 1.0Vp-p
SIG-C6
6dB
1Vp-p


63.556µs
SIG-H1
4.8µs
0.57V
fH = 15.734kHz
1.7µs
0.5µs
fsc
fsc+100kHz, 50mVp-p
SIG-C7
–20dB
50mVp-p
3µs
fsc
fsc+100kHz, 32mVp-p
SIG-C8
–30dB
32mVp-p
fsc
fsc+100kHz, 5mVp-p
SIG-C9
–40dB
5mVp-p
fsc
fsc+500kHz, 0.1Vp-p
SIG-C10
0.5Vp-p
fsc
fsc–500kHz, 0.1Vp-p
SIG-C11
0.5Vp-p

RGB system



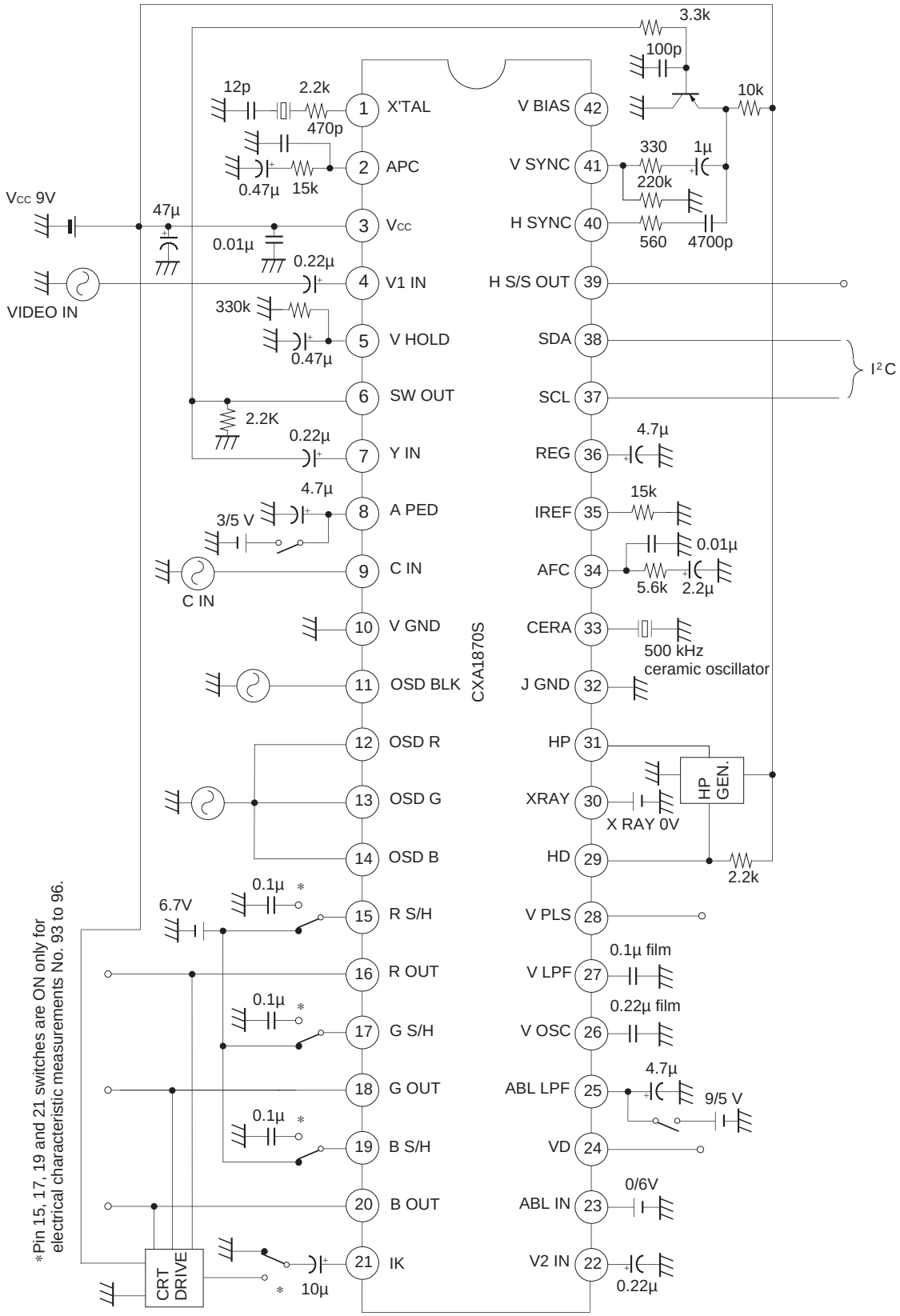
Measurement Method

I²C Bus Register Initial Settings

Register name	No. of bits	Initial setting	Description
PICTURE	6	3F$_H$	Maximum value
RGB LIM	2	3$_H$	Maximum value
HUE	6	1F$_H$	Center point
IN SW	1	0$_H$	V1 IN selected
COLOR	6	1F$_H$	Center point
SW GAIN	1	0$_H$	0 dB gain
BRIGHT	6	1F$_H$	Center point
NR ON	1	0$_H$	NR OFF
SHARPNESS	4	7$_H$	Center point
SUB CONT	4	7$_H$	Center point
SUB HUE	4	7$_H$	Center point
SUB COLOR	4	7$_H$	Center point
SUB BRIGHT	6	1F$_H$	Center point
TRAP ON	1	0$_H$	TRAP OFF
TOT ON	1	0$_H$	TOT OFF
PIX ON	1	1$_H$	Picture mute OFF
R ON	1	1$_H$	R output ON
G ON	1	1$_H$	G output ON
B ON	1	1$_H$	B output ON
PRE OVER	3	0$_H$	Minimum value
AXIS	1	0$_H$	JAPAN detective axis

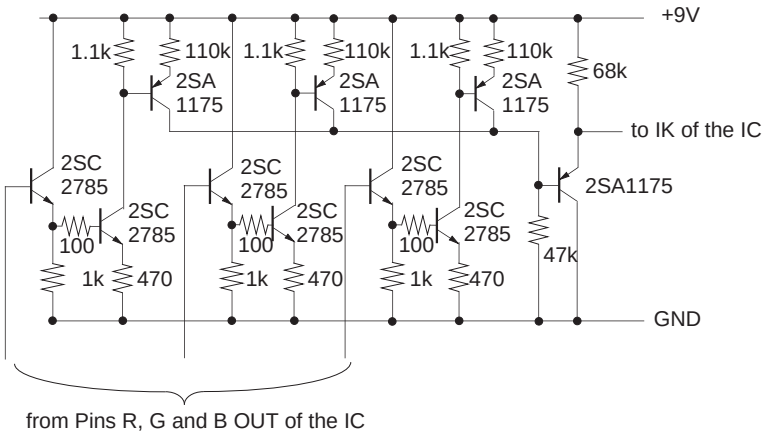
Register name	No. of bits	Initial setting	Description
BLACK	1	0$_H$	BLACK OFF
DYCOL OFF	1	1$_H$	DY COL OFF
REF	2	1$_H$	Center point
ABL	2	0$_H$	Minimum value
BLUE	1	0$_H$	BLUE OFF
OSD	1	0$_H$	Luminance level small
G DRIVE	5	F$_H$	Center point
DC TRAN	3	0$_H$	Minimum value
B DRIVE	5	F$_H$	Center point
GAMMA	3	0$_H$	Correction OFF
G CUTOFF	4	7$_H$	Center point
B CUTOFF	4	7$_H$	Center point
H PHASE	4	7$_H$	Center point
V ON	1	1$_H$	VD output ON
V EX OFF	1	1$_H$	V sync elongation OFF
AFC	2	1$_H$	Center point
V SHIFT	5	F$_H$	Center point
HV COMP	3	3$_H$	Center point
V SIZE	6	1F$_H$	Center point
C MODE	1	0$_H$	Countdown ON
V LIN	4	7$_H$	Center point
SCORR	4	7$_H$	Center point

Electrical Characteristics Measurement Circuit

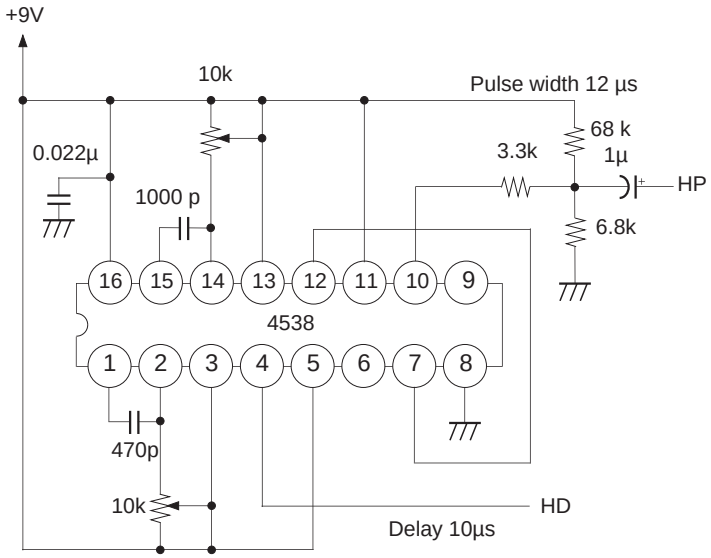


Reference Circuit

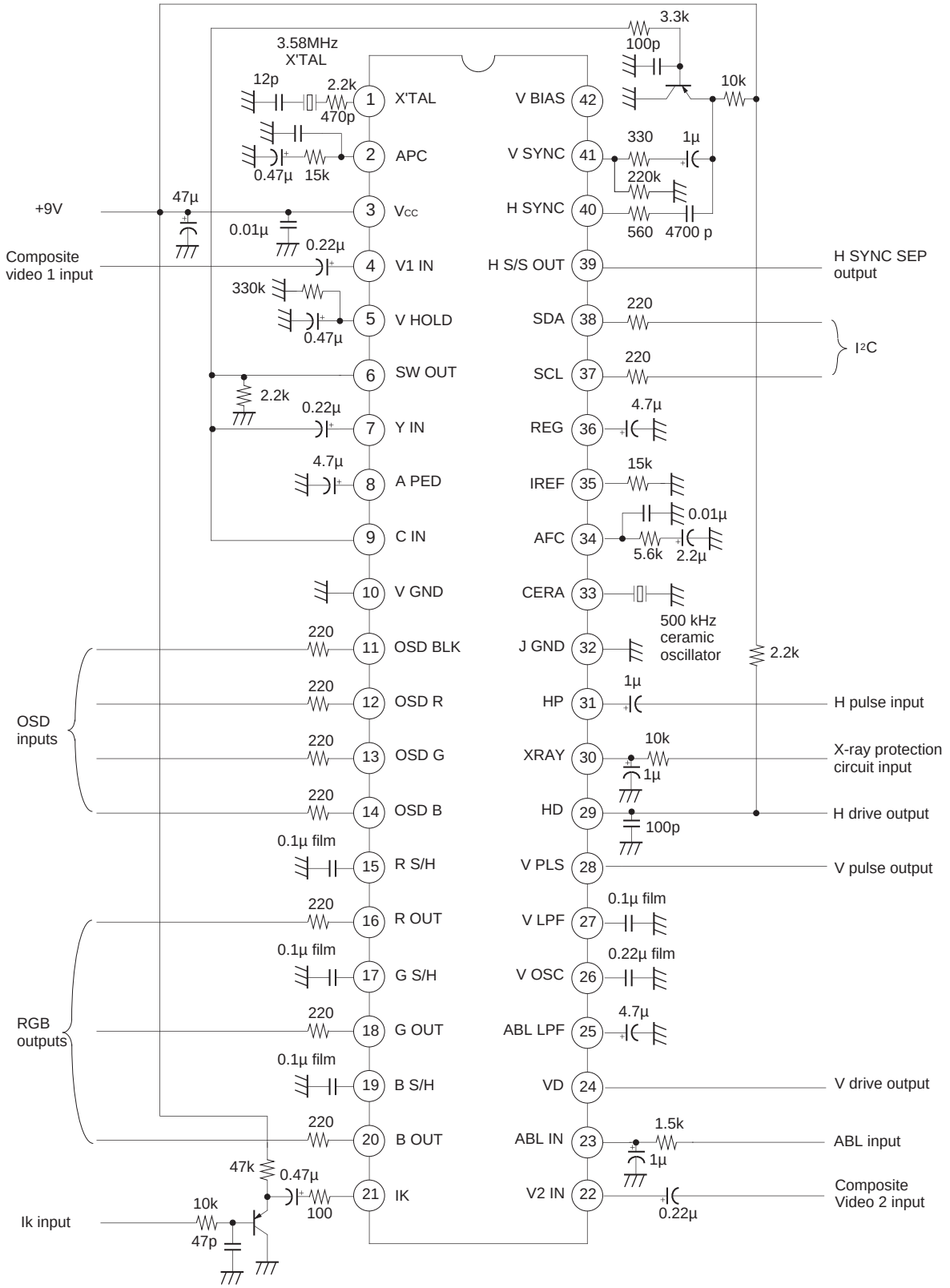
CRT Drive Circuit



HP Gen



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Synchronizing and picture distortion correction systems

The video signals (2 Vp-p standard) input to Pins 40 and 41 are led to the horizontal and vertical sync separation circuits for sync separation. The horizontal sync signal is output from Pin 39 with positive polarity.

This horizontal sync signal is compared with the signal obtained by 1/32 frequency dividing the 32 fH VCO output using the ceramic oscillator (frequency: 503.5 kHz) to detect a phase difference. The error voltage resulting from the phase difference is applied to the H oscillator after attenuating the medium and high frequency components by a lag-lead filter. The phase of the H oscillator output is compared and shifted to match the phase of the H deflection pulse (flyback pulse) input from Pin 31, and then output from Pin 29.

After the vertical sync signal is synchronized to the input signal by the V countdown system, a sawtooth wave is generated by charging and discharging the capacitor attached externally to Pin 26. AGC is performed to ensure that the amplitude of the sawtooth wave is maintained constant regardless of the vertical frequency of the input, after which the sawtooth wave passes through the picture distortion correction circuit and is output from Pin 24.

Note that there is no need to adjust the free running frequency for either the H or V oscillator.

When voltage of 3 V or more is applied to Pin 30, the H drive output is held at low level. A time constant circuit is included to protect against overvoltages, and H drive is output normally when high voltage input continues for less than 7 V cycles. To release holddown, the IC must be turned off and then started up again.

Note)

When the external capacitance at Pin 27 is used with 0.1 µF below of recommended value, VD output at Pin 24 may be unstable. When changing capacitance value, use it more than 0.047 µF.

2. Y/C system

The Y/C system has the following three input systems.

Composite video input (1 Vp-p/2 Vp-p) → 2 systems (The gain can be switched between 0 and 6 dB for both systems.)

Y/C separation input (2 Vp-p) → 1 system

The Y signal (specified input level 2 Vp-p) input to Pin 7 is passed through the sub-contrast control, chroma trap (or delay line), delay line, sharpness control, noise reduction, clamp and auto pedestal circuits. The signal is then mixed with the color difference signal, passed through the clamp and Y/C MIX circuits again, and input to the RGB interface system block.

Since a built-in chroma trap is provided, the video signal can be directly input. Trap frequency adjustment is not necessary as a dummy filter is provided inside the IC and feedback is applied using the 3.58 MHz signal generated by a crystal oscillator for reference. When the chroma trap is off, the Y system frequency response is approximately 8 MHz, –3 dB for R, G and B outputs.

Sharpness control is delay line type with a variable PRE/OVER ratio.

Dynamic picture control consists of pulling in the signal below 40 IRE to the black side so that the signal black peak held by Pin 8 becomes the pedestal level.

The chroma signal (specified input level, burst 570 mVp-p, or video signal 2 Vp-p) input to Pin 9 is passed through the ACC, TOT, color control (saturation control) and killer detection circuits, after which the burst locked VCO oscillation output is detected as the carrier. (The detective output LPF is a quadruple.)

The signal is then separated into color difference signals R-Y, B-Y and G-Y by the matrix circuit, passed through the Y/C MIX circuit, and input together with the Y signal to the RGB interface system block.
The detective axis (Japan/US) can be switched by the I²C bus register.

3. RGB interface system

YS/YM switching is performed according to the amplitude of the OSD RGB input blanking signal input from Pin 11.

0 to 1.5 V → TV (Y/C input)
1.5 to 3.5 V → TV –6 dB
3.5 to 5.5 V → Black

The R, G and B signals of the Y/C system pass through the RGB switch (BLUE and BLACK ON/OFF) and receive picture control. These signals are mixed with the digital R, G and B signals (specified input level 0 to 5 V DC) input from Pins 12, 13 and 14, passed through the dynamic color, gamma correction, bright control, drive adjustment (R channel is fixed, G and B channels are variable.), cut-off adjustment (R channel is fixed, G and B channels are variable.) and auto cut-off DC level shift circuits, and then output from Pins 16, 18 and 20 as the R, G and B signals. The RGB output amplitude has a limit voltage whose setting value can be controlled with the I²C bus register. The digital R, G and B signals are mainly used for on screen display of channels, etc. and the display level can be set with the I²C bus register.
The signal input to Pin 23 (ABL IN) is compared with the internal reference voltage and is then integrated by the capacitor connected to Pin 25 (ABL LPF) for picture and brightness control. Picture ABL mode and combined picture ABL and brightness ABL mode can be switched with the I²C bus register.

Note)

When the digital R, G and B signals and OSDBLK signal are not used, connect Pins 11, 12, 13 and 14 to GND.

Auto cut-off

For white balance, drive control (gain control between R, G and B outputs) and cut-off control (black side DC level control) are involved. This IC uses the I²C bus register for drive control. For cut-off control, a loop is formed between the IC and CRT to achieve auto cut-off control.
This auto cut-off arrangement makes it possible to compensate for CRT changes with time. To absorb the CRT variance, the cut-off voltages of the G and B outputs are adjusted by the I²C bus register.
The auto cut-off loop is configured as described below.

(1) R, G and B reference pulses for auto cut-off, shifted 1H each in the order mentioned, are added to the top of the picture.
(2) The IK of each of the R, G and B outputs is converted to a voltage and input to Pin 21.
(3) The voltage input to Pin 21 is compared with the reference voltage in the IC to change the DC level of the reference pulses.

The loop mentioned above determines the shift level of the R, G and B outputs and lets the capacitances connected to Pins 15, 17 and 19 hold the DC shift level during the 1 V period. If the voltage at any one of Pins 15, 17 or 19 is less than 4.2 V, the status register IK (bit 6) becomes “1”. Use this information to blank the R, G and B outputs with the I²C bus register. The positions of the reference pulses can be changed by the I²C bus register.

Definition of I²C Bus Registers

Slave addresses

88H: Slave receiver

89H: Slave transmitter

Register table

- All registers are set to 0 when the IC power is turned on.
- "X" indicates "don't care"; "∗" indicates undefined.

Control registers

Sub Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
XXXX0000	PICTURE						RGB LIM	
XXXX0001	HUE						∗	IN SW
XXXX0010	COLOR						∗	SW GAIN
XXXX0011	BRIGHT						∗	NR ON
XXXX0100	SHARPNESS				SUB CONT			
XXXX0101	SUB HUE				SUB COLOR			
XXXX0110	SUB BRIGHT						TRAP ON	TOT ON
XXXX0111	PIX ON	R ON	G ON	B ON	PRE OVER			AXIS
XXXX1000	BLACK	DY COL OFF	REF		ABL		BLUE	OSD
XXXX1001	G DRIVE					DC TRAN		
XXXX1010	B DRIVE					GAMMA		
XXXX1011	G CUTOFF				B CUTOFF			
XXXX1100	H PHASE				V ON	VEX OFF	AFC	
XXXX1101	VSHIFT					HV COMP		
XXXX1110	V SIZE						0	C MODE
XXXX1111	V LIN				S CORR			

Status register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit0
H LOCK	IK	KILLER	XRAY	0	0	0	0

Description of I²C Bus Registers

Sub Address 0000

PICTURE (6): Picture control
- 0 = Minimum
- 63 = Maximum

RGB LIM (2): RGB output amplitude limiter voltage control
- 0 = Limited at 4.9 V (with a black level of 2 V)
- 1 = Limited at 5.1 V (with a black level of 2 V)
- 2 = Limited at 5.3 V (with a black level of 2 V)
- 3 = Limited at 5.5 V (with a black level of 2 V)

Sub Address 0001

HUE (6): Hue control
- 0 = Skin color nearer to red
- 63 = Skin color nearer to green

IN SW (1): Input selector switch
- 0 = V1 IN
- 1 = V2 IN

Sub Address 0010

COLOR (6): Color control
- 0 = Minimum
- 63 = Maximum

SW GAIN (1): Switch output gain switching
- 0 = SW GAIN 0 dB
- 1 = SW GAIN 6 dB

Sub Address 0011

BRIGHT (6): Brightness control
- 0 = Minimum
- 63 = Maximum

NR ON (1): Y signal noise reduction ON/OFF
- 0 = OFF
- 1 = ON

Sub Address 0100

SHARPNESS (4): Sharpness control
- 0 = Minimum
- 15 = Maximum

SUB CONT (4): Sub-contrast control
- 0 = Minimum
- 15 = Maximum

Sub Address 0101

SUB HUE (4): Hue center control
- 0 = Skin color nearer to red
- 15 = Skin color nearer to green

SUB COLOR (4): Color center control
- 0 = Minimum
- 15 = Maximum

Sub Address 0110

SUB BRIGHT (6): Sub-bright control
- 0 = Minimum
- 63 = Maximum

TRAP ON (1): Chroma trap in Y system ON/OFF
- 0 = OFF
- 1 = ON

TOT ON (1): Chroma TOT filter ON/OFF
- 0 = OFF
- 1 = ON

Sub Address 0111

PIX ON (1): Picture mute ON/OFF
- 0 = Picture mute (Auto cut-off reference pulse also muted.)
- 1 = Picture mute released.

R ON (1): R OUT ON/OFF
- 0 = R OUT OFF
- 1 = R OUT ON

G ON (1): G OUT ON/OFF
- 0 = G OUT OFF
- 1 = G OUT ON

B ON (1): B OUT ON/OFF
- 0 = B OUT OFF
- 1 = B OUT ON

PRE OVER (3): Sets the sharpness preshoot and overshoot ratio.
- 0 = Pre Shoot 100 %, Over Shoot 0 %
- 7 = Pre Shoot 25 %, Over Shoot 75 %

AXIS (1): Detective axis switching
- 0 = JAPAN
- 1 = USA

Sub Address 1000

BLACK (1): Blanks the Y IN/C IN signals and sets the R, G and B outputs to black level.
- 0 = OFF
- 1 = ON

DY COL OFF (1): Dynamic color ON/OFF
- 0 = Dynamic color ON
- 1 = Dynamic color OFF

REF (2): Switches the auto cut-off reference pulse position.
- 0 = B-18H G-19H R-20H
- 1 = B-20H G-21H R-22H
- 2 = B-22H G-23H R-24H
- 3 = B-24H G-25H R-26H

ABL (2): ABL mode setting
- 0 = Picture ABL mode (including protective bright ABL)
- 1 = Combined picture ABL and bright ABL mode (bright ABL low)
- 2 = Combined picture ABL and bright ABL mode (bright ABL medium)
- 3 = Combined picture ABL and bright ABL mode (bright ABL high)

BLUE (1) On screen display B IN ON/OFF. Setting to ON turns the entire screen blue.
- 0 = OFF
- 1 = ON

OSD (1): On screen display luminance setting
- 0 = Level small
- 1 = Level large

Sub Address 1001

G DRIVE (5): G OUT drive control
- 0 = Minimum
- 31 = Maximum

DC TRAN (3): DC transmission ratio setting
- 0 = Maximum (100 %)
- 7 = Minimum(75 %)

Sub Address 1010

B DRIVE (5): B OUT drive control
- 0 = Minimum
- 31 = Maximum

GAMMA (3): γ correction value setting
- 0 = Correction OFF
- 7 = Maximum correction

Sub Address 1011

G CUTOFF (4): G OUT cut-off voltage control
- 0 = Minimum
- 15 = Maximum

B CUTOFF (4): B OUT cut-off voltage control
- 0 = Minimum
- 15 = Maximum

Sub Address 1100

H PHASE (4): Horizontal position control
- 0 = Screen shifted to right
- 15 = Screen shifted to left

V ON (1): VD output ON/OFF
- 0 = VD output stopped. (Picture mute applied simultaneously. Auto cut-off reference pulse also muted.)
- 1 = VD output

V EX OFF (1): V sync elongation ON/OFF
- 0 = V sync elongation ON
- 1 = V sync elongation OFF

AFC (2): AFC loop gain switching
- 0 = AFC loop gain large
- 1 = AFC loop gain medium
- 2 = AFC loop gain small
- 3 = AFC loop open, free running mode

Sub Address 1101

V SHIFT (5): Vertical position control
- 0 = Rise
- 31 = Lower

HV COMP (3): Vertical correction amount setting for high voltage fluctuations
- 0 = Correction amount minimum
- 7 = Correction amount maximum

Sub Address 1110

V SIZE (6): Vertical amplitude control
- 0 = V size minimum
- 63 = V size maximum

C MODE (1): V countdown system mode switching
- 0 = Non-standard signal mode, standard signal mode and no signal mode switched automatically.
- 1 = Fixed to non-standard signal mode (wide V sync window mode).

Sub Address 1111

V LIN (4): Vertical linearity control

0 = Top of screen compressed, bottom of screen expanded.

15 = Top of screen expanded, bottom of screen compressed.

S CORR (4): Vertical S correction control

0 = S correction amount minimum

15 = S correction amount maximum

H LOCK (1): Returns whether the H oscillator of the IC and the signal input to H SYNC are locked.

0 = Not locked

1 = Locked

IK (1): Returns the AKB loop stable status by detecting the IK current.

0 = IK current stable for each of R, G and B

1 = IK current unstable

KILLER (1): Returns the color killer ON/OFF status.

0 = OFF

1 = ON

XRAY (1): Returns the X-ray protection status.

0 = OFF (X-ray protection is not functioning.)

1 = ON (X-ray protection is functioning.)

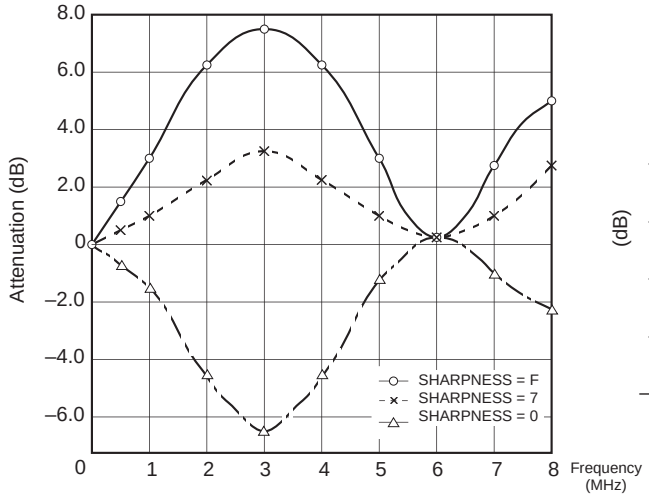


Fig 1. Sharpness characteristics

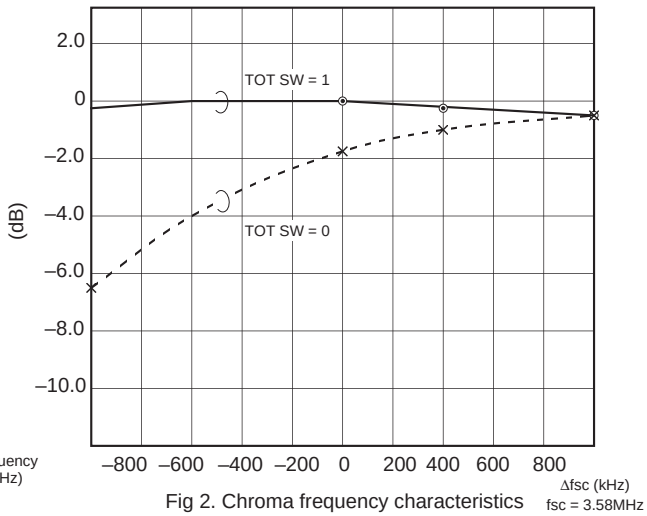


Fig 2. Chroma frequency characteristics

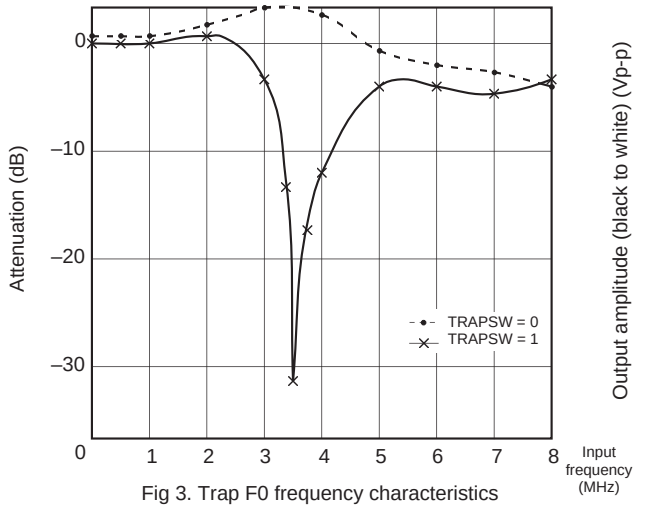


Fig 3. Trap F0 frequency characteristics

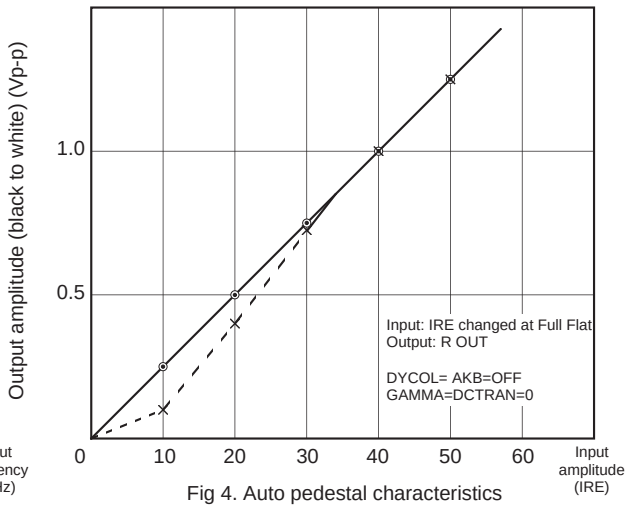


Fig 4. Auto pedestal characteristics

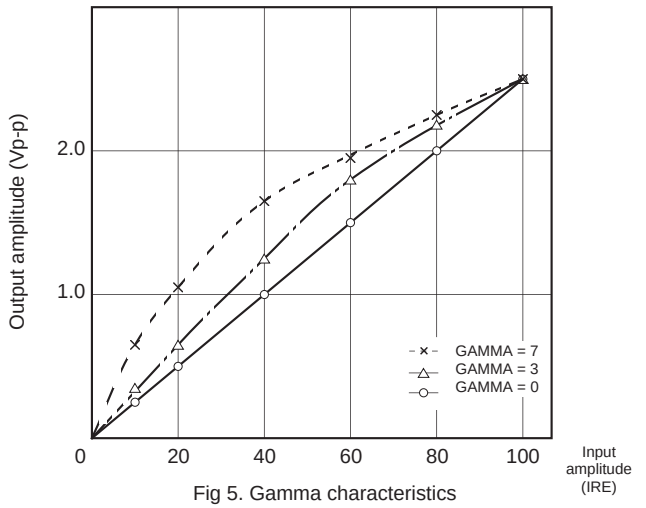


Fig 5. Gamma characteristics

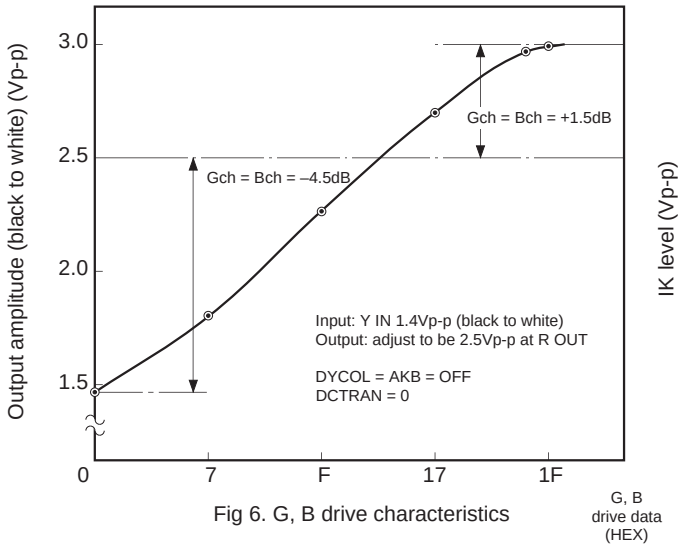


Fig 6. G, B drive characteristics

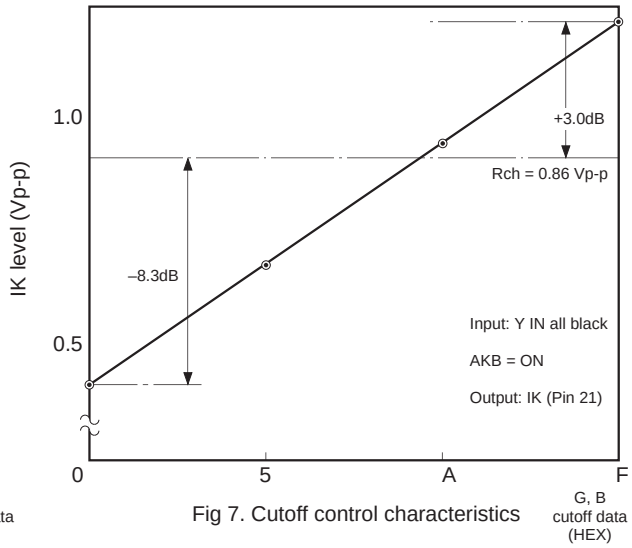


Fig 7. Cutoff control characteristics

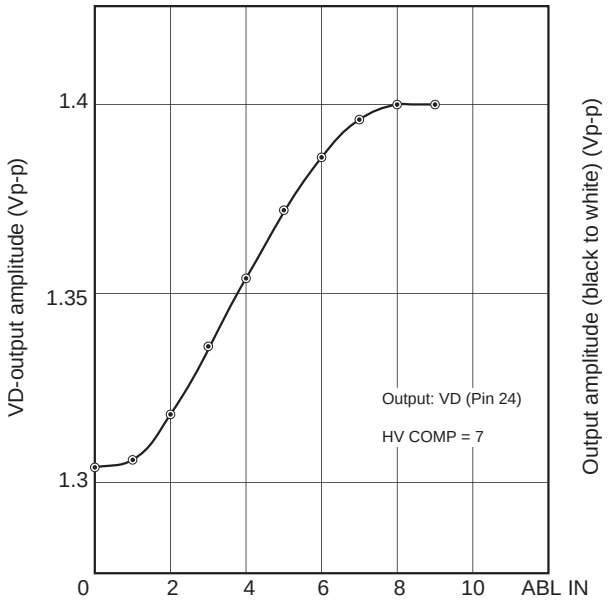


Fig 8. HV COMP characteristics

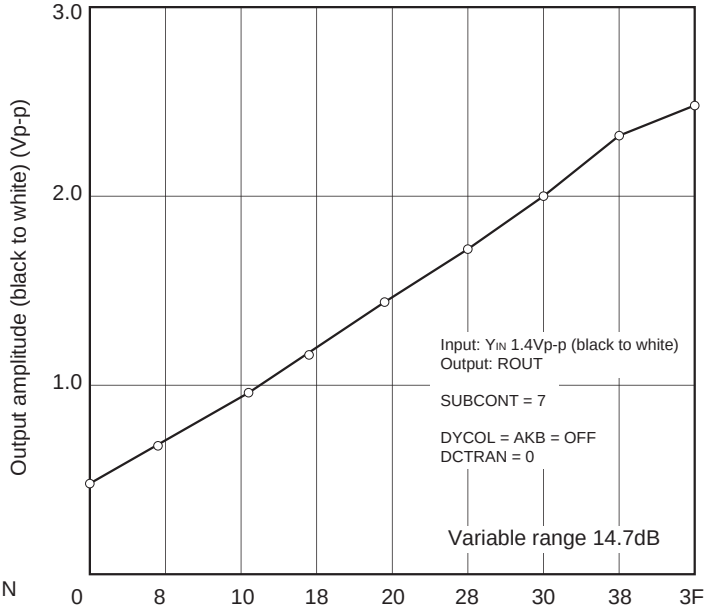


Fig 9. Picture control data (HEX)

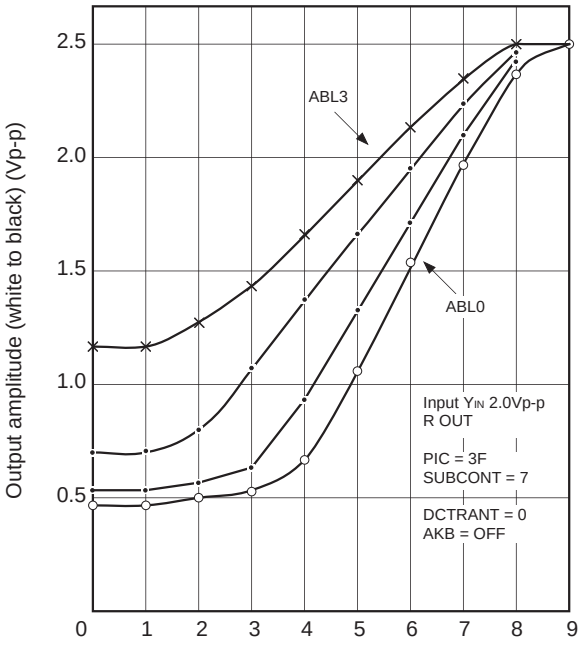


Fig 10. ABL characteristics (picture)

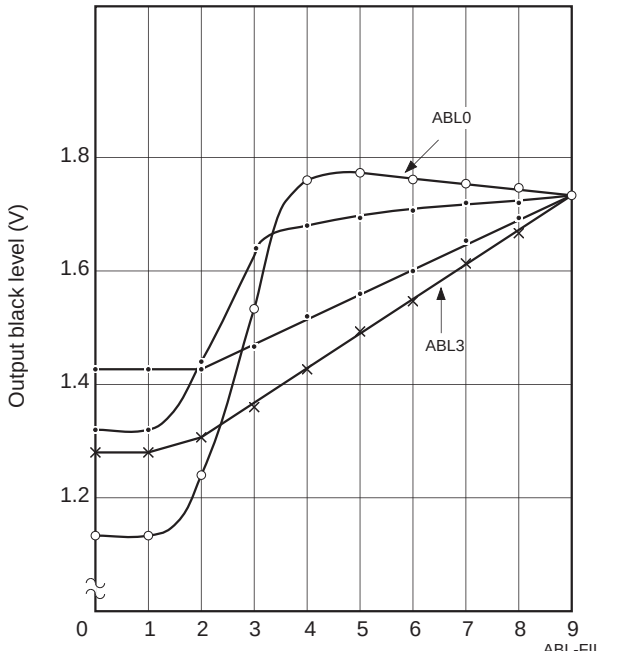


Fig 11. ABL characteristics (bright)

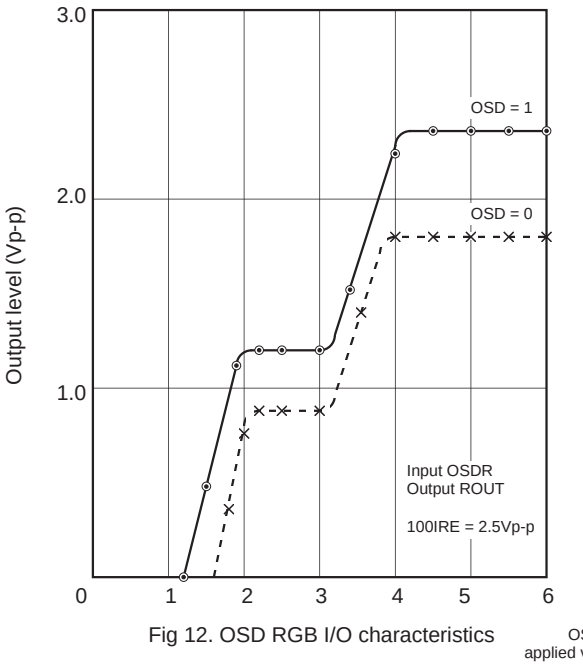


Fig 12. OSD RGB I/O characteristics

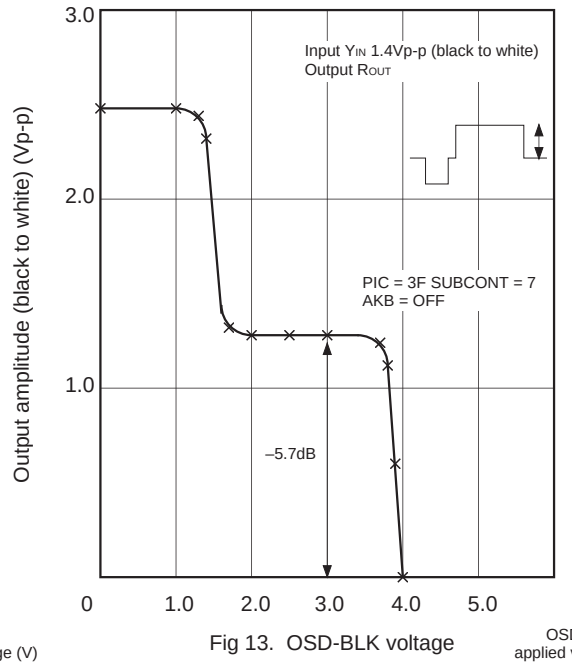
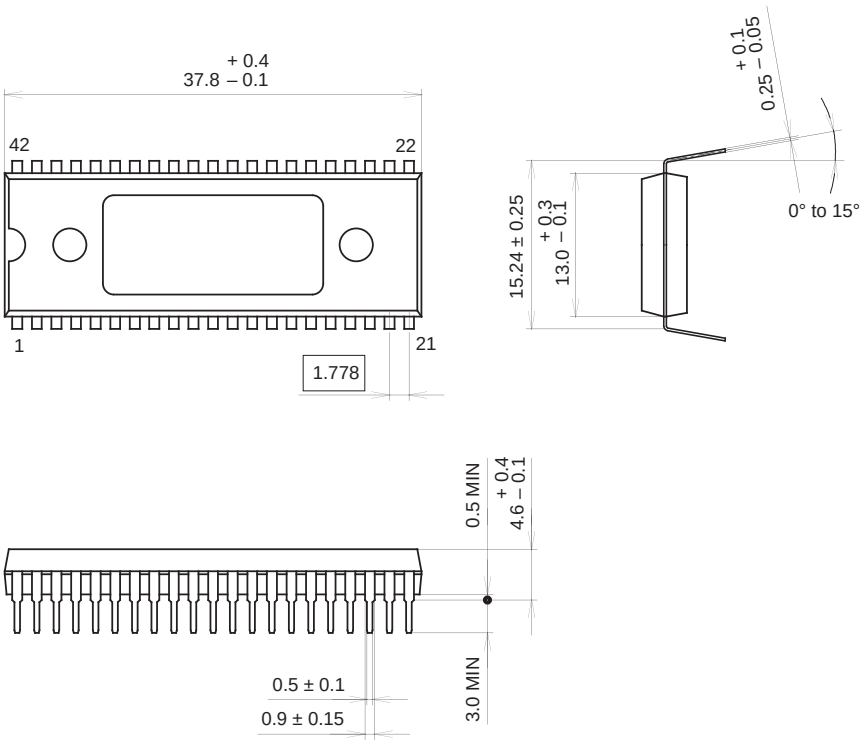


Fig 13. OSD-BLK voltage

Package Outline Unit : mm

42PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	SDIP-42P-02
EIAJ CODE	SDIP042-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	4.4g