SONY

CXA3174N

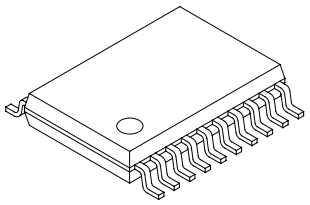
AGC IF for GSM/PCS

For the availability of this product, please contact the sales office.

Description

The CXA3174N is a 4-bit digital control variable gain amplifier suitable for the communications.

20 pin SSOP (Plastic)



Features

- Gain control amplifier with the wide gain variable range
- Doubler circuit for the LO (local) signal eliminates need for the phase shifter

Functions

- IF signal gain control circuit
- I/Q quadrature demodulator
- Doubler circuit for the LO signal
- Gain control by the 4-bit digital data
- Power saving

Applications

GSM and PCS portable telephones

Structure

Bipolar silicon monolithic IC

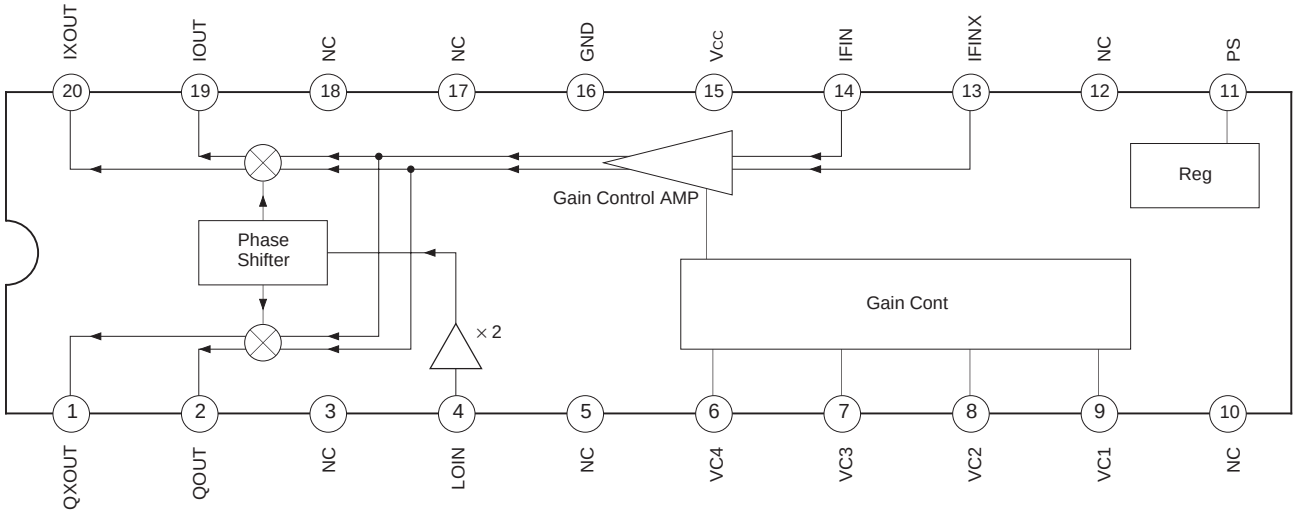
Absolute Maximum Ratings (Ta = 25 °C)

• Supply voltage	V_{CC}	14	V
• Operating temperature range	Topr	–35 to +80	°C
• Storage temperature range	Tstg	–65 to +150	°C

Operating Conditions

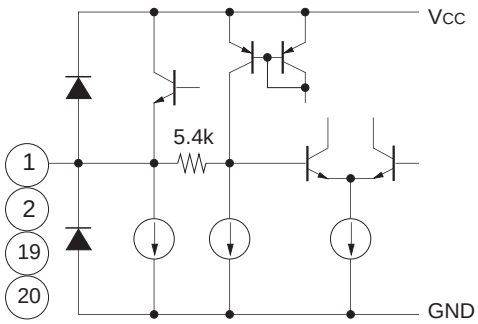
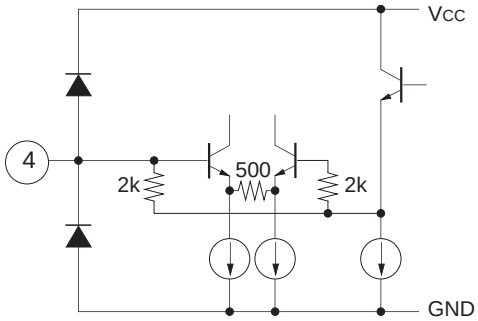
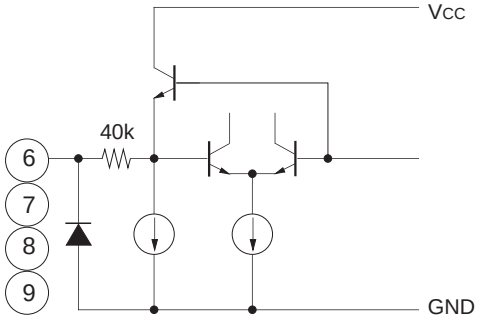
Supply voltage	V_{CC}	2.7 to 3.3	V

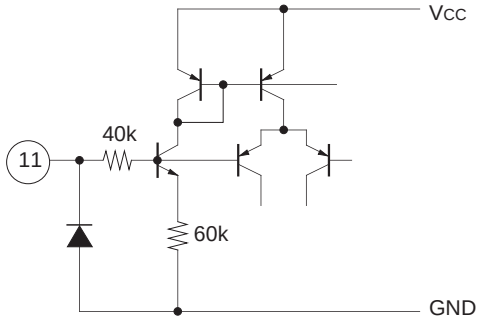
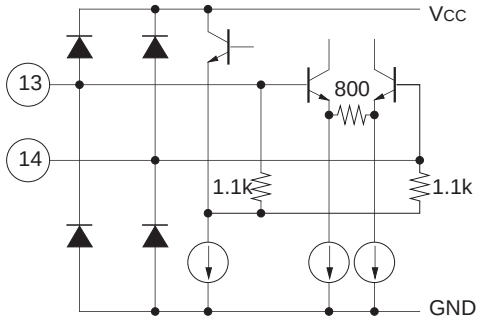
Block Diagram and Package Outline



E96932A8Z

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	QXOUT	1.5 V		Q inverted signal output.
2	QOUT			Q signal output.
19	IOUT			I signal output.
20	IXOUT			I inverted signal output.
3 5 10 12 17 18	NC	—		Not connected.
4	LOIN	1.3 V		Local signal input.
6	VC4	—		AGC control signal input. MSB.
7	VC3			AGC control signal input. 3LSB.
8	VC2			AGC control signal input. 2LSB.
9	VC1			AGC control signal input. LSB.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	PS	—		Power saving control.
13	IFINX	1.25 V		IF inverted signal input.
14	IFIN			IF signal input.
15	Vcc	—		Power supply.
16	GND	—		Ground.

Electrical Characteristics V_{CC} = 3.0 V, Ta = 27 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Icc			10	15	mA
Current consumption for standby	Iccps	PS=0 V		10	100	µA
IF input frequency range	IFINf		5		20	MHz
Maximum gain	Gmax	VC1, 2, 3, 4 = all "Low" *1, *2 Temperature fluctuation : ±2 dB IF input level : –80 dBm (330 Ω conversion)	57	60	63	dB
Minimum gain	Gmin	VC1, 2, 3, 4 = all "High" *1, *2 Temperature fluctuation : ±2 dB IF input level : –20 dBm (330 Ω conversion)	–3	0	–3	dB
Gain variable step	Gstep			4		dB
Gain setting deviation	Gdev		–3		+3	dB
Gain setting time	Gt				5	µS
LO input frequency range	LOINf		5		20	MHz
LO input level	LOINv		30	55	80	mVrms
I/Q output frequency range	IQf				2000	kHz
I/Q output signal amplitude	IQv	Differential I/Q output amplitude *1, *2 10 kΩ load IF input level : –20 dBm (330 Ω conversion) Gain=0 dB	45	64	91	mVp-p
I/Q output maximum amplitude1	IQvmax1	Differential I/Q output amplitude 10 kΩ load Gain=60 dB *2	2.0	2.7		Vp-p
I/Q output maximum amplitude2	IQvmax2	Differential I/Q output amplitude 10 kΩ load Gain=40 dB *2	2.0	2.4		Vp-p
I/Q output maximum amplitude3	IQvmax3	Differential I/Q output amplitude 10 kΩ load Gain=20 dB *2	400	480		mVp-p
I/Q output maximum amplitude4	IQvmax4	Differential I/Q output amplitude 10 kΩ load Gain=0 dB *2	210	250		mVp-p
I/Q output amplitude deviation	IQvdev	Differential I/Q output amplitude *1, *2 10 kΩ load IF input level : –20 dBm (330 Ω conversion) Gain=0 dB	–0.5		0.5	dB

*1 The IF input level is the value of C4 in the Application Circuit.

*2 The measured value is for the differential output.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
I/Q output phase deviation1	IQpdev1	Differential I/Q output *1, *2 10 kΩ load IF input level : –20 dBm (330 Ω conversion) Gain=0 dB LO input level : 30 mVrms	–2.5		2.5	deg
I/Q output phase deviation2	IQpdev2	Differential I/Q output *1, *2 10 kΩ load IF input level : –20 dBm (330 Ω conversion) Gain=0 dB LO input level : 80 mVrms	–2.5		2.5	deg
I/Q output DC voltage	IQvdc		1.4	1.5	1.6	V
I/Q output DC voltage deviation	IQvdcd	I-IX, Q-QX Output voltage difference	–30		30	mV
Noise figure1	NF 1	Gain=60 dB			22.5	dB
Noise figure2	NF 2	Gain=20 dB			40	dB
Tertiary intercept point1	$IP3_1$	Gain=60 dB, 330 Ω conversion *1	–49			dBm
Tertiary intercept point2	$IP3_2$	Gain=20 dB, 330 Ω conversion *1	–30			dBm
PS input ON voltage	VpsL		0		0.8	V
Logic input High voltage	VCvH		2.2		V_{CC}+0.3	V
Logic input Low voltage	VCvL		0		0.8	V
Logic input resistance	VCr		30			kΩ
LOIN input resistance	LOINr		1.4	2	2.6	kΩ
IFIN input resistance	IFINr	Differential input	1.5	2.2	2.9	kΩ
IFIN input level	IFINv	330 Ω conversion	–90		–10	dBm

Design Reference

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOIN input capacitance	LOINc			2		pF
IFIN input capacitance	IFINc	Differential input		1.2		pF

*1 The IF input level is the value of C4 in the Application Circuit.

*2 The measured value is for the differential output.

Control 1 Power saving

Pin 11 (PS)	Power saving	IC status
H	off	Active
L	on	Sleep

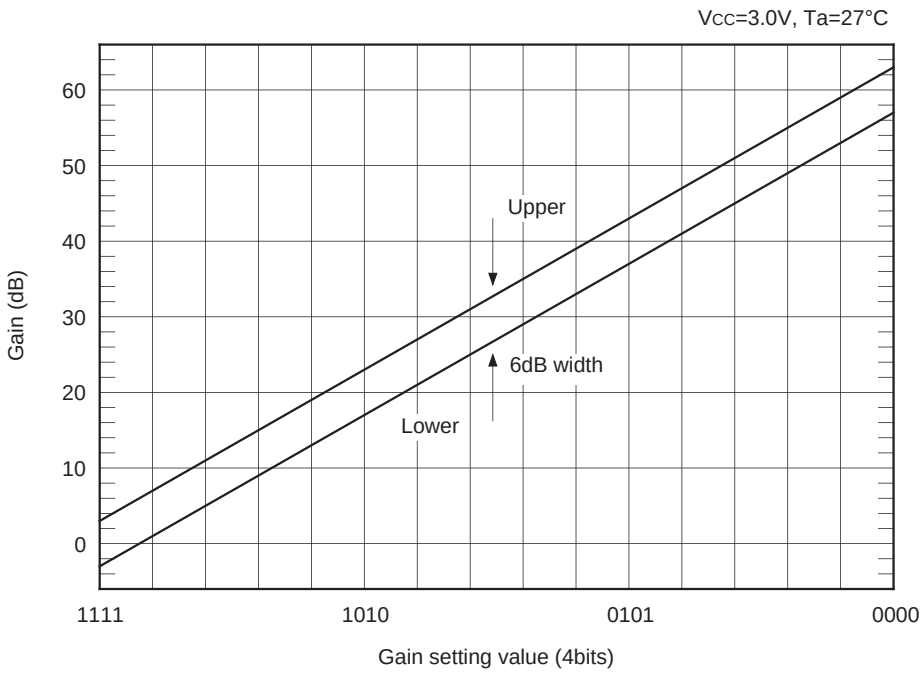
Control 2 Gain setting

Pin No.	6	7	8	9	4-bit display	Setting gain (dB)
Symbol	VC4	VC3	VC2	VC1		
	MSB	3LSB	2LSB	LSB		
MAX	L	L	L	L	“0000”	60
	L	L	L	H	“0001”	56
	L	L	H	L	“0010”	52
	L	L	H	H	“0011”	48
	L	H	L	L	“0100”	44
	L	H	L	H	“0101”	40
	L	H	H	L	“0110”	36
	L	H	H	H	“0111”	32
	H	L	L	L	“1000”	28
	H	L	L	H	“1001”	24
	H	L	H	L	“1010”	20
	H	L	H	H	“1011”	16
	H	H	L	L	“1100”	12
	H	H	L	H	“1101”	8
	H	H	H	L	“1110”	4
MIN	H	H	H	H	“1111”	0

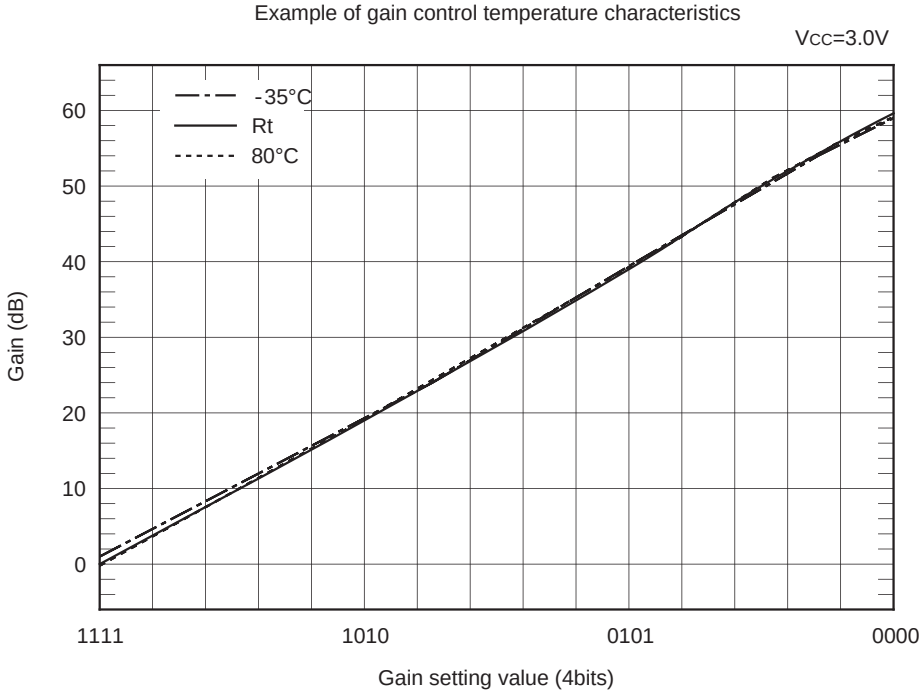
Note on Operation

Take care to handle the IC because the electrostatic discharge strength is weak for Pins 6, 7, 8, 9 and 11.

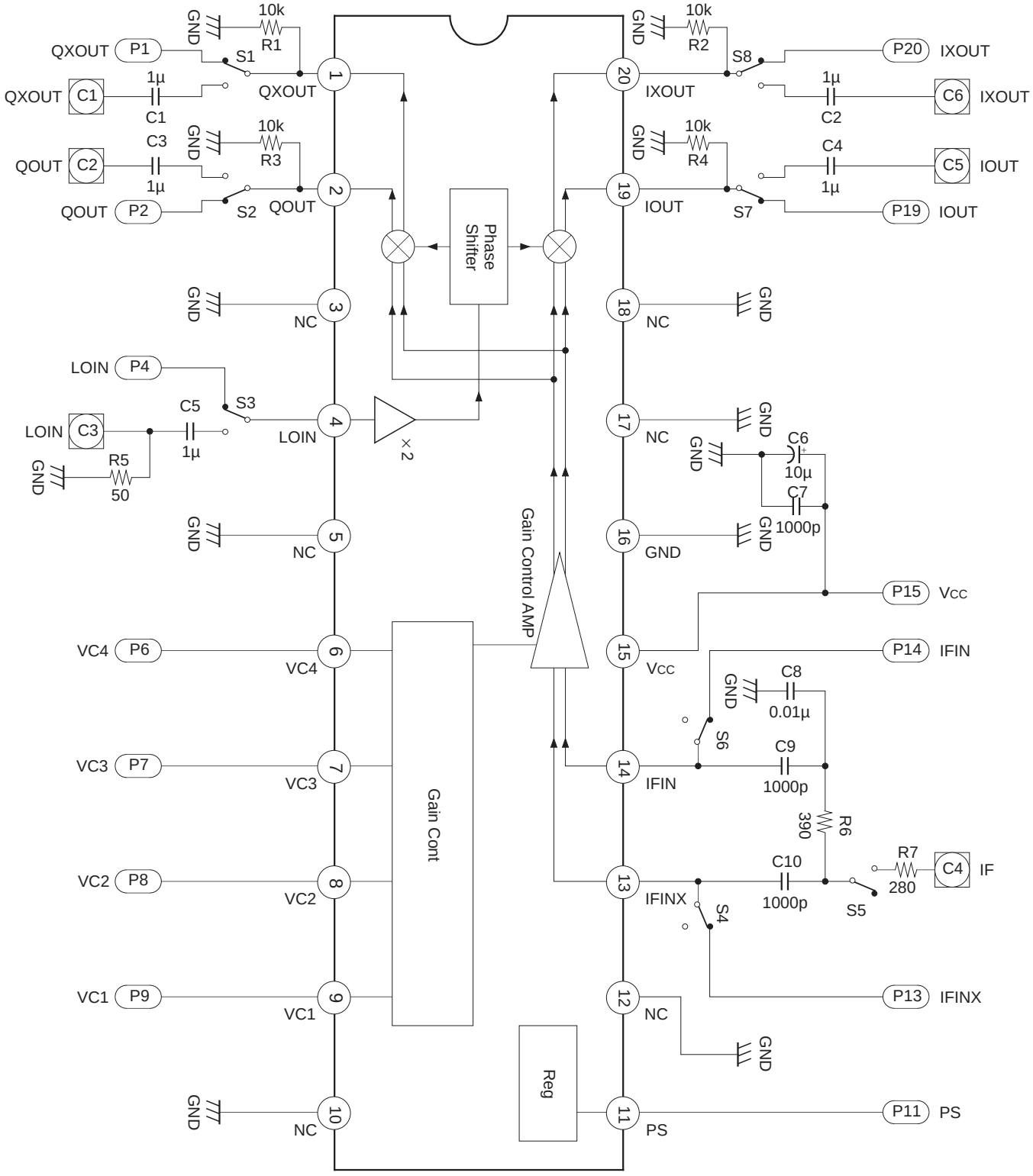
Gain control characteristics



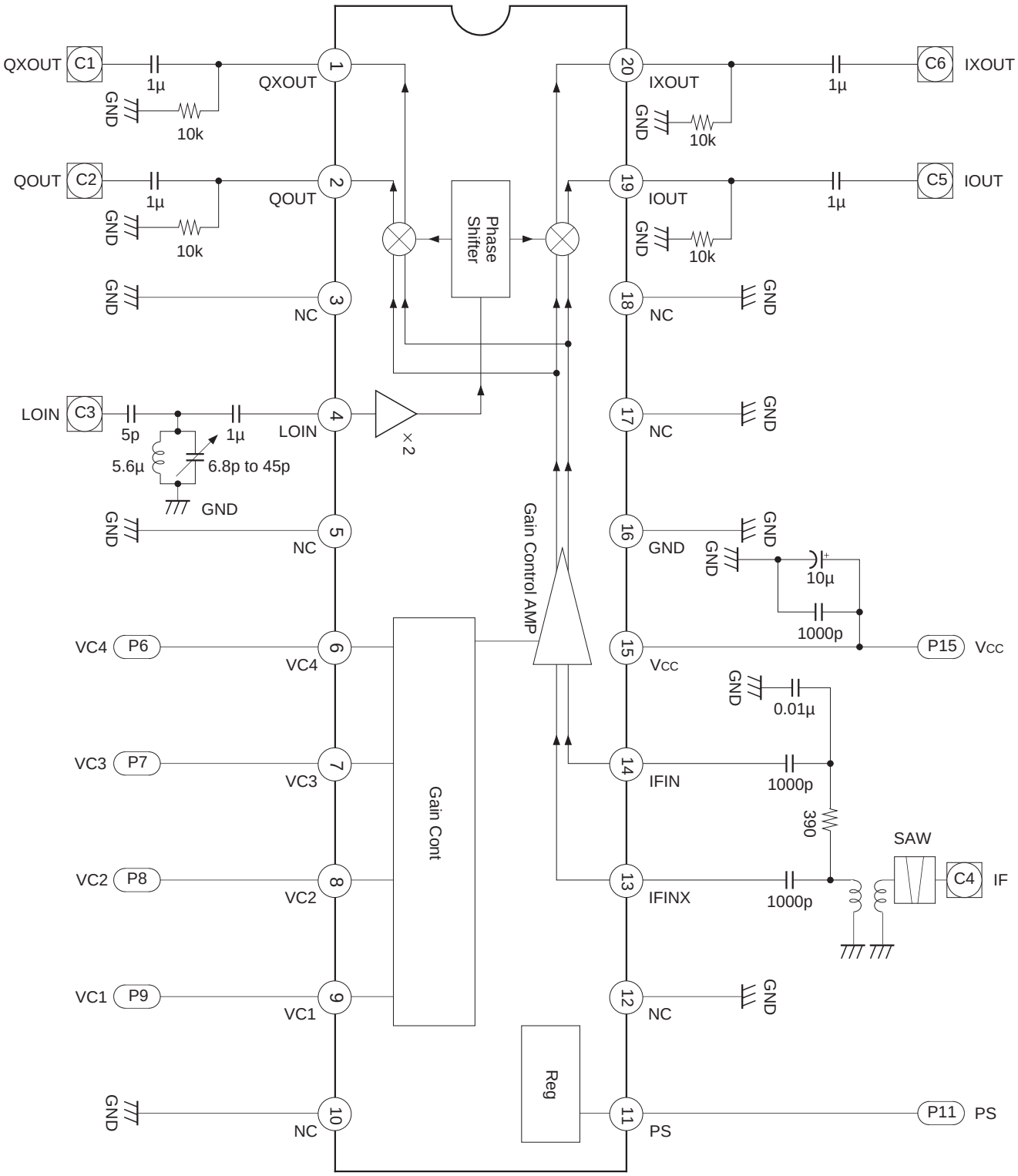
Example of gain control temperature characteristics



Electrical Characteristics Measurement Circuit



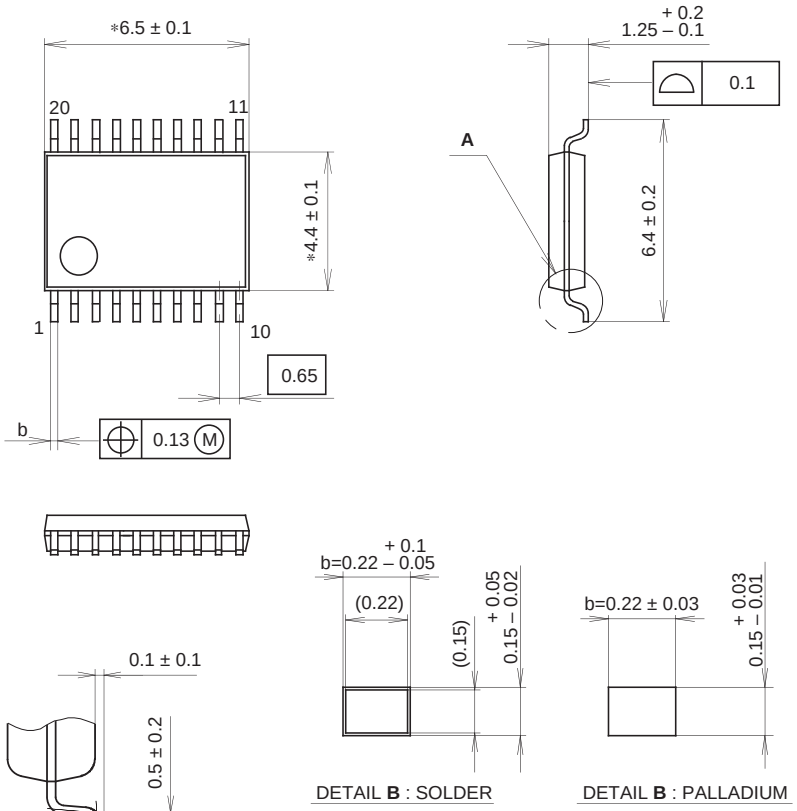
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

20PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).