SONY

CXD2073Q

Digital Comb Filter (NTSC)

Description

The CXD2073Q is an adaptive comb filter compatible with NTSC system, and provide high-precision Y/C separation with a single chip.
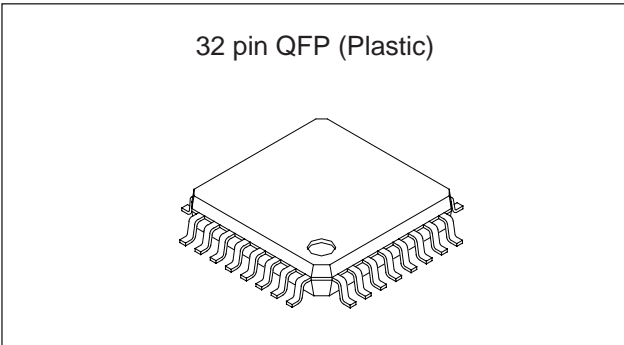
Features

- Y/C separation by adaptive processing
- Horizontal aperture compensation circuit
- 8-bit A/D converter (1 channel)
- 8-bit D/A converter (2 channels)
- One 1H delay line
- 4 PLL
- Clamp circuit

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

- Supply voltage DV_{DD} V_{SS} – 0.5 to +7.0   V
  - DAVD V_{SS} – 0.5 to +7.0   V
  - ADVD V_{SS} – 0.5 to +7.0   V
  - PLVD V_{SS} – 0.5 to +7.0   V
- Input voltage V_I V_{SS} – 0.5 to V_{DD} +0.5 V
- Output voltage V_O V_{SS} – 0.5 to V_{DD} +0.5 V
- Operating temperature
  - Topr   –20 to +75   °C
- Storage temperature
  - Tstg   –55 to +150   °C

Recommended Operating Conditions

- Supply voltage DV_{DD} 5.0 ± 0.25   V
  - DAVD   5.0 ± 0.25   V
  - ADVD   5.0 ± 0.25   V
  - PLVD   5.0 ± 0.25   V
- Operating temperature
  - Topr   –20 to +75   °C

32 pin QFP (Plastic)

Structure

Silicon gate CMOS IC

Applications

Y/C separation for color TVs and VCRs

E97411B86-PS

Pin Configuration (Top View)

Block Diagram

Pin Description

Pin No.	Symbol	I/O	Description
1	ADIN	I	Comb filter analog input (A/D converter input)
2	ADVS	—	Analog ground for A/D converter
3	ADVD	—	Analog power supply for A/D converter (+5V)
4	ACO	O	Analog chroma signal output
5	NC	—	Leave this pin open.
6	DAVD	—	Analog power supply for D/A converter (+5V)
7	AYO	O	Analog luminance signal output
8	DAVS	—	Analog ground for D/A converter
9	VRF	I	D/A converter reference voltage setting. Sets the full-scale value for D/A converter.
10	VG	O	Connect to DAVD via a capacitor of approximately 0.1µF.
11	VB	O	Connect to DAVS via a capacitor of approximately 0.1µF.
12	IRF	O	Connect a resistor of 16 times (16R) that of the output resistor "R" of AYO pin.
13	INIT	I	Test. Normally, fix to Low.
14	MOD2	I	Y/C separation status setting pins 　MOD2　MOD1 　　L　　　L　　　　Adaptive processing mode 　　L　　　H　　　　BPF separation fixed mode 　　H　　　L　　　　Y through mode 　　H　　　H　　　　Simple comb mode
15	MOD1	I	
16	APCN	I	Aperture compensation switching 　L: Aperture compensation OFF 　H: Aperture compensation ON
17	TST3	O	Test. Normally, leave this pin open.
18	DV$_{SS}$	—	Digital ground
19	DV$_{DD}$	—	Digital power supply (+5V)
20	NC	—	Leave this pin open.
21	DV$_{DD}$	—	Digital power supply (+5V)
22	DV$_{SS}$	—	Digital ground
23	TST2	O	Test. Normally, leave this pin open.
24	TST1	I	Test. Normally, fix to Low.
25	FIN	I	Clock input. Input burst-locked clock. Input fsc when the PLL is used. Input 4fsc when the PLL is not used.
26	CKSL	I	PLL control. 　L: When the PLL is not used. The 4fsc clock input to FIN is supplied internally. 　H: When the PLL is used. The 4fsc clock from VCO oscillation output is 　　　supplied internally.
27	CPO	O	Phase comparison output for the internal PLL. Leave open when the PLL is not used.
28	VCV	I	VCO oscillation control voltage input for the internal PLL. Connect to PLVS when the PLL is not used.
29	PLVD	—	PLL analog power supply (+5V)
30	PLVS	—	PLL analog ground
31	CLPEN	I	Clamp enable 　L: Clamp function is enabled. Set to L when the internal clamp is used. 　H: Clamp function is disabled. Set to H when the internal clamp is not used.
32	CLPO	O	Connect to ADIN when clamp circuit is used. Leave this pin open when clamp circuit is not used.

Electrical Characteristics   (V_{DD} = 5 ± 0.25V, V_{SS} = 0V, Ta = −20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	DV_{DD}	—	4.75	5.0	5.25	V
	$ADVD$					
	$DAVD$					
	$PLVD$					
Operating temperature	$Topr$	—	−20	—	+75	°C
Supply current	I_{DD}	Clock 14MHz	—	55	80	mA
High level input voltage	V_{IH}	CMOS level (Pin 13 to 16, 24, 26, 31)	$V_{DD} \times 0.7$	—	V_{DD}	V
Low level input voltage	V_{IL}		V_{SS}	—	$V_{DD} \times 0.3$	V
High level output voltage	V_{OH}	I_{OH} = −2mA (Pin 17 and 23)	$V_{DD} - 0.8$	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL} = 4mA (Pin 17 and 23)	V_{SS}	—	0.4	V
Logical Vth	$LVth$		—	$V_{DD}/2$	—	V
Input voltage	V_{IN}	FIN (Pin 27)	0.5	—	V_{DD}	Vp-p
Feedback resistor	R_{FB}		250k	1M	2.5M	Ω

A/D Converter Characteristics   (V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		14.3	—	—	MSPS
Analog input band width	BW	−3dB	—	18	—	MHz
Input bias	BOTTOM		0.48	0.52	0.56	V
	TOP − BOTTOM		1.96	2.08	2.22	V
Differential linearity error	E_D		−1.0	—	+1.0	LSB
Integral linearity error	E_L		−3.0	—	+3.0	LSB

D/A Converter Characteristics   (V_{DD} = 5V, V_{RF} = 2V, I_{RF} = 3.3kΩ, R = 200Ω, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax	—	14.3	—	—	MSPS
Differential linearity error	E_D	—	−0.8	—	+0.8	LSB
Integral linearity error	E_L	—	−2.0	—	+2.0	LSB
Output full-scale voltage	V_{FS}	—	1.805	1.90	1.995	V
Output full-scale current	I_{FS}	—	—	9.5	15	mA
Output offset voltage	V_{OS}	—	—	—	1.0	mV
Precision guaranteed output voltage range	V_{OC}	—	1.8	—	2.1	V

Clamp (V_{DD} = 5V, Ta = 25°C, f = 10MHz)

(V$_{DD}$ = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clamp level[1]	CLV		—	0.67	—	V

[1] Sync tip clamp

Description of Functions

- Horizontal aperture compensation

  Compensates aperture degradation accompanied by D/A conversion.

  This compensation is effective for the following modes; adaptive processing, Y through, and simple comb modes.

- Switching of Y/C separation modes

  The following four modes can be set; however, the adaptive processing mode or Y through mode is normally used.

  (1) Adaptive processing mode

  This mode detects interline correlation, switches between comb filter processing and BPF processing, and operates Y/C separation.

  (2) Y through mode

  The composite video signal input from ADIN (Pin 1) is A/D converted. It is also D/A converted, and then output from AYO (Pin 7).

  At this time, the output of ACO (Pin 4) is the same output as that of adaptive processing mode.

  (3) BPF mode

  C signal is generated by passing composite video signal through BPF.

  Y output is a signal in which the C signal generated is subtracted from input composite video signal.

  (4) Simple comb mode

  Y/C separation is operated by the comb filter processing forcibly.

Modes	MOD1 (Pin 15)	MOD2 (Pin 14)
Adaptive processing mode	L	L
Y through mode	L	H
BPF mode	H	L
Simple comb mode	H	H

- Selection Pin Setting Table

Pin No.	Symbol	H	L
14 15	MOD2 MOD1	See the table above.	
16	APCN	Horizontal aperture compensation ON	Horizontal aperture compensation OFF
26	CKSL	Internal 4-multiple PLL used	Internal 4-multiple PLL not used
31	CLPEN	Internal clamp not used	Internal clamp used

Application Circuit for D/A Converter

↑ : analog power supply 5V   ⏚ : analog ground
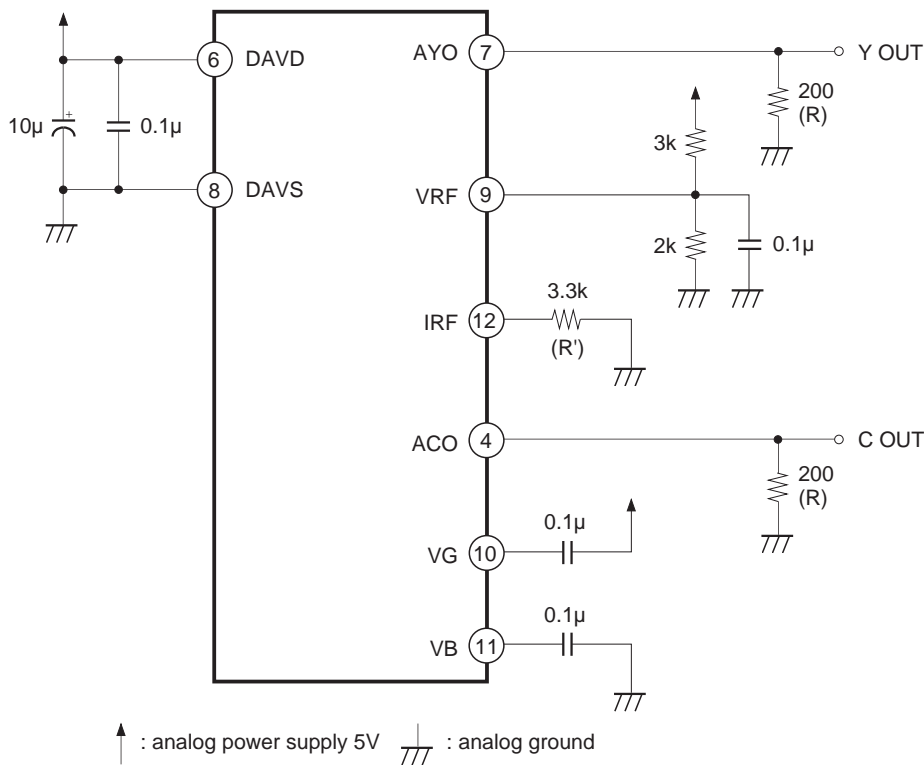
• Method of selecting output resistance

The CXD2073Q has a built-in current output-type D/A converter. To obtain the output voltages, connect resistors to AYO and ACO pins.

$$VFS = IFS \times R$$

Here, VFS is output full-scale voltage, IFS is output full-scale current, and R is the output resistance connected to each IO.

In addition, connect a resistance of 16 times the output resistor to the reference current pin IRF. In the case where the value comes to be impractical, use a value of resistance as close to the value calculated as possible. At that time,

$$VFS = VRF \times 16 \times R/R'.$$

R is the output resistance connected to each IO, R' is the resistance connected to IRF, and VRF is the VRF pin voltage. Power consumption can be reduced by using higher resistance values, but then glitch energy and data settling time increase contrastingly. Select optimum resistance values according to the system applications.

In case of the circuit above, VFS = 2 [V] × 16 × 0.2k/3.3k ≈ 1.93 [V], IFS = 1.93/0.2k ≈ 9.65 [mA].

Notes on Operation

• Power supply, ground

Separate the analog and digital systems around the device to reduce noise effect. Both analog and digital V_{DD} are respectively bypassed to V_{SS} as close to these V_{DD} and V_{SS} pins as possible through ceramic capacitors of approximately 0.1μF.

Also, layout the power supply and ground pattern of the board substrate as wide as possible to lower impedance.

• Clock

Use the burst-locked clock. Separate the clock line on the board substrate as far as possible from analog-related pins, analog power supply, and analog ground.
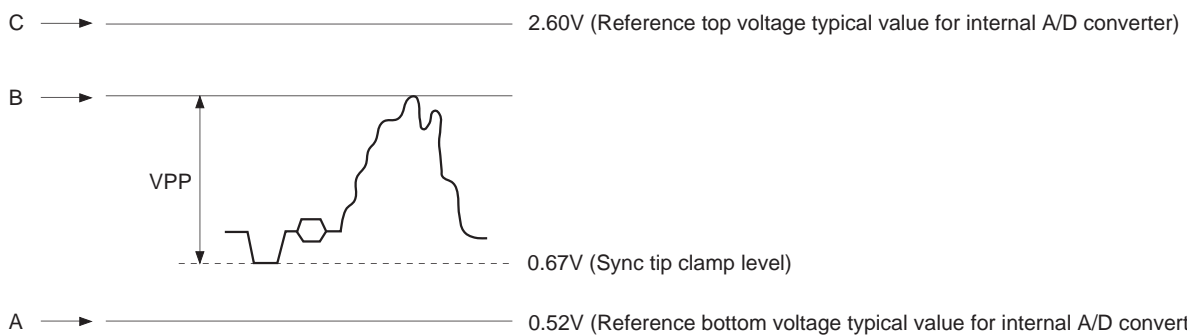
• ADIN (analog input signal)

(1) Low impedance drive

The input signal to ADIN (Pin 1) should be driven at the low impedance and its wiring should be as short as possible.

(2) Input level

Set the input signal peak-to-peak value VPP to 1.75V or less. Additionally, VPP is recommended to be 1.3V or more since the A/D converter input dynamic range should be made as large as possible.

C ⟶ ——————————————— 2.60V (Reference top voltage typical value for internal A/D converter)

B ⟶ |

VPP

———— 0.67V (Sync tip clamp level)

A ⟶ ——————————————— 0.52V (Reference bottom voltage typical value for internal A/D converter)

The DC level at the ADIN pin is as shown in the diagram above when the internal sync tip clamp is used.

Labeling the internal D/A converter AYO output full-scale voltage as VFS, the correspondence between the ADIN pin voltage and AYO output pin voltage (DC level) is as follows;

DC voltage at point A → 0 [V]

DC voltage at point B → AYO maximum output voltage [V]

DC voltage at point C → VFS [V]

The VFS is the AYO output voltage generated when the voltage equivalent to the point C is input.

• Internal delay

The delay from the internal A/D converter to the D/A converter output is 21.5 clocks + αns (α: D/A converter analog output delay = approximately 20ns).

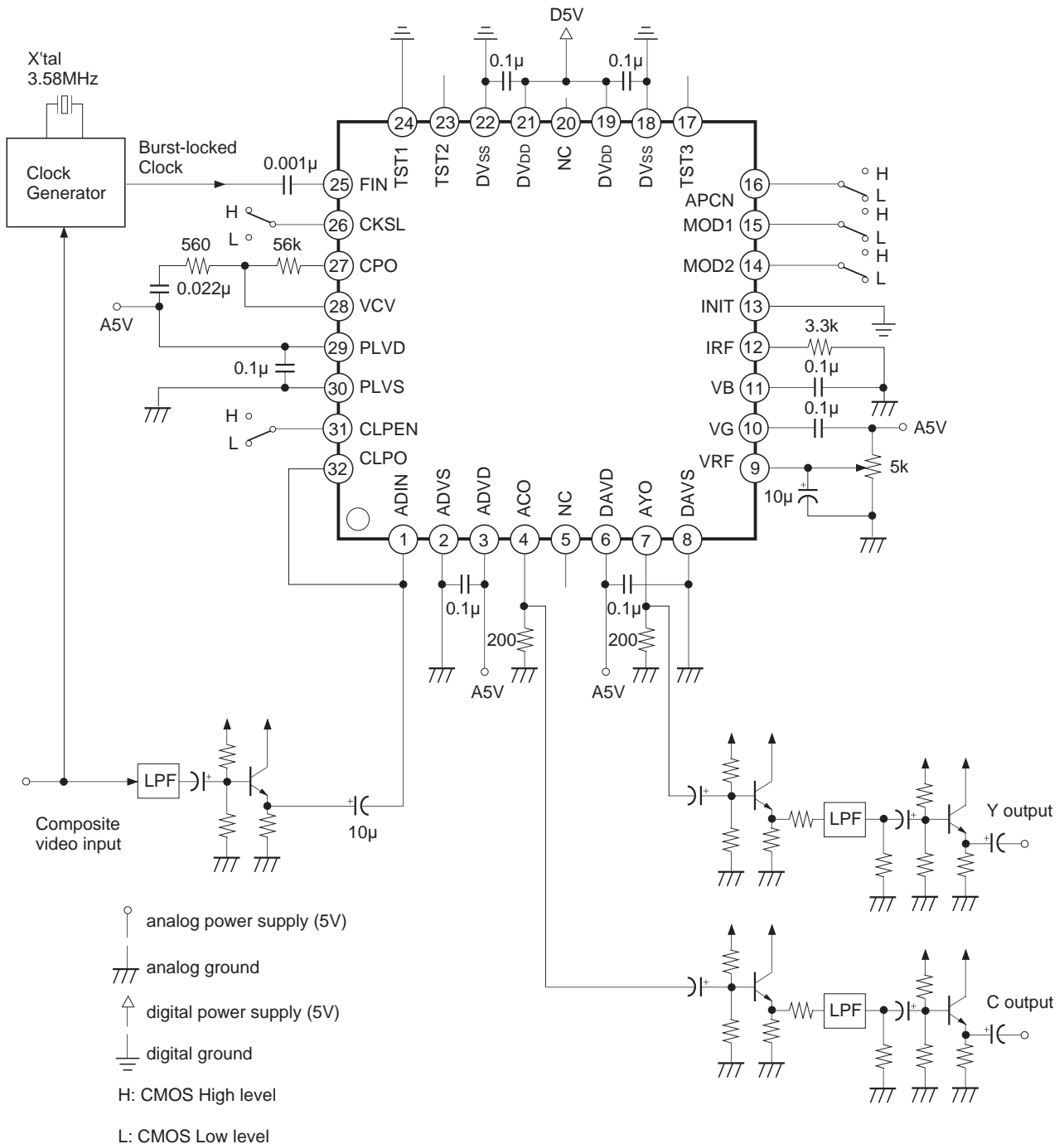The 21.5 clocks are the sum of the clocks shown below;

A/D converter: 3.5 clocks ("0.5" is for fetching the data at the fall of the clock.)
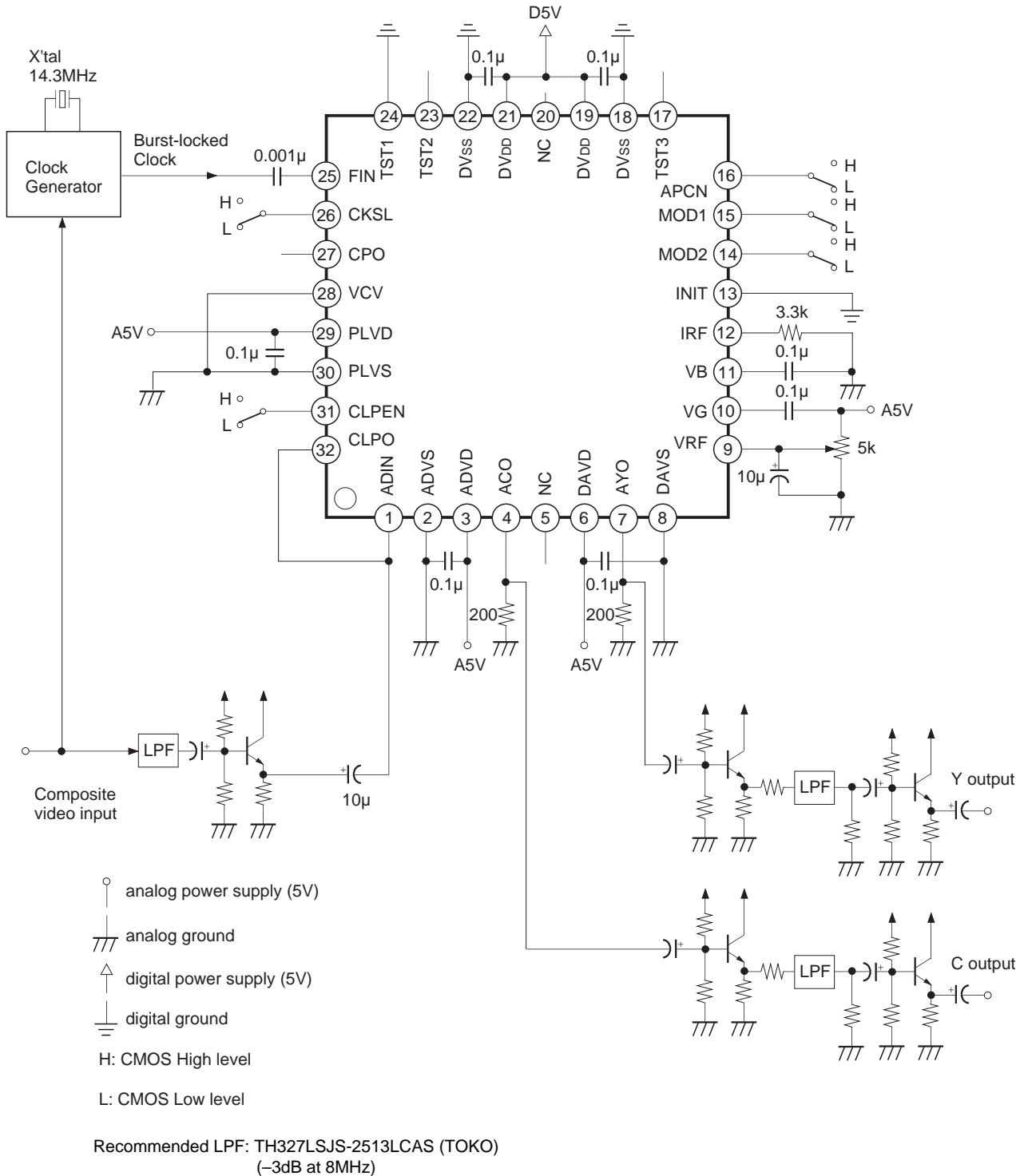
Internal logic : 17 clocks

D/A converter: 1 clock

Application Circuit

(1) In case that fsc is used as clock

analog power supply (5V)

analog ground

digital power supply (5V)

digital ground

H: CMOS High level

L: CMOS Low level

Recommended LPF: TH327LSJS-2513LCAS (TOKO)
            (−3dB at 8MHz)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.
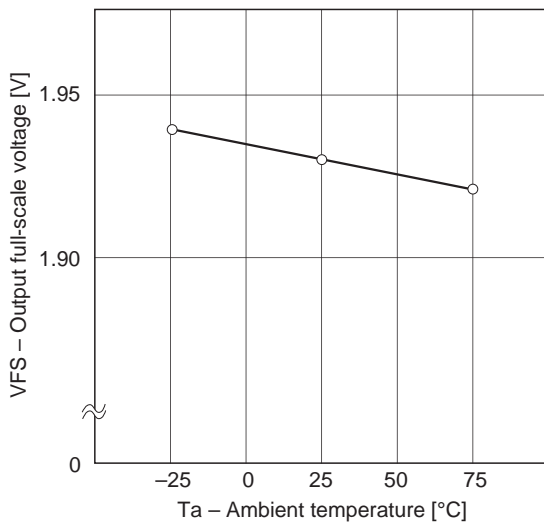
(2) In case that 4fsc is used as clock

analog power supply (5V)

analog ground

digital power supply (5V)

digital ground

H: CMOS High level

L: CMOS Low level

Recommended LPF: TH327LSJS-2513LCAS (TOKO)
                 (–3dB at 8MHz)

Example of Representative Characteristics

Analog I/O amplitude ratio vs. VRF pin voltage
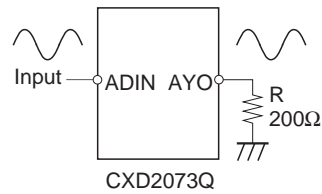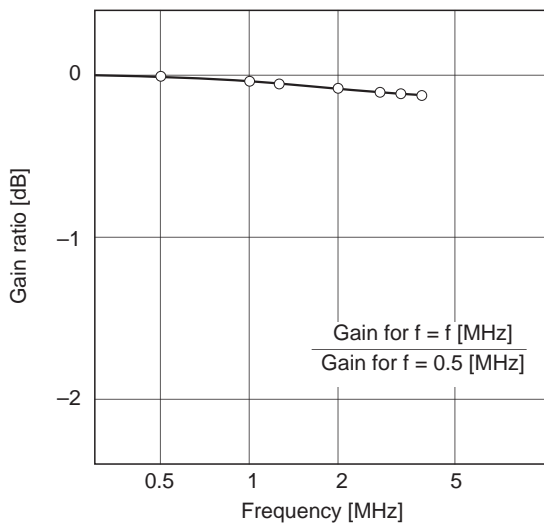Input signal peak-to-peak voltage ≤ 1.75V

$$\frac{\text{D/A output amplitude}}{\text{A/D input amplitude}}$$
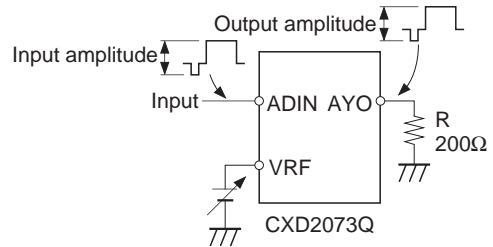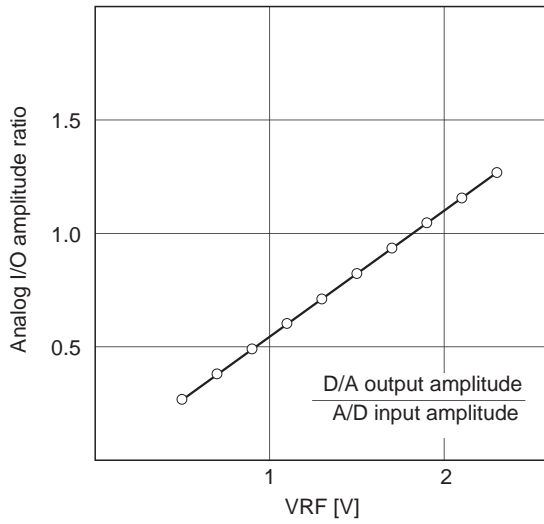
Output full-scale voltage vs. Ambient temperature

$V_{DD} = 5V$
$VRF = 2V$
$IRF = 3.3k\Omega$
$R = 200\Omega$

AYO (Y output) frequency response

$$\frac{\text{Gain for } f = f \text{ [MHz]}}{\text{Gain for } f = 0.5 \text{ [MHz]}}$$

Package Outline   Unit: mm

32PIN QFP (PLASTIC)

□ 9.0 ± 0.2

+ 0.3
□ 7.0 − 0.1

24   17

25   16

32   9

1   8

0.8

+ 0.15
0.3 − 0.1

⊕ | 0.24 Ⓜ

⌒ | 0.1

+ 0.35
1.5 − 0.15

(8.0)

+ 0.2
0.1 − 0.1

0.50

+ 0.1
0.127 − 0.05

0° to 10°
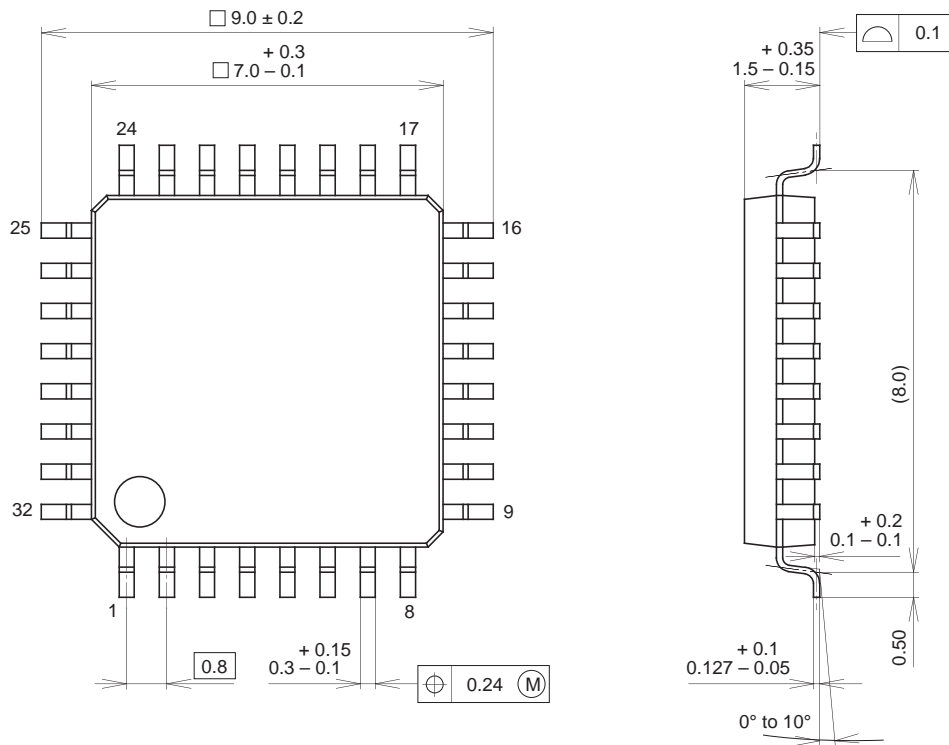
SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g