SONY

CXD2301Q

8-bit 30MSPS Video A/D Converter with Built-in Amplifier/Clamp

For the availability of this product, please contact the sales office.

Description

The CXD2301Q is an 8-bit CMOS A/D converter for video applications with built-in amplifier/sync-clamp circuits. A maximum conversion rate of 30MSPS is attained at a low power consumption by adopting a 2-step parallel system.

Features

- Resolution: 8 bits ±1/2LSB (DL)
- Maximum sampling frequency: 30MSPS
- Low power consumption: 120mW (at 30MSPS typ.)
  (Including reference current)
- Standby function:
  0.5mW power consumption in standby
- Amplifier functions: Built-in 3x amplifier (15MHz band), 2-input selector function provided
- Synchronous clamp function
- Clamp ON/OFF function
- Reference voltage self-bias circuit
- TTL compatible output
- 3V digital interface capability
- Single 5V or dual 4.75/3.3V power supplies
- Low input capacitance: 8pF
- Reference impedance: 330Ω (typ.)

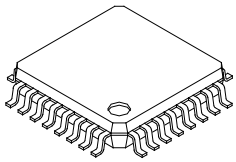
Applications

Wide range of application fields where high-speed A/D conversion is required such as in the digital systems of TVs, VCRs, etc.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

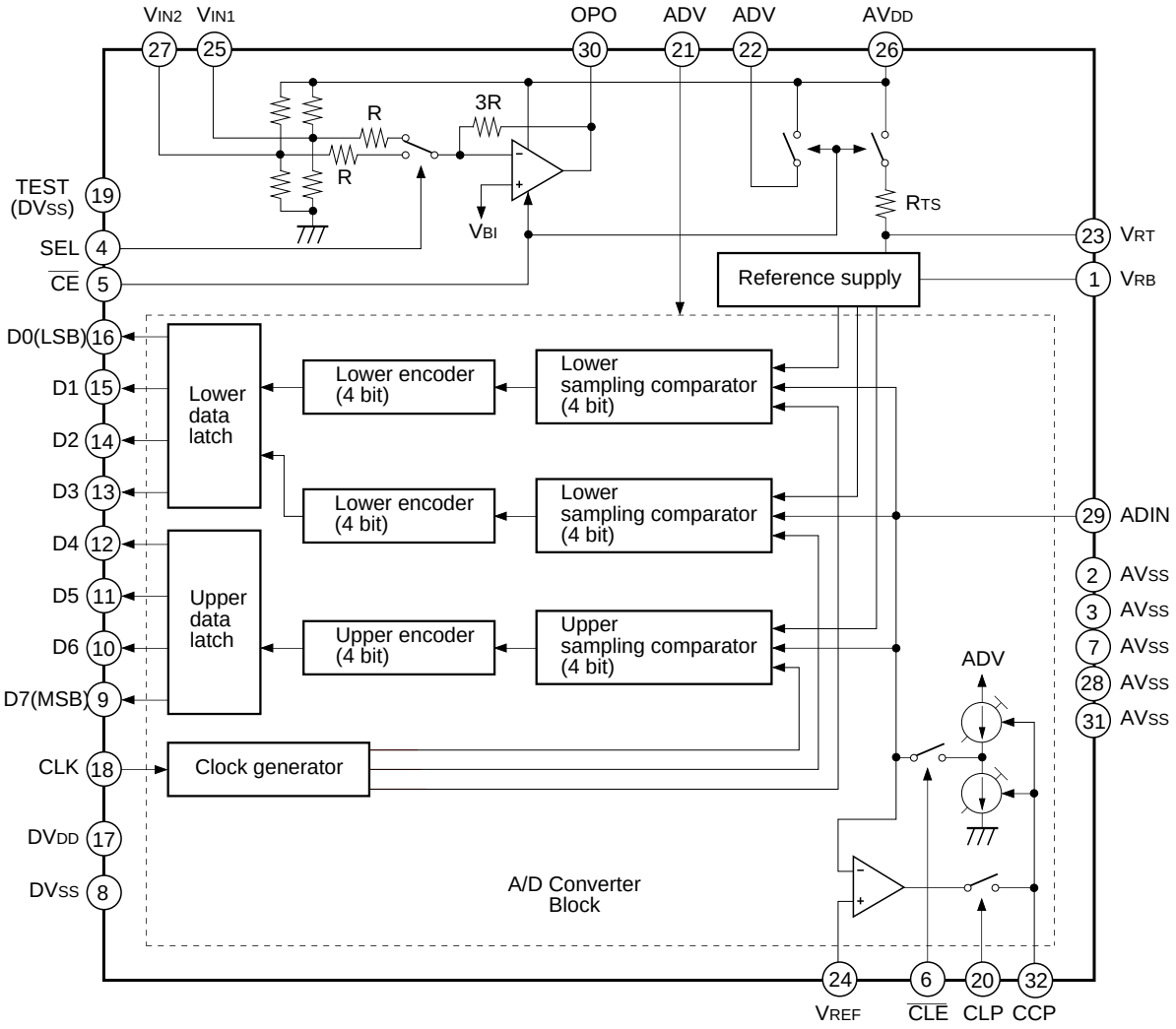
• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}		
		V_{DD} +0.5 to V_{SS} –0.5	V
• Input voltage (analog)	V_{IN}		
		V_{DD} +0.5 to V_{SS} –0.5	V
• Input voltage (digital)	V_{IH}, V_{IL}		
		V_{DD} +0.5 to V_{SS} –0.5	V
• Output voltage (digital)	V_{OH}, V_{OL}		
		V_{DD} +0.5 to V_{SS} –0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

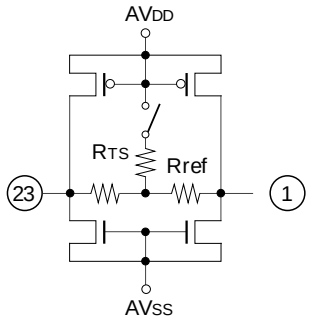
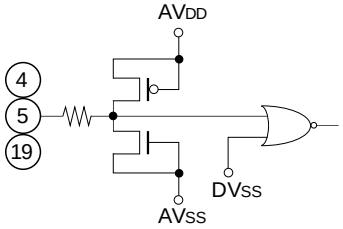
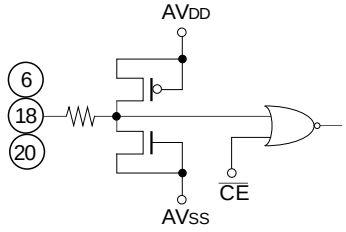
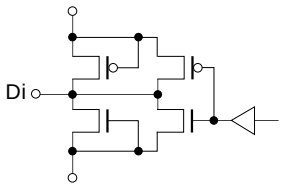
• Supply voltage	$\lvert DV_{SS}–AV_{SS}\rvert$	0 to 100	mV
Single power supply	AV_{DD}, DV_{DD}	5.0 ± 0.25	V
Dual power supply	AV_{DD}	4.75 ± 0.25	V
	DV_{DD}	3.3 ± 0.3	V
• Reference input voltage			
	V_{RB}	0 to	V
	V_{RT}	to 2.2	V
• Analog input	ADIN	More than 1.2Vp-p	
• Clock pulse width	T_{PWI}	16 (min)	ns
	T_{PWO}	16 (min)	ns
• Operating ambient temperature			
	Topr	–20 to +75	°C

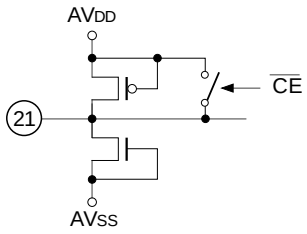
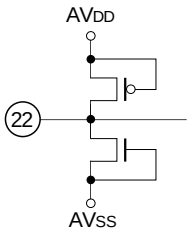
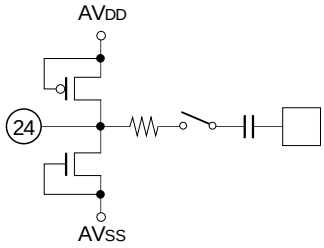
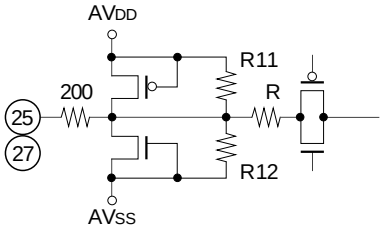
E92Y50B4X-PK

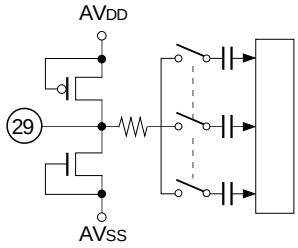
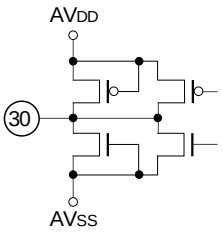
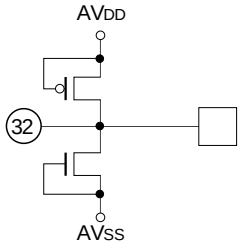
Block Diagram



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1	V_{RB}		Reference voltage (bottom) Connect to AV_{SS} for normal use. When another external voltage is input, connect an external 0.1µF capacitor and retain a 1.5V differential compared to the top reference voltage.
23	V_{RT}		Reference voltage (top) By setting V_{RB} to AV_{SS}, outputs approximately 1.5V. Connect only a 0.1µF external by-pass capacitor for normal use. When another external voltage is input, it must be 2.2V or lower.
2, 3, 7, 28, 31	AV_{SS}		Analog GND.
4	SEL		Switches the input of the 3x amplifier. When SEL is at Low level, V_{IN1} is selected. When SEL is at High level, V_{IN2} is selected.
5	$\overline{CE}$		Standby function ON/OFF selector. In standby state when High.
19	TEST		Fix to V_{SS} for normal use.
6	$\overline{CLE}$		When $\overline{CLE}$ = Low: Clamp functiion is enabled. When $\overline{CLE}$ = High: Clamp function is disabled, and only the normal A/D converter function is enabled.
18	CLK		Clock input
20	CLP		Inputs the clamp pulse to Pin 20 (CLP). Clamps the High interval signal voltage.
8	DV_{SS}		Digital GND.
9 to 16	D_7 to D_0		D_7 (MSB) to D_0 (LSB) output Outputs Low level in standby. In operation, the phase of D_7 to D_0 output is inverted against the phase of ADIN.
17	DV_{DD}		5V or 3.3V

Pin No.	Symbol	Equivalent circuit	Description
21	ADV		Short Pins 21 and 22, and connect 0.1µF external capacitor.
22	ADV		
24	V_{REF}		Clamp reference voltage input. Clamps so that the reference voltage and the clamp interval ADIN input signal are equal. The reference voltage is more than 0.5V.
25 27	V_{IN1} V_{IN2}		Amplifier input pin. Biased internally at 1.9V (when AV_{DD} = 5V) or at 1.8V (when AV_{DD} = 4.75V). When in standby as well. When SEL is at Low level, V_{IN1} is selected for input; When SEL is at High level, V_{IN2} is selected for input.
26	AV_{DD}		5V or 4.75V

Pin No.	Symbol	Equivalent circuit	Description
29	ADIN		A/D converter block analog input.
30	OPO		Amplifier output. The phase of this output is inverted against the phase of $V_{IN1, 2}$. In standby mode, it becomes high-impedance output condition.
32	CCP		Integrates the clamp control voltage. The relationship between the CCP voltage variation and the ADIN voltage is positive phase.

• The following table shows the status of the digital output pins when the TEST pin is used with the $\overline{CE}$ and SEL pins.

TEST	$\overline{CE}$	SEL	D1	D2	D3	D4	D5	D6	D7	D8
L	L	X	D1	D2	D3	D4	D5	D6	D7	D8
L	H	X	L	L	L	L	L	L	L	L
H	L	X	← TEST mode →							
H	H	L	H	L	H	L	H	L	H	L
H	H	H	L	H	L	H	L	H	L	H

Digital Output

The following table shows the correlation between the ADIN input voltage and the digital output code.
Take notice that the phase of ADIN input signal voltage is inverted against the phase of the digital output.

ADIN Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	0 0 0 0 0 0 0 0
:	:	:
:	127	0 1 1 1 1 1 1 1
:	128	1 0 0 0 0 0 0 0
:	:	:
V_{RB}	255	1 1 1 1 1 1 1 1

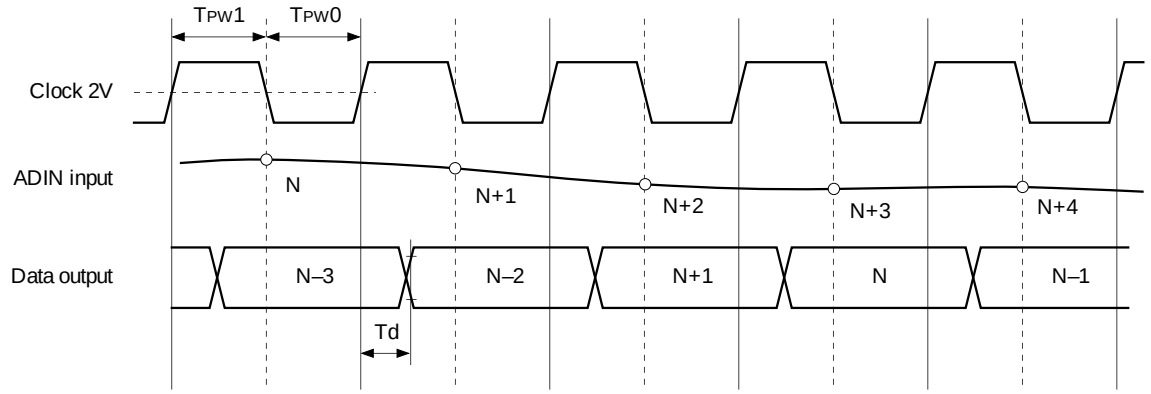


Fig. 1. Timing Chart

Electrical Characteristics

(1) When using a single power supply (Fc = 30MSPS, AV_{DD} = DV_{DD} = +5V, V_{RB} = 0V, V_{RT} = 1.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	I_{AD} + I_{DD}	Fc = 35MSPS NTSC ramp wave input			27	35	mA
Standby supply current	I_{STB}	$\overline{CE}$ = DV_{DD}			130	200	µA
Max. conversion rate	Fc max	V_{IN} = 0 to 1.5V f_{IN} = 1kHz ramp		30			MSPS
Min. conversion rate	Fc min					0.5	
ADIN input band (at –1dB)	BW				20		MHz
ADIN input capacitance	C_{ADIN}	V_{IN} = 0.75V + 0.07Vrms			8		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self bias	V_{RT}	V_{RB} = AV_{SS}		1.38	1.52	1.66	V
Offset voltage	E_{OT}			–40	–20	0	mV
	E_{OB}			+25	+45	+65	
Digital input voltage	V_{IH}			3.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	DV_{DD} = max.	V_{IH} = V_{DD}			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	DV_{DD} = min.	V_{OH} = V_{DD}–0.5V	–1.1	–2.5		mA
	I_{OL}		V_{OL} = 0.4V	3.7	6.5		
Output data delay	T_{DL}	With TTL 1gate and 10pF load		7	13	25	ns
Integral nonlinearity error	E_L	Fc = 30MSPS V_{IN} = 0 to 1.5V			+0.5	+1.3	LSB
Differential nonlinearity error	E_D	Fc = 30MSPS V_{IN} = 0 to 1.5V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40IRE mod ramp, Fc = 14.3MSPS			1		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tsd				2		ns
Clamp offset voltage	Eoc	V_{ADIN} = DC, PWS = 3µsec	V_{REF} = 0.5V	0	+20	+40	mV
			V_{REF} = 1.5V	–40	–20	0	
Clamp pulse delay	tcpd				25		ns
Amplifier gain		DC to 15MHz		8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} bias voltage	$V_{BI1, 2}$	When open			1.9		V
V_{IN1} and V_{IN2} input resistance	$R_{I1, 2}$			19	27	35	kΩ
V_{IN1} and V_{IN2} input capacitance	$C_{I1, 2}$				15		pF

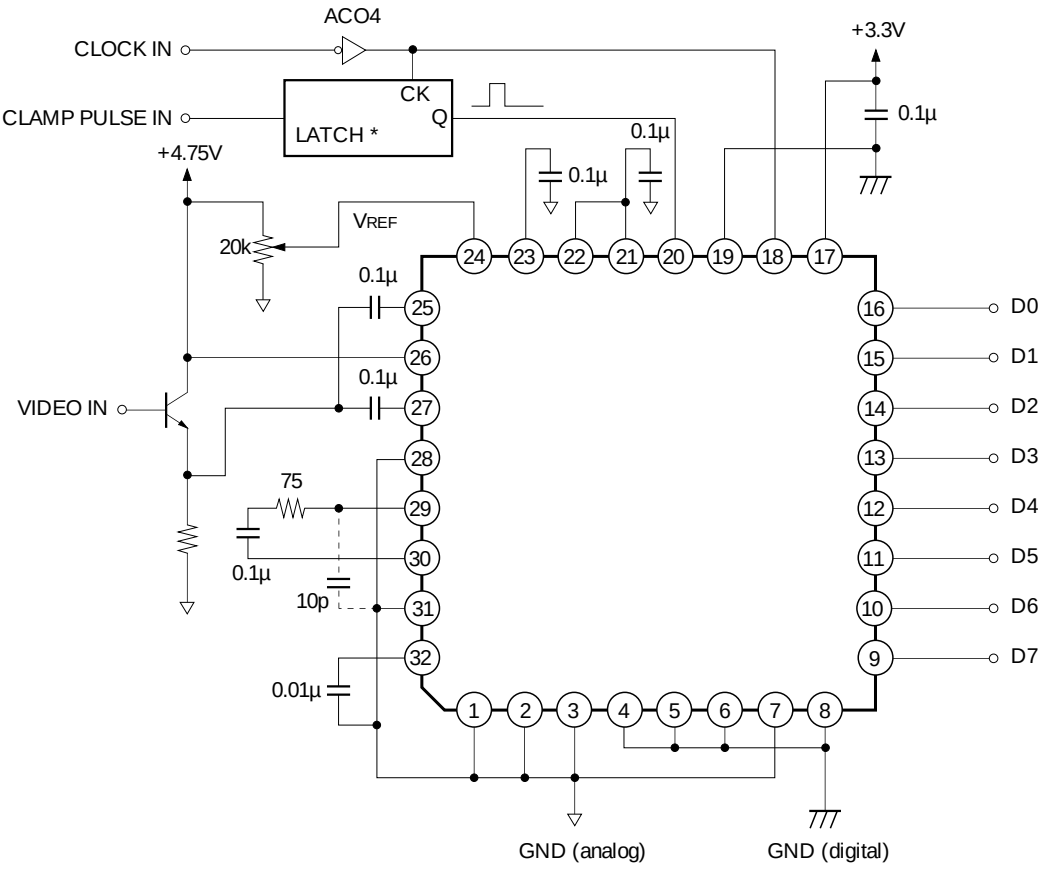
(2) When using a dual power supply (Fc = 30MSPS, AV_{DD} = 4.75V, DV_{DD} = 3.3V, V_{RB} = 0V, V_{RT} = 1.5V, Ta = 25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Analog supply current	I_{AD}	Fc = 30MSPS NTSC ramp wave input			24	32	mA
Digital supply current	I_{DD}	Fc = 30MSPS NTSC ramp wave input			1	2	mA
Standby supply current	I_{STB}	$\overline{CE}$ = DV_{DD}			130	200	µA
Max. conversion rate	Fc max	V_{IN} = 0 to 1.5V f_{IN} = 1kHz ramp		30			MSPS
Min. conversion rate	Fc min					0.5	
ADIN input band (at –1dB)	BW				20		MHz
ADIN input capacitance	C_{ADIN}	V_{IN} = 0.75V + 0.07Vrms			8		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self bias	V_{RT}	V_{RB} = AV_{SS}		1.44	1.52	1.6	V
Offset voltage	E_{OT}			–40	–20	0	mV
	E_{OB}			+25	+45	+65	
Digital input voltage	V_{IH}			2.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	DV_{DD} = max.	V_{IH} = DV_{DD}			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	DV_{DD} = min.	V_{OH} = V_{DD}–0.5V	–1.1	–2.5		mA
	I_{OL}		V_{OL} = 0.4V	3.7	6.5		
Output data delay	T_{DL}	With TTL 1gate and 10pF load		7	13	25	ns
Integral nonlinearity error	E_L	Fc = 30MSPS V_{IN} = 0 to 1.5V			+0.5	+1.3	LSB
Differential nonlinearity error	E_D	Fc = 30MSPS V_{IN} = 0 to 1.5V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40IRE mod ramp, Fc = 14.3MSPS			1		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tsd				2		ns
Clamp offset voltage	Eoc	V_{IN} = DC, PWS = 3µsec	V_{REF} = 0.5V	0	+20	+40	mV
			V_{REF} = 1.5V	–40	–20	0	
Clamp pulse delay	tcpd				25		ns
3x amplifier gain		DC to 15MHz		8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} bias voltage	$V_{BI1, 2}$	When open			1.8		V
V_{IN1} and V_{IN2} input resistance	$R_{I1, 2}$			19	27	35	kΩ
V_{IN1} and V_{IN2} input capacitance	$C_{I1, 2}$				15		pF

Application Circuit

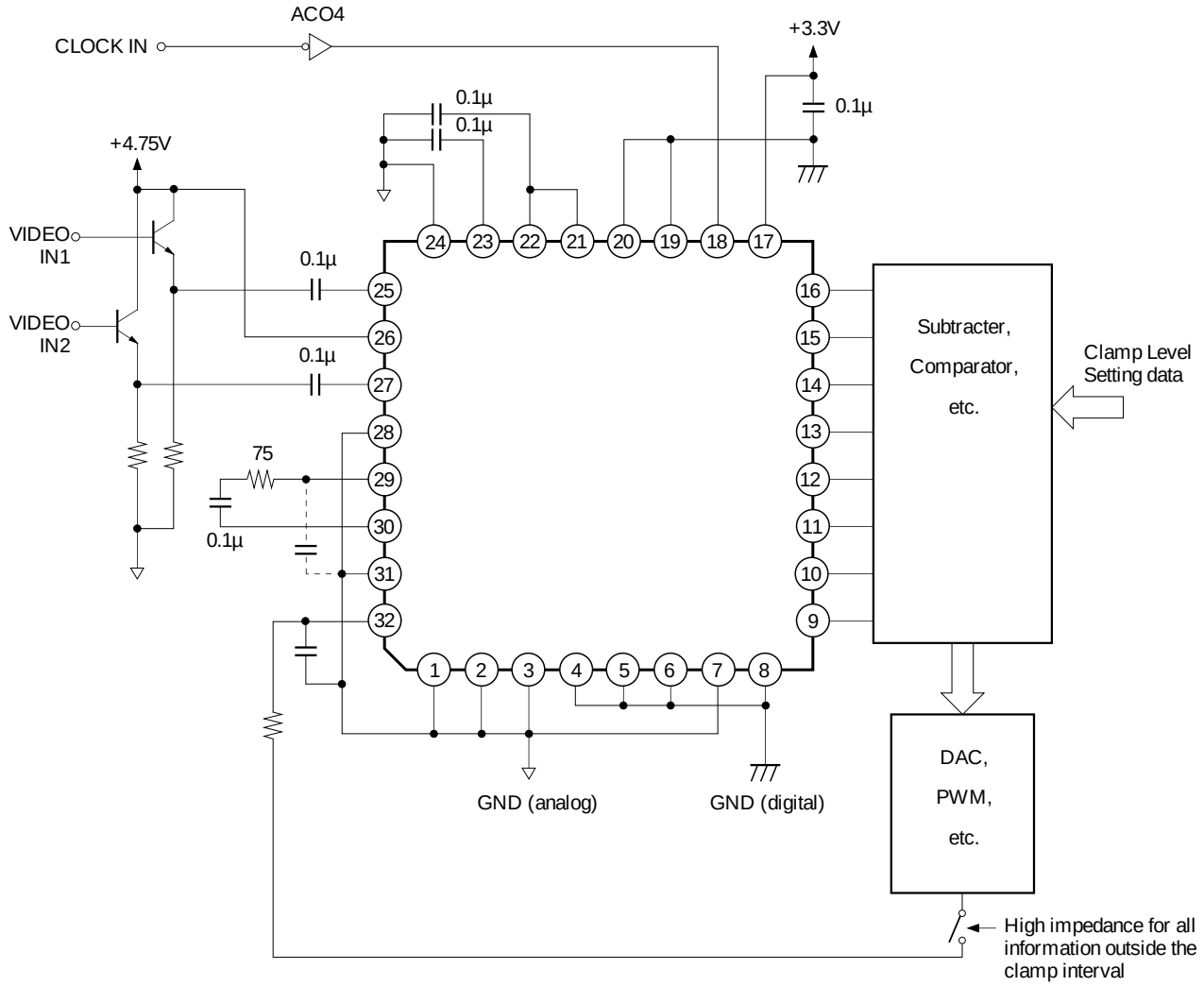
(1) When using the internal amplifier

a) Clamp usage example (using self bias)



* Although the ADC sampling clock latches the clamp pulse, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small beat might be generated as V sag. The latch circuit is valid at this time.

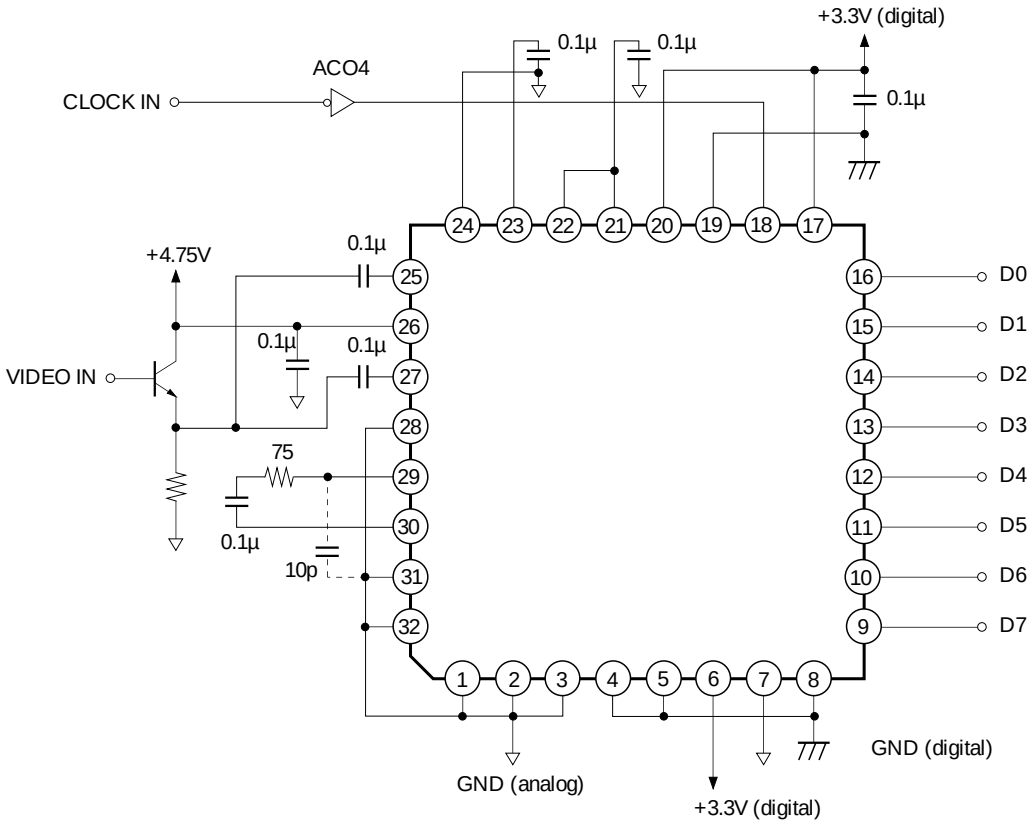
b) Digital clamp usage example (using self bias)



* The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is positive phase.

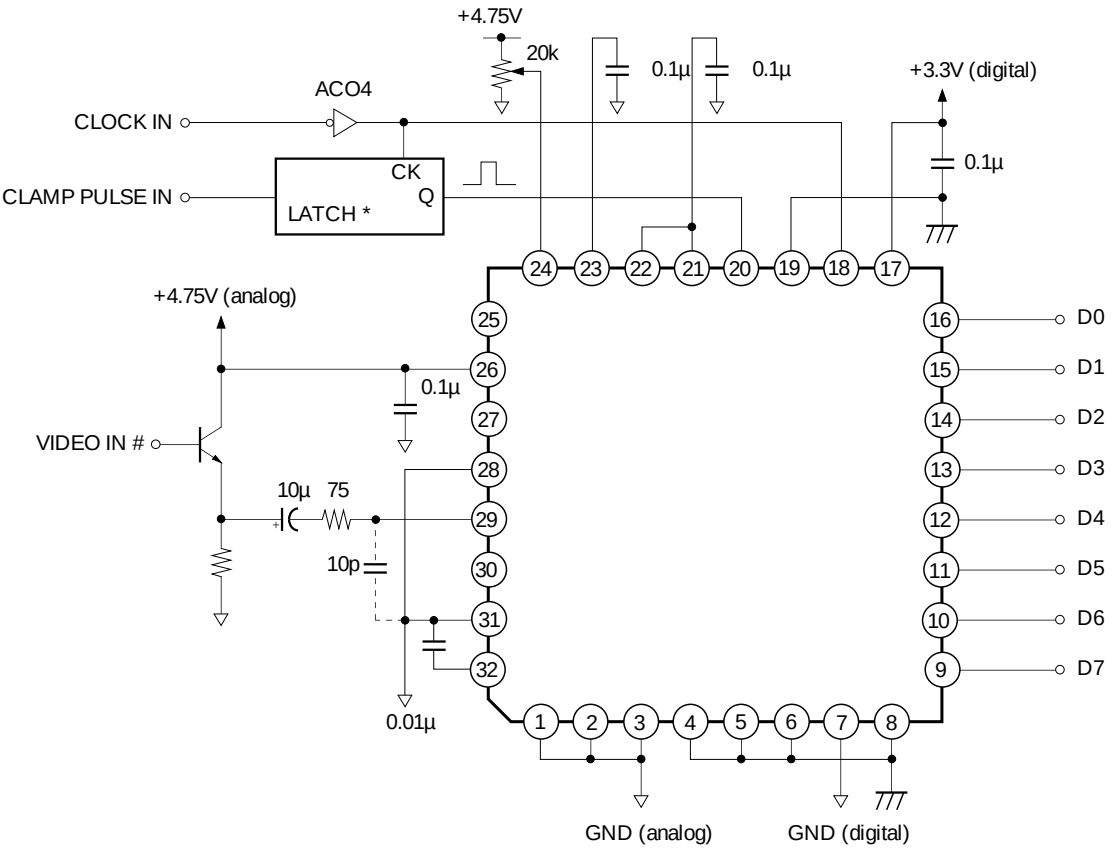
* $\Delta ADIN/\Delta V_{CCP} = 3.0$ (fs = 30MSPS)

c) When not using the clamp



(2) When not using the internal amplifier

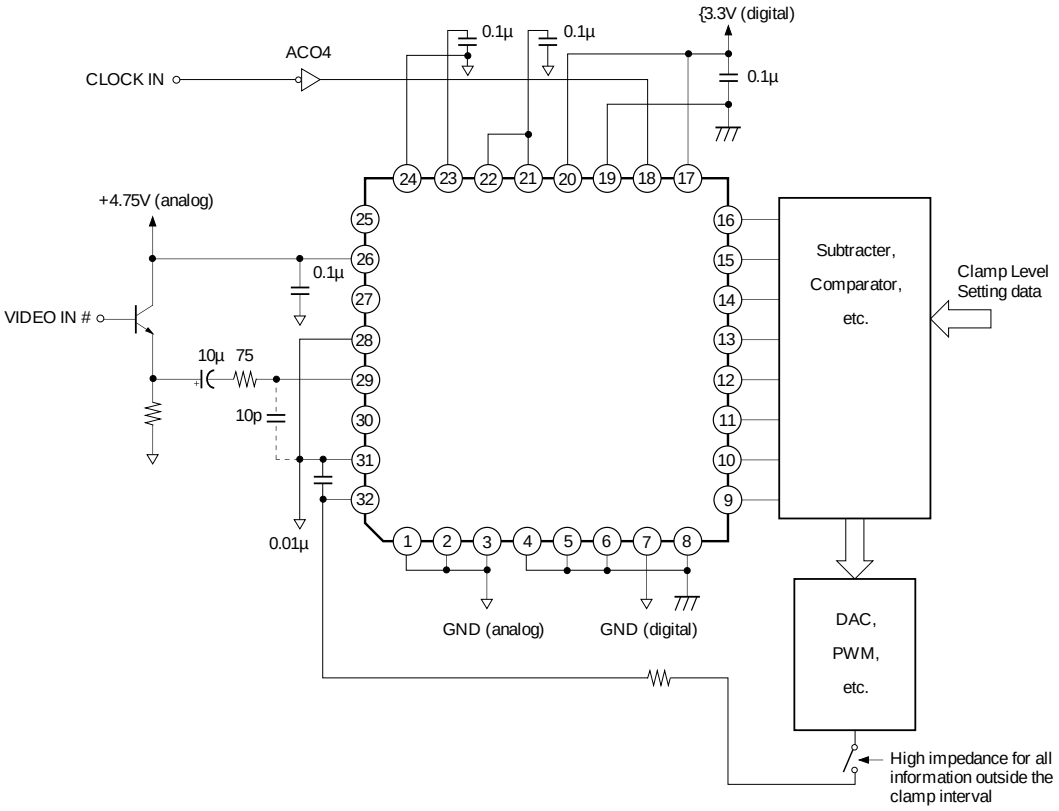
a) Clamp usage example



* Although the ADC sampling clock latches the clamp pulse, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small beat might be generated as V sag. The latch circuit is valid at this time.

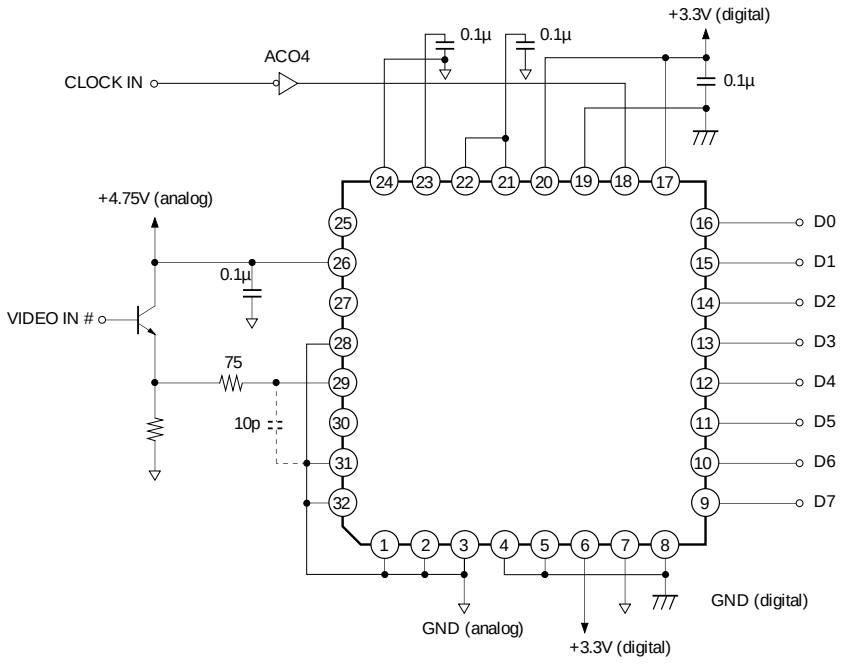
\# Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to “Digital Output” on page 6.)

b) Digital clamp usage example



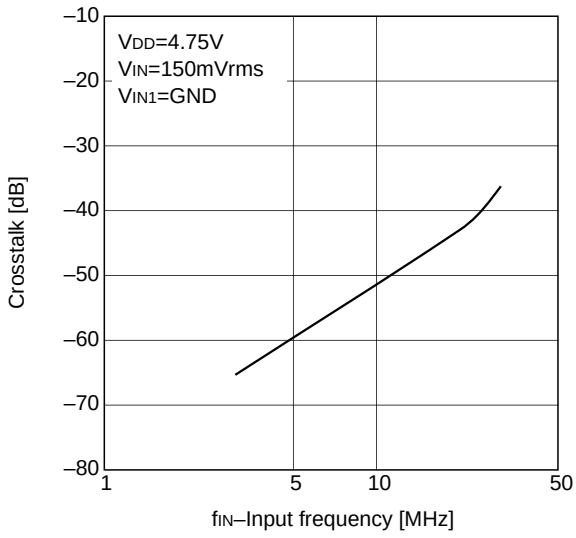
* The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is positive phase.
* $\Delta V_{ADIN}/\Delta V_{CCP}$ = 3.0 (fs = 20MSPS)

c) When not using the clamp

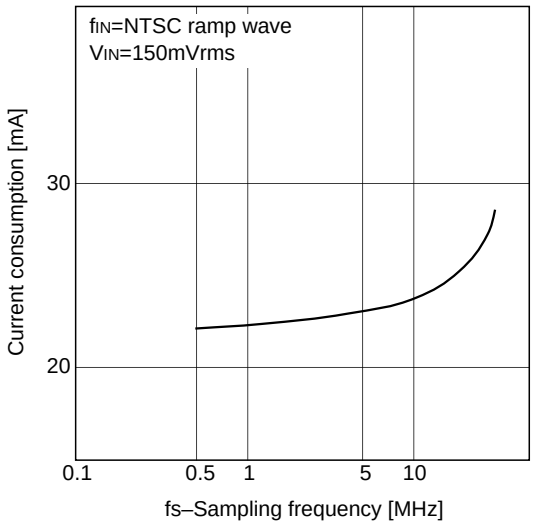


Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to “Digital Output” on page 6.)

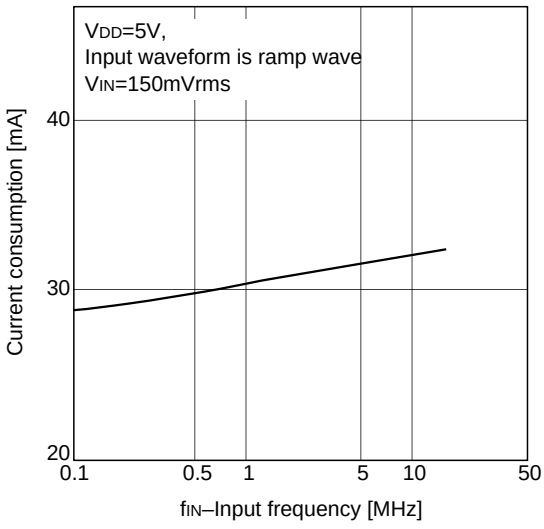
Example of Representative Characteristics



Input frequency of V_{IN2} vs. Crosstalk $V_{IN2} \rightarrow V_{IN1}$



Sampling frequency vs. Current consumption



Input frequency vs. Current consumption

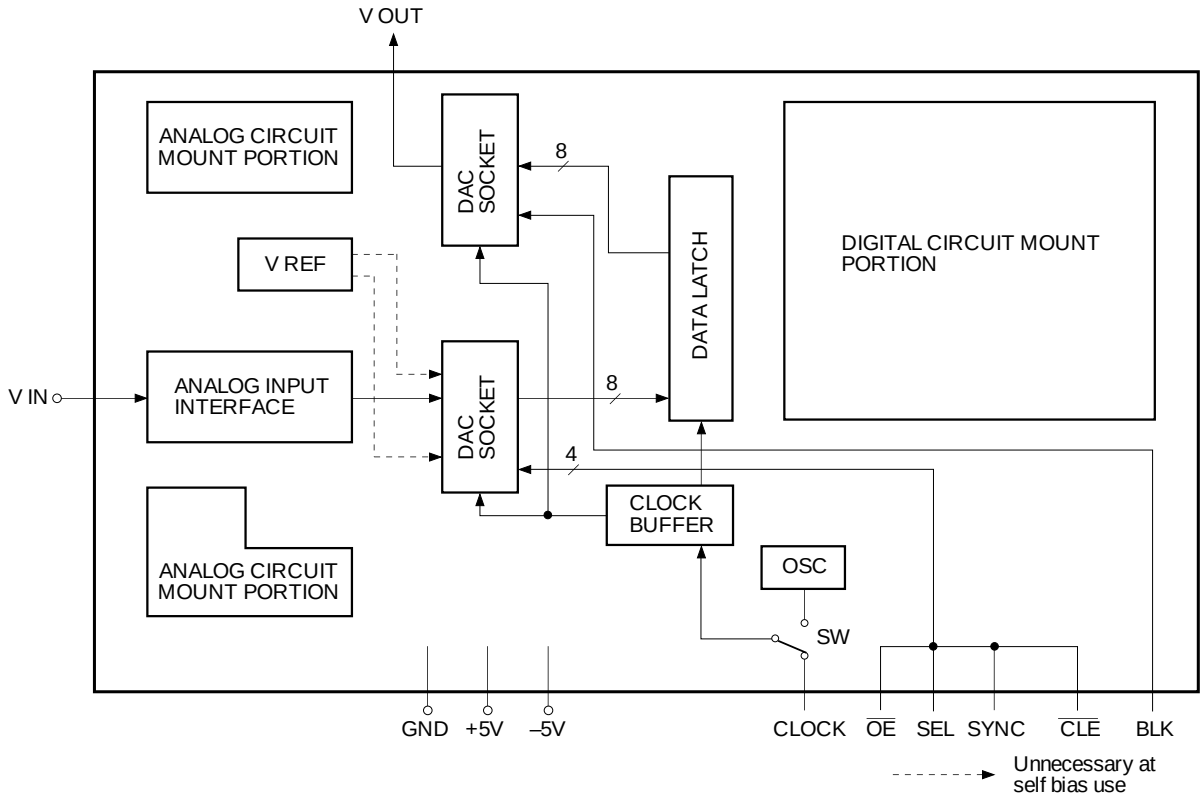
8bit ADC and DAC Evaluation Board

Evaluation boards are available for the high speed, low power consumption CMOS converters, CXD2301Q (8-bit 30MHz A/D) and CXD1171M (8-bit 40MHz D/A).

The evaluation board is composed of a main board common to either type, to which is added sub board D2301Q or sub board D1171M. The junction is made through a socket.

To the main board are mounted an input interface, clock buffer and latch. To each of the sub boards is mounted CXD2301Q and CXD1171M respectively. Those IC's are mounted according to recommended print patterns designed to provide maximum performance to the A/D and D/A converters.

Block Diagram



Characteristics

- Resolution 8bit
- Maximum conversion rate 30MHz
- Digital input level CMOS level
- Supply voltage ±5.0V (Single +5V power supply possible at self bias use)

Supply Voltage

Item	Min.	Typ.	Max.	Unit
+5V –5V			165 20	mA

Clock Input

CMOS compatible

Pulse width T_{CW1} 16ns (min)

T_{CW0} 16ns (min)

Analog Output (CXD1171M) (RL > 10kΩ)

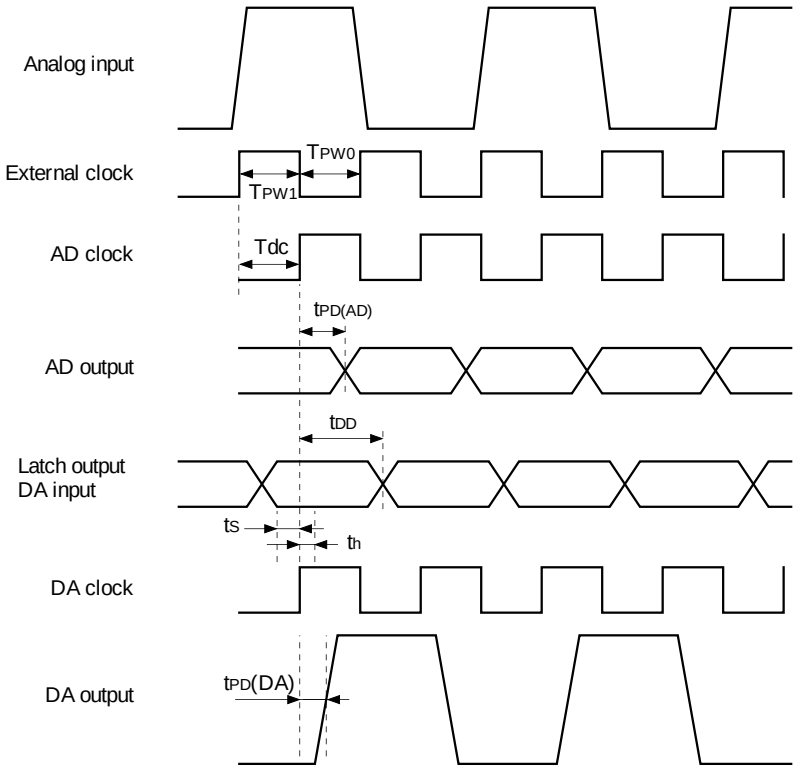
Item	Min.	Typ.	Max.	Unit
Analog output	1.8	2.0	2.1	V

Output Format (CXD2301Q)

The table shows the output format of AD Converter

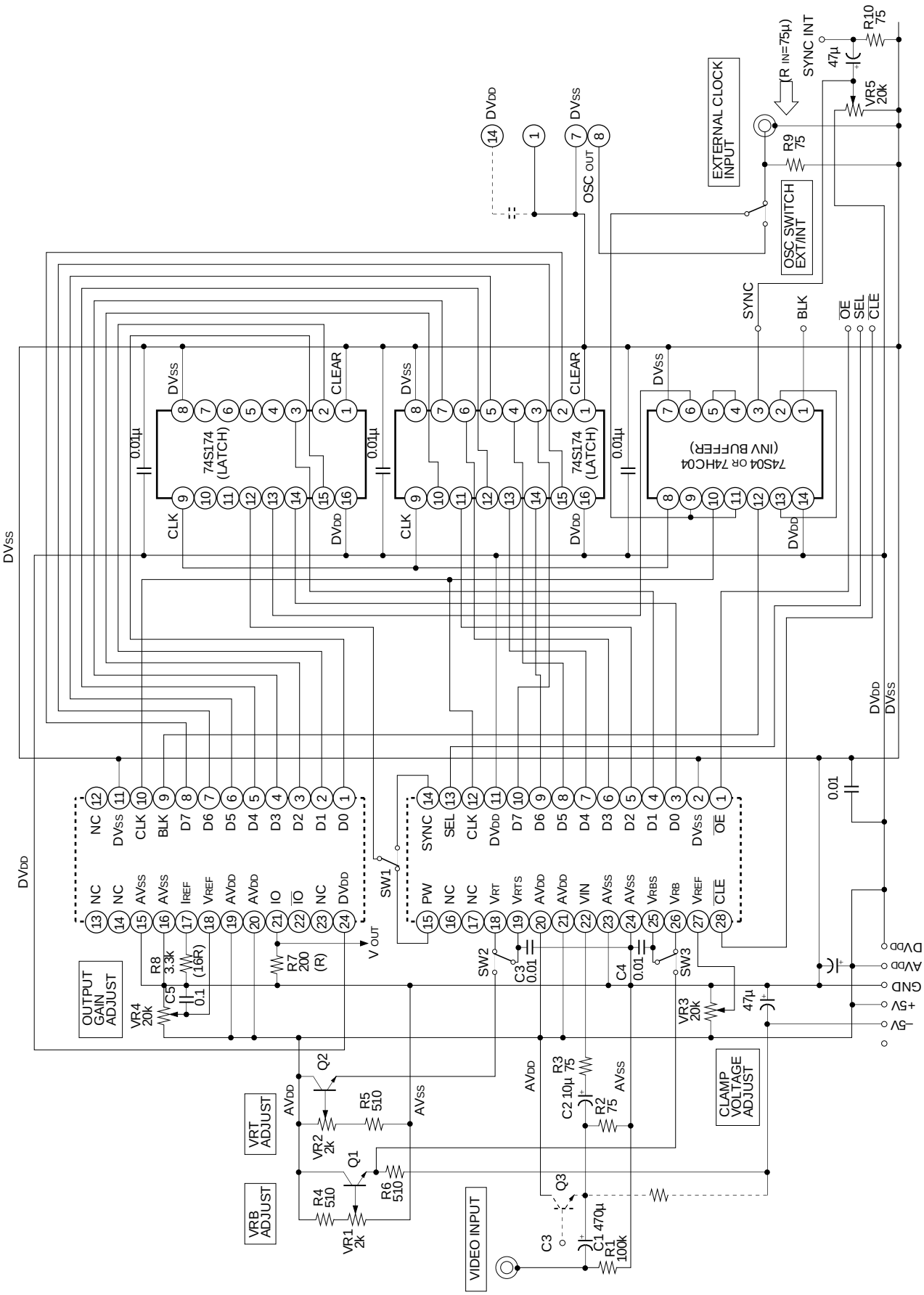
Analog input voltage	Step	Digital output code MSB LSB
V_{RT}	0	0 0 0 0 0 0 0 0
:	:	:
:	127	0 1 1 1 1 1 1 1
:	128	1 0 0 0 0 0 0 0
:	:	:
V_{RB}	255	1 1 1 1 1 1 1 1

Timing Chart

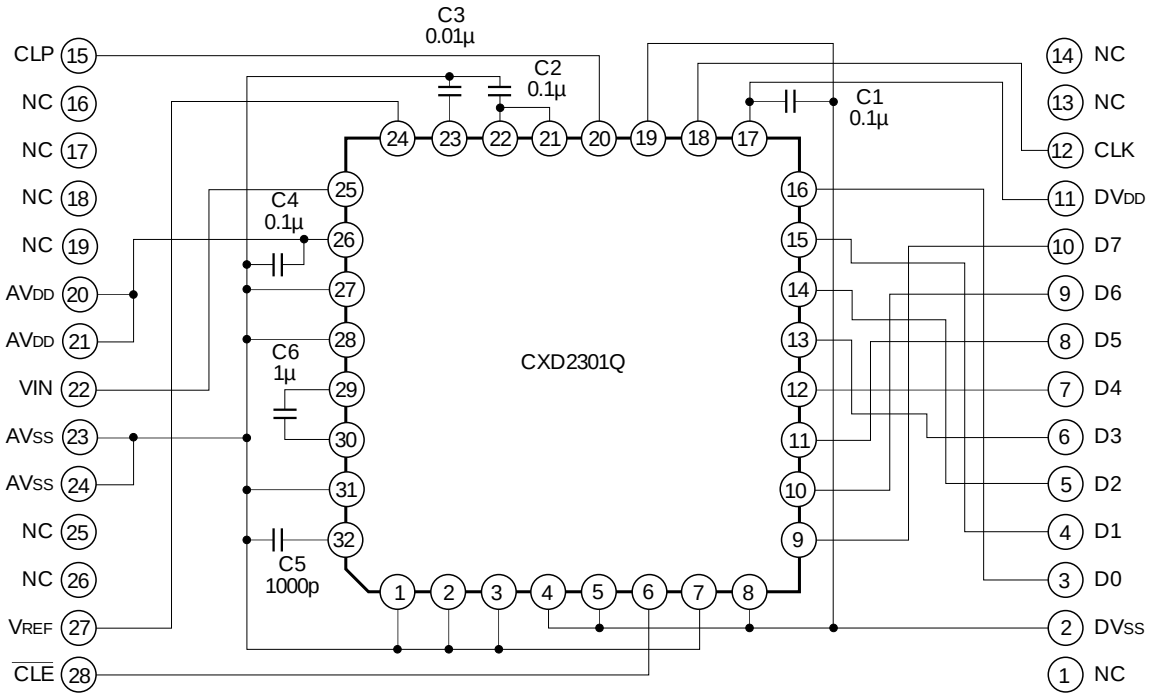


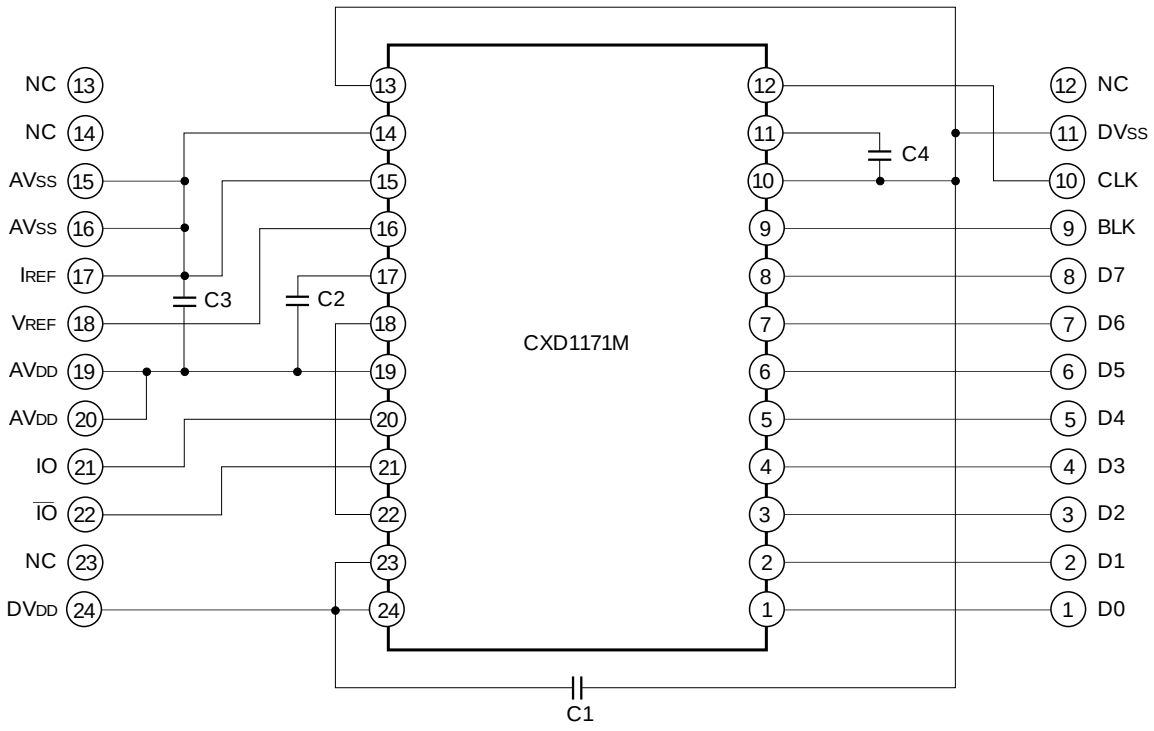
Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	16			ns
Clock Low time	T_{PW0}	16			ns
Clock Delay	Tdc			24	ns
Data delay AD	$t_{PD\ (AD)}$		13	25	ns
Data delay (latch)	t_{DD}			5	ns
Settling time	t_S	5			ns
Hold time	th	10			ns
Data delay DA	$t_{PD\ (DA)}$		10		ns

CMOS ADC/DAC Peripheral Circuit Board (Main Board)



CMOS ADC/DAC Peripheral Circuit Board (Sub Board)





List of Parts

resitance	
R1	100k
R2	75Ω
R3	75Ω
R4	510Ω
R5	510Ω
R6	510Ω
R7	R = 200
R8	18R ≈ 3.3k
R9	75Ω
R10	75Ω
VR1	2k
VR2	2k
VR3	20k
VR4	20k
VR5	20k

transistor	
Q1	2SC2785
Q2	2SC2785
Q3	2SC2785

ic	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator
OSC

others	
connector	BNC071
SW	AT1D2M3

capacitance	
C1	470µF/6.3V (chemical)
C2	10µF/16V (chemical)
C3	0.01µF
C4	0.01µF
C5	0.1µF
C6	0.1µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	47µF/10V (chemical)
C12	47µF/10V (chemical)
C13	47µF/10V (chemical)
C14	0.1µF

Adjustment

1. Vref adjustment (VR1, VR2)
   Adjustment of A/D converter reference voltage. V_{RB} is adjusted through VR1 and V_{RT} through VR2. When self bias is used, there is no need for adjustment. Reference voltage is set through self bias at delivery.

2. Setting of clamp reference voltage (VR3)
   Clamp reference voltage is set.

3. DAC output full scale adjustment (VR4)
   Full scale voltage of D/A converter output is adjusted at the PCB shipment, the full scale voltage is adjusted to approx. 2V.

4. Sync (clamp) pulse interface (VR5)
   This adjustment enables interface with the signal generator and others at the PCB shipment, adjustment is performed to obtain a threshold of approx. 2.5V to an H sync of 0 to 5V.

5. $\overline{OE}$, SEL, Sync, BLK, $\overline{CLE}$, Sync INT
   The following pins are set on the main board: Sync, $\overline{CLE}$, Sync INT (CXD2301Q) and BLK (CXD1171M), OE, SEL (not used). For the pins function, refer to the specifications. The difference between Sync pin and Sync INT pin is that you input a pulse above 3.5Vp-p to Sync INT pin. The pulse threshold is set through VR5. For input through Sync pin, pulse is input at TTL or CMOS level. In this case cut off the junction line between Sync pin and Sync INT pin.
   At the PCB shipment the main board pins are set as follows.
   - $\overline{OE}$ ····· Low
   - SEL ····· Low
   - Sync ····· Line junction with Sync INT pin
   - $\overline{CLE}$ ····· Low (Clamp function ON)
   - BLK ····· Low (Blanking OFF)

6. Clamp pulse input method
   The clamp pulse is directly input to CXD2301Q as show in Application Circuit examples (1) and (2). Use the direct input that is set at the PCB shipment.

Points on the PCB Pattern Layout

1. Set the layout not to have Digital current flow into Analog GND (Part 1). (For 1, see P.17 Component side diagram.)

2. At CXD2301Q sub board, C_2 and C_3 capacitors serve the important role of bringing out CXD2301Q's full performance.
   These are over 0.1µF (ceramic) capacitors with good high frequency characteristics. Layout as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) are on a common voltage and power source. Keeping ADC's DV_{SS} (Part 2) as close as possible to the voltage supply source will provide better results. That is, a layout where ADC is close to the voltage supply source, is recommended. (For 2, see P.17 Component side diagram.)

4. ADC samples analog signals at the clock falling edge point. Accordingly clocks supplied to ADC should not have any jitter.

5. The PCB layout shows ADC and DAC's Analog GND independently from the voltage supply source. The layout aims at providing an independent evaluation of ADC and DAC, as much as possible. On the actual board, common use will not cause any problems.

Notes on Operation

1. Reference voltage
   By shorting V_{RT} and V_{RTS}, V_{RB} and V_{RBS}, CXD2301 has the self bias function that generates V_{RT} = about 2.6V and V_{RB} = about 0.5V. On the PCB, either self bias or the external reference voltage can be selected depending on the junction method of the jumper line. At shipment from the factory, reference voltage is provided in self bias. Also, to provide external reference voltage, adjust the dynamic range (V_{RT} – V_{RB}) to above 1.8Vp-p.

2. Clock input
   There are 2 modes for the PCB clock input.
   1) Provided from the external signal generator (External clock)
   2) Using the crystal oscillator (built-in clock driver). (Internal clock)
   The 2 modes are selected using the switch on the PCB.

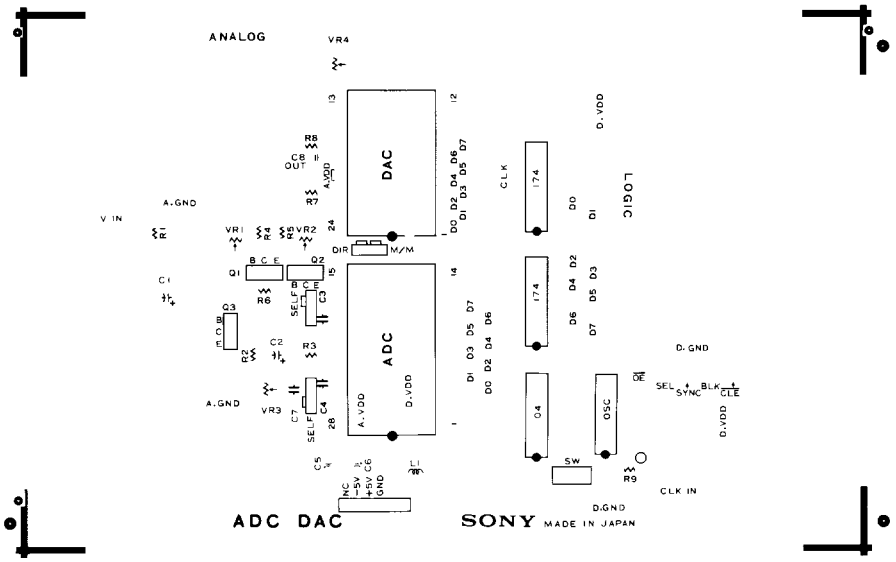
3. The 2 Latch IC's (74S174) are not absolutely necessary for the evaluation of ADC and DAC. That is, operation will still be normal if ADC output data is directly input to DAC input. However, as ADC output data is hardly ever D/A converted without executing Digital signal processing, it was mounted to indicate an example layout of Digital signal processing IC. When the ADC output data is used, use the output of the latch IC.

4. When $\overline{\text{clamp}}$ is not used
   Turning CLE to H will set OFF the clamp function. In this case, the DC element is cut off by means of C_2 on the main board and DC voltage on the ADC side of C_2 turns to about (V_{RT} + V_{RB}). To transfer DC elements of input signals, short C_2. At that time, it is necessary to bias input signals, but keeping R_2 open, Q_3 can also be used as buffer. Use the open space for the bias circuit.

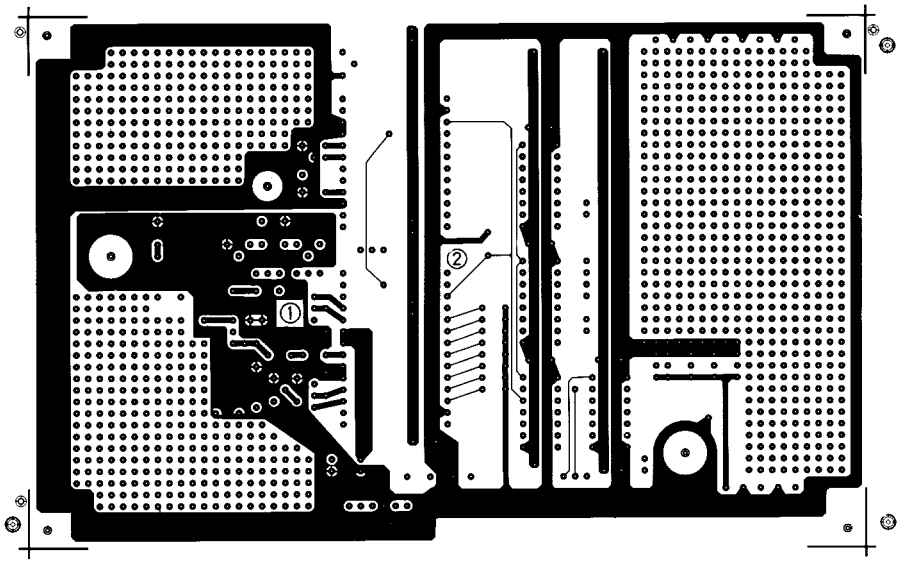
5. Clamp pulse latch
   On the evaluation board, the clamp pulse is latched with ADC sampling CLK and then input to the CLP pin. This is to minimize Vsag due the synchronizing of noise and clamp pulse beat elements with GND sampling clock around ADC. If there are no problems with Vsag, latch is not necessary.

6. Peripheral through hole
   There is a group of through holes on the Analog input, output and Logic. These are to be used when mounting additional circuits to the PCB. Use when necessary.
   The connector hole on DAC part is used to mount the test chassis and the mount jack.

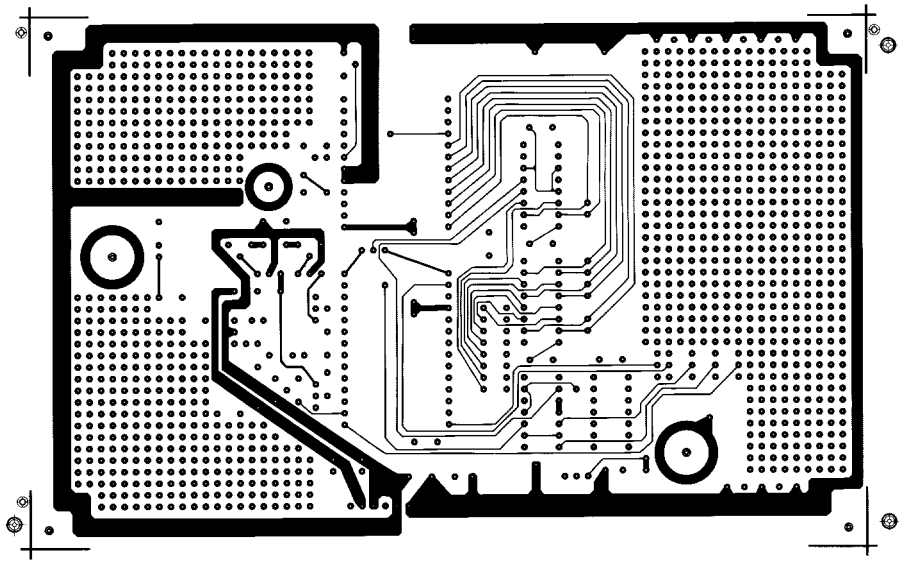
Silk Side



Component Side

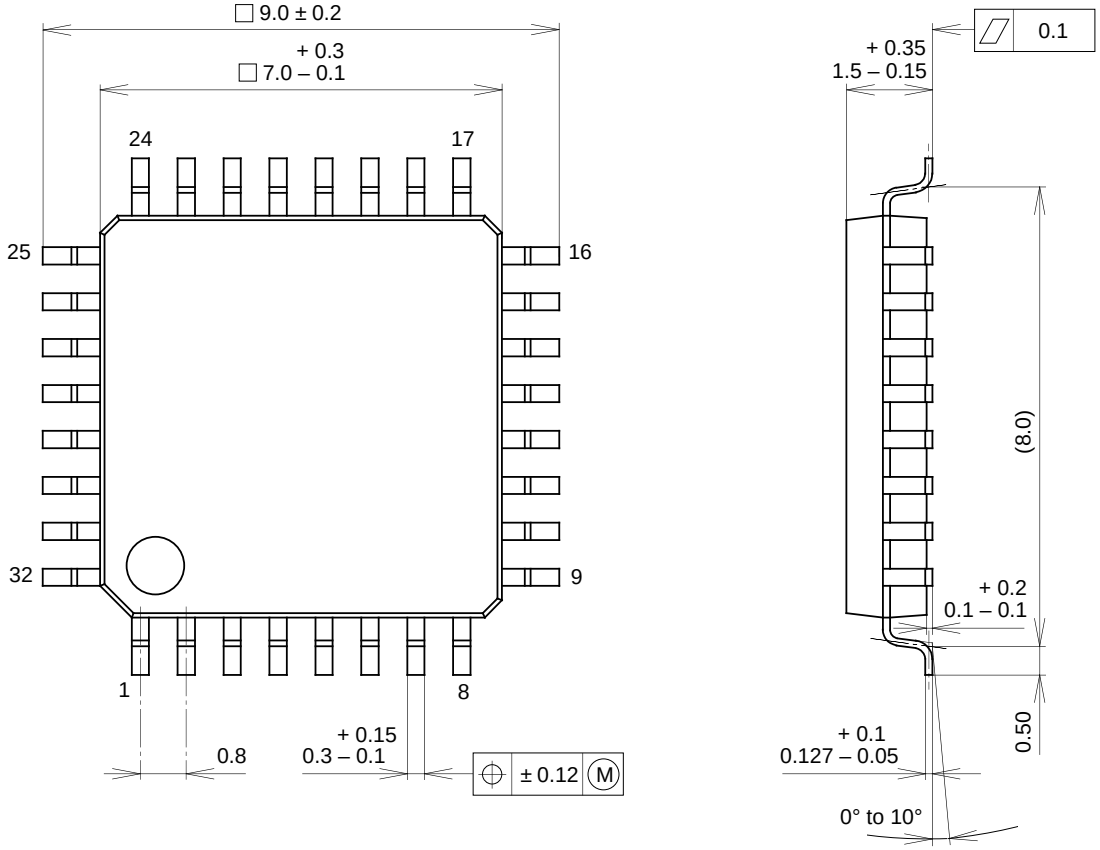


Soldering Side (Diagram seen from the component side)



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	∗QFP032-P-0707-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g