SONY

CXD2492R

Timing Generator for Frame Readout CCD Image Sensor

For the availability of this product, please contact the sales office.

Description

The CXD2492R is a timing generator IC which generates the timing pulses for performing frame readout using the ICX252 CCD image sensor.

Features

- Base oscillation frequency 24 to 36MHz
- High-speed/low-speed shutter function
- Draft (sextuple speed)/AF (auto focus) drive
- Horizontal driver for CCD image sensor
- Vertical driver for CCD image sensor

Applications

Digital still cameras

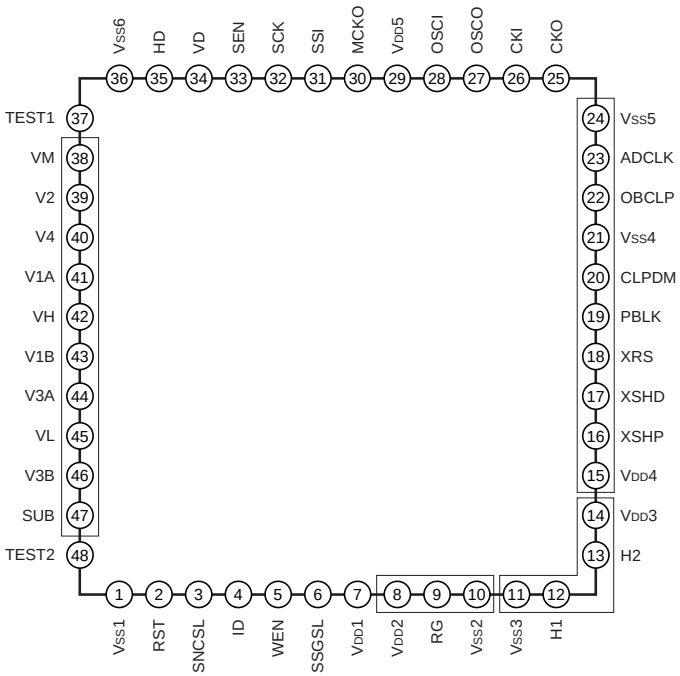
Structure

Silicon gate CMOS IC

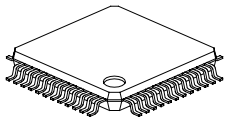
Applicable CCD Image Sensors

ICX252 (Type 1/1.8, 3240K pixels)

Pin Configuration



48 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.3 to +7.0	V
	V_L	–10.0 to V_{SS}	V
	V_H	V_L – 0.3 to +26.0	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_{O1}	V_{SS} – 0.3 to V_{DD} + 0.3	V
	V_{O2}	V_L – 0.3 to V_{SS} + 0.3	V
	V_{O3}	V_L – 0.3 to V_H + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

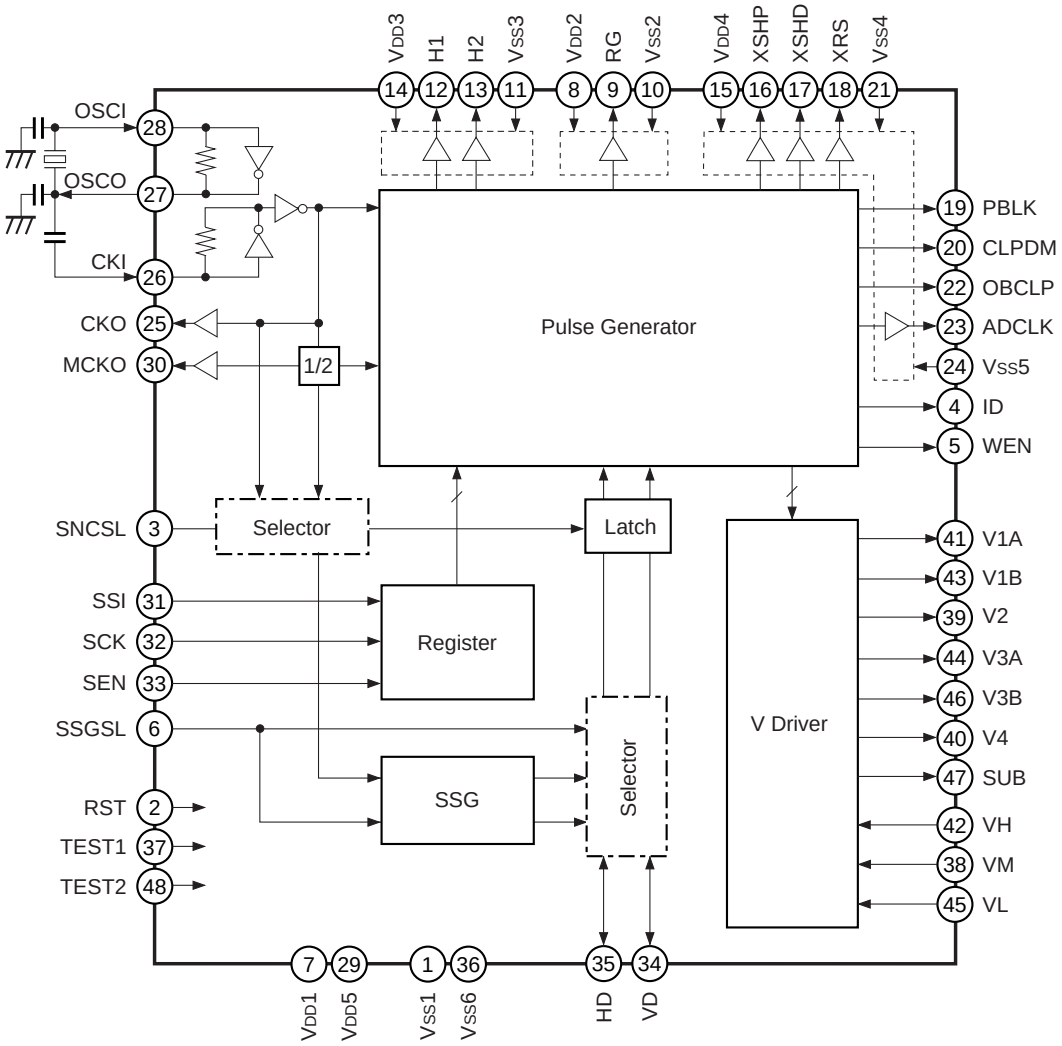
Recommended Operating Conditions

• Supply voltage	V_{DD}b	3.0 to 5.5	V
	V_{DD}a, V_{DD}c, V_{DD}d		
		3.0 to 3.6	V
	V_M	0.0	V
	V_H	14.5 to 15.5	V
	V_L	–7.0 to –8.0	V
• Operating temperature			
	Topr	–20 to +75	°C

* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

E99730-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{SS}1$	—	GND
2	RST	I	Internal system reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input/No protective diode on power supply side
3	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync With pull-down resistor
4	ID	O	Vertical direction line identification pulse output.
5	WEN	O	Memory write timing pulse output.
6	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External sync valid With pull-down resistor
7	$V_{DD}1$	—	3.3V power supply. (Power supply for common logic block)
8	$V_{DD}2$	—	3.3V power supply. (Power supply for RG)
9	RG	O	CCD reset gate pulse output.
10	$V_{SS}2$	—	GND
11	$V_{SS}3$	—	GND
12	H1	O	CCD horizontal register clock output.
13	H2	O	CCD horizontal register clock output.
14	$V_{DD}3$	—	3.3 to 5.0V power supply. (Power supply for H1/H2)
15	$V_{DD}4$	—	3.3V power supply. (Power supply for CDS block)
16	XSHP	O	CCD precharge level sample-and-hold pulse output.
17	XSHD	O	CCD data level sample-and-hold pulse output.
18	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment.
19	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
20	CLPDM	O	CCD dummy signal clamp pulse output.
21	$V_{SS}4$	—	GND
22	OBCLP	O	CCD optical black signal clamp pulse output.
23	ADCLK	O	Clock output for analog/digital conversion IC. Logical phase adjustment possible using the serial interface data.
24	$V_{SS}5$	—	GND
25	CKO	O	Inverter output.
26	CKI	I	Inverter input.
27	OSCO	O	Inverter output for oscillation. When not used, leave open or connect a capacitor.
28	OSCI	I	Inverter input for oscillation. When not used, fix low.
29	$V_{DD}5$	—	3.3V power supply. (Power supply for common logic block)
30	MCKO	O	System clock output for signal processing IC.

Pin No.	Symbol	I/O	Description
31	SSI	I	Serial interface data input for internal mode settings. Schmitt trigger input/No protective diode on power supply side
32	SCK	I	Serial interface clock input for internal mode settings. Schmitt trigger input/No protective diode on power supply side
33	SEN	I	Serial interface strobe input for internal mode settings. Schmitt trigger input/No protective diode on power supply side
34	VD	I/O	Vertical sync signal input/output.
35	HD	I/O	Horizontal sync signal input/output.
36	$V_{SS}6$	—	GND
37	TEST1	I	IC test pin 1; normally fixed to GND. With pull-down resistor
38	VM	—	GND (GND for vertical driver)
39	V2	O	CCD vertical register clock output.
40	V4	O	CCD vertical register clock output.
41	V1A	O	CCD vertical register clock output.
42	VH	—	15.0V power supply. (Power supply for vertical driver)
43	V1B	O	CCD vertical register clock output.
44	V3A	O	CCD vertical register clock output.
45	VL	—	–7.5V power supply. (Power supply for vertical driver)
46	V3B	O	CCD vertical register clock output.
47	SUB	O	CCD electronic shutter pulse output.
48	TEST2	I	IC test pin 2; normally fixed to GND. With pull-down resistor

Electrical Characteristics

DC Characteristics (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD2}	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	V_{DD3}	$V_{DD}b$		3.0	3.3	5.5	V
Supply voltage 3	V_{DD4}	$V_{DD}c$		3.0	3.3	3.6	V
Supply voltage 4	V_{DD1}, V_{DD5}	$V_{DD}d$		3.0	3.3	3.6	V
Input voltage 1*1	RST	V_{t+}		0.8V_{DD}d			V
		V_{t-}				0.2V_{DD}d	V
Input voltage 2*2	SSI, SCK, SEN,	V_{t+}		0.8V_{DD}d			V
		V_{t-}				0.2V_{DD}d	V
Input voltage 3*3	TEST1, TEST2	V_{IH1}		0.7V_{DD}d			V
		V_{IL1}				0.2V_{DD}d	V
Input voltage 4*4	SNCSL, SSGSL	V_{IH2}		0.7V_{DD}d			V
		V_{IL2}				0.3V_{DD}d	V
Input/output voltage	VD, HD	V_{IH3}		0.8V_{DD}d			V
		V_{IL3}				0.2V_{DD}d	V
		V_{OH1}	Feed current where I_{OH} = –1.2mA	V_{DD}d – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 1	H1, H2	V_{OH2}	Feed current where I_{OH} = –22.0mA	V_{DD}b – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 14.4mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	V_{DD}a – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, XRS, PBLK, OBCLP, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	V_{DD}c – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	CKO	V_{OH5}	Feed current where I_{OH} = –6.9mA	V_{DD}d – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 5	MCKO	V_{OH6}	Feed current where I_{OH} = –3.3mA	V_{DD}d – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output current 1	V1A, V1B, V3A, V3B, V2, V4	I_{OL}	V1A/B, V2, V3A/B, V4 = –8.25V	10.0			mA
		I_{OM1}	V1A/B, V2, V3A/B, V4 = –0.25V			–5.0	mA
		I_{OM2}	V1A/B, V3A/B = 0.25V	5.0			mA
		I_{OH}	V1A/B, V3A/B = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 This input pin is a schmitt trigger input and it does not have protective diode of the power supply side in the IC.
*2 These input pins are schmitt trigger inputs.
*3 These input pins are with pull-down resistor in the IC.
*4 These input pins are with pull-down resistor in the IC and they do not have protective diode of the power supply side in the IC.

Note) The above table indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DD}d/2$		V
Input voltage	OSCI	V_{IH}		$0.7V_{DD}d$			V
		V_{IL}				$0.3V_{DD}d$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –3.6mA	$V_{DD}d$ – 0.8			V
		V_{OL}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	$V_{IN} = V_{DD}d$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DD}d/2$		V
Input voltage		V_{IH}		$0.7V_{DD}d$			V
		V_{IL}				$0.3V_{DD}d$	V
Input amplitude		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

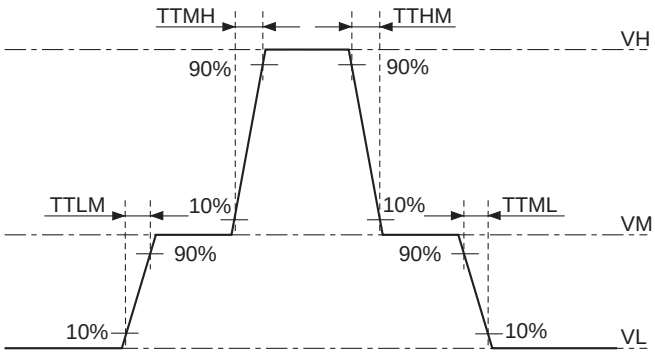
Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

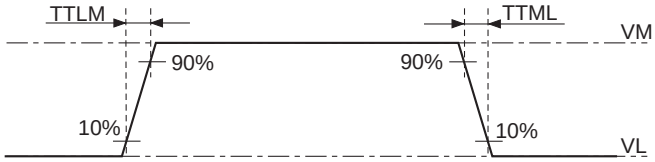
Notes) 1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3. To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

Switching Waveforms

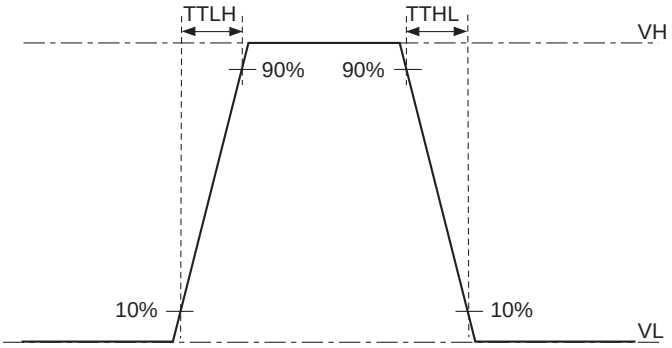
V1A (V1B, V3A, V3B)



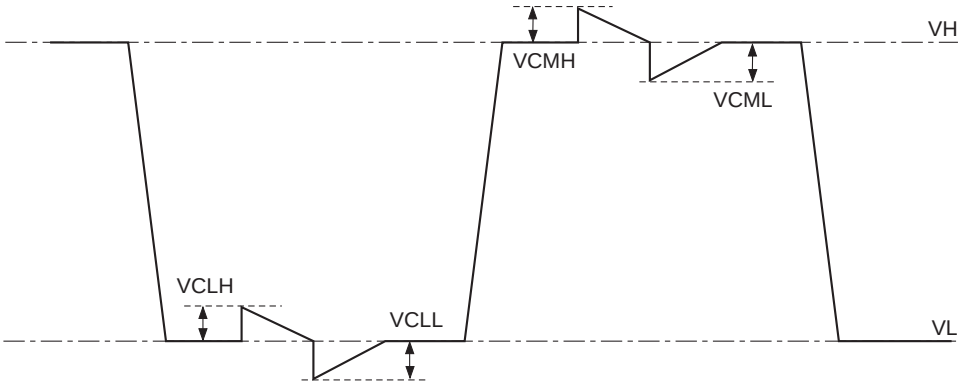
V2 (V4)



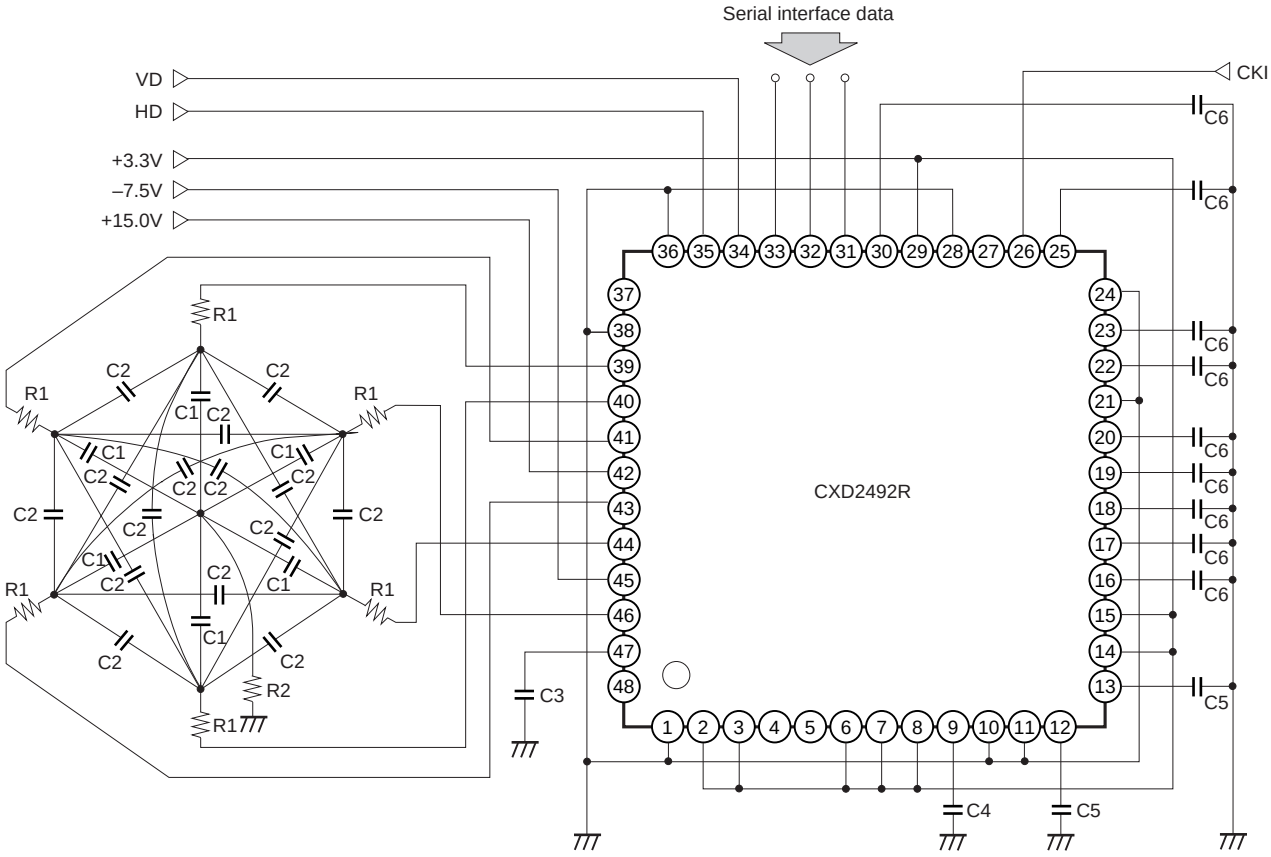
SUB



Waveform Noise



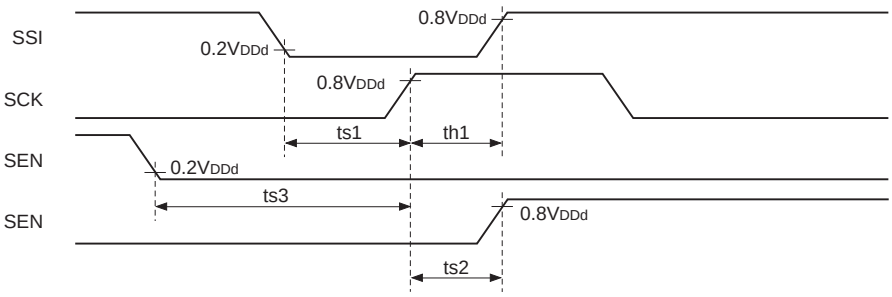
Measurement Circuit



C1 3300pF C2 560pF C3 820pF C4 30pF C5 215pF C6 10pF
R1 30Ω R2 10Ω

AC Characteristics

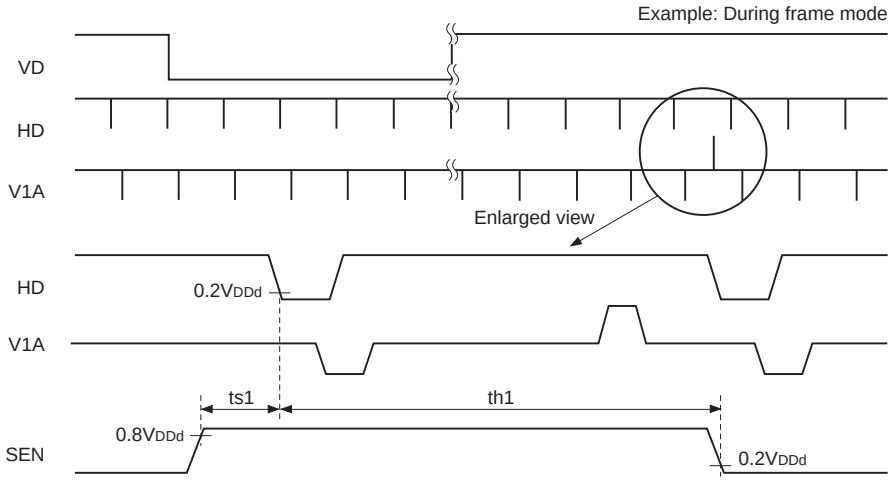
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SCK	20			ns
th1	SSI hold time, activated by the rising edge of SCK	20			ns
ts2	SCK setup time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SCK	20			ns

Serial interface clock internal loading characteristics (1)

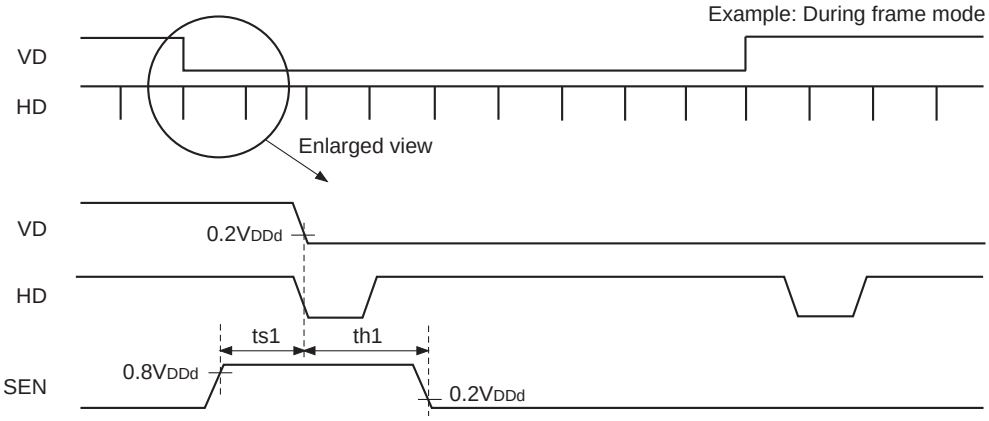


* Be sure to maintain a constantly high SEN logic level near the falling edge of the HD in the horizontal period during which V1A/B and V3A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of HD	0			ns
th1	SEN hold time, activated by the falling edge of HD	102			µs

Serial interface clock internal loading characteristics (2)



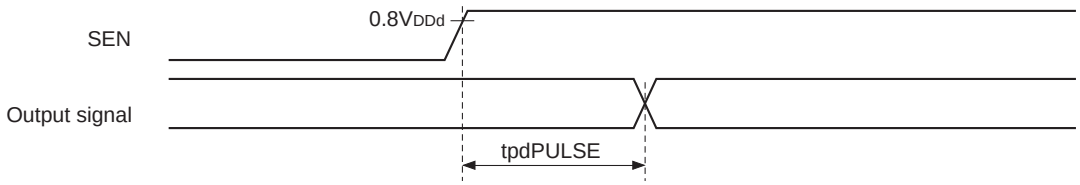
* Be sure to maintain a constantly high SEN logic level near the falling edge of VD.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of VD	0			ns
th1	SEN hold time, activated by the falling edge of VD	200			ns

Serial interface clock output variation characteristics

Normally, the serial interface data is loaded to the CXD2492R at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD2492R and controlled at the rising edge of SEN. See "Description of Operation".



(Within the recommended operating conditions)

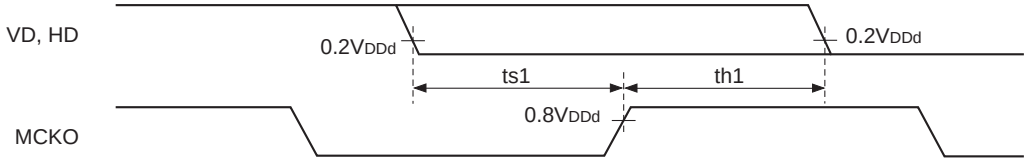
Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		100	ns

RST loading characteristics

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

VD and HD loading characteristics

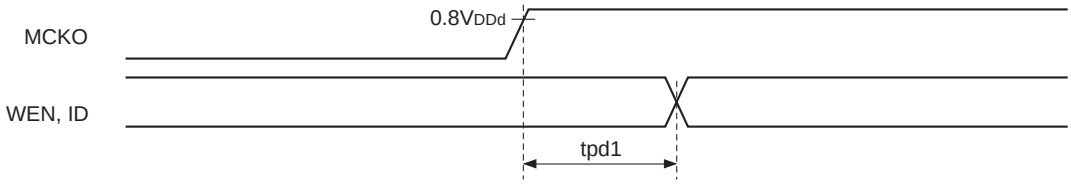


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VD and HD setup time, activated by the rising edge of MCKO	20			ns
th1	VD and HD hold time, activated by the rising edge of MCKO	5			ns

Output variation characteristics



WEN and ID load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	20		60	ns

Description of Operation

Pulses output from the CXD2492R are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on the following pages.

Pin Status Table

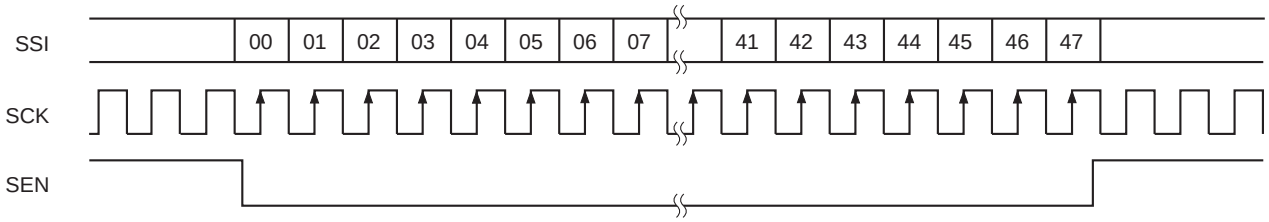
Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
1	$V_{SS}1$	—				25	CKO	ACT	ACT	L	ACT
2	RST	ACT	ACT	ACT	L	26	CKI	ACT	ACT	ACT	ACT
3	SNCSL	ACT	ACT	ACT	ACT	27	OSCO	ACT	ACT	ACT	ACT
4	ID	ACT	L	L	L	28	OSCI	ACT	ACT	ACT	ACT
5	WEN	ACT	L	L	L	29	$V_{DD}5$	—			
6	SSGSL	ACT	ACT	ACT	ACT	30	MCKO	ACT	ACT	L	ACT
7	$V_{DD}1$	—				31	SSI	ACT	ACT	ACT	DIS
8	$V_{DD}2$	—				32	SCK	ACT	ACT	ACT	DIS
9	RG	ACT	L	L	ACT	33	SEN	ACT	ACT	ACT	DIS
10	$V_{SS}2$	—				34	VD*1	ACT	L	L	H
11	$V_{SS}3$	—				35	HD*1	ACT	L	L	H
12	H1	ACT	L	L	ACT	36	$V_{SS}6$	—			
13	H2	ACT	L	L	ACT	37	TEST1	—			
14	$V_{DD}3$	—				38	VM	—			
15	$V_{DD}4$	—				39	V2	ACT	VM	VM	VM
16	XSHP	ACT	L	L	ACT	40	V4	ACT	VM	VM	VL
17	XSHD	ACT	L	L	ACT	41	V1A	ACT	VH	VH	VM
18	XRS	ACT	L	L	ACT	42	VH	—			
19	PBLK	ACT	L	L	H	43	V1B	ACT	VH	VH	VM
20	CLPDM	ACT	L	L	H	44	V3A	ACT	VH	VH	VL
21	$V_{SS}4$	—				45	VL	—			
22	OBCLP	ACT	L	L	H	46	V3B	ACT	VH	VH	VL
23	ADCLK	ACT	L	L	ACT	47	SUB	ACT	VH	VH	VL
24	$V_{SS}5$	—				48	TEST2	—			

*1 It is for output. For input, all items are "ACT".

Note) ACT means that the circuit is operating, and DIS means that loading is stopped.
L indicates a low output level, and H a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin 42), VM (Pin 38) and VL (Pin 45), respectively, in the controlled status.

Serial Interface Control

The CXD2492R basically loads and reflects the serial interface data sent in the following format in the readout portion at the falling edge of HD. Here, readout portion specifies the horizontal period during which V1A/B and V3A/B, etc. take the ternary value.
Note that some items reflect the serial interface data at the falling edge of VD or the rising edge of SEN.



There are two categories of serial interface data: CXD2492R drive control data (hereafter "control data") and electronic shutter data (hereafter "shutter data").
The details of each data are described below.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D12	MODE	Drive mode switching	See D10 to D12 MODE.		All 0
D13 to D14	SMD	Electronic shutter mode switching	See D13 to D14 SMD.		All 0
D15	PTSG	Internal SSG output pattern switching	NTSC equivalent	PAL equivalent	0
D16 to D23	CDAT	AF drive control data	See D16 to D23 CDAT.		All 0
D24 to D33	—	—	—	—	All 0
D34	—	—	—	—	1
D35	—	—	—	—	0
D36 to D37	LDAD	ADCLK logic phase switching	See D36 to D37 LDAD.		1 0
D38 to D39	STB	Standby control	See D38 to D39 STB.		All 0
D40 to D47	—	—	—	—	All 0

Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08 to D09	CTG	Category switching	See D08 to D09 CTG.		All 0
D10 to D19	SVD	Electronic shutter vertical period specification	See D10 to D19 SVD.		All 0
D20 to D31	SHD	Electronic shutter horizontal period specification	See D20 to D31 SHD.		All 0
D32 to D41	SPL	High-speed shutter position specification	See D32 to D41 SPL.		All 0
D42 to D47	—	—	—	—	All 0

Detailed Description of Each Data

Shared data: D08 to D09 CTG [Category]

Of the data provided to the CXD2492R by the serial interface, the CXD2492R loads D10 and subsequent data to each data register as shown in the table below according to the combination of D08 and D09.

D09	D08	Description of operation
0	0	Loading to control data register
0	1	Loading to shutter data register
1	X	Test mode

Note that the CXD2492R can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D10 to D12 MODE [Drive mode]

The CXD2492R drive mode can be switched as follows. However, the drive mode bits are loaded to the CXD2492R and reflected at the falling edge of VD.

D12	D11	D10	Description of operation
0	0	0	Draft mode (sextuple speed: default)
0	0	1	Frame mode (A field readout)
0	1	0	Frame mode (B field readout)
0	1	1	Frame mode
1	0	X	AF1 mode
1	1	X	AF2 mode

Control data: D15 PTSG [Internal SSG output pattern]

The CXD2492R internal SSG output pattern can be switched as follows. However, the drive mode bits are loaded to the CXD2492R and reflected at the falling edge of VD.

D15	Description of Operation
0	NTSC equivalent pattern
1	PAL equivalent pattern

VD period in each pattern is defined as follows.

	Frame mode	Draft mode	AF1 mode	AF2 mode
NTSC equivalent pattern	918H + 1716ck	262H + 1144ck	131H + 572ck	65H + 1430ck
PAL equivalent pattern	945H*1	314H + 1568ck	157H + 784ck	78H + 1536ck

*1 Only 944H and 945H are 1208ck period.

See the Timing Charts for the actual operation.

Control data: D36 to D37 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is 90° relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: D38 to D39 STB [Standby]

The operating mode is switched as follows. However, the standby bits are loaded to the CXD2492R and control is applied immediately at the rising edge of SEN.

D39	D38	Symbol	Operating mode
X	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	1	STB	Standby mode

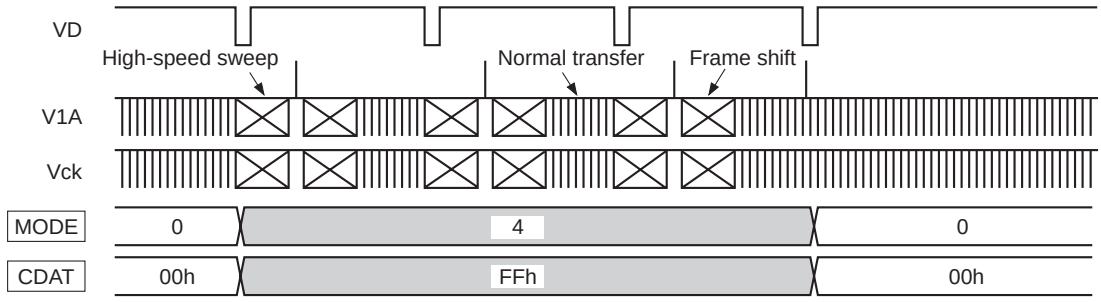
See the Pin Status Table for the pin status in each mode.

Control data: [AF drive]

The CXD2492R controls the drive of the vertical cut-out area of line in AF1/AF2 mode by using control data D16 to D23 CDAT. This mode has a function on purpose to raise frame rate for auto focus (AF), and this mode cannot support operation such as electrical image stabilization.

AF drive bits are loaded to the CXD2492R and reflected at the falling edge of VD. As shown in the figure below, first, the fixed stage is swept at high speed, and it goes to readout period and vertical OB period. Then normal transfer is performed equivalent to draft mode from the frame shift of the stage specified by the serial interface data to the timing of the falling edge of the next VD.

Therefore, the number of frame shift stages applied to CDAT and the control by VD period are conditions for its application.



The number of high-speed sweeps are different according to the selected mode. It is specified as follows.

AF1 mode: 138 stages (0 to 7H)
AF2 mode: 208 stages (0 to 11H)

The frame shift data is expressed as shown in the table below using D16 to D23 CDAT.

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16
0	1	1	0	1	0	0	1
	↓				↓		
	6				9		

→ CDAT is expressed as 69h.

Its definition area is specified as follows.

AF1 mode: 00h ≤ CDAT ≤ FFh (11 to 23H)
AF2 mode: 00h ≤ CDAT ≤ FFh (14 to 27H)

Control data/shutter data: [Electronic shutter]

The CXD2492R realizes various electronic shutter functions by using control data D13 to D14 SMD and shutter data D10 to D19 SVD, D20 to D31 SHD and D32 to D41 SPL.
These functions are described in detail below.
First, the various modes are shown below.
These modes are switched using control data D13 to D14 SMD.

D14	D13	Description of operation
0	0	Electronic shutter stopped mode
0	1	High-speed/low-speed shutter mode
1	0	
1	1	HTSG control mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHD as an example. However, MSB (D31) is a reserve bit for the future specification, and it is handled as dummy on this IC.

MSB											LSB
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

→ SHD is expressed as 1C3h.

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.
SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

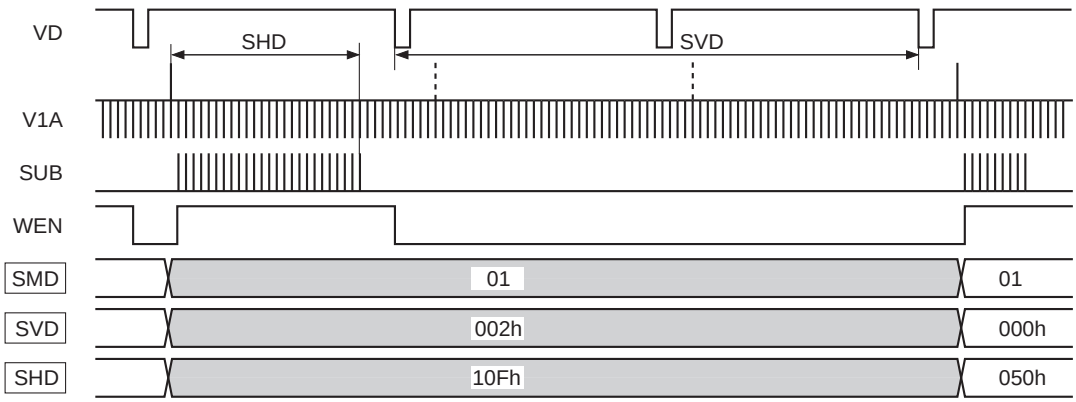
[High-speed/low-speed shutter mode]

During this mode, the shutter data items have the following meanings.

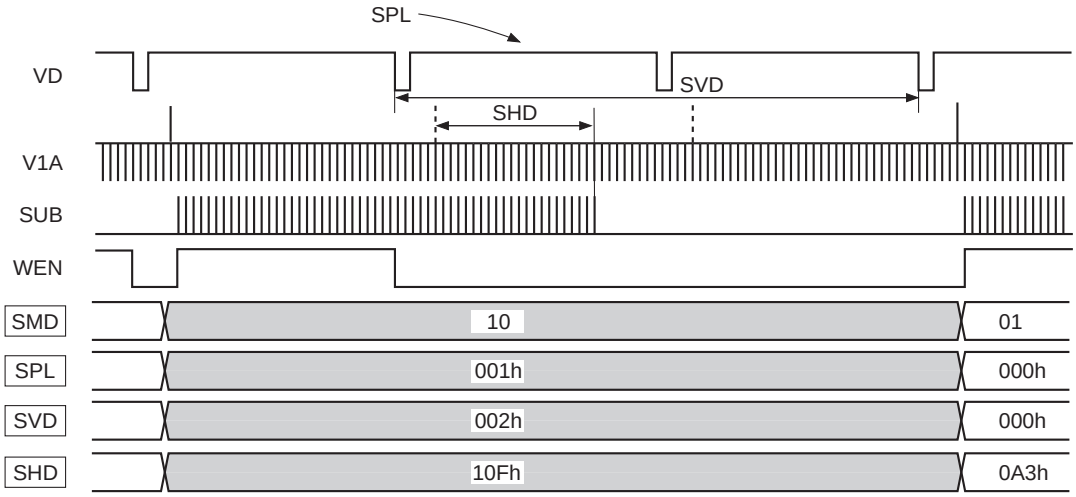
Symbol	Data	Description
SVD	D10 to D19	Number of vertical periods specification (000h ≤ SVD ≤ 3FFh)
SHD	D20 to D31	Number of horizontal periods specification (000h ≤ SHD ≤ 7FFh)
SPL	D32 to D41	Vertical period specification for high-speed shutter operation (000h ≤ SPL ≤ 3FFh)

The period during which SVD and SHD are specified together is the shutter speed. Concretely, when specifying high-speed shutter, SVD is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVD is set to "001h" or higher, the serial interface data is not loaded until this period is finished.
The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1). However, in the frame mode A field, it matches (number of SUB pulses + 1). This is a specification for flickerless when the same mode is repeated. But this change may not occur because of flickerless by the conditions during low-speed shutter.

Note) The bit data definition area is assured in terms of the CXD2492R functions, and does not assure the CCD characteristics.



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.
In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.



Incidentally, SPL is counted as "000h", "001h", "002h" and so on in conformance with SVD.
Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice versa.

[HTSG control mode]

During this mode, all shutter data items are invalid.

The V1A/B and V3A/B ternary level outputs are stopped, so the shutter speed is the value obtained by adding the shutter speed specified in the preceding vertical period to the vertical period during which these readout pulses are stopped as shown in the figure.

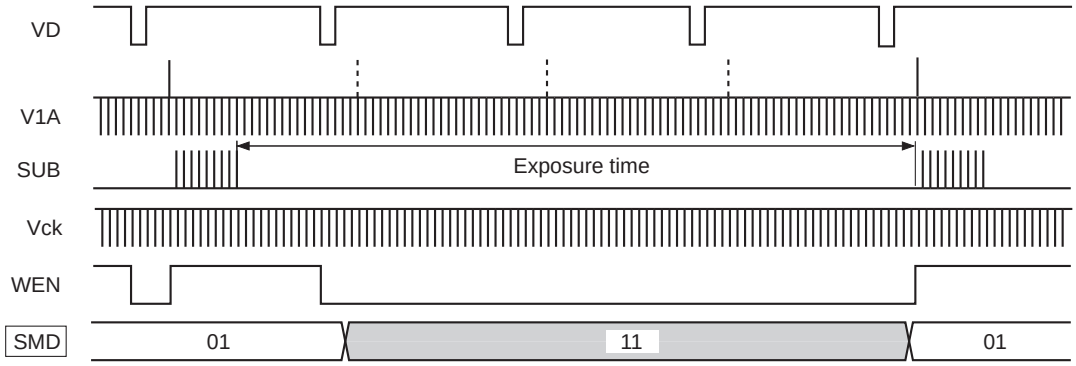
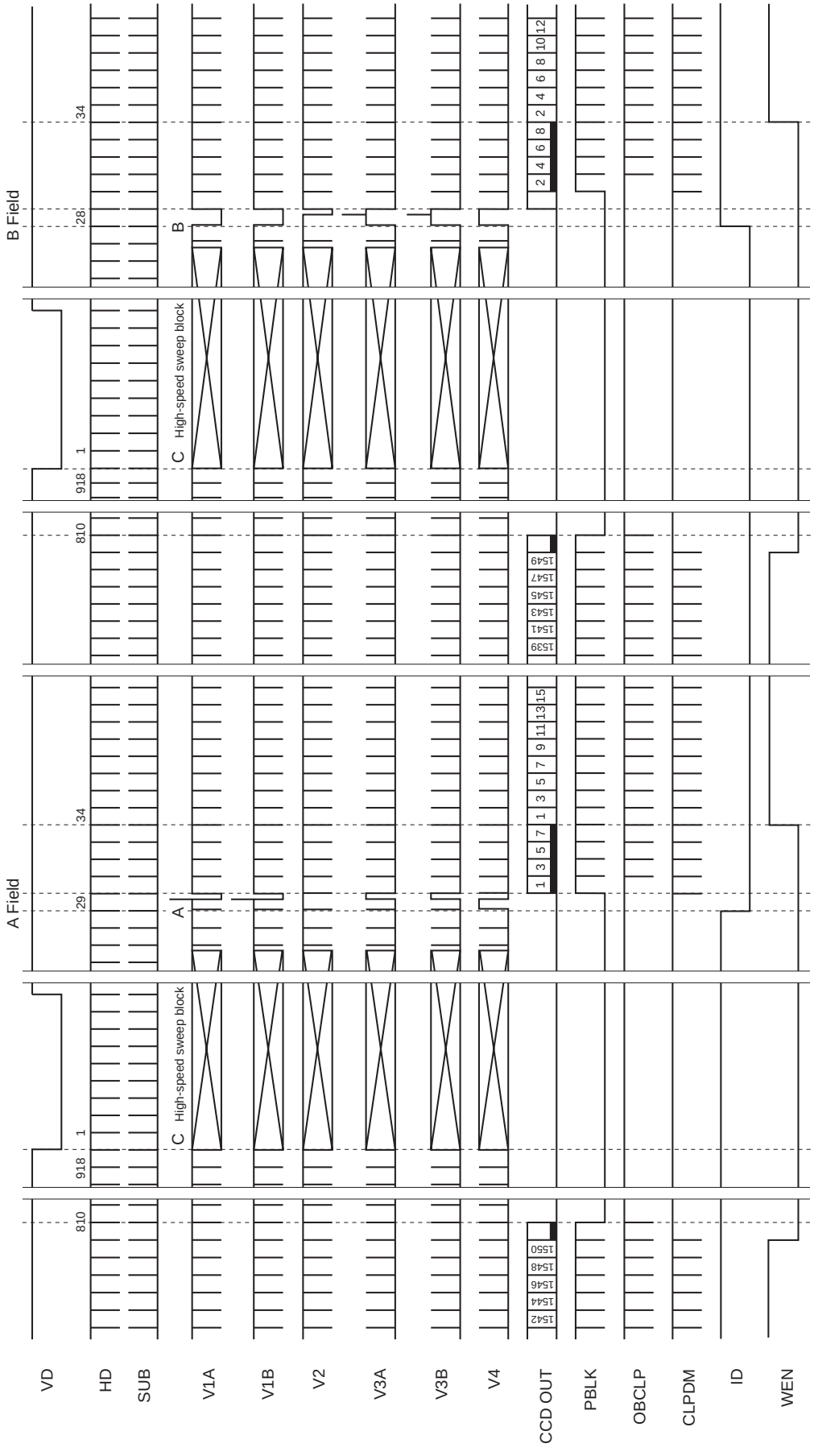


Chart-1 Vertical Direction Timing Chart

MODE
Frame mode

Applicable CCD image sensor
• ICX252

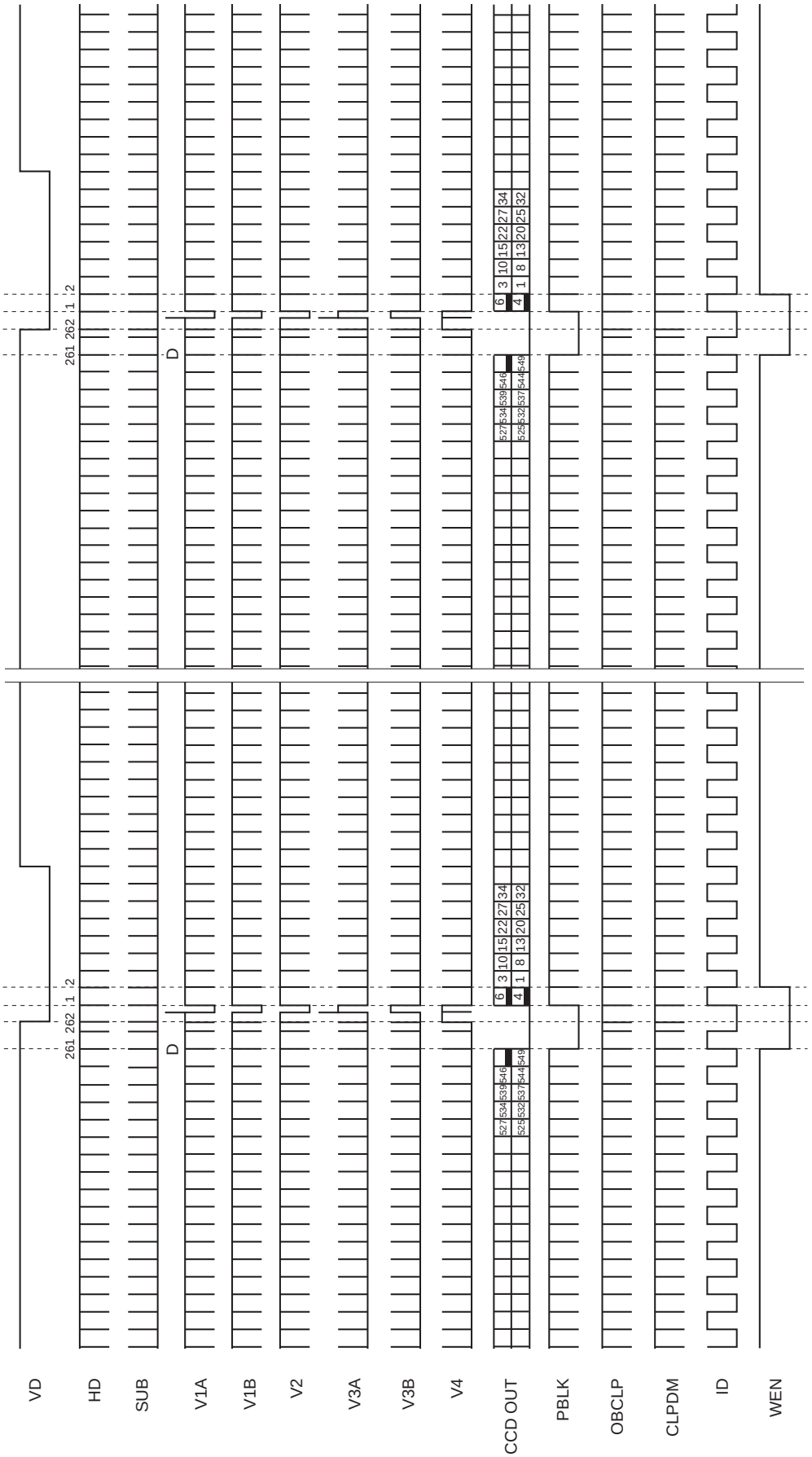


* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
* * ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* VD of this chart is NTSC equivalent pattern (918H + 1716ck units). For PAL equivalent pattern, it is 945H units, but 1208ck period as for 944H and 945H.

Chart-2 Vertical Direction Timing Chart

MODE
Draft mode

Applicable CCD image sensor
• ICX252



* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* VD of this chart is NTSC equivalent pattern (262H + 1144ck units). For PAL equivalent pattern, it is 314H + 1568ck units.

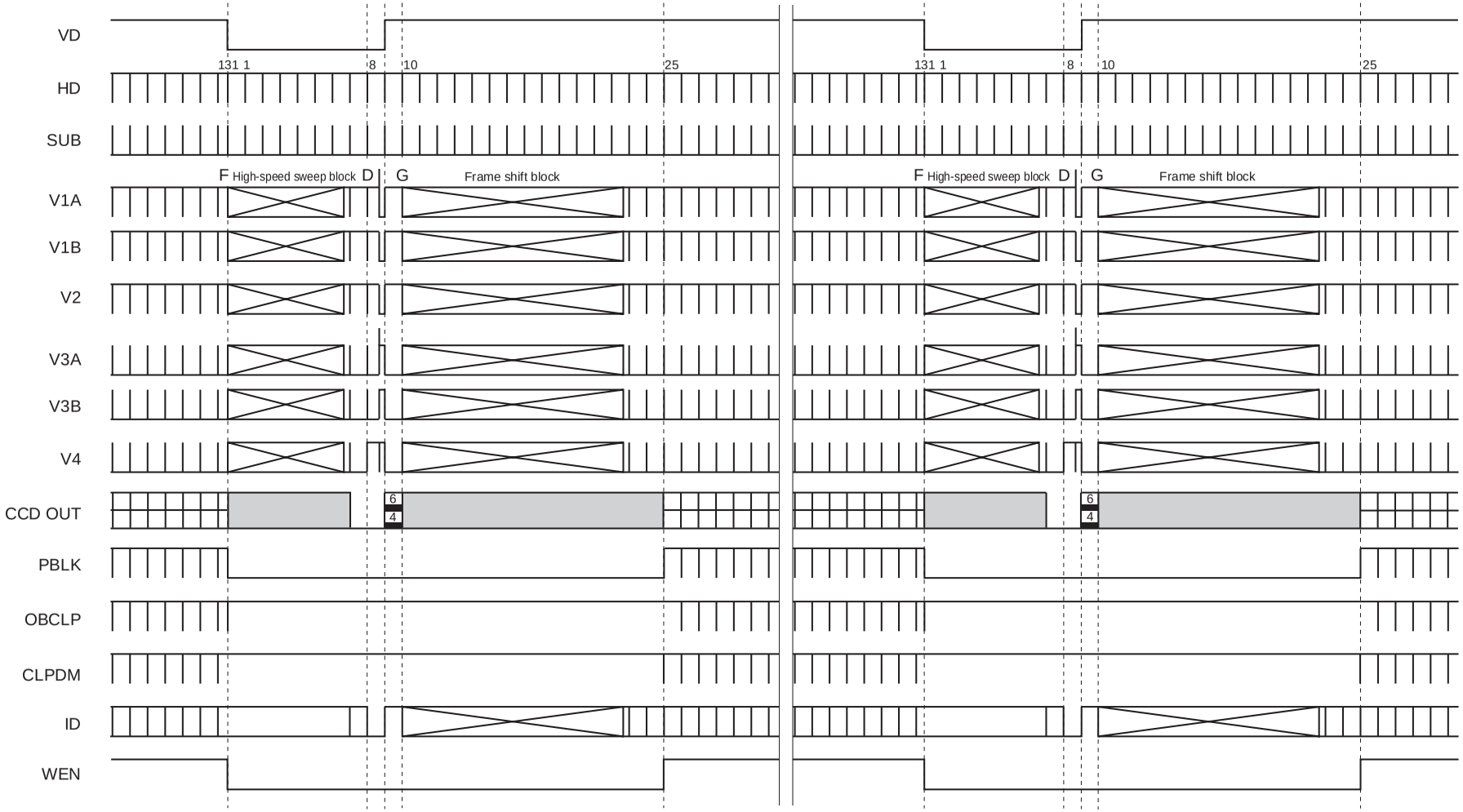
Chart-3 Vertical Direction Timing Chart

MODE

AF1 mode

Applicable CCD image sensor

• ICX252



* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* 138 stages are fixed for high-speed sweep block; 0 to 255 stages are specified by the serial interface for frame shift block.
* VD of this chart is NTSC equivalent pattern (131H + 572ck units). For PAL equivalent pattern, it is 157H + 784ck units.

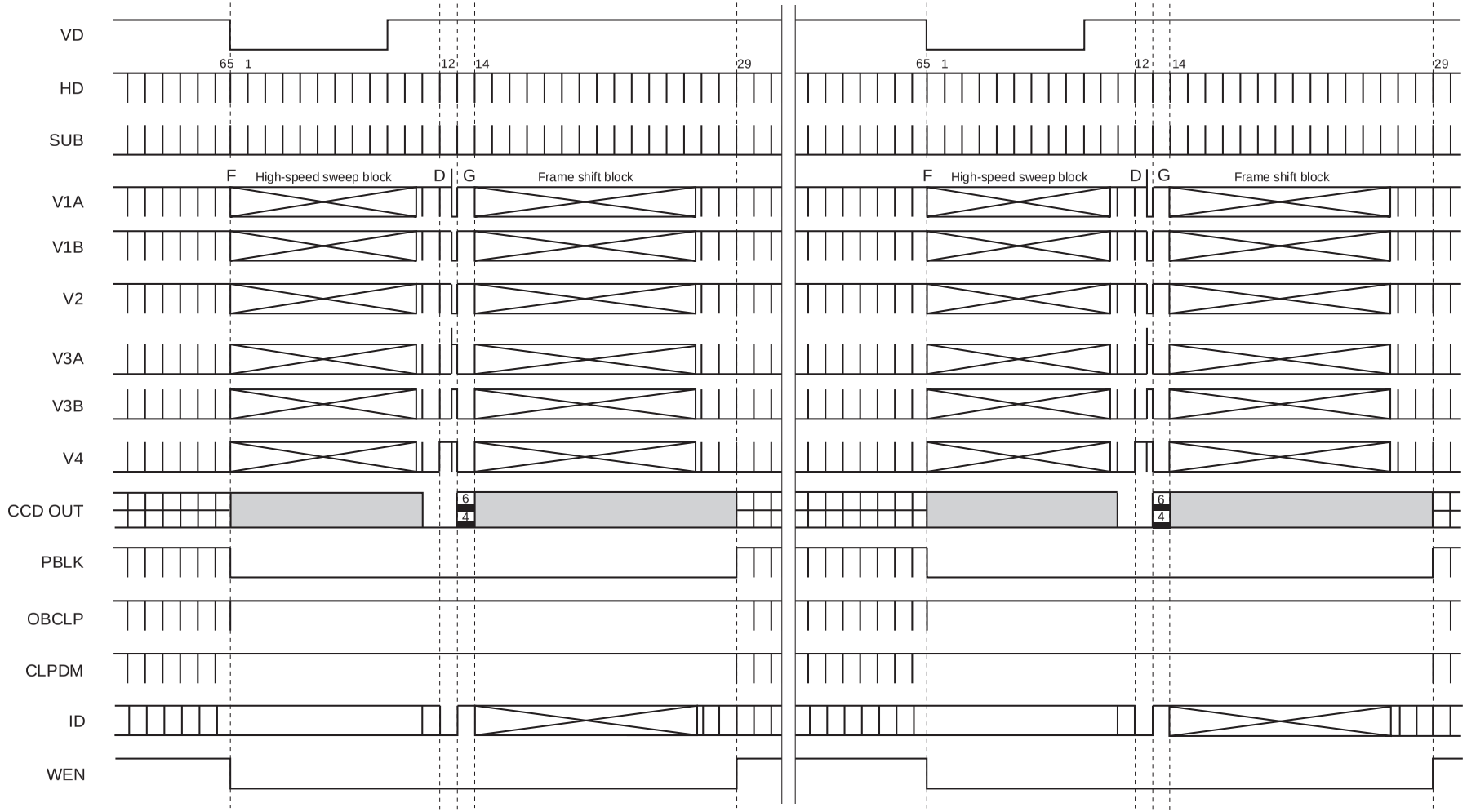
Chart-4 Vertical Direction Timing Chart

MODE

AF2 mode

Applicable CCD image sensor

• ICX252



* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
* 208 stages are fixed for high-speed sweep block; 0 to 255 stages are specified by the serial interface for frame shift block.
* VD of this chart is NTSC equivalent pattern (65H + 1430ck units). For PAL equivalent pattern, it is 78H + 1536ck units.

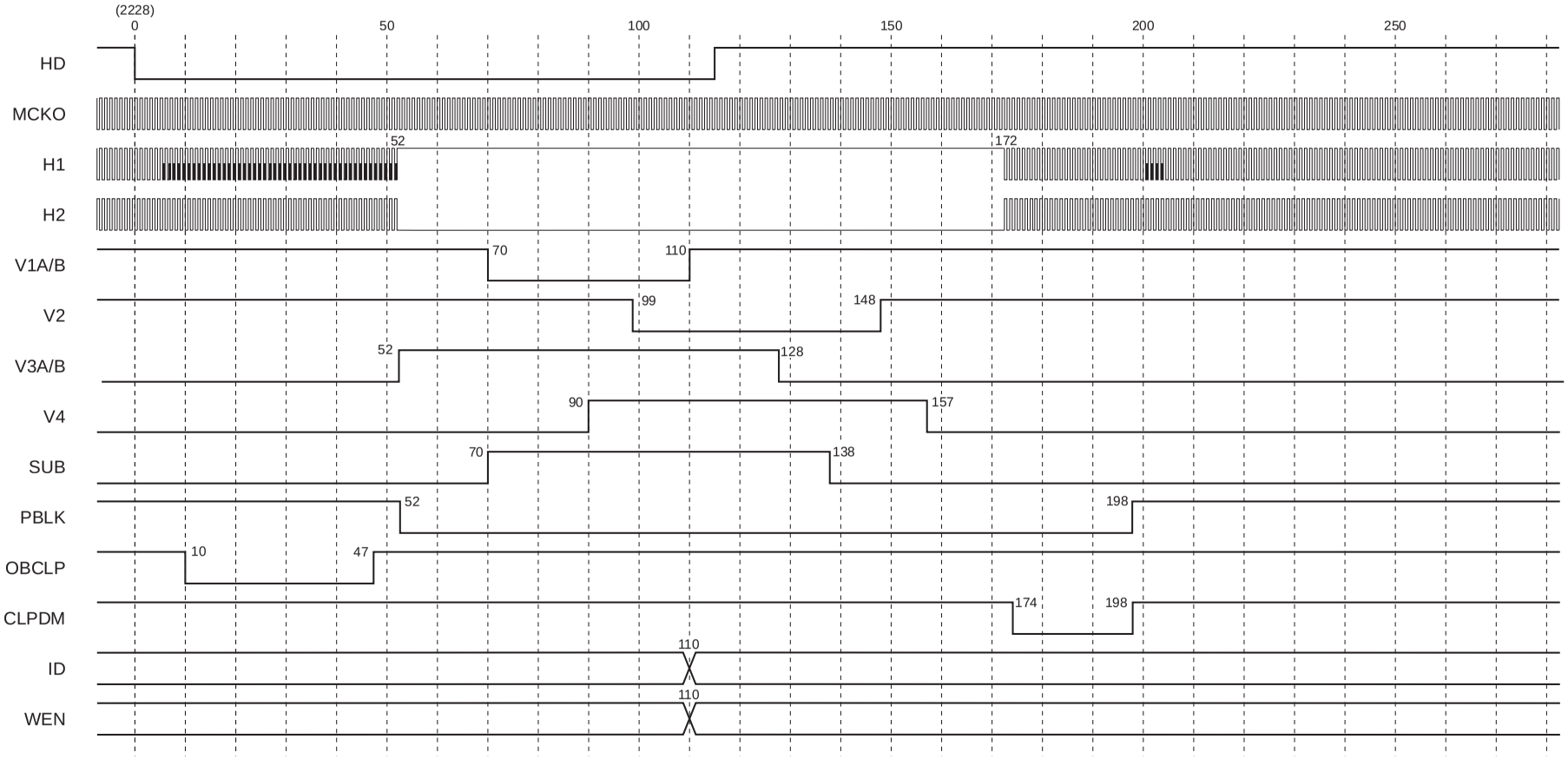
Chart-5 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX252



* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-1.

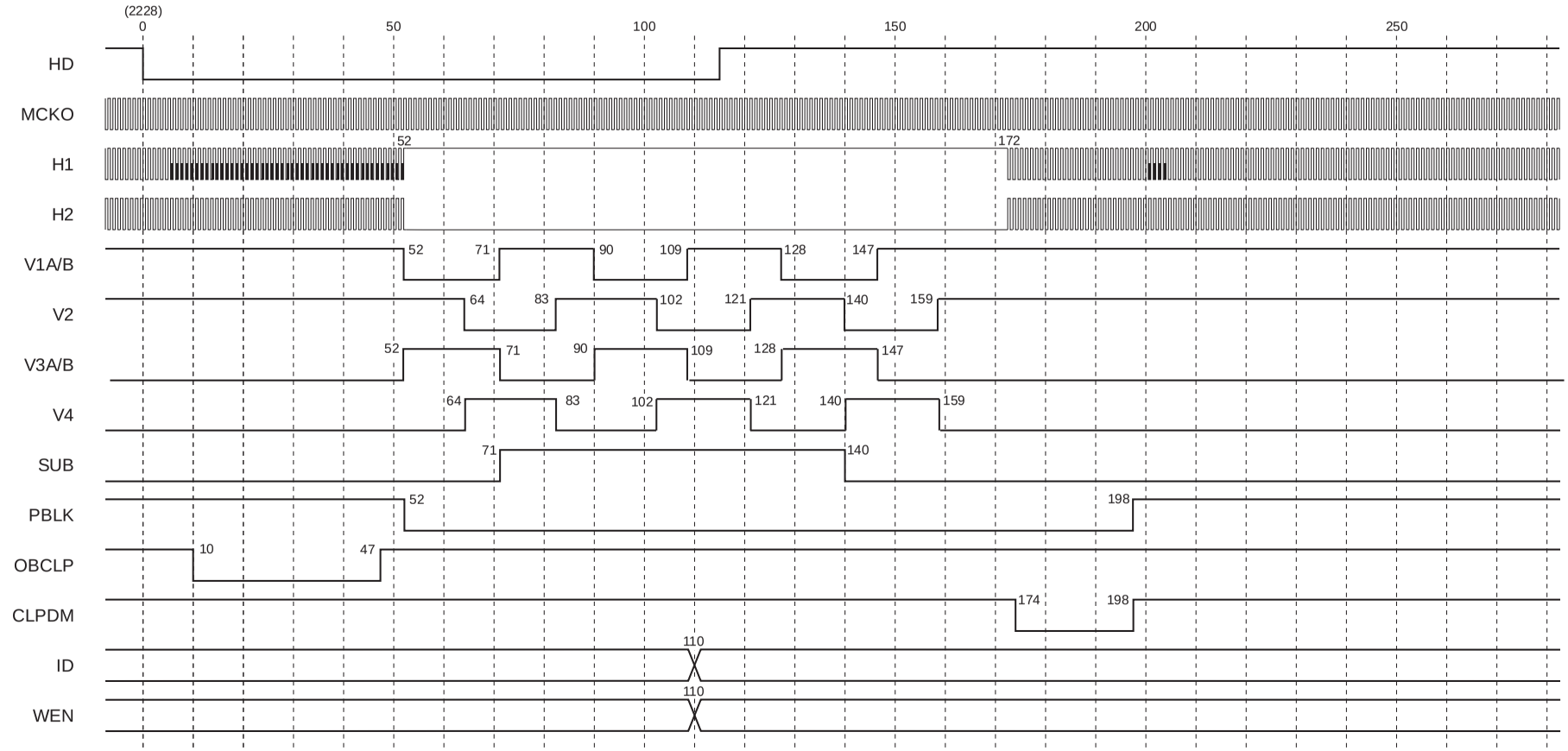
Chart-6 Horizontal Direction Timing Chart

MODE

Draft/AF1/AF2 mode

Applicable CCD image sensor

• ICX252

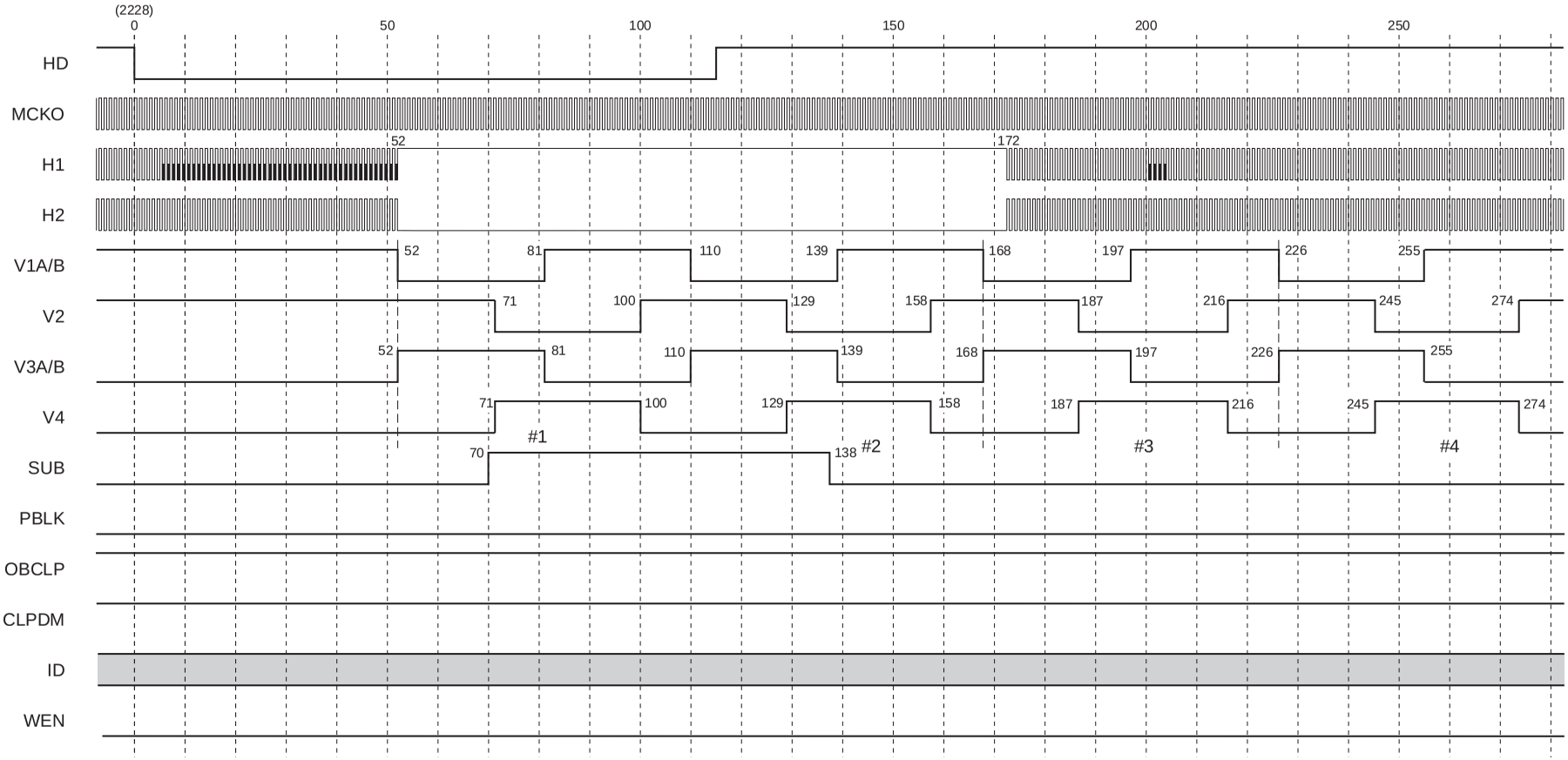


* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-2, 3 and 4.

Chart-7 **Horizontal Direction Timing Chart**
(High-speed sweep: C)

MODE
Frame mode

Applicable CCD image sensor
• ICX252

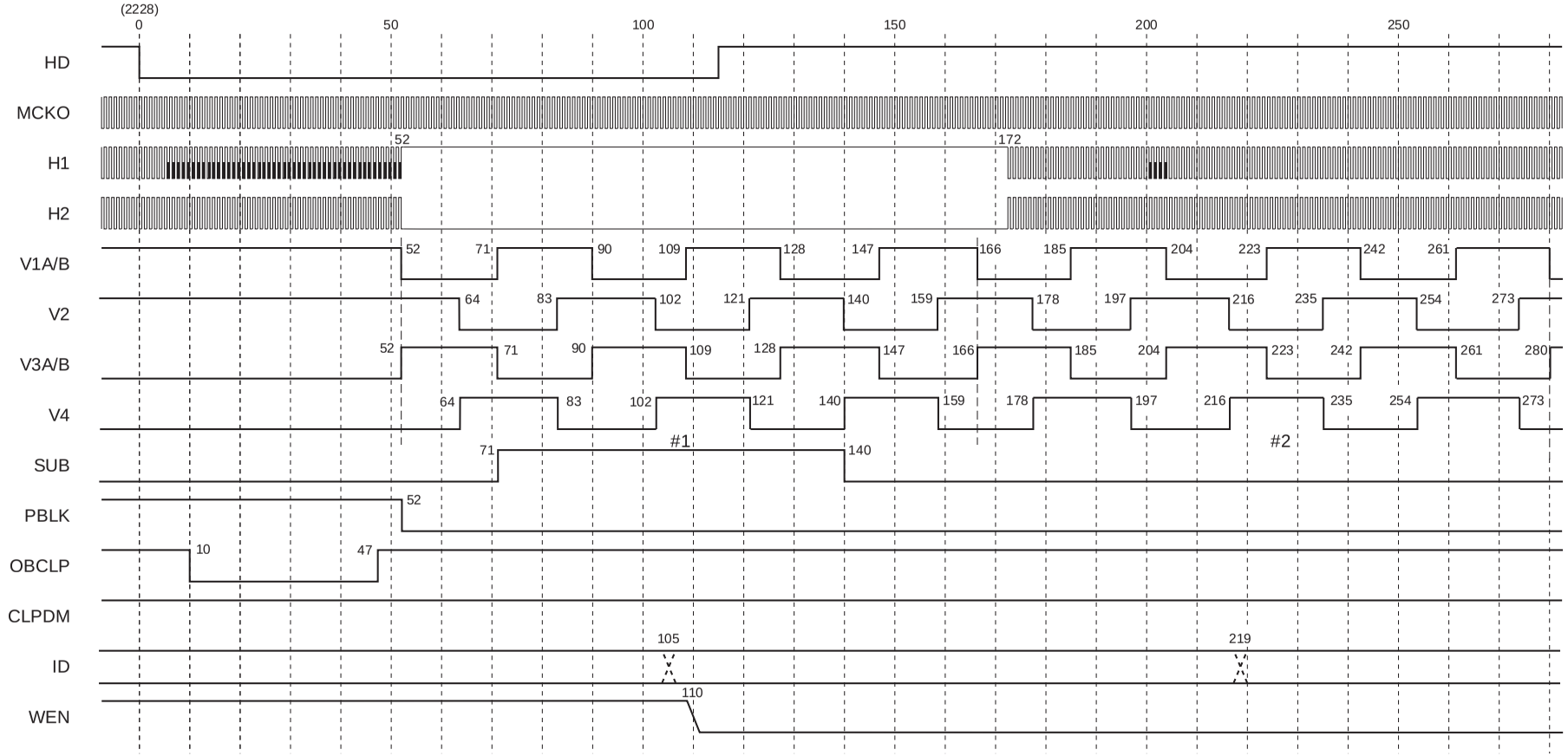


* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 26H of 768ck (#1038).

Chart-8 **Horizontal Direction Timing Chart**
(High-speed sweep: F)
(Frame shift: G)

MODE
AF1/AF2 mode

Applicable CCD image sensor
• ICX252



* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* WEN are output at the timing shown above at the position shown in Chart-3 and 4.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 6H of 2056ck (#138) in AF1 mode and 10H of 884ck (#208) in AF2 mode.
* Frame shift of V1A/B, V2, V3A/B and V4 receives the output control by the serial interface data and it can specify up to #255 for both of AF1/AF2 mode.
* ID is output at the timing shown with dotted line during frame shift.

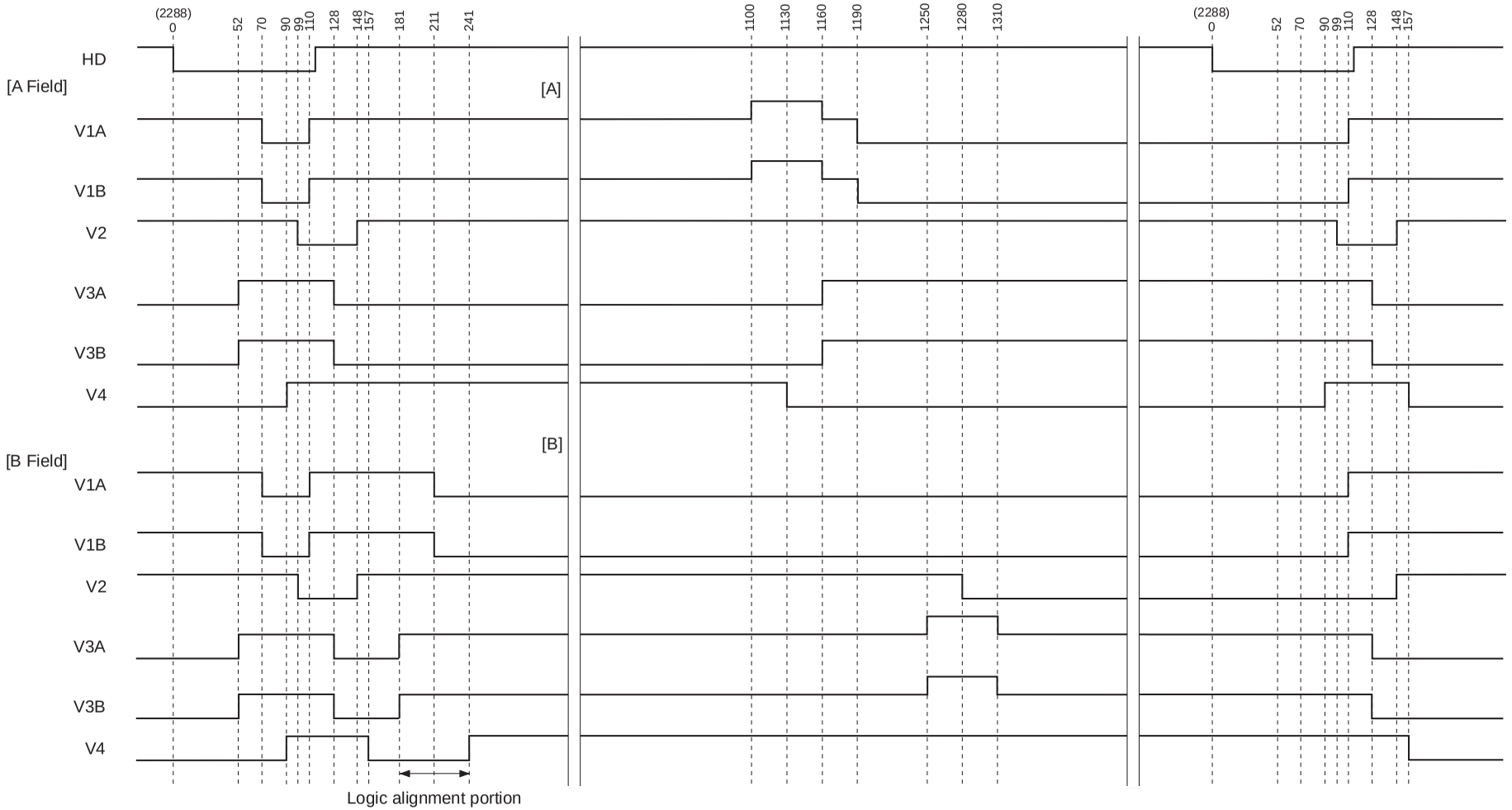
Chart-9 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX252



* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.

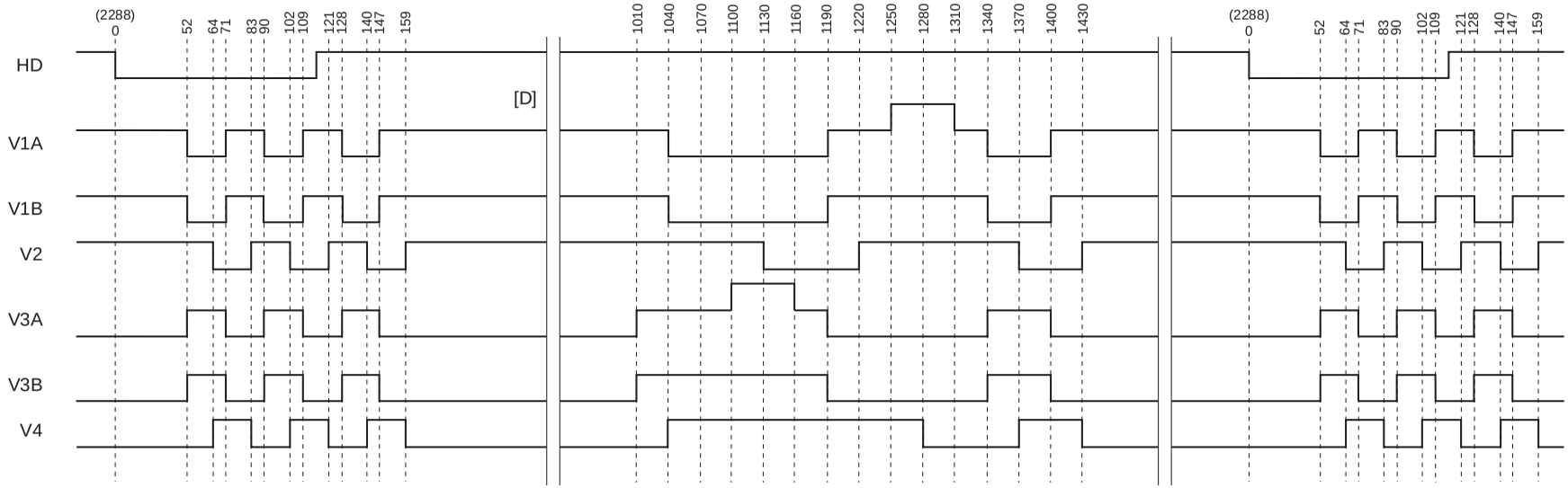
Chart-10 Horizontal Direction Timing Chart

MODE

Draft /AF1/AF2 mode

Applicable CCD image sensor

• ICX252



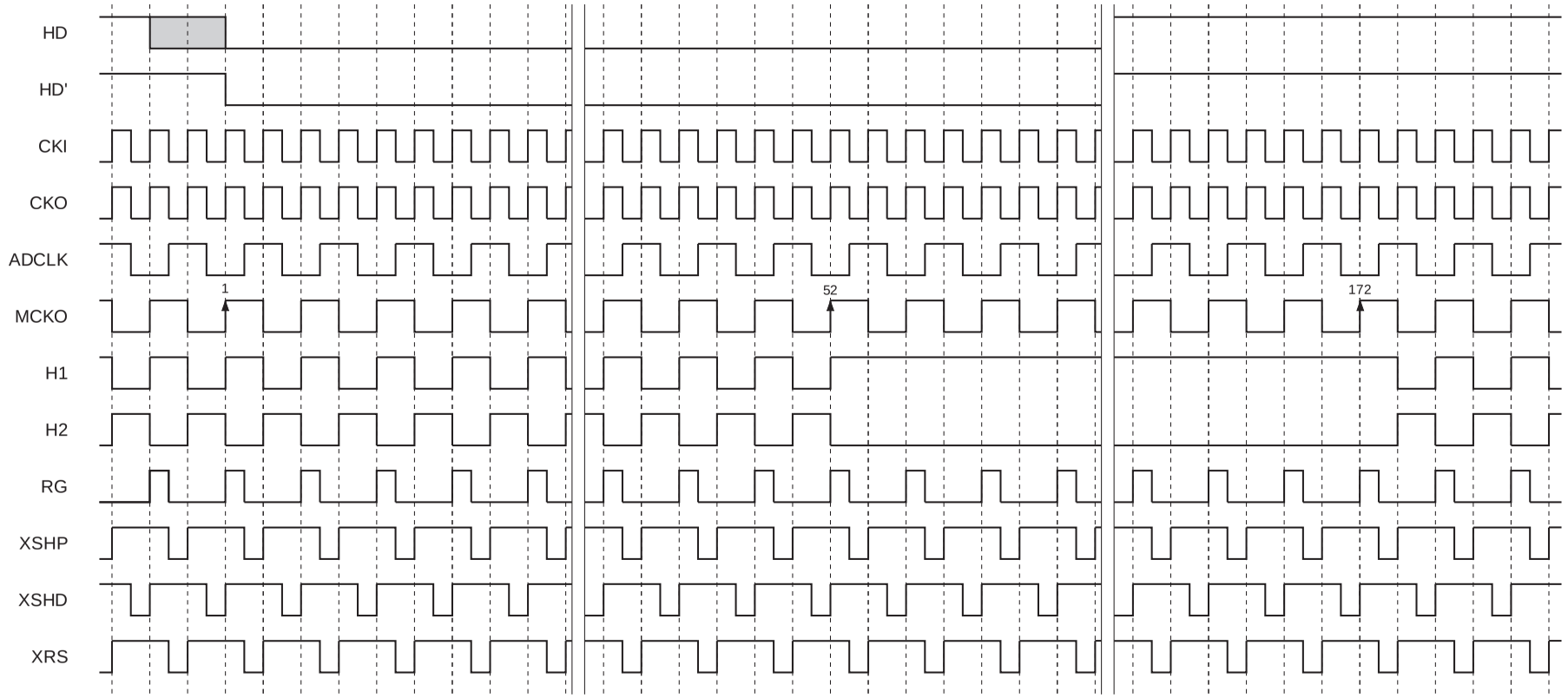
* The HD of this chart indicates the actual CXD2492R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.9 to 9.5µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs). Internal SSG is at the timing.

Chart-11 High-speed Phase Timing Chart

MODE

Applicable CCD image sensor

• ICX252



* HD' indicates the HD which is the actual CXD2492R load timing.
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phase of ADCLK can be specified by the serial interface data.

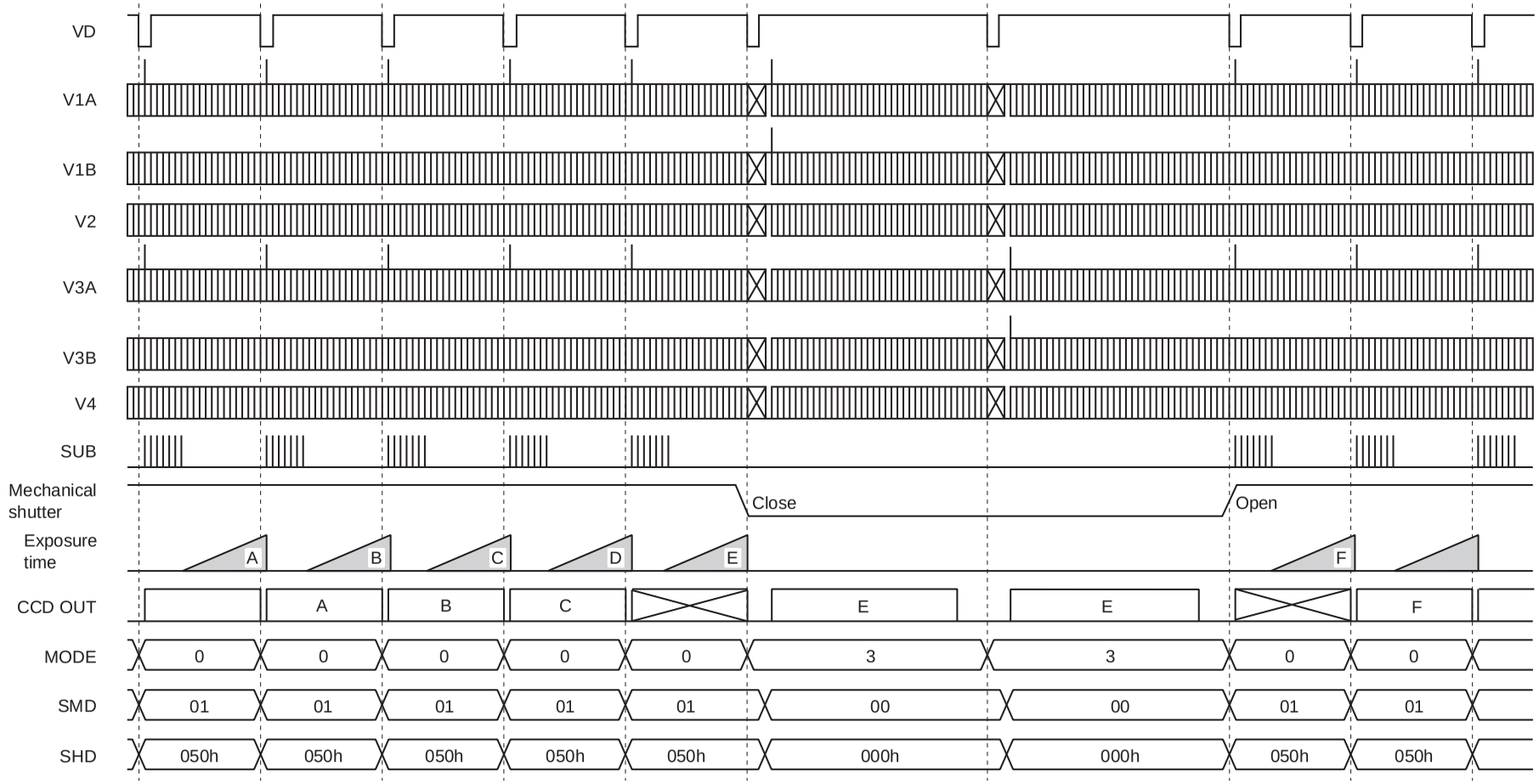
Chart-12 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

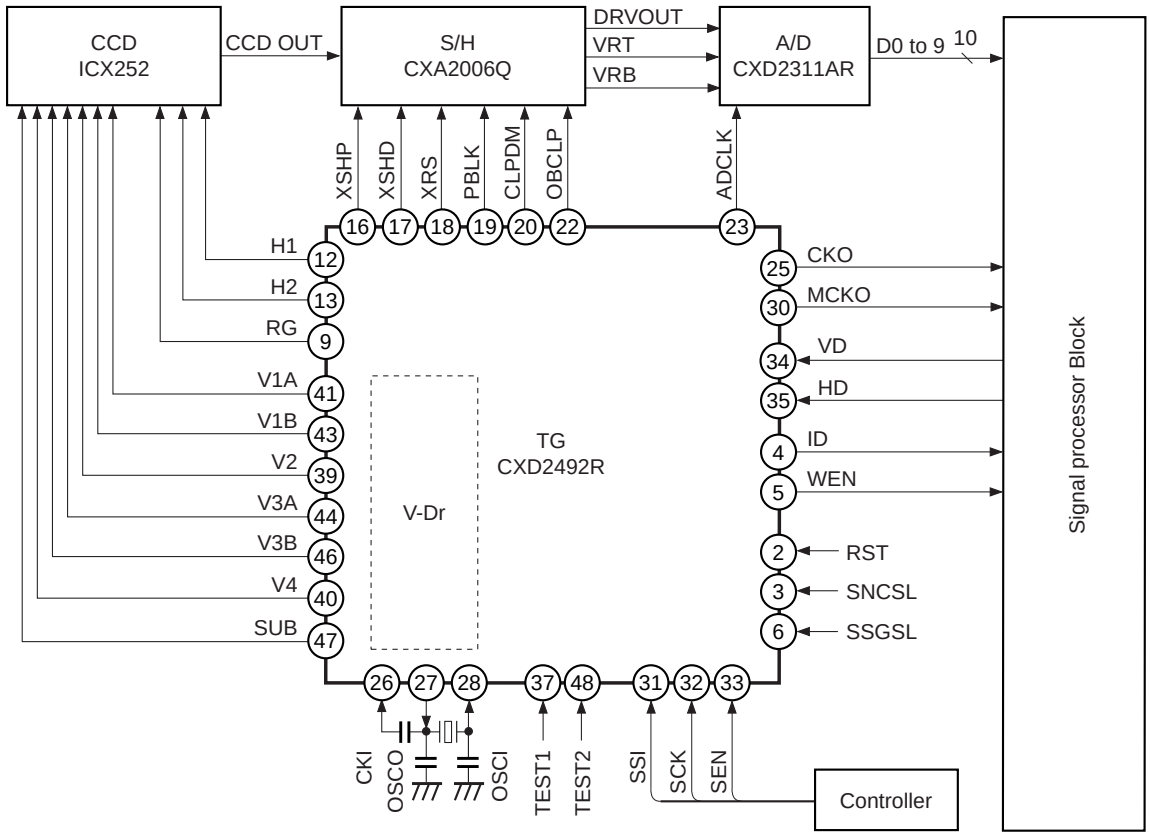
Applicable CCD image sensor

• ICX252



* This chart is a drive timing chart example of electronic shutter normal operation.
* Data exposed at D includes blooming component. For details, see CCD image sensor specification.
* CXD2492R does not generate the pulse to control mechanical shutter operation.
* The switching timing of drive mode and electronic shutter data is not the same.

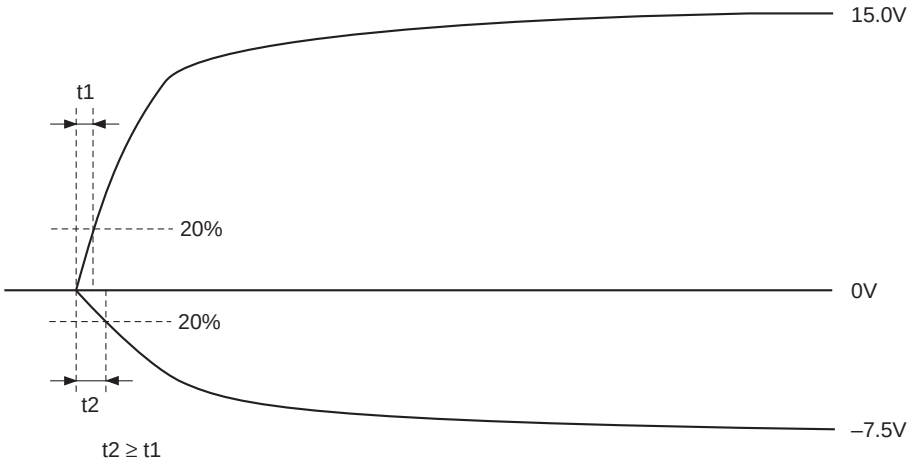
Application Circuit Block Diagram



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

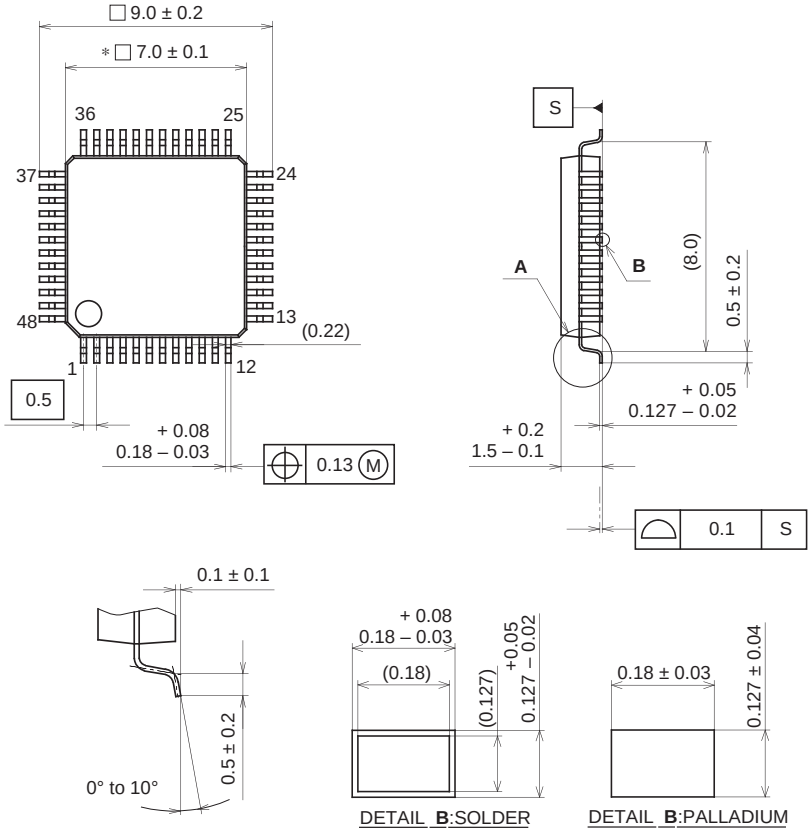
Notes for Power-on

Of the three –7.5V, +15.0V and +3.3V power supplies, be sure to start up the –7.5V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g