

## Low Noise Amplifier with Bypass Switch/Mixer

**Description**

The CXG1097EN is a dual mode low noise amplifier with a bypass switch/ mixer MMIC for Japan CDMA cellular. This IC is designed using the Sony's GaAs J-FET process.

**Features**

- Dual mode low noise amplifier with a bypass switch
- High gain

Low noise amplifier high current mode:

$$G_p = 14.5\text{dB (Typ.)}$$

Mixer:

$$G_c = 12.0\text{dB (Typ.)}$$

- Low noise

Low noise amplifier high current mode:

$$NF = 1.6\text{dB (Typ.)}$$

Mixer:

$$NF = 4.5\text{dB (Typ.)}$$

- Low distortion

Low noise amplifier high current mode:

$$IIP3 = +4.5\text{dBm (Typ.)}$$

Mixer:

$$IIP3 = +3\text{dBm (Typ.)}$$

- Small package 16-pin VSON

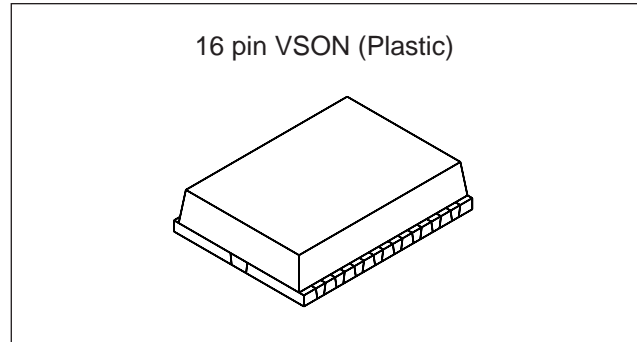
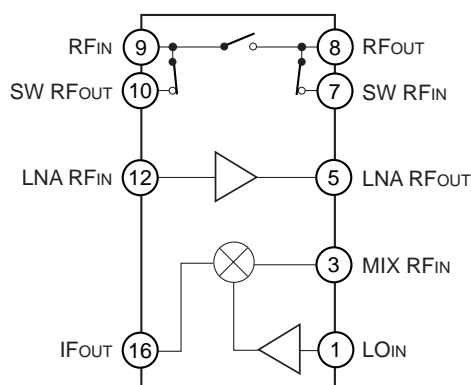
**Applications**

Japan CDMA cellular (J-CDMA)

**Element Structure**

GaAs J-FET MMIC

**Block Diagram**



**Absolute Maximum Ratings (Ta = 25°C)**

• Supply voltage	V <sub>DD</sub>	4.5	V
• Input power	P <sub>IN</sub>	+5	dBm
• Operating temperature	T <sub>opr</sub>	-35 to +85	°C
• Storage temperature	T <sub>stg</sub>	-65 to +150	°C

**Recommended Operating Conditions**

• Supply voltage	V <sub>DD</sub>	2.7 to 3.3	V
• Control voltage	V <sub>CTL</sub> (H)	2.4 to 3.3	V
	V <sub>CTL</sub> (L)	0 to 0.3	V

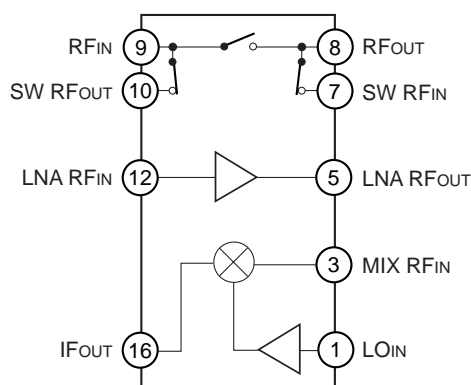
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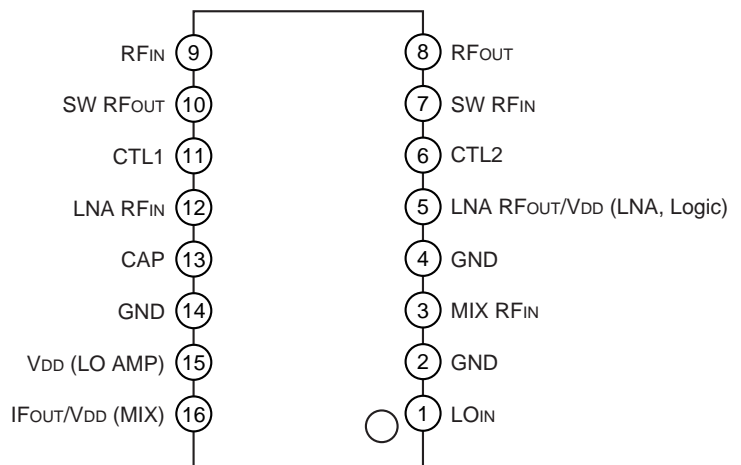
**Element Structure**

GaAs J-FET MMIC

**Block Diagram**



**Pin Configuration**



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**Electrical Characteristics**

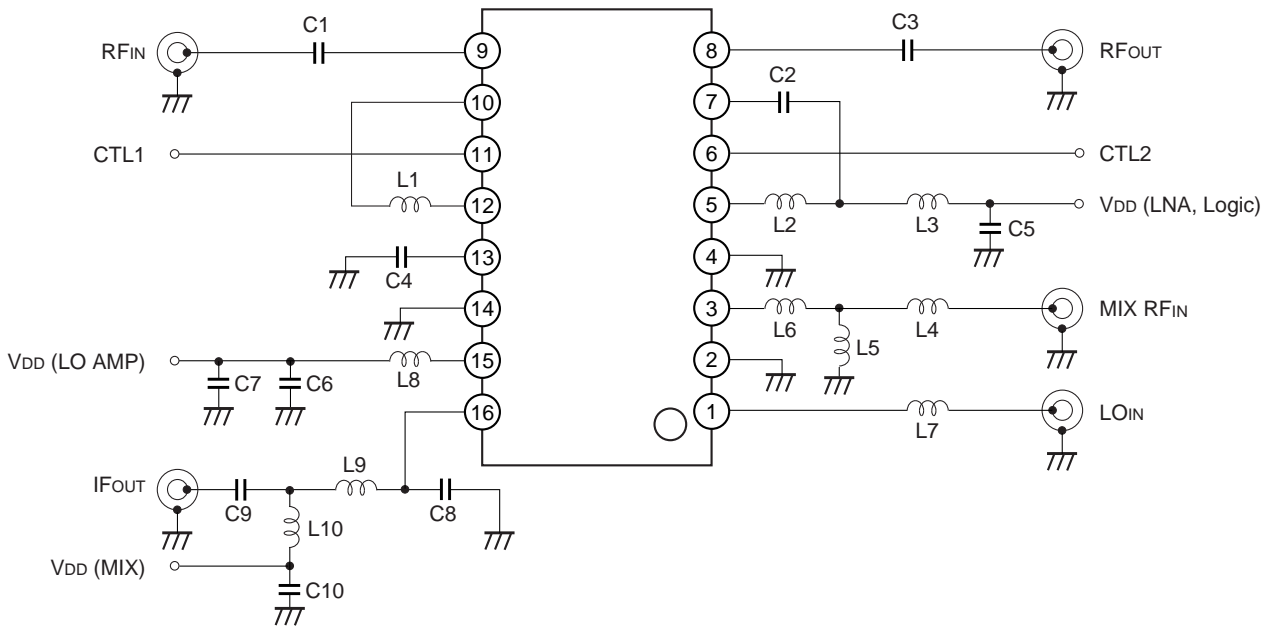
Conditions:  $V_{DD} = 2.7V$ ,  $V_{CTL} (H) = 2.7V$ ,  $V_{CTL} (L) = 0V$ ,  $f_{RF} = 850MHz$ ,  $f_{LO} = 740MHz$ ,  $P_{LO} = -10dBm$ ,  
 unless otherwise specified ( $T_a = 25^{\circ}C$ )

Block	Item	V <sub>CTL1</sub>	V <sub>CTL2</sub>	Symbol	Min.	Typ.	Max.	Unit	Measurement condition		
Low noise amplifier block	Control current for High state	H	L	I <sub>CTLH</sub>	—	50	70	μA	When no signal		
		L	H								
	Current consumption	L	L or H	I <sub>DDSW</sub>	—	0.3	0.6	mA			
		H	L	I <sub>DDL</sub>	—	3.8	5				
		H	H	I <sub>DDH</sub>	—	10.5	17				
	Power gain	L	L or H	G <sub>PSW</sub>	-3.7	-3.2	-2.7	dB		When a small signal	
		H	L	G <sub>PL</sub>	11	12.5	14				
		H	H	G <sub>PH</sub>	13	14.5	16				
	Noise figure	H	L	N <sub>FL</sub>	—	1.8	2.3	dB			
		H	H	N <sub>FH</sub>	—	1.6	2.1				
	Input IP3	L	L or H	IIP3 <sub>sw</sub>	25	35	—	dBm			*1
		H	L	IIP3 <sub>L</sub>	-3	0	—				
H		H	IIP3 <sub>H</sub>	2	4.5	—					
Isolation	H	L	Iso	20	24	—	dB	When a small signal			
	H	H									
Mixer block	Current consumption			I <sub>DD</sub>	—	7.5	10		mA		When no signal
	Conversion gain			G <sub>c</sub>	10.5	12	13.5		dB		When a small signal
	Noise figure			N <sub>F</sub>	—	4.5	6		dB		
	Input IP3			IIP3	0.5	3	—		dBm	*1	
	LO to RF leak level			P <sub>LK</sub>	—	-30	-25		dBm	—	

\*1  $f_{RF}=850MHz/850.9MHz$ ,  $P_{RF} = -25dBm$  (low noise amplifier mode, mixer)/0dBm (bypass switch mode)  
 Conversion by the IM3 suppression ratio for two-wave input.

**Note)** The values shown above are the specified values on the Sony's recommended evaluation board.

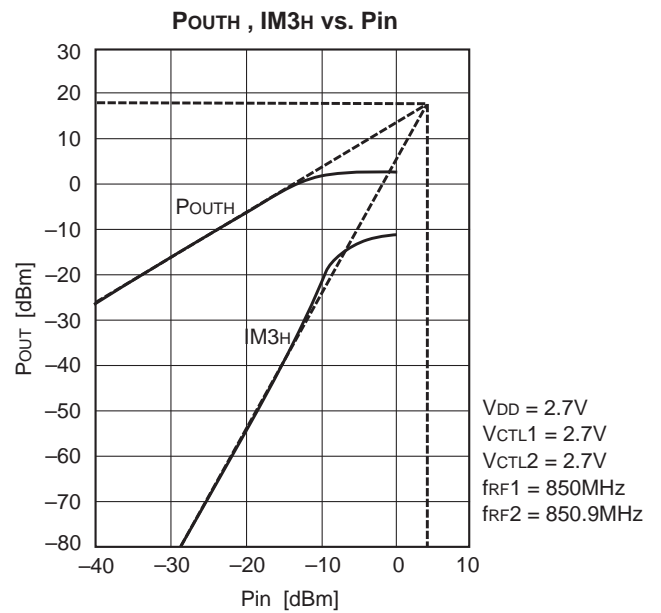
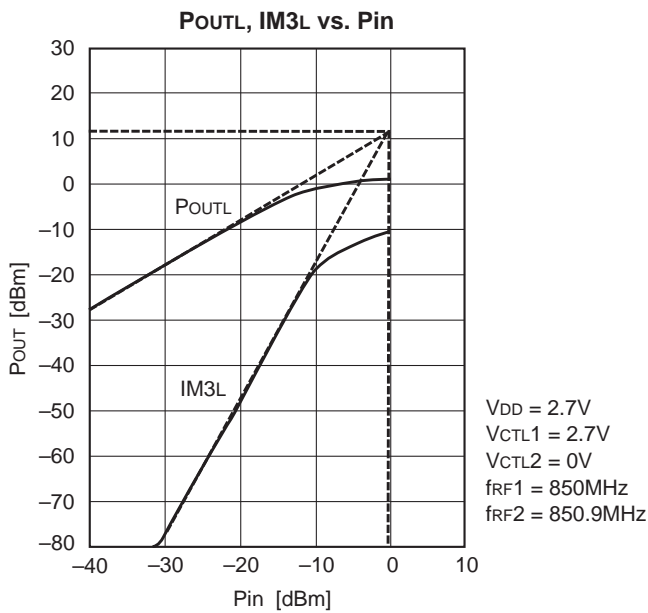
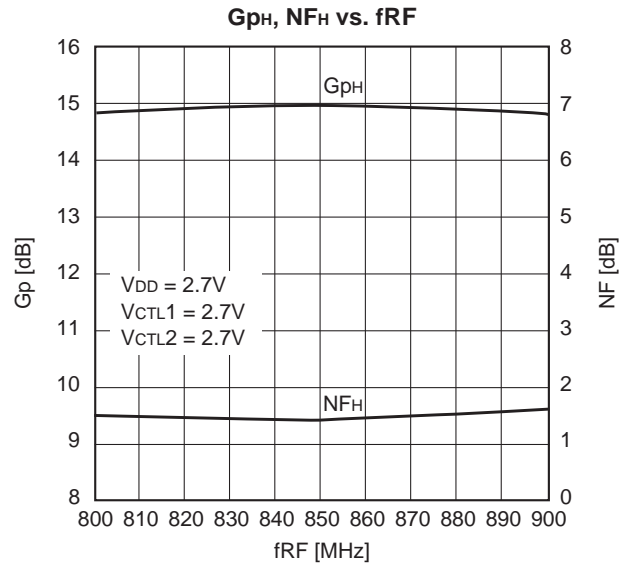
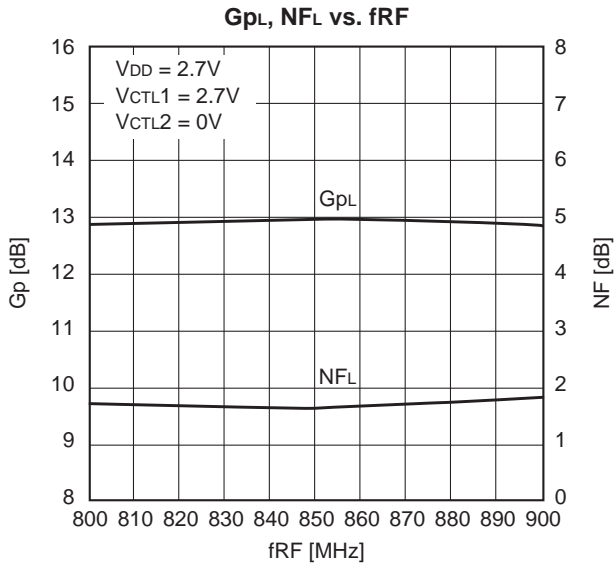
Recommended Evaluation Circuit



L1	18nH	C1	100pF
L2	18nH	C2	100pF
L3	33nH	C3	100pF
L4	10nH	C4	1000pF
L5	15nH	C5	1000pF
L6	27nH	C6	100pF
L7	33nH	C7	1000pF
L8	33nH	C8	6pF
L9	220nH	C9	1000pF
L10	180nH	C10	1000pF

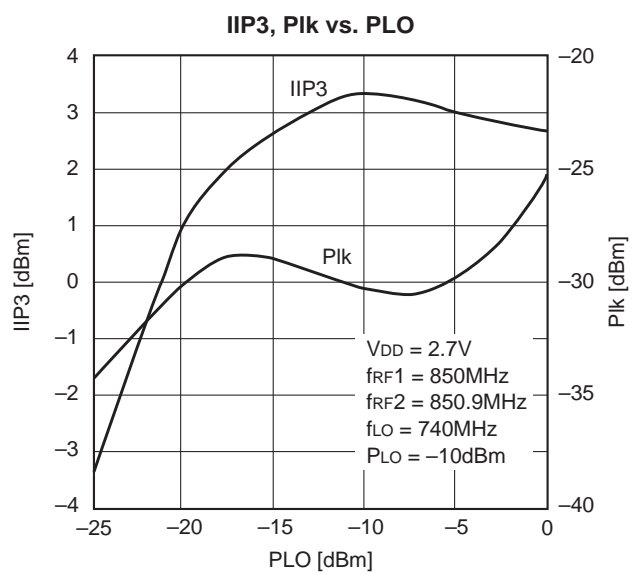
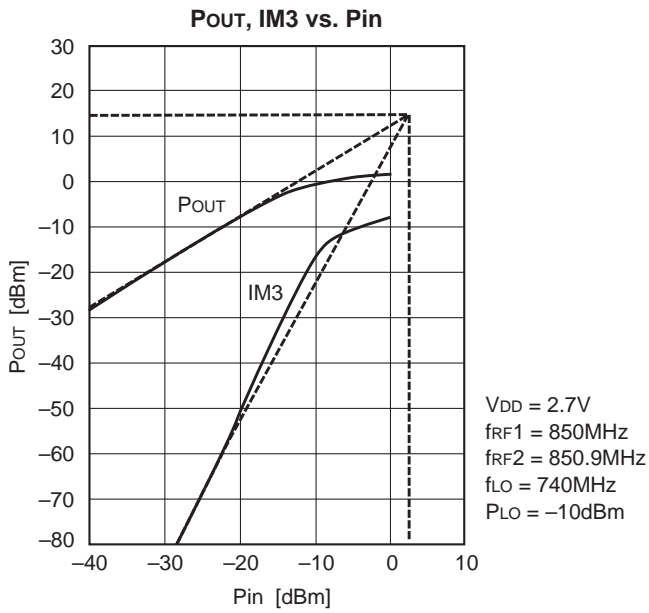
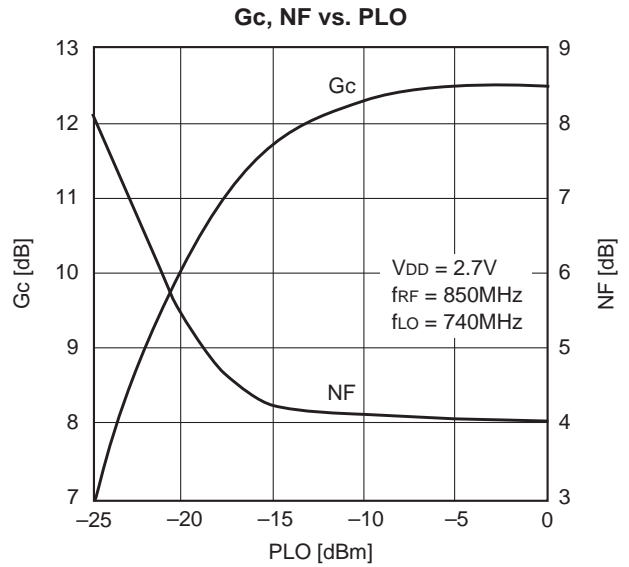
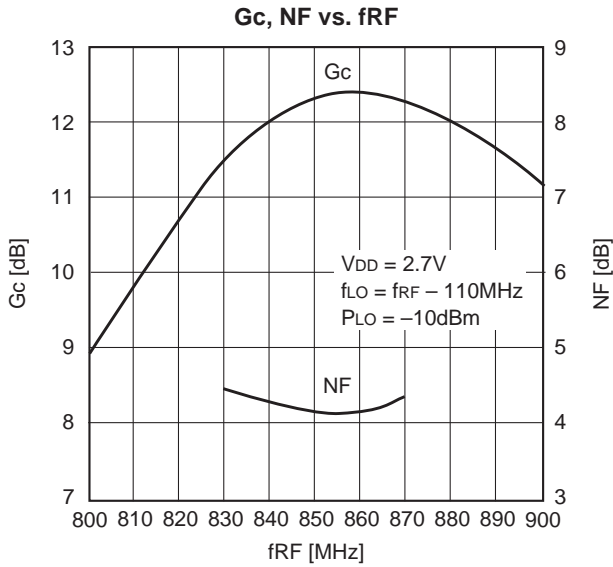
Example of Representative Characteristics (Ta = 25°C)

Low Noise Amplifier Block

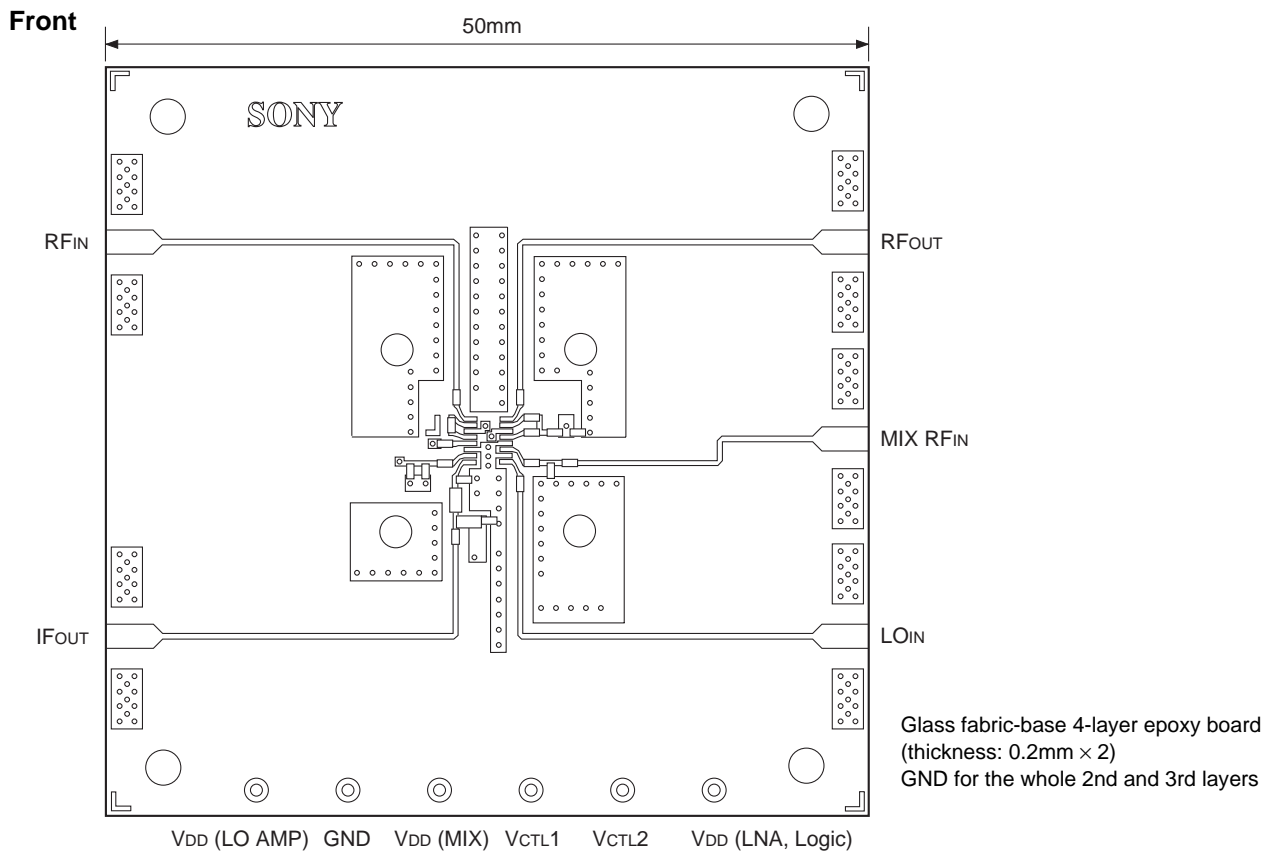


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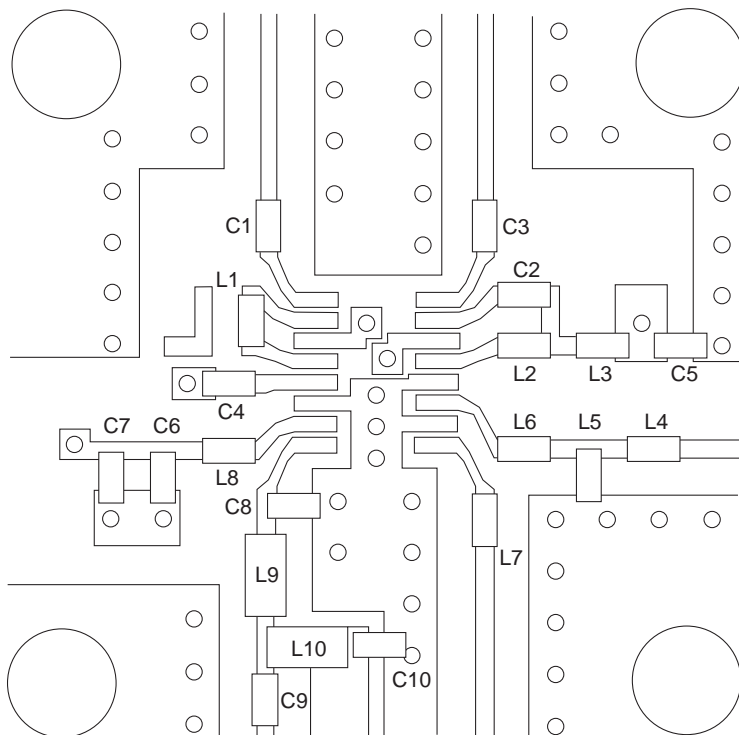
Mixer Block



**Recommended Evaluation Board**



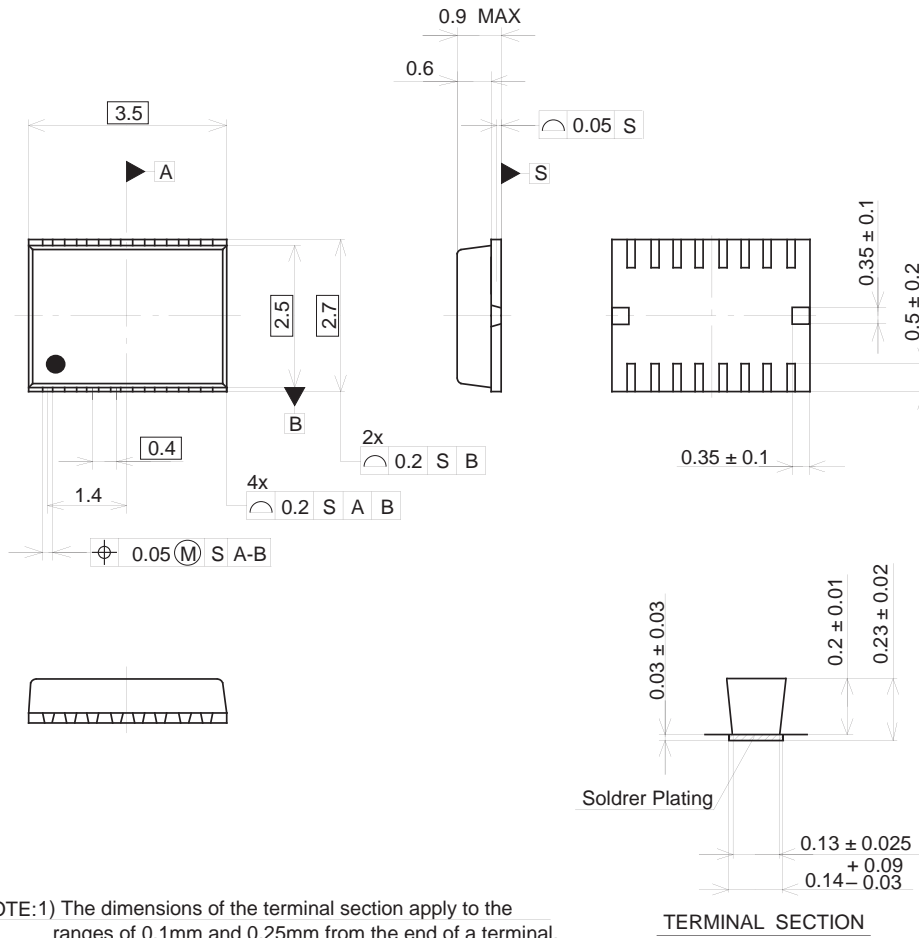
**Enlarged Diagram of Center Part**



Package Outline

Unit: mm

16PIN VSON(PLASTIC)



NOTE:1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

TERMINAL SECTION

PACKAGE STRUCTURE

SONY CODE	VSON-16P-01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g