

CXK5V81000ATM -85LLX/10LLX

131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK5V81000ATM is a high speed CMOS static RAM organized as 131072-words by 8-bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Operating on a single 3.3V supply, and special feature are low power consumption, high speed.

The CXK5V81000ATM is a suitable RAM for portable equipment with battery back up.



Features

- Extended operating temperature range: -25 to +85°C
- Fast access time:

	(Access time)
-85LLX	85ns (Max.)
-10LLX	100ns (Max.)
- Low standby current: 28µA (Max.)
- Low data retention current: 24µA (Max.)
- Single 3.3V supply: 3.3V ± 0.3V
- Low voltage data retention: 2.0V (Min.)
- Package
8mm × 20mm 32 pin TSOP package

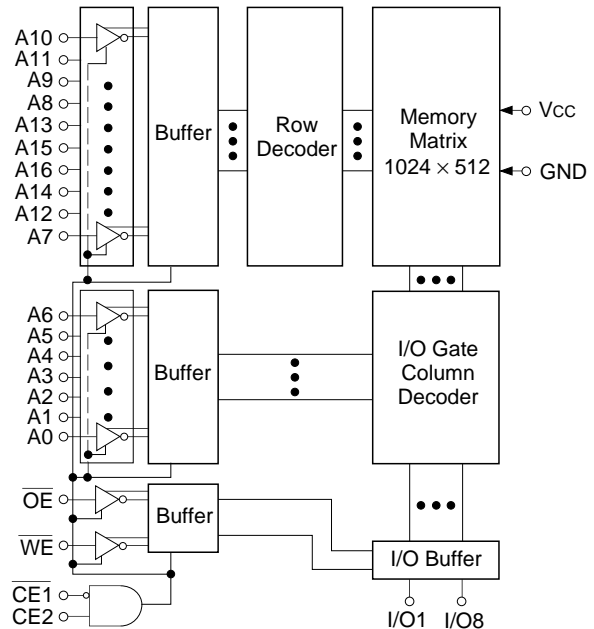
Function

131072-word x 8-bit static RAM

Structure

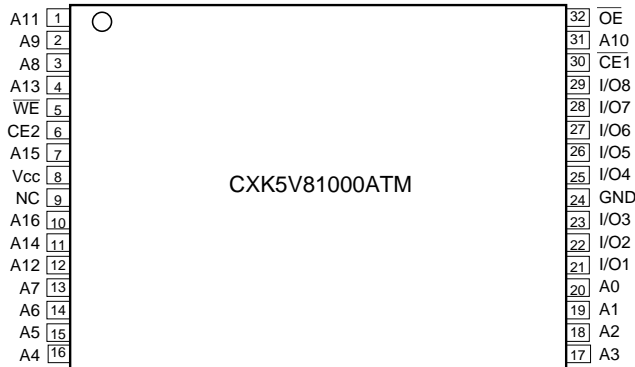
Silicon gate CMOS IC

Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Input voltage	VIN	-0.5* to Vcc + 0.5	V
Input and output voltage	VIO	-0.5* to Vcc + 0.5	V
Allowable power dissipation	Pd	0.7	W
Operating temperature	Topr	-25 to +85	°C
Storage temperature	Tstg	-55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

* VIN, VIO = -3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	ISB1, ISB2
×	L	×	×	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	×	L	Write	Data in	Icc1, Icc2, Icc3

×: "H" or "L"

DC Recommended Operating Conditions

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Input high voltage	VIH	2.2	—	Vcc + 0.3	V
Input low voltage	VIL	-0.3*	—	0.6	V

* VIL = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC Characteristics

(V_{CC} = 3.3V ± 0.3V, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	+1	μA	
Output leakage current	I _{LO}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	-1	—	+1	μA	
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, CE2 = V _{IH} V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA	—	1	3	mA	
Average operating current	I _{CC2}	Min. cycle duty = 100% I _{OUT} = 0mA	85LLX	—	30	40	mA
			10LLX	—	25	35	
	I _{CC3}	Cycle time 1μs duty = 100% I _{OUT} = 0mA CE1 ≤ 0.2V CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V V _{IH} ≥ V _{CC} - 0.2V	—	5	10	mA	
Standby current	I _{SB1}	CE2 ≤ 0.2V or { CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	-25 to +85°C	—	—	28	μA
			-25 to +70°C	—	—	14	
			+25°C	—	0.48	—	
	I _{SB2}	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL}	—	0.12	1.4	mA	
Output high voltage	V _{OH}	I _{OH} = -2.0mA	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.0mA	—	—	0.4	V	

* V_{CC} = 3.3V, T_a = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

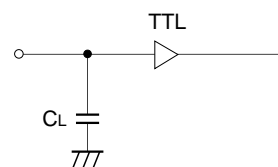
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (V_{CC} = 3.3V ± 0.3V, Ta = -25 to +85°C)

Item	Conditions	
Input pulse high level	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.6V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.4V	
Output load conditions	-85LLX	CL* = 30pF, 1TTL
	-10LLX	CL* = 100pF, 1TTL

• Test circuit



* CL includes scope and jig capacitances.

• Read cycle ($\overline{WE} = "H"$)(V_{CC} = 3.3V ± 0.3V, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	85	—	100	—	ns
Address access time	t _{AA}	—	85	—	100	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	85	—	100	ns
Chip enable access time (CE2)	t _{CO2}	—	85	—	100	ns
Output enable to output valid	t _{OE}	—	40	—	50	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1*} , t _{HZ2*}	—	35	—	40	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ*}	—	30	—	35	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

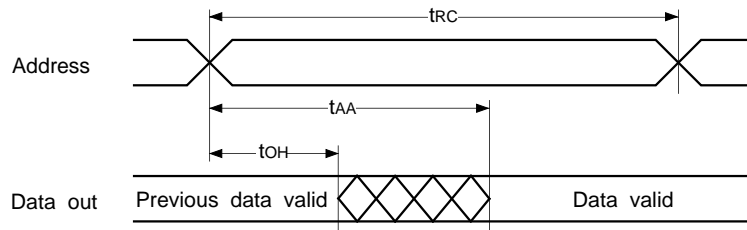
(V_{CC} = 3.3V ± 0.3V, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	85	—	100	—	ns
Address valid to end of write	t _{AW}	70	—	80	—	ns
Chip enable to end of write	t _{CW}	70	—	80	—	ns
Data to write time overlap	t _{DW}	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	5	—	5	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ*}	—	35	—	40	ns

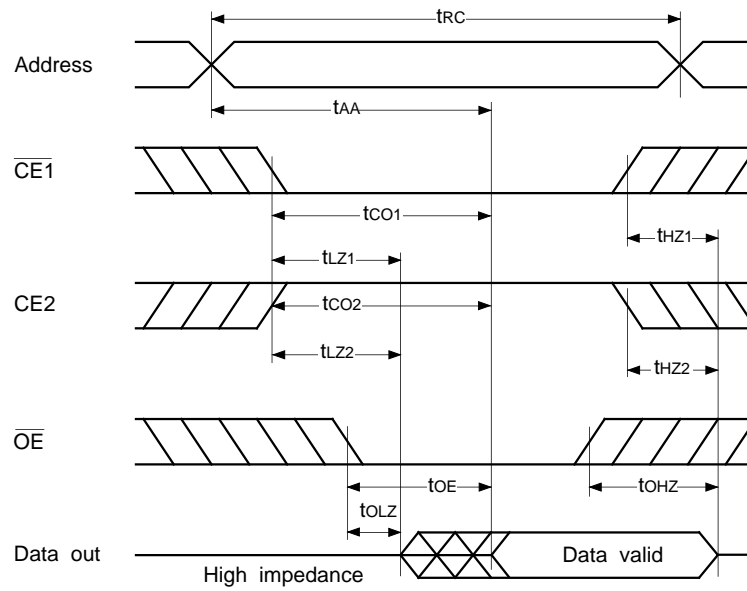
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

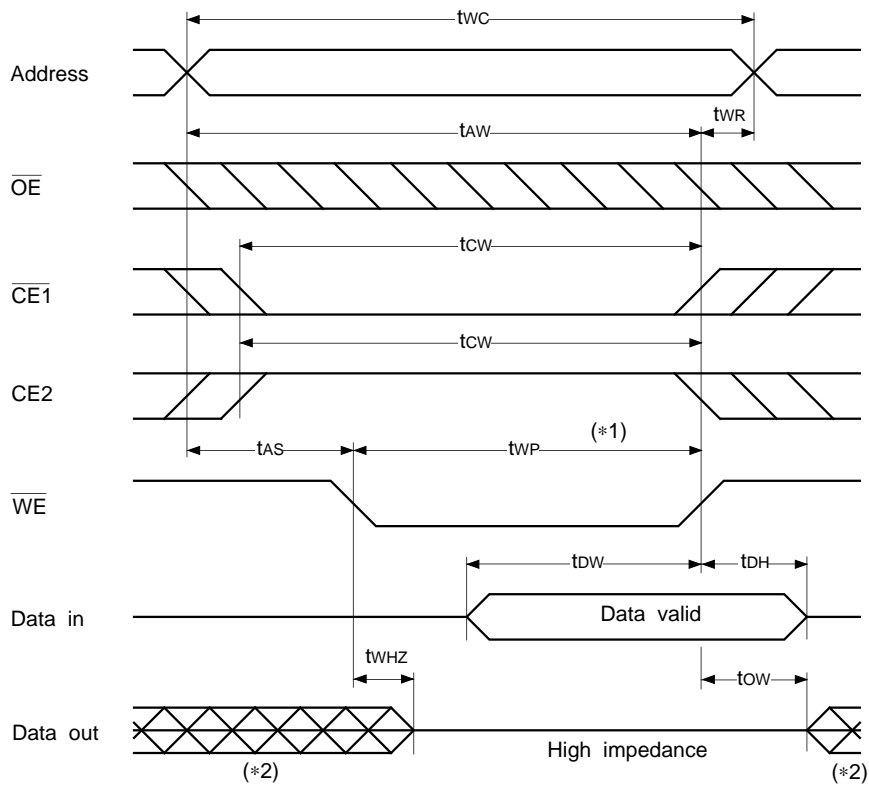
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



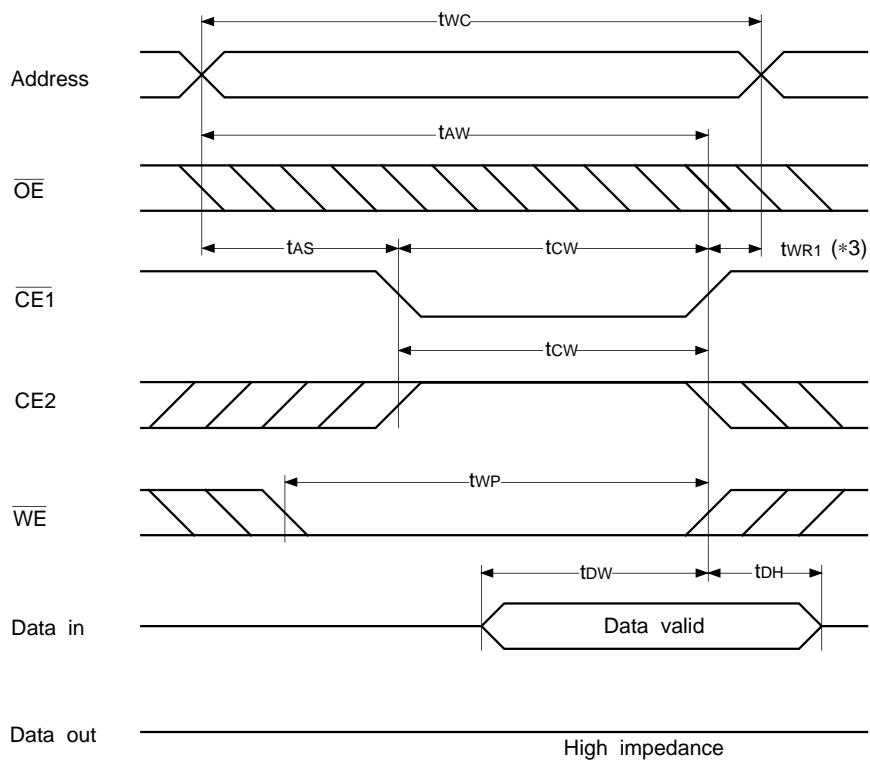
- Read cycle (2) : $\overline{WE} = V_{IH}$



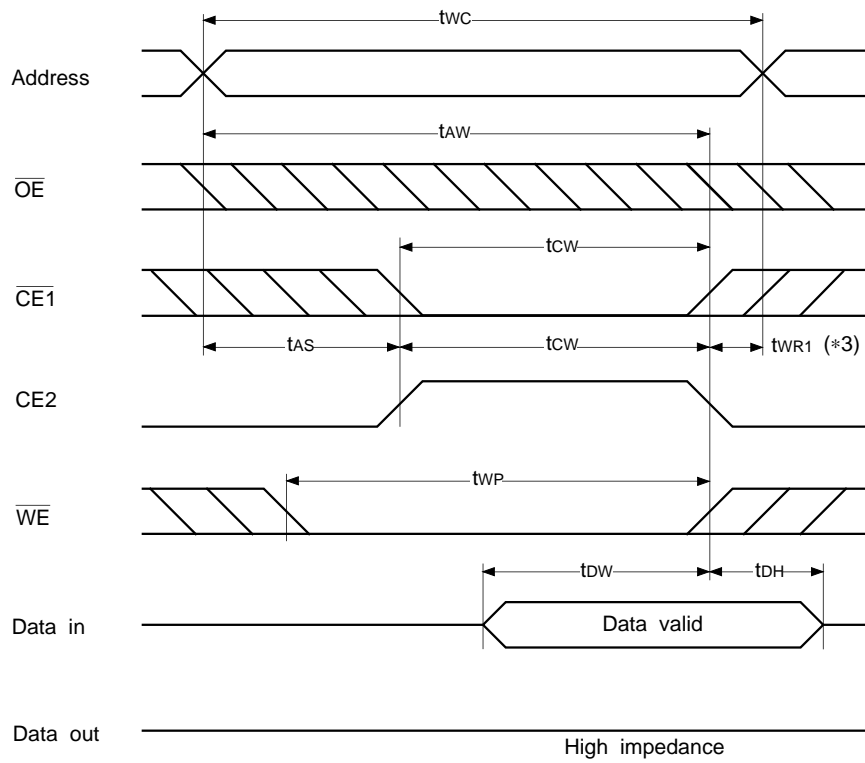
• Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



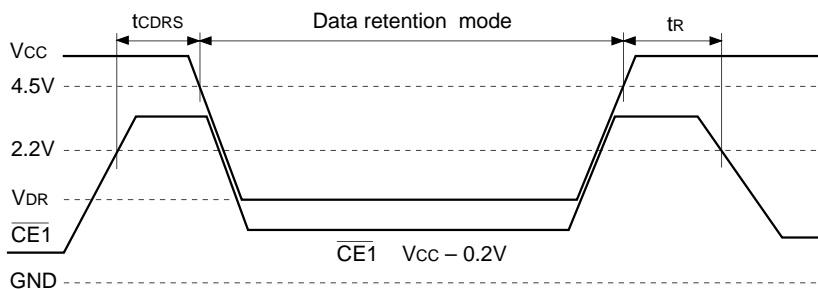
• Write cycle (3) : CE2 control



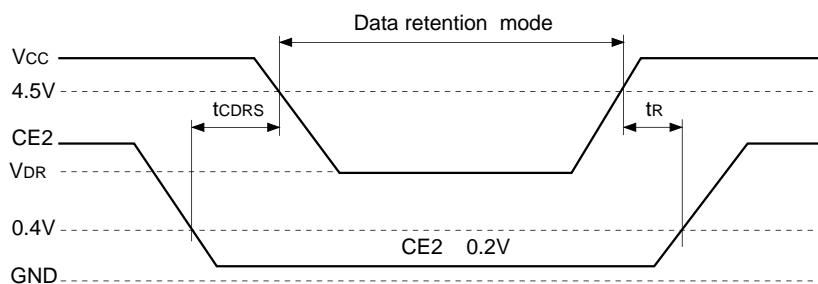
- *1 Write is executed when both $\overline{CE1}$ and \overline{WE} are at low and CE2 is at high simultaneously.
- *2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



• Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics

($T_a = -25$ to $+85^\circ\text{C}$)

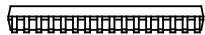
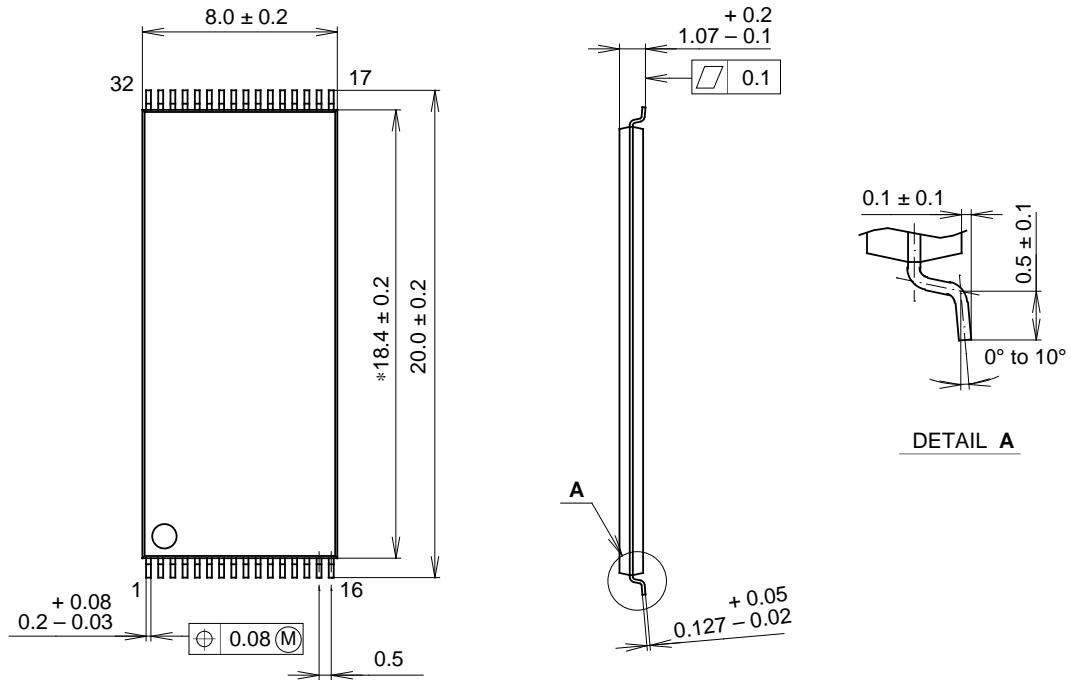
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V_{DR}	*1	2.0	—	3.6	V	
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V^{*1}$	-25 to $+85^\circ\text{C}$	—	—	24	μA
			-25 to $+70^\circ\text{C}$	—	—	12	
			$+25^\circ\text{C}$	—	0.4	—	
	I_{CCDR2}	$V_{CC} = 2.0$ to $3.6V^{*1}$	—	0.48^{*2}	28	μA	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t_R		5	—	—	ms	

*1 $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ (CE2 control)

*2 $V_{CC} = 3.3V$, $T_a = 25^\circ\text{C}$

Package Outline Unit: mm

32PIN TSOP (I) (PLASTIC)



NOTE : *NOT INCLUDE MOLD FINIS.

PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01
EIAJ CODE	TSOP032-P-0820-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____