SONY

CXP861P16

CMOS 8-bit Single-chip Microcomputer

For the availability of this product, please contact the sales office.

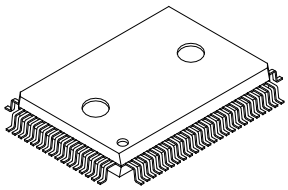
Description

The CXP861P16 is a highly integrated CMOS 8-bit single-chip microcomputer which is mainly composed of an 8-bit CPU, PROM, RAM and I/O ports. This microcomputer features many other high-performance circuits in a single-chip CMOS design, including an A/D converter, clock synchronized serial interface, UART, stepping motor controller, PWM generator, 16-bit timer/counter, and watchdog timer.

Also, the CXP861P16 provides the power-on reset function as well as the sleep/stop function which enables to lower power consumption.

This IC is the PROM-incorporated version of the CXP86116 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

80 pin QFP (PIastic)



Structure

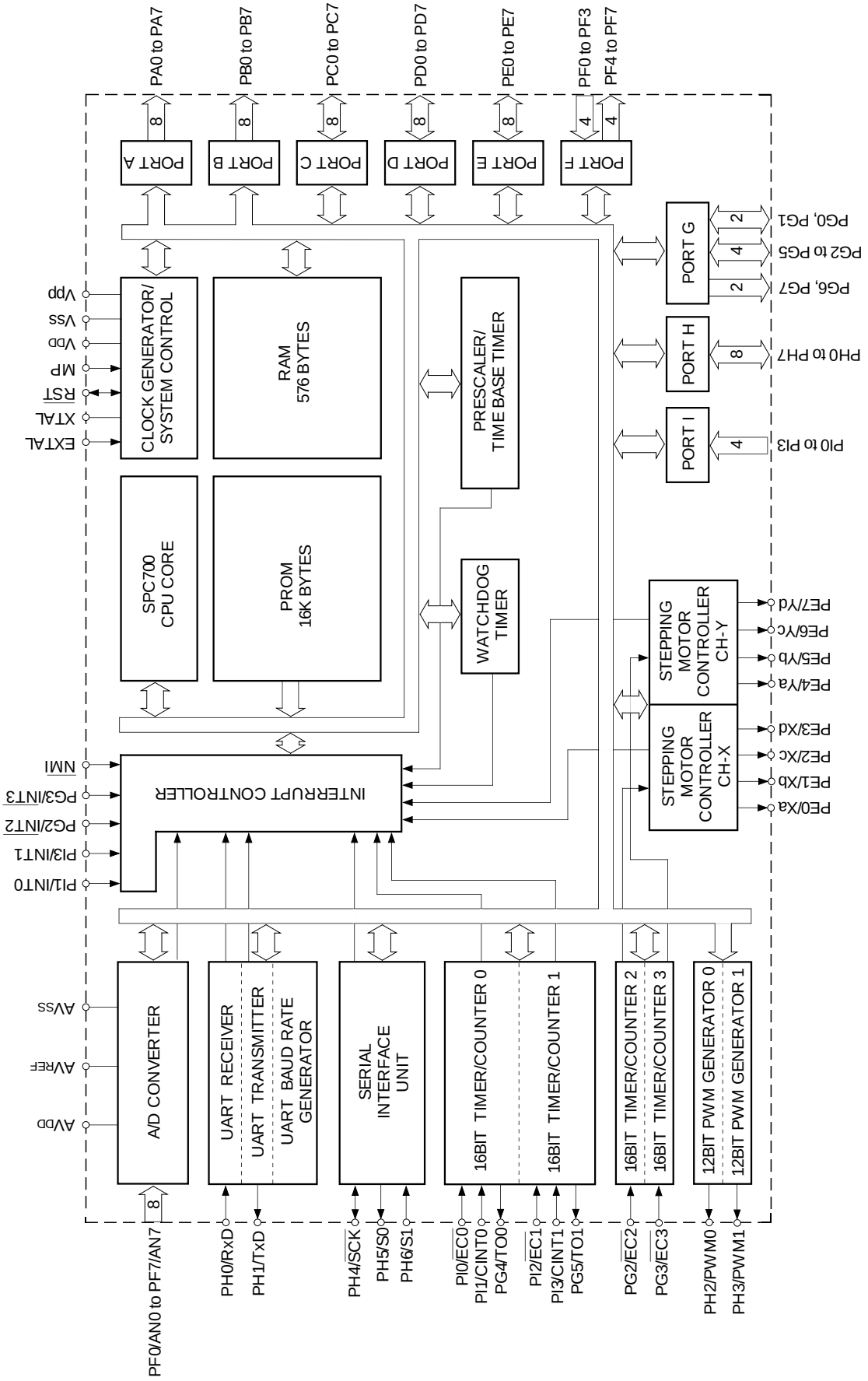
Silicon gate CMOS IC

Features

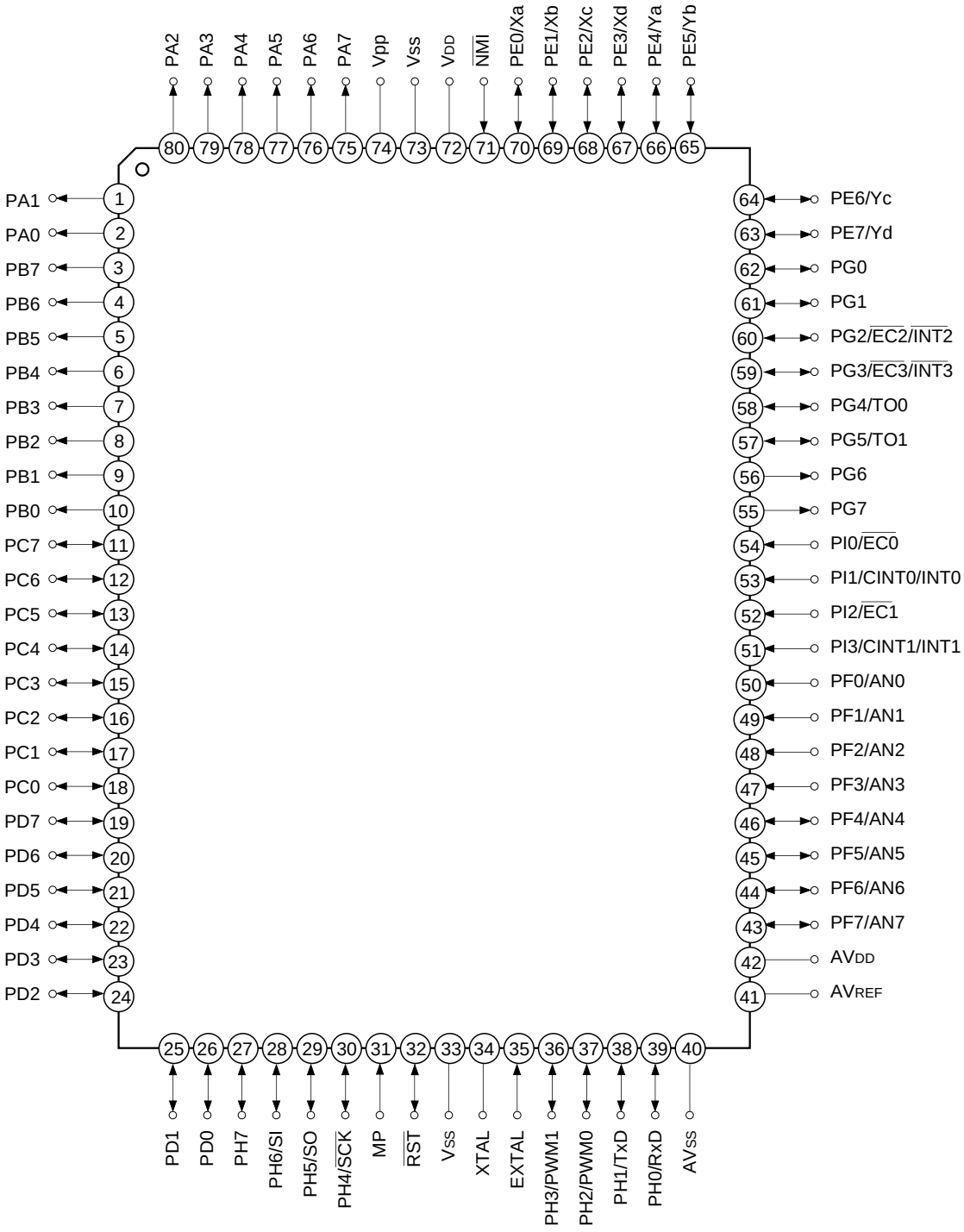
- Instruction set which supports a wide array of data types 213 types
  - — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation
- Minimum instruction cycle During operation 400ns/instruction 10MHz
- Incorporated PROM capacity 16K bytes
- Incorporated RAM capacity 576 bytes
- Peripheral functions
  - — A/D converter 8-bit, 8-channel, successive comparison type (conversion time: 32µs at 10MHz)
  - — Serial interface Universal Asynchronous Receiver Transmitter (baud-rate generator incorporated)
    8-bit clock synchronized type
  - — Stepping motor controller 2-channel stepping motor excitation output
  - — PWM output 2-channel 12-bit output
  - — Timer 2-channel 16-bit capture timer/counter
    2-channel 16-bit timer/counter (step rate generation function incorporated)
    19-bit time-base timer
  - — Watchdog timer
- Interrupts 17 factors, 15 vectors, multiple interrupt processing
- Standby mode SLEEP/STOP
- Package 80-pin plastic QFP

E95308-ST

Block Diagram



Pin Configuration (Top View)



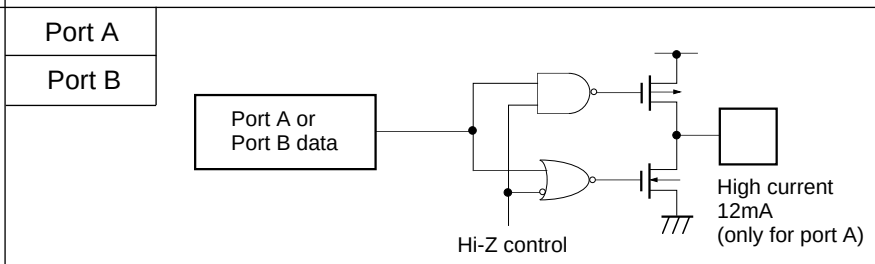
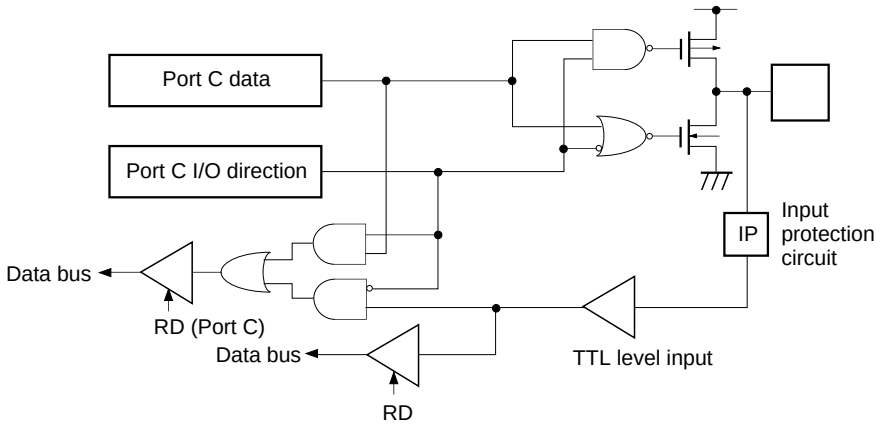
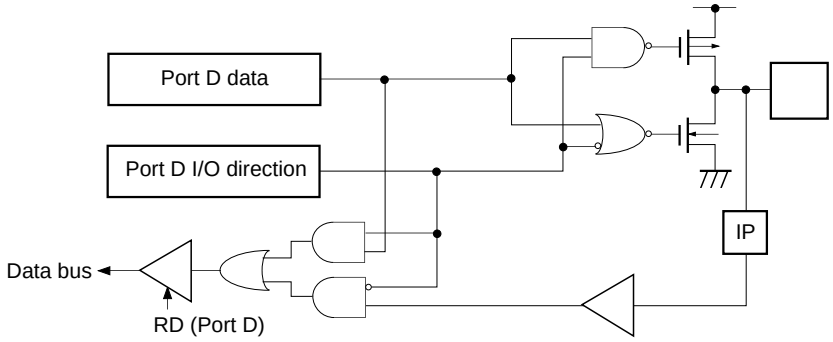
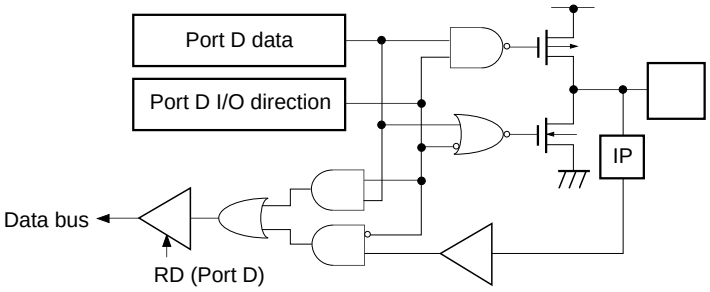
Note) 1. Vpp (Pin 74) is always connected to V_{DD}.
2. Vss (Pins 33 and 73) are both connected to GND.
3. MP (Pin 31) is always connected to V_{SS}.

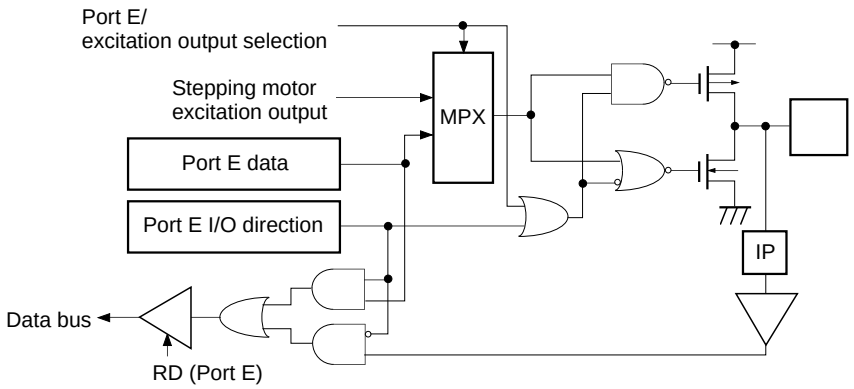
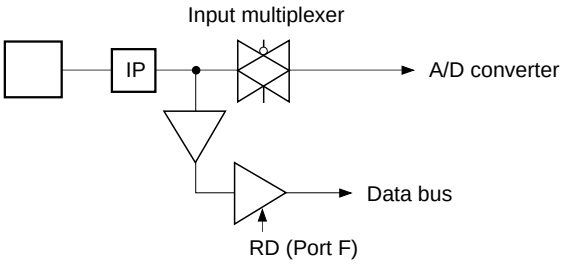
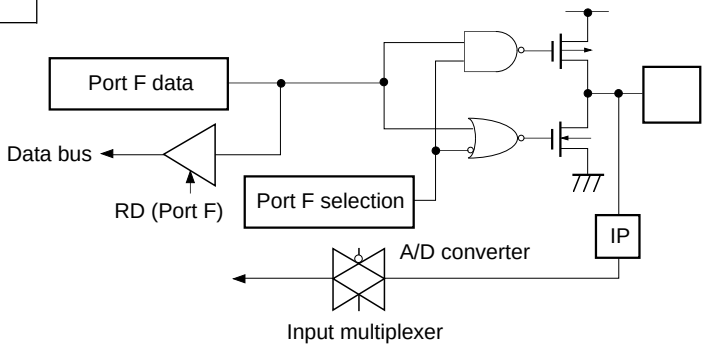
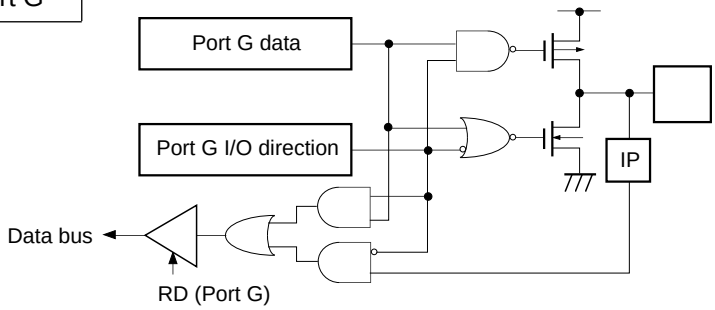
Pin Description

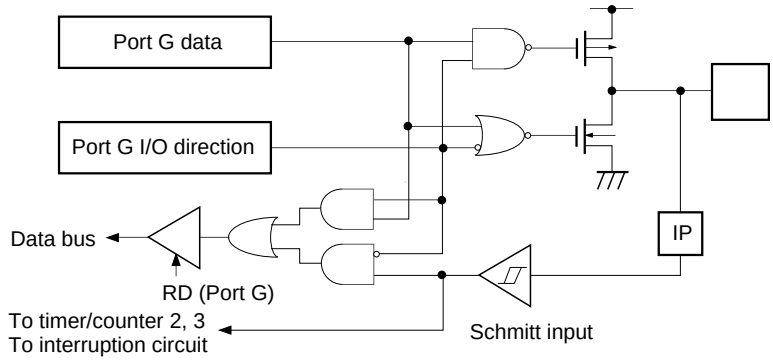
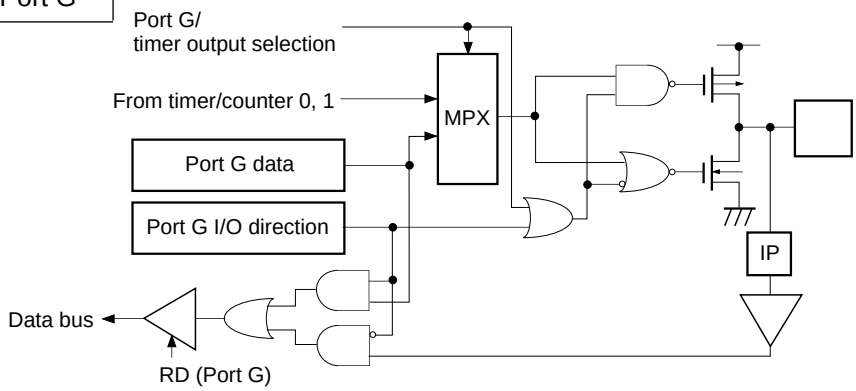
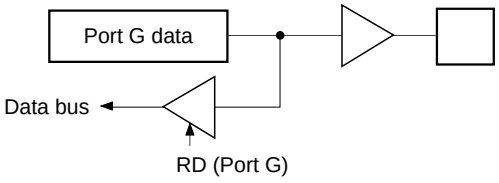
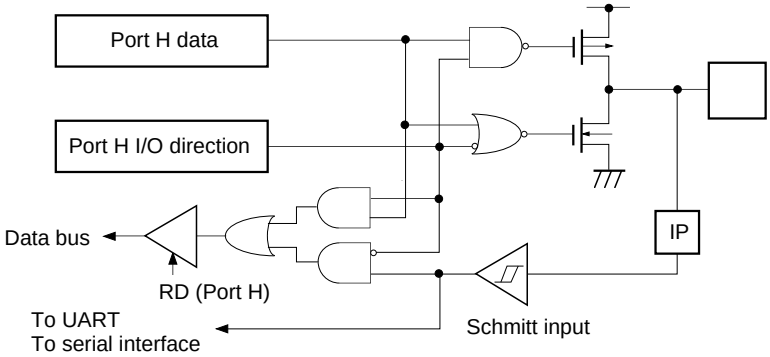
Symbol	I/O	Description		
PA0 to PA7	Output	(Port A) 8-bit output port. 12mA sink current can be driven. (8 pins)		
PB0 to PB7	Output	(Port B) 8-bit output port. (8 pins)		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. Enable to specify input/output by 4-bit unit. (8 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify input/output by 4-bit unit. (8 pins)		
PE0/Xa to PE3/Xd	I/O/output	(Port E) 8-bit I/O port. I/O can be selected in a unit of 4 bits. (8 pins)	Output for stepping motor control circuit CH-X. (4 pins)	
PE4/Ya to PE7/Yd	I/O/output		Output for stepping motor control circuit CH-Y. (4 pins)	
PF0/AN0 to PF3/AN3	Input/input	(Port F) Input port for the lower 4 bits; output port for the upper 4 bits. (8 pins)	Analog input to A/D converter. (8 pins)	
PF4/AN4 to PF7/AN7	Output/input			
PG0 PG1	I/O	(Port G) I/O port for the lower 6 bits; output port for the upper 2 bits. Enable to specify input/output by bit unit. (8 pins)		
PG2/$\overline{EC2}$/$\overline{INT2}$ PG3/$\overline{EC3}$/$\overline{INT3}$	I/O/input/input		External event input for timer/counter 2 and 3.	Input for external interrupt request.
PG4/TO0 PG5/TO1	I/O/output		Output for capture and timer/counter. (2 pins)	
PG6 PG7	Output			
PH0/RxD	I/O/input	(Port H) 8-bit I/O port. Enable to specify input/output by bit unit. (8 pins)	Input for UART reception data.	
PH1/TxD	I/O/output		Output for UART transmission data.	
PH2/PWM0	I/O/output		PWM output. (2 pins)	
PH3/PWM1	I/O/output			
PH4/$\overline{SCK}$	I/O/I/O		I/O for serial clock.	
PH5/SO	I/O/output		Output for serial data.	
PH6/SI	I/O/input		Input for serial data.	
PH7	I/O			

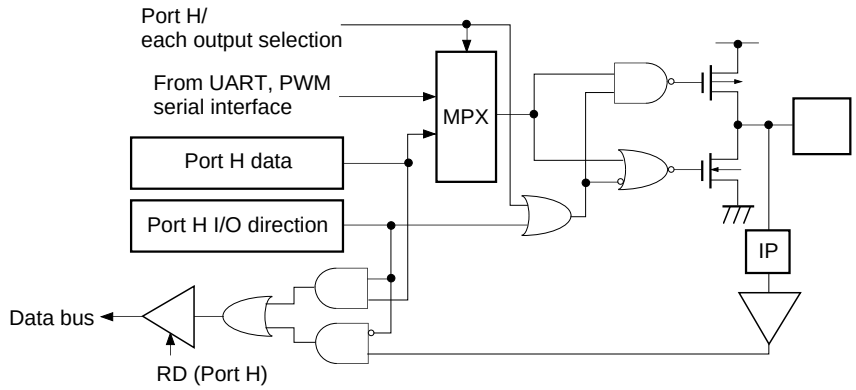
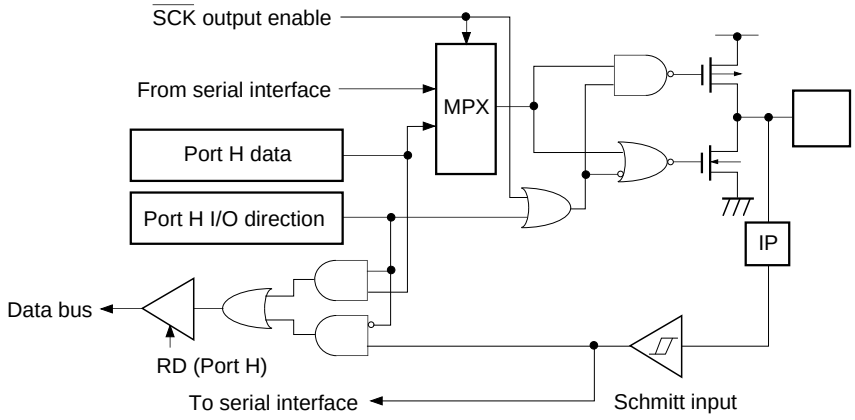
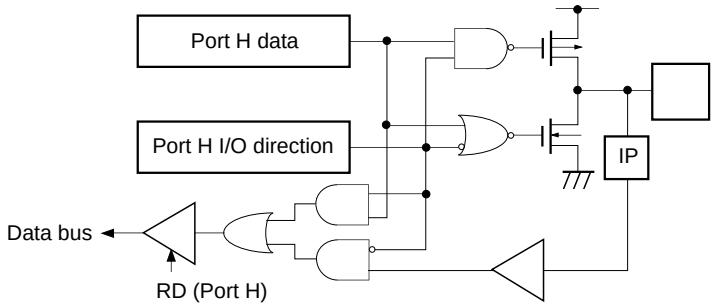
Symbol	I/O	Description		
PI0/$\overline{EC0}$	Input/input/input	(Port I) 4-bit input port. (4 pins)	External event input for timer/counter 0.	
PI1/CINT0 / INT0			Capture input for timer/counter 0.	Input for external interruption request.
PI2/$\overline{EC1}$			External event input for timer/counter 1.	
PI3/CINT1/ INT1			Capture input for timer/counter 1.	Input for external interruption request.
$\overline{NMI}$	Input	Non-maskable interruption request for active at falling edge.		
EXTAL	Input	Crystal connection for system clock oscillation. Input the clock to EXTAL pin and at the same time input the clock with reversed phase to XTAL pin when clock is input externally.		
XTAL	Output			
$\overline{RST}$	I/O	System reset for active at low level. $\overline{RST}$ pin becomes I/O pin, and outputs low level at the power on with power-on reset function executed. (mask option)		
MP	Input	Always connect to V_{SS}.		
AV_{DD}		Positive power supply for A/D converter.		
AV_{REF}	Input	Reference supply voltage input for A/D converter.		
AVss		GND for A/D converter.		
V_{DD}		Positive power supply.		
Vpp		Positive power supply for built-in PROM writing. Connect to V_{DD} for normal operation.		
Vss		GND. Connect both of Vss to GND.		

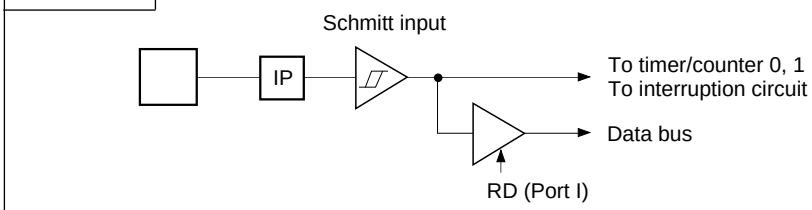
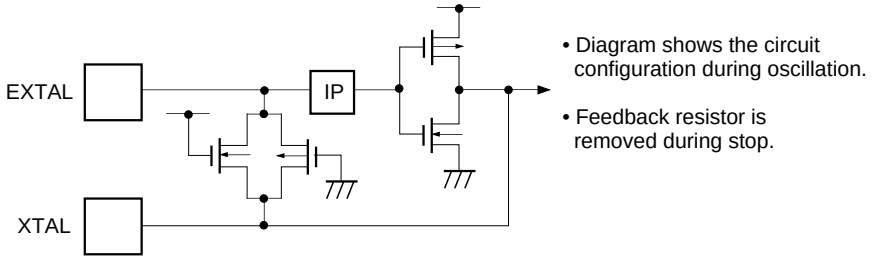
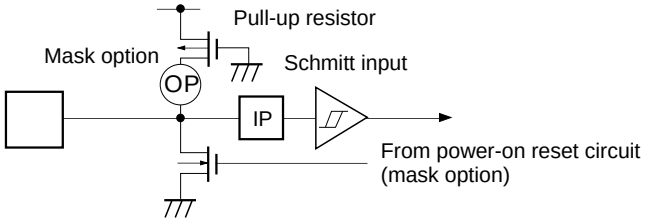
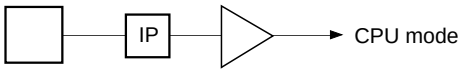
I/O Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA7 PB0 to PB7 16 pins	Port A Port B 	Hi-Z
PC0 to PC7 8 pins	Port C 	Hi-Z
PD0 to PD5 6 pins	Port D 	Hi-Z
PD6 PD7 2 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE0/Xa PE1/Xb PE2/Xc PE3/Xd PE4/Ya PE5/Yb PE6/Yc PE7/Yd 8 pins	Port E 	Hi-Z
PF0/AN0 to PF3/AN3 4 pins	Port F 	Hi-Z
PF4/AN4 to PF7/AN7 4 pins	Port F 	Hi-Z
PG0 PG1 2 pins	Port G 	Hi-Z

Pin	Circuit format	When reset
PG2/$\overline{EC2}$/$\overline{INT2}$ PG3/$\overline{EC3}$/$\overline{INT3}$ 2 pins	Port G 	Hi-Z
PG4/TO0 PG5/TO1 2 pins	Port G 	H level
PG6 PG7 2 pins	Port G 	Hi-Z
PH0/RxD PH6/SI 2 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
PH1/TxD PH2/PWM0 PH3/PWM1 PH5/SO 4 pins	Port H 	Hi-Z
PH4/$\overline{\text{SCK}}$ 1 pin	Port H 	Hi-Z
PH7 1 pin	Port H 	Hi-Z

Pin	Circuit format	When reset
PI0/$\overline{EC0}$ PI1/$\overline{CINT0}$/INT0 PI2/$\overline{EC1}$ PI3/$\overline{CINT1}$/INT1 4 pins	Port I 	Hi-Z
EXTAL XTAL 2 pins		Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total output pins
Low level output current	I_{OL}	15	mA	Other than high current output pins: per pin
	I_{OLC}	20	mA	High current port pin*3: per pin
Low level total output current	$\sum I_{OL}$	130	mA	Total output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The high current operation transistors are the N-CH transistors of the PA port.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5		Guaranteed data hold operation range during STOP
	Vpp	Vpp = V_{DD}		V	*6
Analog power supply	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input*3
	V_{IHT}	2.0	V_{DD}	V	TTL input*4
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*5
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input*3
	V_{ILT}	0	0.8	V	TTL input*4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5
Operating temperature	Topr	–10	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PD, PE, PF0 to PF3, PG0, PG1, PG4, PG5, PH1 to PH3, PH5, PH7), MP pin.

*3 Each pin of $\overline{NMI}$, PH6/SI, PH4/$\overline{SCK}$, PH0/RxD, $\overline{RST}$, PI0/$\overline{EC0}$, PI1/CINT0/INT0, PI2/$\overline{EC1}$, PI3/CINT1/INT1, PG2/$\overline{EC2}$/$\overline{INT2}$, PG3/$\overline{EC3}$/$\overline{INT3}$.

*4 Each pin of PC.

*5 It specifies only when the external clock is input.

*6 Vpp and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PH7, $\overline{PG}$, PH, $\overline{RST}$ (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PA	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PI, MP	V_{DD} = 5.5V V_1 = 0, 5.5V			±10	µA
Supply current*1	I_{DD}	V_{DD}	Crystal oscillation (C_1 = C_2 = 12pF) of 12MHz V_{DD} = 5V ± 0.5V*2		20	45	mA
	I_{DDS1}		SLEEP mode V_{DD} = 5V ± 0.5V		0.8	5	mA
	I_{DDS2}		STOP mode V_{DD} = 5V ± 0.5V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, V_{SS}, AV_{DD}, AV_{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

($Ta = -10$ to $+75°C$, $V_{DD} = 4.5$ to $5.5V$, $Vss = 0V$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1	10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	40		ns
System clock input rising and falling times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event clock input pulse width	t_{EH}, t_{EL}	$\overline{EC0}$, $\overline{EC1}$ $\overline{EC2}$, $\overline{EC3}$	Fig. 3	2tsys*		ns
Event count clock input rising and falling times	t_{ER}, t_{EF}	$\overline{EC0}$, $\overline{EC1}$ $\overline{EC2}$, $\overline{EC3}$	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Fig. 1. Clock timing

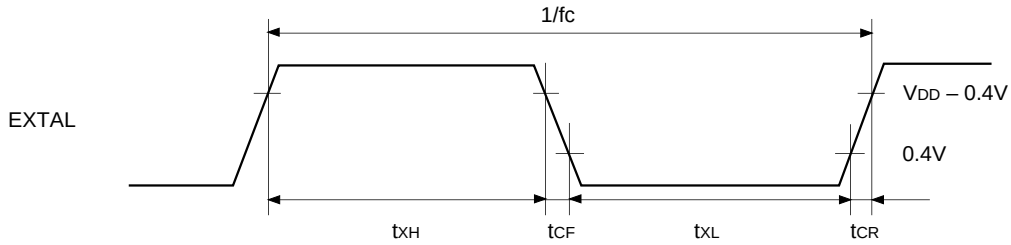


Fig. 2. Clock applying condition

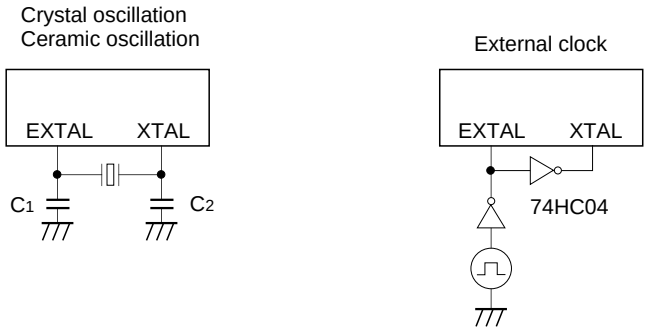
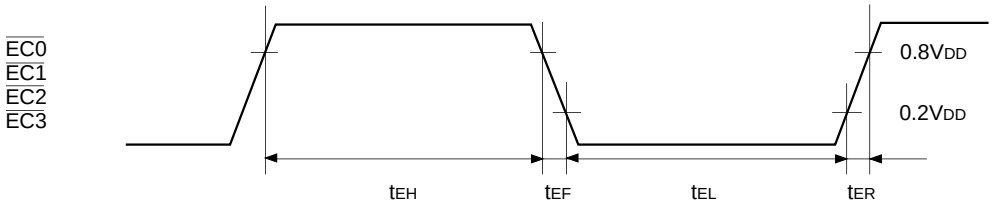


Fig. 3. Event count clock timing

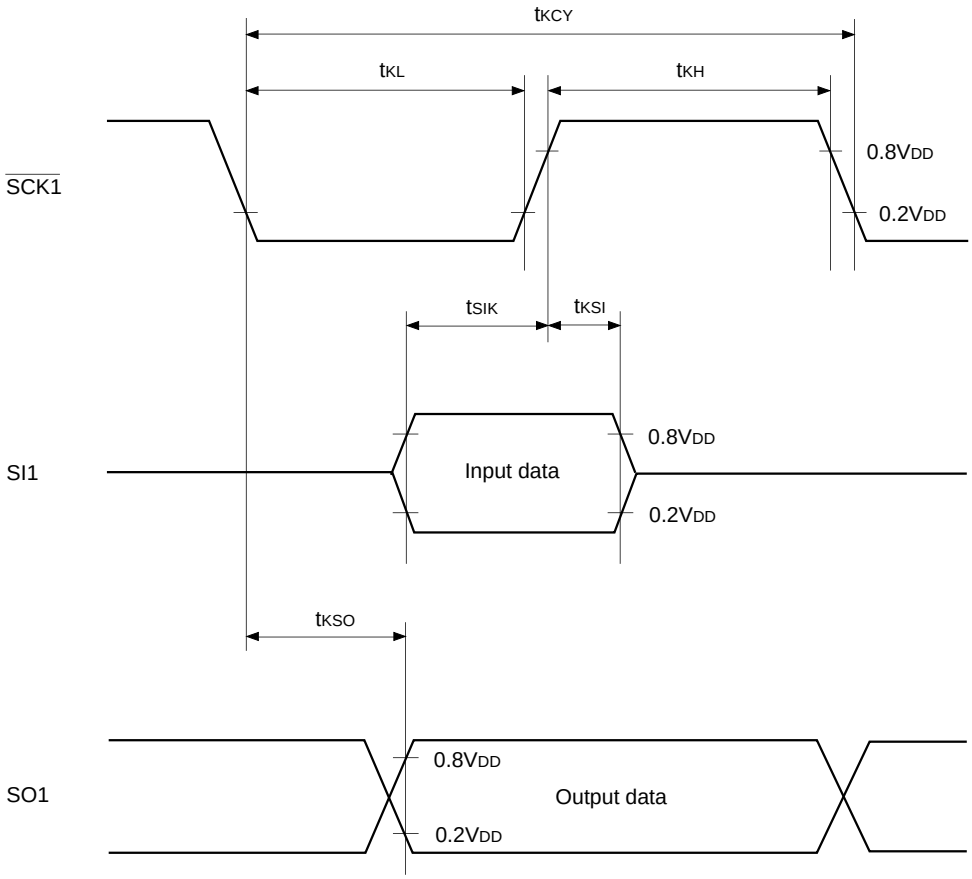


(2) Serial transfer (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI input setup time (against $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI input hold time (against $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ outptut mode and SO1 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing



(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Absolute error			Ta = 25°C V_{DD} = AV_{DD} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Conversion time	t_{CONV}			160/f_{ADC}*			µs
Sampling time	t_{SAMP}			12/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode			10	µA

* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FF$_H$ bit 0).

When PS2 is selected, f_{ADC} = fc/2

When PS1 is selected, f_{ADC} = fc

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 $\overline{INT2}$ $\overline{INT3}$ $\overline{NMI}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 5. Interruption input timing

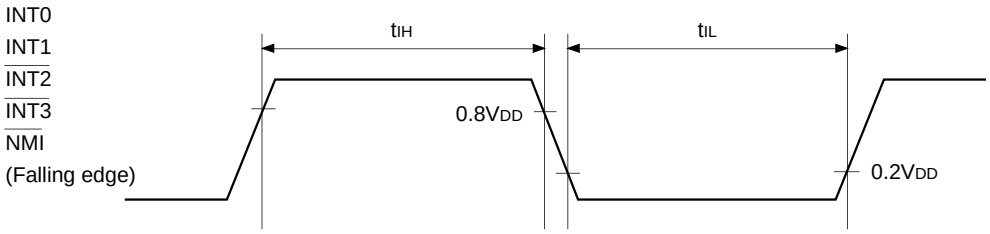
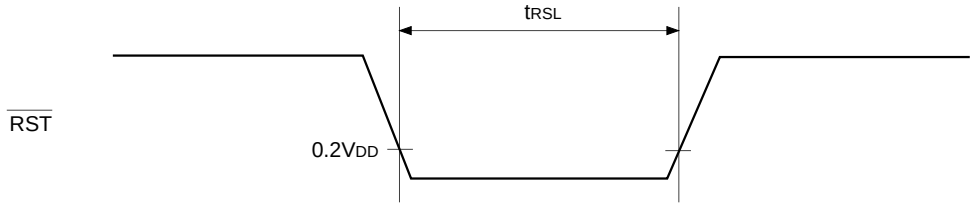


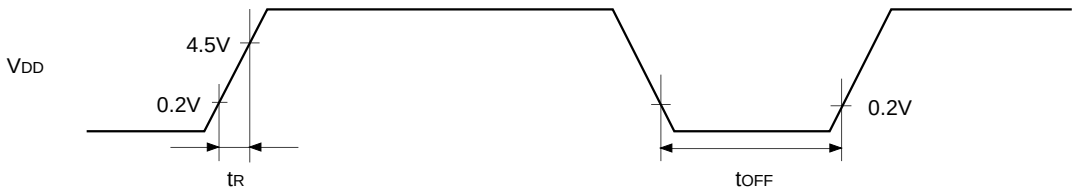
Fig. 6. Reset input timing



(5) Power on reset (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

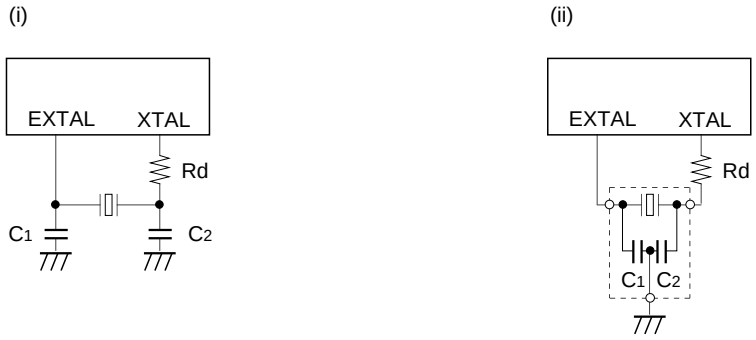
Fig. 7. Power on reset



The power supply should be rise smoothly.

Supplement

Fig. 8. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CST8.00MTW*					(ii)
	CSA10.0MTZ	10.00	30	30	0	(i)
	CST10.0MTW*					(ii)
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	12	12	470	(i)
		10.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22	22	0	(i)
		10.00				

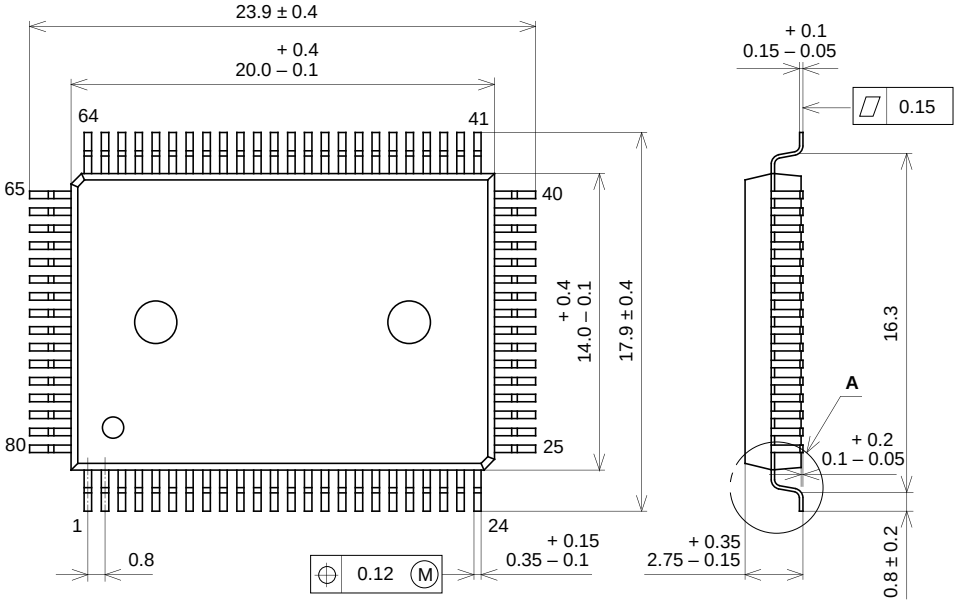
Those marked with an asterisk (*) signify types with built-in ground capacitance. (C_1, C_2)

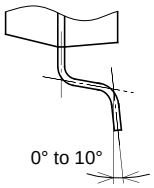
Mask option table

Item	Mask product	CXP861P16Q-1-□□□
Reset pin pull-up resistor	Non-existent/Existent	Existent
Power on reset circuit	Non-existent/Existent	Existent

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g