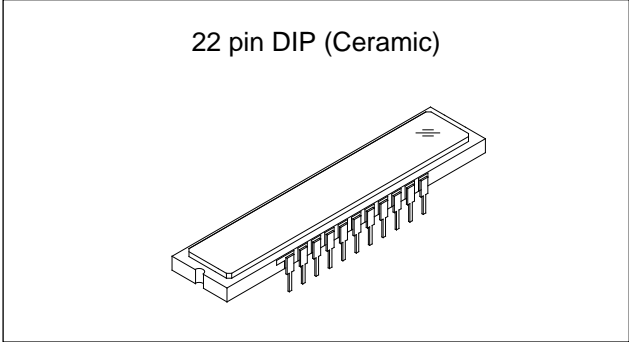


**5000-pixel CCD Linear Image Sensor (B/W)**

**Description**

The ILX506 is a reduction type CCD linear sensor developed for high resolution facsimiles and copiers. This sensor reads A3-size documents at a density of 400 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use. In addition, reset pulse can be switched between internal generation and external input.



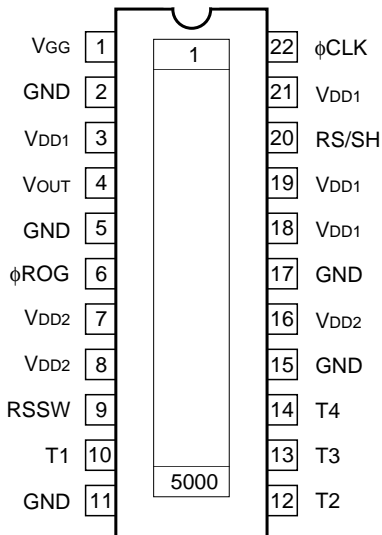
**Features**

- Number of effective pixels: 5000 pixels
- Pixel size: 7µm × 7µm (7µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag/ultra high sensitivity/low dark output
- Single output method
- Maximum clock frequency: 12.5MHz

**Absolute Maximum Ratings**

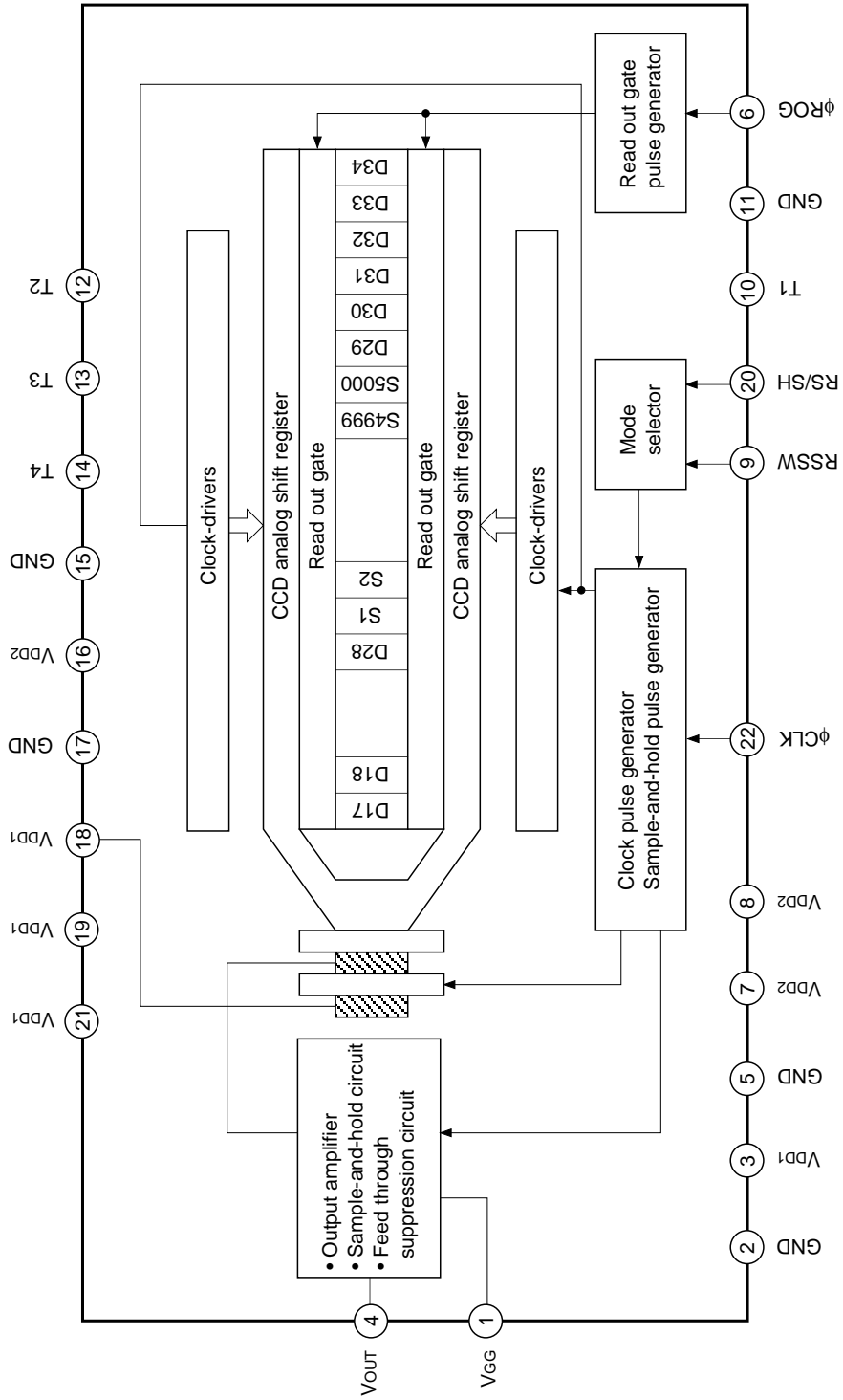
- Supply voltage V<sub>DD1</sub> 11 V  
V<sub>DD2</sub> 6 V
- Operating temperature -10 to +60 °C
- Storage temperature -30 to +80 °C

**Pin Configuration (Top View)**



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Block Diagram



## Pin Description

Pin No.	Symbol	Description
1	V <sub>GG</sub>	Output circuit gate bias
2	GND	GND
3	V <sub>DD1</sub>	9V power supply
4	V <sub>OUT</sub>	Signal output
5	GND	GND
6	φ <sub>ROG</sub>	Clock pulse
7	V <sub>DD2</sub>	5V power supply
8	V <sub>DD2</sub>	5V power supply
9	RSSW*1	Reset pulse switchover pin
10	T1	Test pin (5V)
11	GND	GND
12	T2	Test pin (GND)
13	T3	Test pin (5V)
14	T4	Test pin (GND)
15	GND	GND
16	V <sub>DD2</sub>	5V power supply
17	GND	GND
18	V <sub>DD1</sub>	9V power supply
19	V <sub>DD1</sub>	9V power supply
20	RS/SH*1	Clock pulse or with S/H; without S/H switch
21	V <sub>DD1</sub>	9V power supply
22	φ <sub>CLK</sub>	Clock pulse

\*1 Output mode is changeable as follows.

20pin 9pin	GND	V <sub>DD1</sub>	φ <sub>RS</sub>
GND	Internal RS without S/H	Internal RS with S/H	—
V <sub>DD1</sub>	—	—	External RS without S/H

**Recommended Voltage**

Item	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	8.5	9.0	9.5	V
V <sub>DD2</sub>	4.75	5.0	5.25	V

**Note)** Rules for raising and lowering power supply voltage

To raise power supply voltage, first raise V<sub>DD1</sub> (9V) and then V<sub>DD2</sub> (5V).

To lower voltage, first lower V<sub>DD2</sub> (5V) and then V<sub>DD1</sub> (9V).

**Clock Characteristics**

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of $\phi$ CLK pin	C $\phi$ CLK	—	10	—	pF
Input capacity of $\phi$ ROG pin	C $\phi$ ROG	—	10	—	pF
Input capacity of RS/SH pin	C <sub>RS/SH</sub>	—	10	—	pF
Frequency of $\phi$ CLK	f $\phi$ CLK	—	1	12.5	MHz
Frequency of $\phi$ RS	f $\phi$ RS	—	1	12.5	MHz

**Electro-optical Characteristics (Note 1)**

(Ta = 25°C, V<sub>DD1</sub> = 9V, V<sub>DD2</sub> = 5V, φCLK = 1MHz, Internal φRS mode without S/H,  
Light source = 3200K, IR cut filter, CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	7.5	10.8	13.9	V/(lx · s)	Note 2
Sensitivity 2	R2	—	24.6	—	V/(lx · s)	Note 3
Sensitivity nonuniformity	PRNU	—	4	10	%	Note 4
Saturation output voltage	V <sub>SAT</sub>	1.0	1.5	—	V	Note 5
Saturation exposure	SE	0.072	0.139	—	lx · s	Note 6
Even and odd black level DC difference	ΔV	—	1.0	10.0	mV	Note 7
Dark voltage average	V <sub>DRK</sub>	—	0.3	2	mV	Note 8
Dark signal nonuniformity	DSNU	—	0.6	3	mV	Note 9
Image lag	IL	—	0.02	—	%	Note 10
9V supply current	I <sub>VDD1</sub>	—	16	32	mA	—
5V supply current	I <sub>VDD2</sub>	—	3	7	mA	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Z <sub>o</sub>	—	600	—	Ω	—
Offset level	V <sub>OS</sub>	—	3.0	—	V	Note 11
Dynamic range	DR	500	5000	—	—	Note 12

**Notes)**

- 1) In accordance with the given electrooptical characteristics, the even black level is defined as the mean value of D8, D10, D12 to D14.  
The odd black level is defined as the mean value of D7, D9, D11 and D13.
- 2) For the sensitivity test light is applied with a uniform intensity of illumination.
- 3) W lamp (2854K)
- 4) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$\text{PRNU} = \frac{(V_{\text{MAX}} - V_{\text{MIN}})/2}{V_{\text{AVE}}} \times 100 [\%]$$

Where the 5000 pixels are divided into blocks of 100, even and odd pixels, respectively. The maximum output of each block is set to V<sub>MAX</sub>, the minimum output to V<sub>MIN</sub> and the average output to V<sub>AVE</sub>.

- 5) Use below the minimum value of the saturation output voltage.
- 6) Saturation exposure is defined as follows.

$$\text{SE} = \frac{V_{\text{SAT}}}{R1}$$

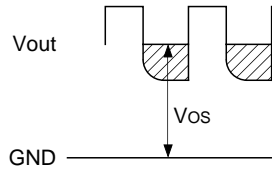
- 7) Indicates the DC difference in value between odd black level and even black level.
- 8) Optical signal accumulated time τ int stands at 10ms.

- 9) The difference between the maximum and mean values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity.

Optical signal accumulated time  $\tau_{int}$  stands at 10ms.

- 10)  $V_{OUT} = 500\text{mV}$  (Typ.)

- 11)  $V_{OS}$  is defined as indicated below.

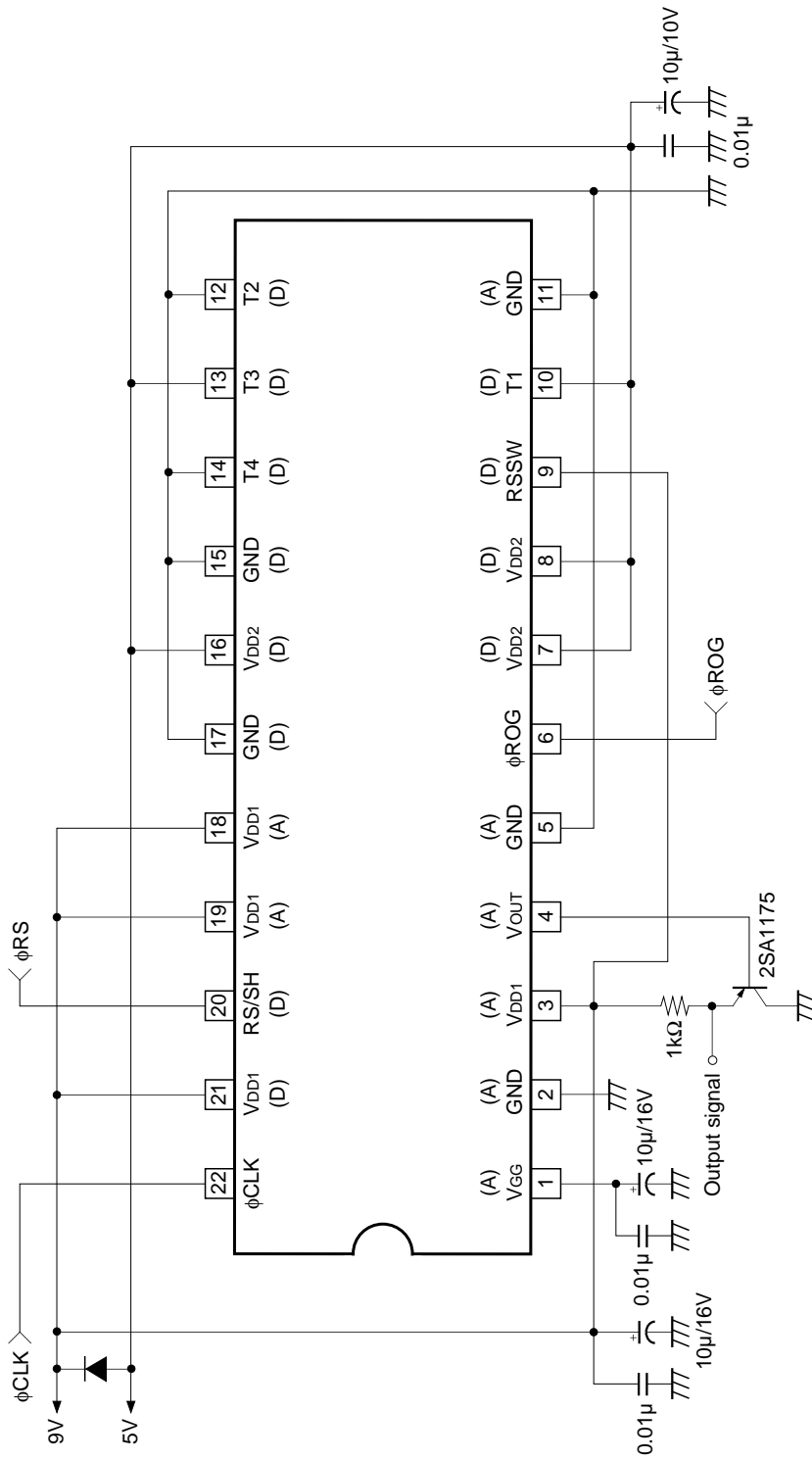


- 12) Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

When optical accumulated time is shorter, the dynamic range gets wider because dark voltage is in proportion to optical accumulated time.

Application Circuit\*

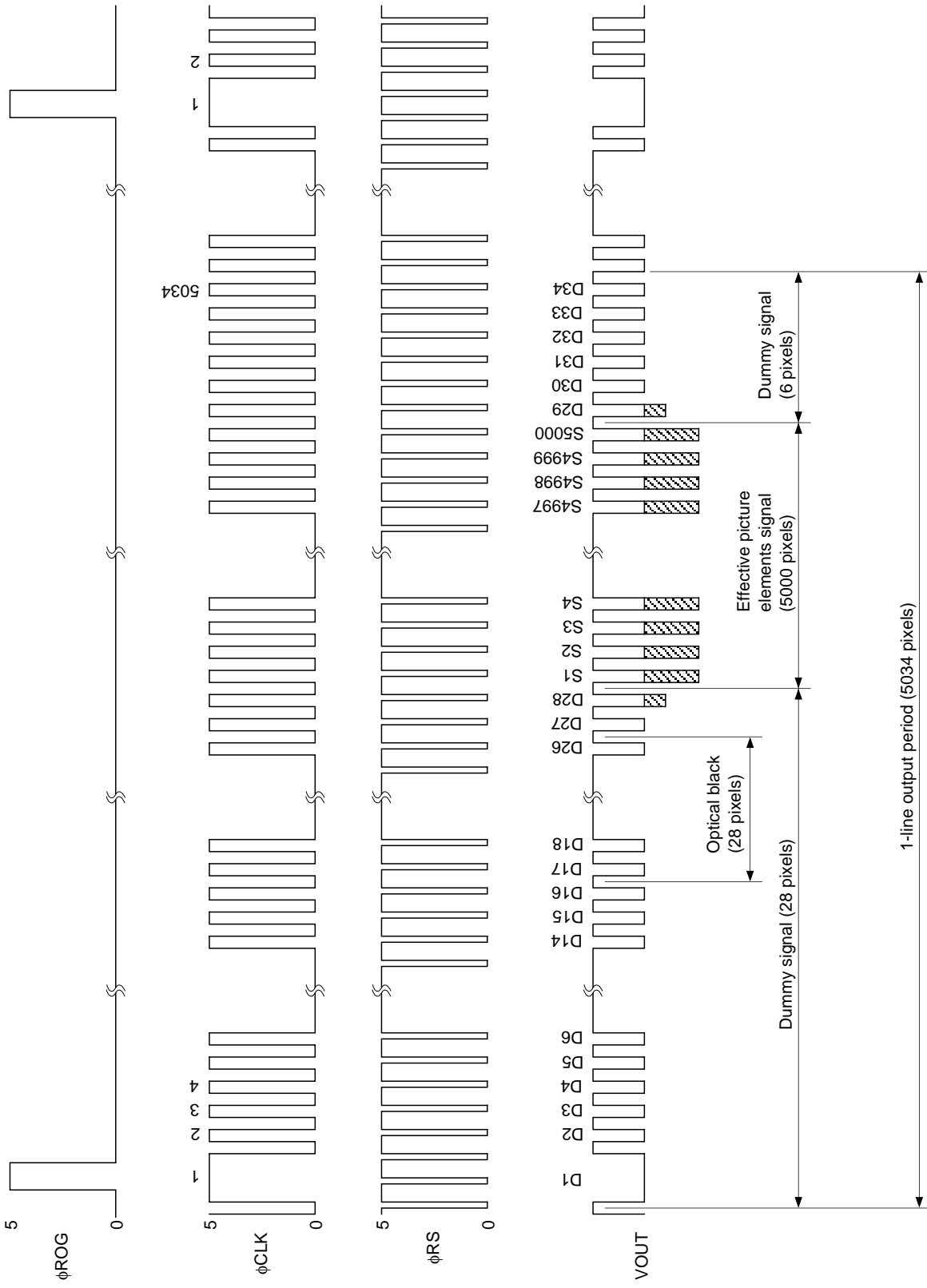


\* This application circuit shows when φRS is used externally.

( When noise influence into output signal is large, connect pins indicated by (A) to the analog power supply and )  
 ( pins indicated by (D) to the digital power supply, and also use a decoupling capacitor of large capacitance. )

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Clock Timing Diagram\***

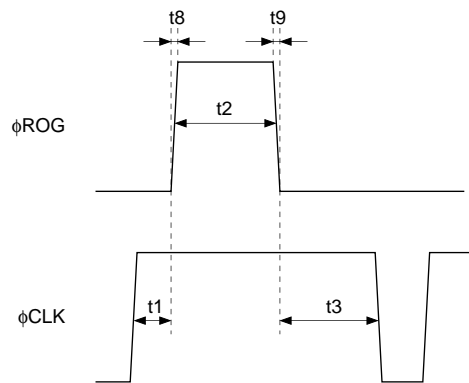


\* This clock timing diagram shows when  $\phi$ RS is used externally.

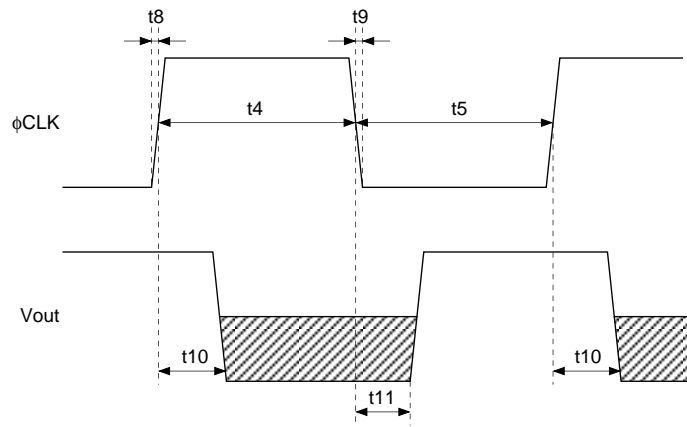


**Clock Pulse Waveform Conditions**

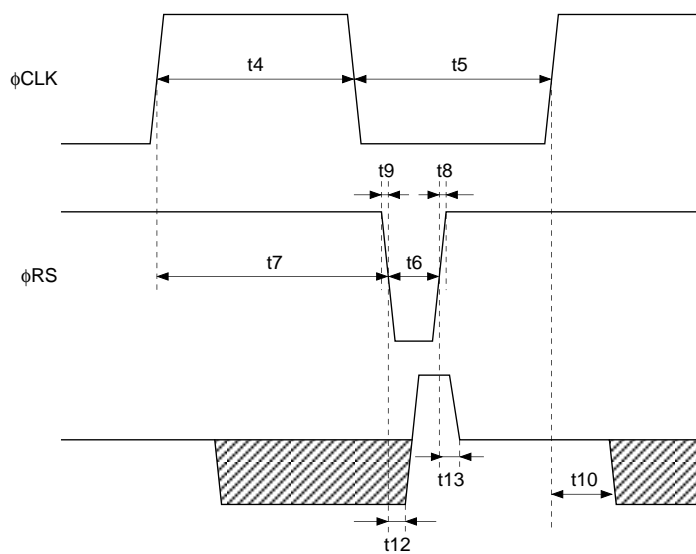
**$\phi$ CLK,  $\phi$ ROG pulse related**



**Internal  $\phi$ RS mode**



**External  $\phi$ RS mode**

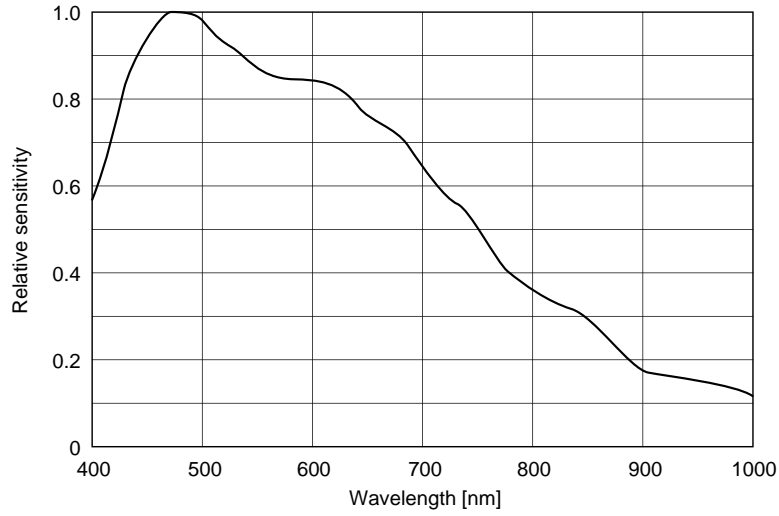


Item		Symbol	Min.	Typ.	Max.	Unit
$\phi$ ROG, $\phi$ CLK pulse timing		t1	100	200	—	ns
$\phi$ ROG, $\phi$ CLK pulse timing		t3	800	1000	—	ns
$\phi$ ROG pulse high level period		t2	800	1000	—	ns
$\phi$ CLK pulse high level period		t4	40	500*1	—	ns
$\phi$ CLK pulse low level period		t5	40	500*1	—	ns
$\phi$ RS pulse low level period		t6	25	100*1	—	ns
$\phi$ CLK, $\phi$ RS pulse timing		t7	60	550*1	10 + t4 + t5	ns
Input clock pulse rise/fall time		t8, t9	—	5	10	ns
Input clock pulse voltage	High level	$V_{\phi\text{CLK}}, V_{\phi\text{ROG}}$	4.5	5.0	5.5	V
	Low level	$V_{\phi\text{RS}}$	0	—	0.5	V
Signal output delay time	Internal $\phi$ RS	t10	—	95	—	ns
		t11	—	70	—	ns
	External $\phi$ RS	t12	—	45	—	ns
		t13	—	60	—	ns

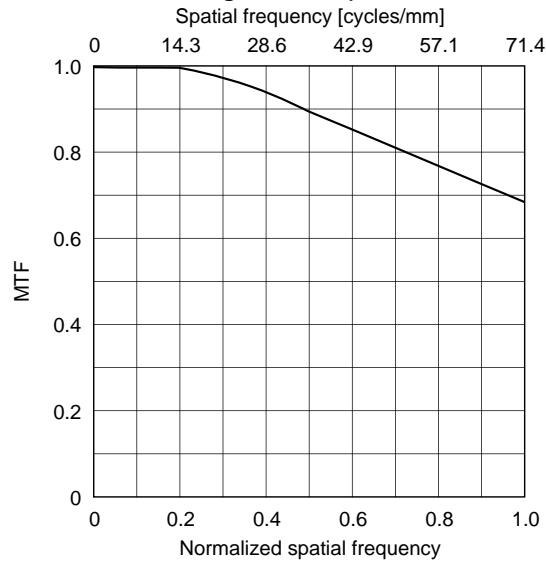
\*1 Recommended condition during  $\phi$ CLK = 1MHz.

Example of Representative Characteristics ( $V_{DD1} = 9V$ ,  $V_{DD2} = 5V$ ,  $T_a = 25^\circ C$ )

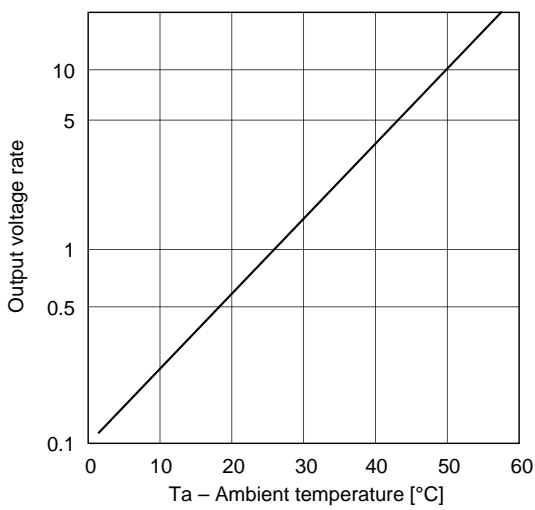
**Spectral sensitivity characteristics  
(Standard characteristics)**



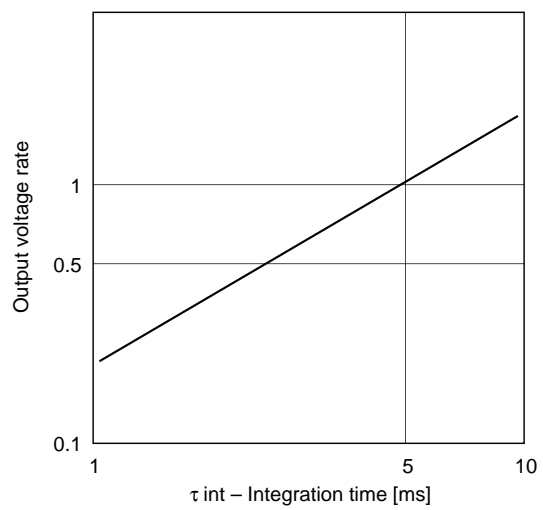
**MTF of main scanning direction (Standard characteristics)**



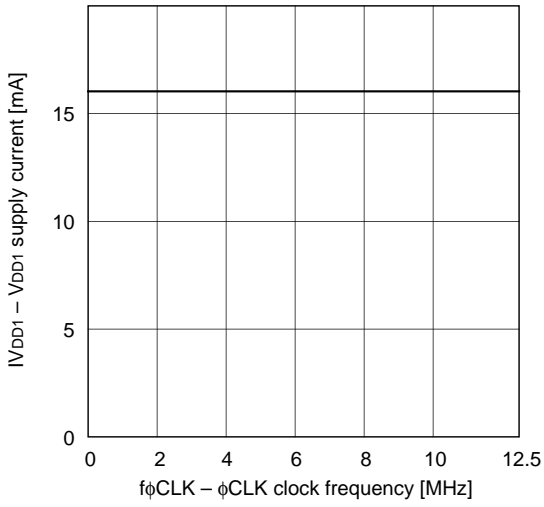
**Dark signal output temperature characteristics  
(Standard characteristics)**



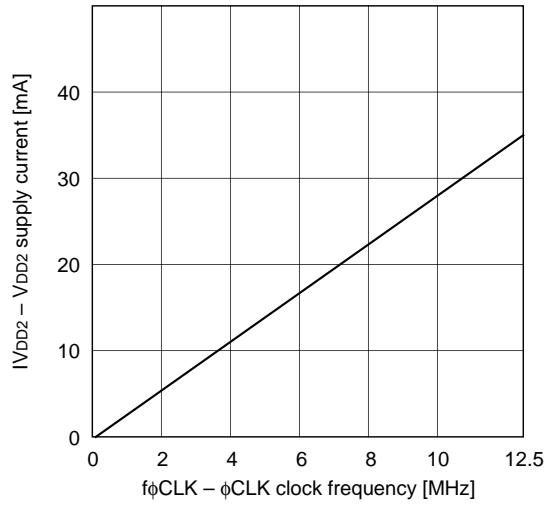
**Integration time output voltage characteristics  
(Standard characteristics)**



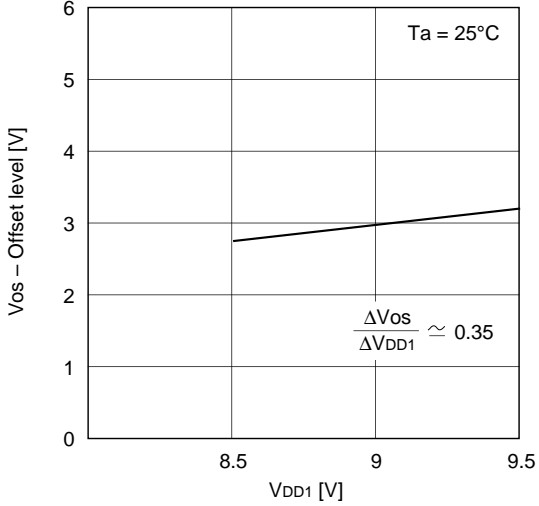
**Operational frequency characteristics of the VDD1 supply current (Standard characteristics)**



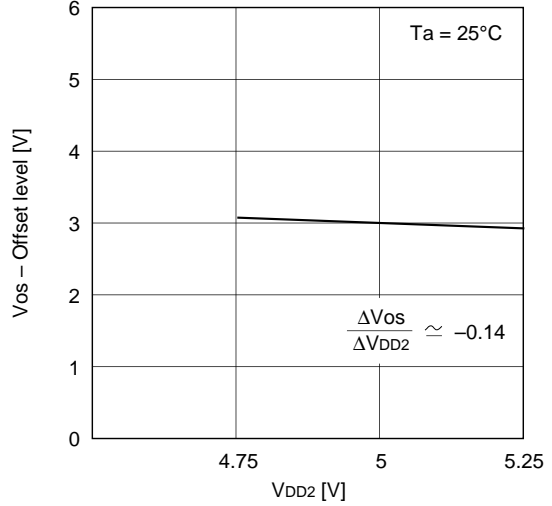
**Operational frequency characteristics of the VDD2 supply current (Standard characteristics)**



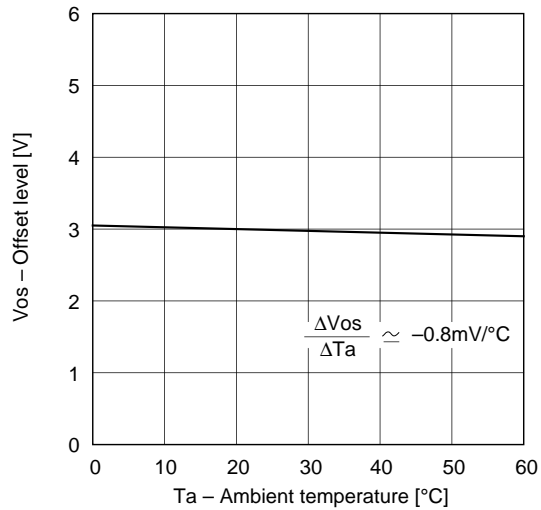
**Offset level vs. VDD1 characteristics (Standard characteristics)**



**Offset level vs. VDD2 characteristics (Standard characteristics)**



**Offset level vs. Temperature characteristics (Standard characteristics)**

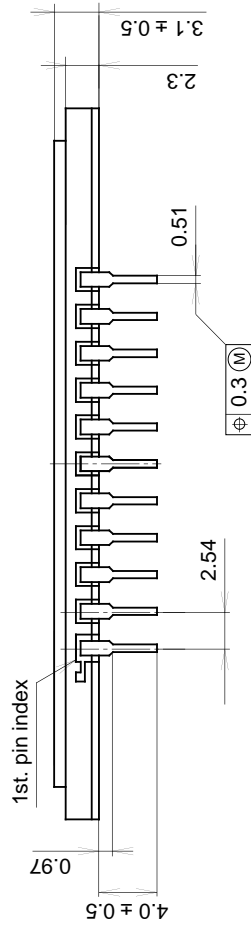
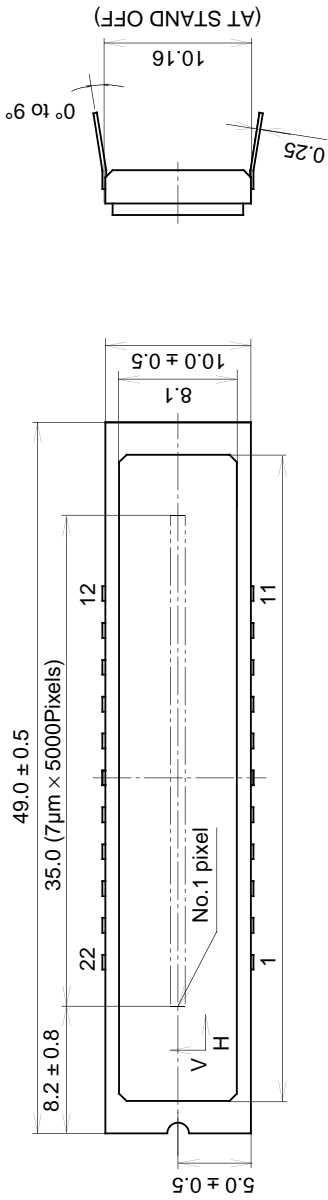


## Notes on Handling

- 1) Static charge prevention  
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
  - a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
  - b) When handling directly use an earth band.
  - c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
  - d) Ionized air is recommended for discharge when handling CCD image sensor.
  - e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.
  
- 2) Regulation for raising and lowering the power supply voltage  
When raising the supply voltage, first raise  $V_{DD1}$  (9V) and then  $V_{DD2}$  (5V).  
Similarly, lower  $V_{DD2}$  (5V) first and then  $V_{DD1}$  (9V).
  
- 3) Soldering
  - a) Make sure the package temperature does not exceed 80°C.
  - b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
  - c) To dismount an image sensor, do not use a solder suction equipment.  
When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.
  
- 4) Dust and dirt protection
  - a) Operate in clean environments.
  - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
  - c) Clean with a cotton bud and ethyl alcohol if the grease stained.  
Be careful not to scratch the glass.
  - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
  
- 5) Exposure to high temperatures or humidity will affect the characteristics.  
Accordingly avoid storage or usage in such conditions.
  
- 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is  $1.42 \pm 0.3$ mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	3.9g