SONY

ILX514

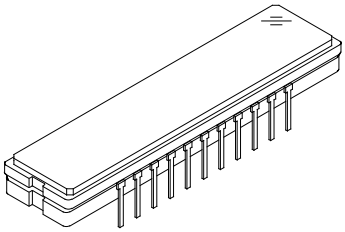
3918-pixel CCD Linear Image Sensor (B/W)

For the availability of this product, please contact the sales office.

Description

The ILX514 is a reduction type CCD linear sensor developed for high resolution facsimiles and copiers. This sensor reads A4-size documents at a density of 400 DPI (Dot Per Inch). A built-in timing generator and clock-drivers ensure direct drive at 5V logic for easy use. In addition, reset pulse can be switched between internal generation and external input.

22 pin DIP (Cer-DIP)



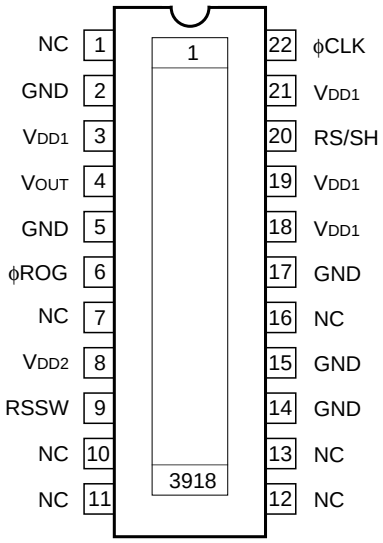
Features

- Number of effective pixels: 3918 pixels
- Pixel size: 7µm × 7µm (7µm pitch)
- Built-in timing generator and clock-drivers
- Ultra low lag/ultra high sensitivity/low dark output
- Single output method
- Maximum clock frequency: 5MHz

Absolute Maximum Ratings

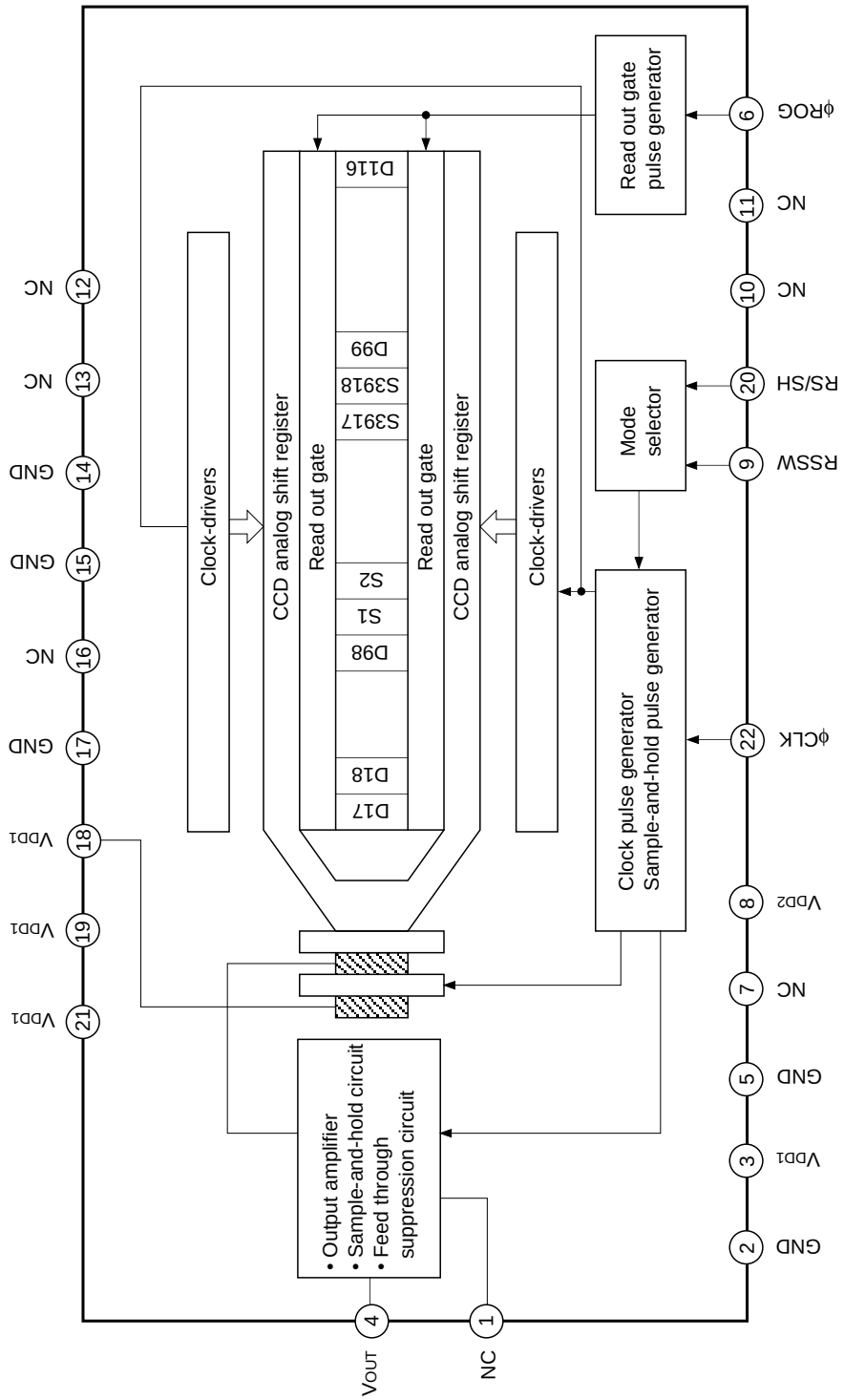
• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



E93302C78-PS

Block Diagram



Pin Description

Pin No.	Symbol	Description
1	NC	NC
2	GND	GND
3	V_{DD1}	9V power supply
4	V_{OUT}	Signal output
5	GND	GND
6	ϕROG	Clock pulse
7	NC	NC
8	V_{DD2}	5V power supply
9	RSSW*1	Reset pulse swithover pin
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	GND	GND
15	GND	GND
16	NC	NC
17	GND	GND
18	V_{DD1}	9V power supply
19	V_{DD1}	9V power supply
20	RS/SH*1	Clock pulse or with S/H; without S/H switch
21	V_{DD1}	9V power supply
22	ϕCLK	Clock pulse

*1 Output mode is changeable as follows.

9pin \ 20pin	GND	V_{DD1}	ϕRS
GND	Internal RS without S/H	Internal RS with S/H	—
V_{DD1}	—	—	External RS without S/H

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage
To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φCLK pin	$C_{\phi CLK}$	—	10	—	pF
Input capacity of φROG pin	$C_{\phi ROG}$	—	10	—	pF
Input capacity of RS/SH pin	$C_{RS/SH}$	—	10	—	pF
Frequency of φCLK	$f_{\phi CLK}$	—	1	5	MHz
Frequency of φRS	$f_{\phi RS}$	—	1	5	MHz

Electro-optical Characteristics (Note 1)

(Ta = 25°C, V_{DD1} = 9V, V_{DD2} = 5V, ϕCLK = 1MHz, Internal ϕRS mode without S/H, Light source = 3200K, IR cut filter, CM-500S (t = 1.0mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	7.5	10.8	13.9	V/(lx · s)	Note 2
Sensitivity 2	R2	—	24.6	—	V/(lx · s)	Note 3
Sensitivity nonuniformity	PRNU	—	4	10	%	Note 4
Saturation output voltage	V_{SAT}	1.0	1.5	—	V	Note 5
Saturation exposure	SE	0.072	0.139	—	lx · s	Note 6
Even and odd black level DC difference	ΔV	—	1.0	10	mV	Note 7
Dark voltage average	V_{DRK}	—	0.3	2	mV	Note 8
Dark signal nonuniformity	DSNU	—	0.6	3	mV	Note 9
Image lag	IL	—	0.02	—	%	Note 10
9V supply current	I_{VDD1}	—	16	32	mA	—
5V supply current	I_{VDD2}	—	2.1	5.0	mA	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Z_O	—	600	—	Ω	—
Offset level	V_{OS}	—	3.0	—	V	Note 11
Dynamic range	DR	500	5000	—	—	Note 12

Notes)

1) In accordance with the given electrooptical characteristics, the even black level is defined as the mean value of D8, D10, D12 and D14.
   The odd black level is defined as the mean value of D7 , D9, D11 and D13.
2) For the sensitivity test light is applied with a uniform intensity of illumination.
3) W lamp (2854K)
4) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   Where the 3918 pixels are divided into blocks of 98, even and odd pixels, respectively (Even and odd last blocks are 97). The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
5) Use below the minimum value of the saturation output voltage.
6) Saturation exposure is defined as follows.

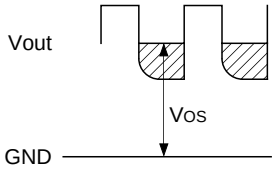
$$SE = \frac{V_{SAT}}{R1}$$

7) Indicates the DC difference in value between odd black level and even black level.
8) Optical signal accumulated time τ int stands at 10ms.

9) The difference between the maximum and mean values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity.
Optical signal accumulated time τ int stands at 10ms.

10) V_{OUT} = 500mV (Typ.)

11) Vos is defined as indicated below.

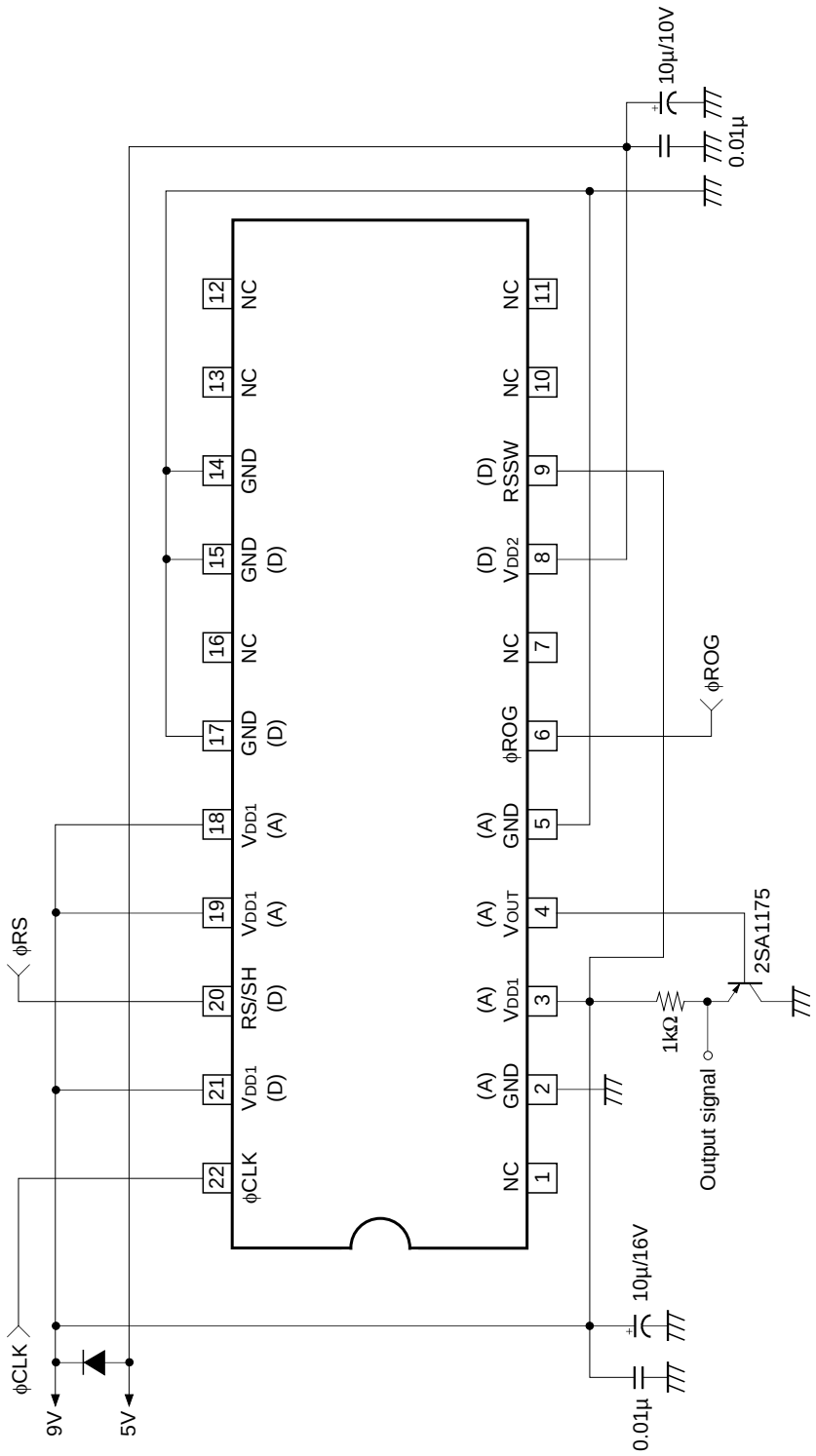


12) Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

When optical accumulated time is shorter, the dynamic range gets wider because dark voltage is in proportion to optical accumulated time.

Application Circuit*

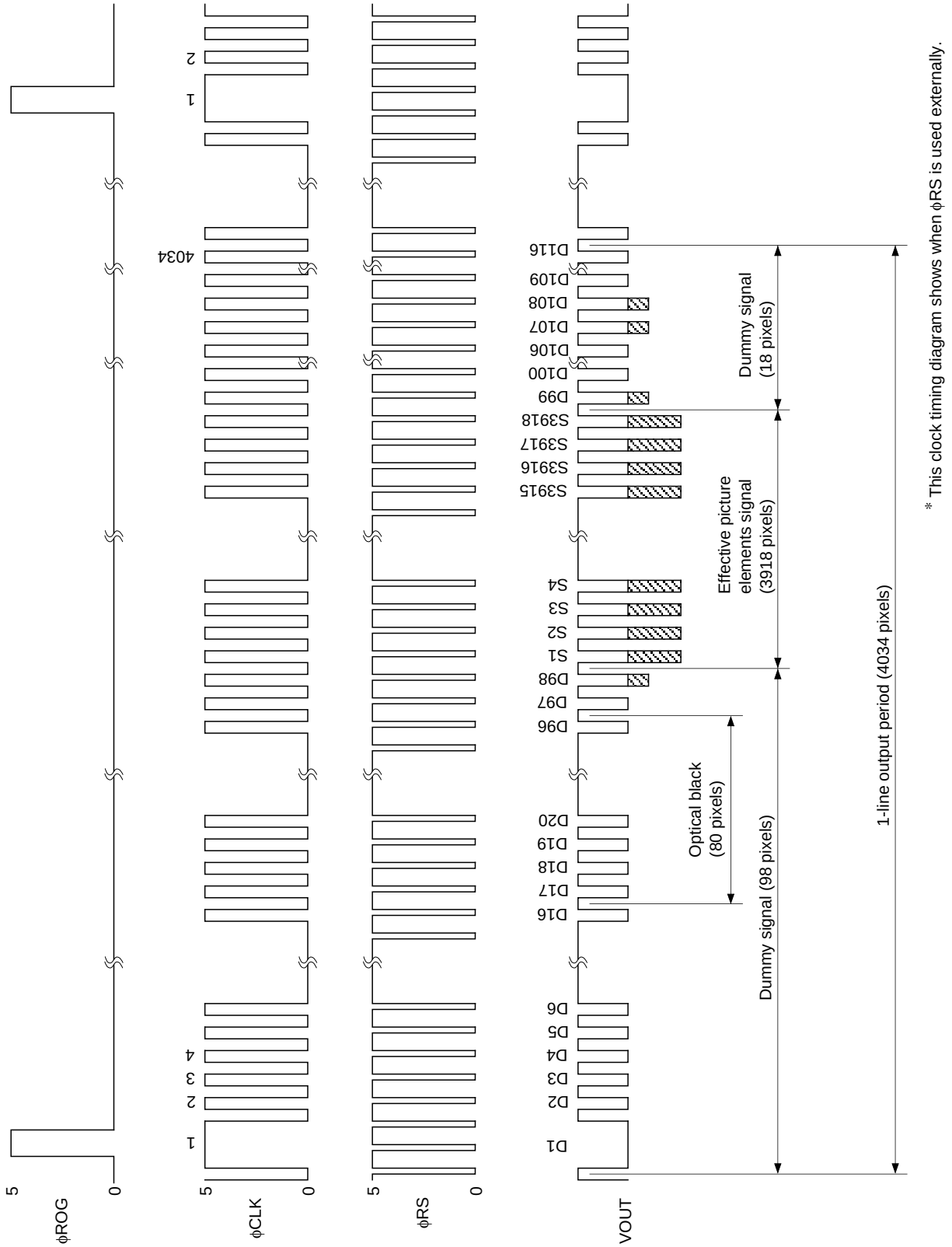


* This application circuit shows when φRS is used externally.

(When noise influence into output signal is large, connect pins indicated by (A) to the analog power supply and pins indicated by (D) to the digital power supply, and also use a decoupling capacitor of large capacitance.)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

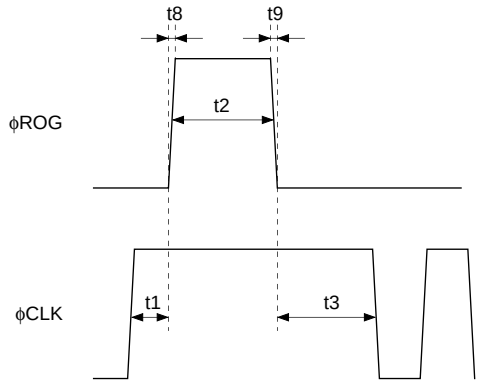
Clock Timing Diagram*



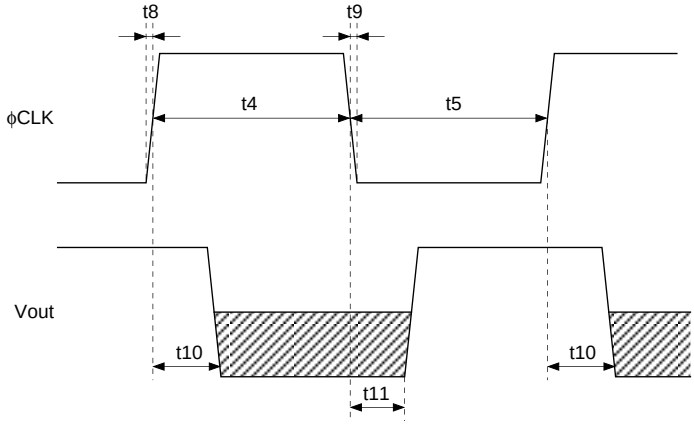
* This clock timing diagram shows when φRS is used externally.

Clock Pulse Waveform Conditions

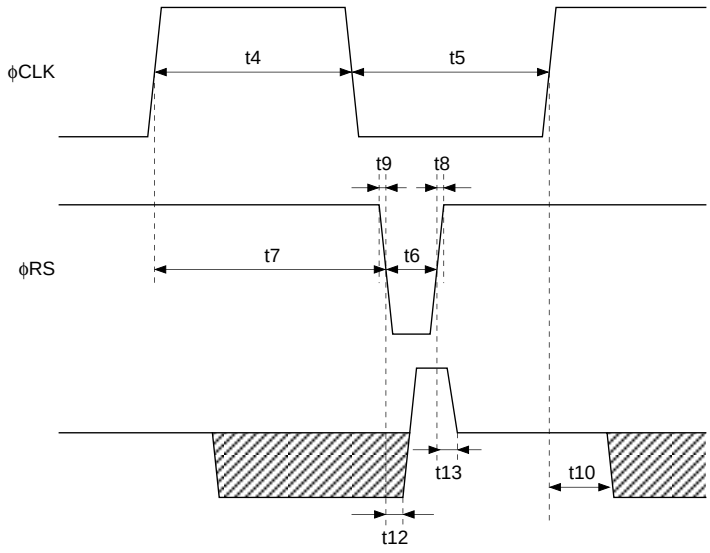
φCLK, φROG pulse related



Internal φRS mode



External φRS mode

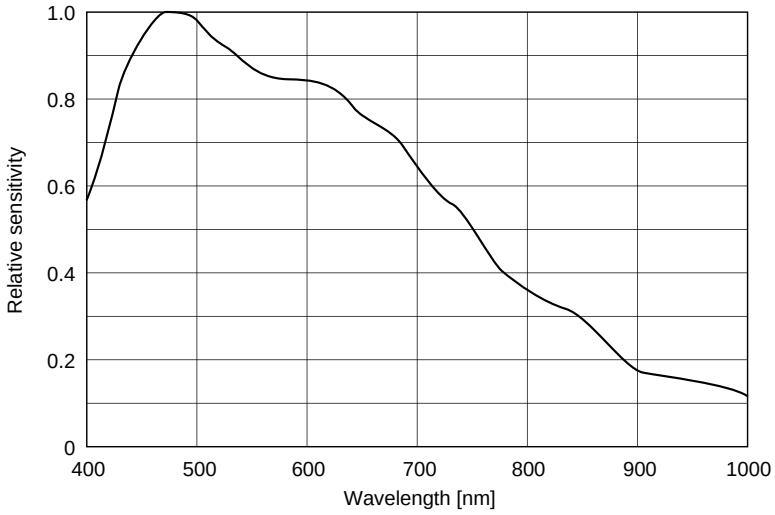


Item		Symbol	Min.	Typ.	Max.	Unit
φROG, φCLK pulse timing		t1	100	200	—	ns
φROG, φCLK pulse timing		t3	800	1000	—	ns
φROG pulse high level period		t2	800	1000	—	ns
φCLK pulse high level period		t4	100	500*1	—	ns
φCLK pulse low level period		t5	100	500*1	—	ns
φRS pulse low level period		t6	40	100*1	—	ns
φCLK, φRS pulse timing		t7	100	550*1	t1 + t2	ns
Input clock pulse rise/fall time		t8, t9	—	5	10	ns
Input clock pulse voltage	High level	$V_{\phi CLK}$, $V_{\phi ROG}$	4.5	5.0	5.5	V
	Low level	$V_{\phi RS}$	0	—	0.5	V
Signal output delay time	Internal φRS	t10	—	110	—	ns
		t11	—	65	—	ns
	External φRS	t12	—	40	—	ns
		t13	—	75	—	ns

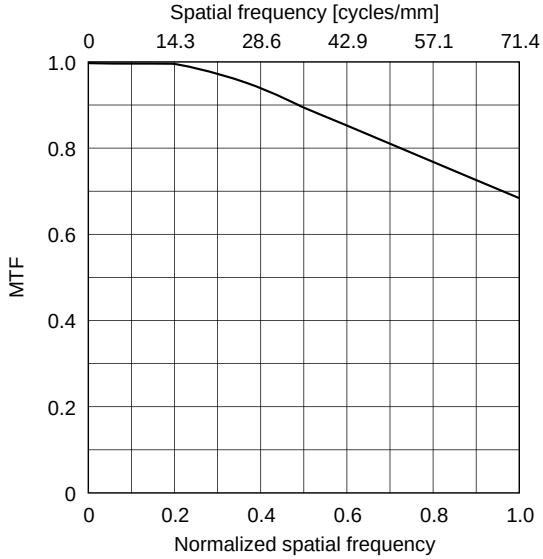
*1 Recommended condition during φCLK = 1MHz.

Example of Representative Characteristics (V_{DD1} = 9V, V_{DD2} = 5V, Ta = 25°C)

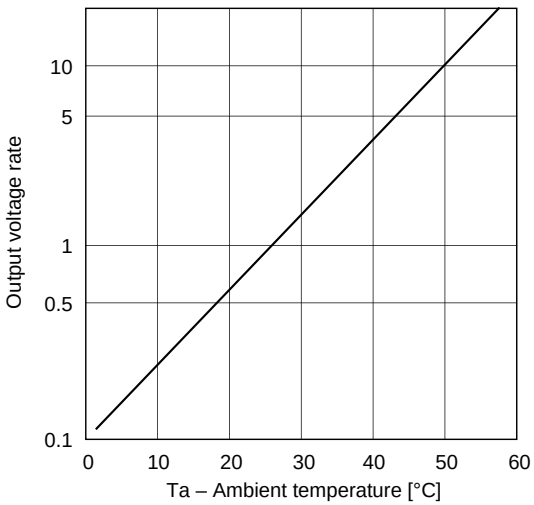
Spectral sensitivity characteristics (Standard characteristics)



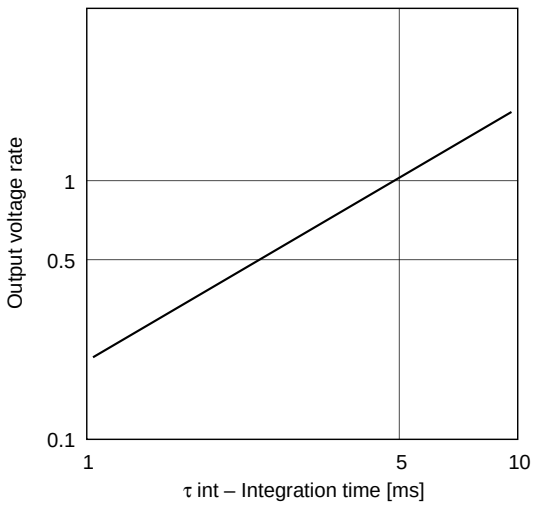
MTF of main scanning direction (Standard characteristics)



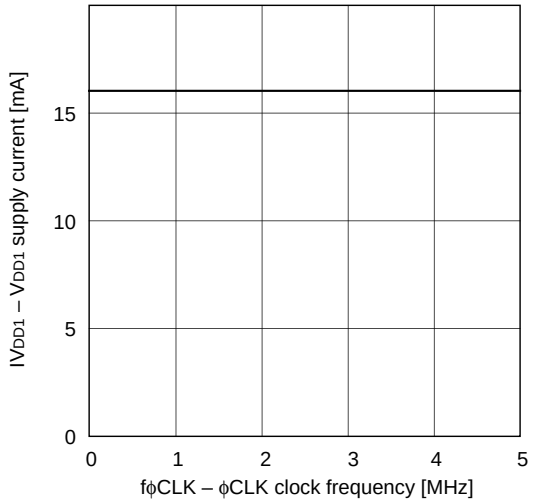
Dark signal output temperature characteristics (Standard characteristics)



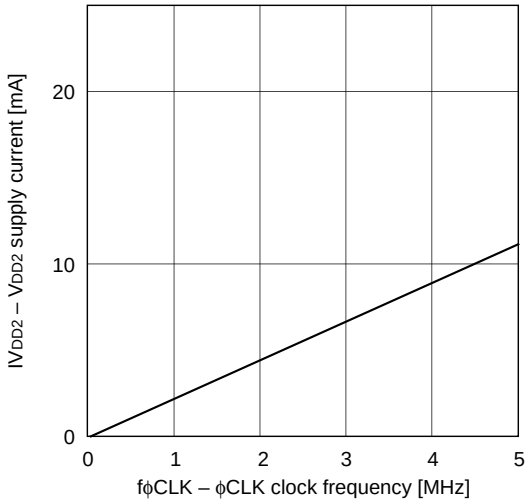
Integration time output voltage characteristics (Standard characteristics)



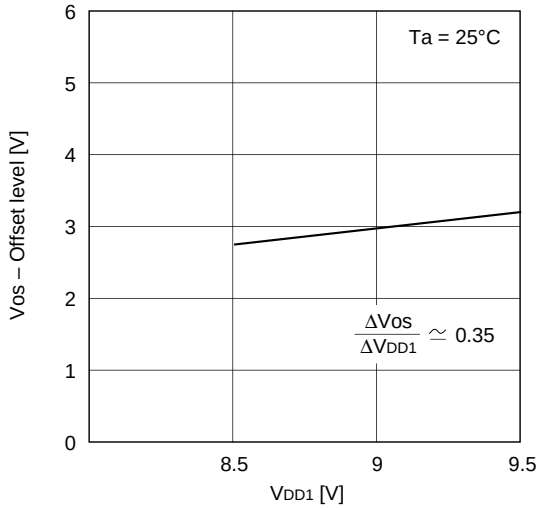
Operational frequency characteristics of the V_{DD1} supply current (Standard characteristics)



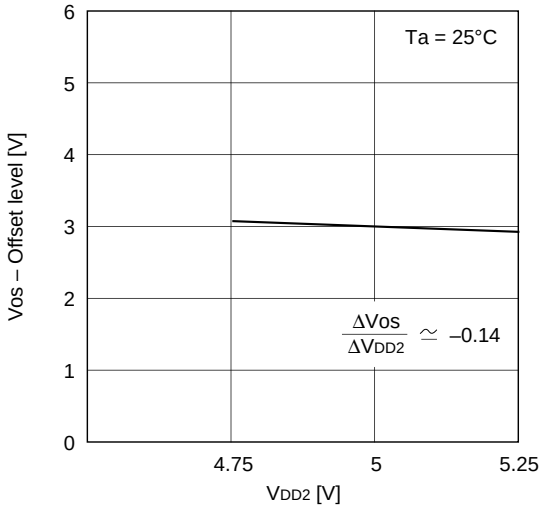
Operational frequency characteristics of the V_{DD2} supply current (Standard characteristics)



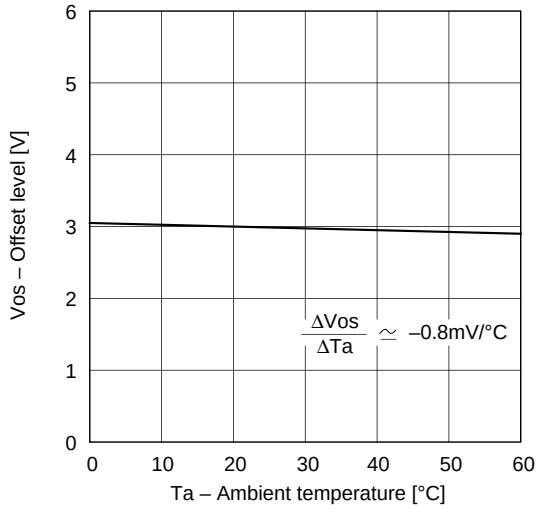
Offset level vs. V_{DD1} characteristics (Standard characteristics)



Offset level vs. V_{DD2} characteristics (Standard characteristics)



Offset level vs. Temperature characteristics (Standard characteristics)

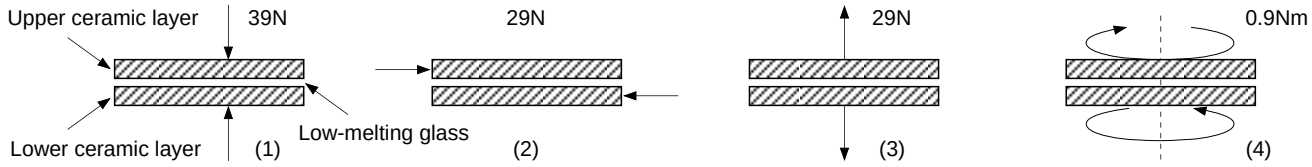


Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Regulation for raising and lowering the power supply voltage
   When raising the supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
   Similarly, lower V_{DD2} (5V) first and then V_{DD1} (9V).

3) Notes on handling CCD Cer-DIP Packages
   The following points should be observed when handling and installing cer-DIP packages.
   a) Remain within the following limits when applying a static load to the ceramic portion of the package:
      (1) Compressive strength: 39N/surface (Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

   c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
      (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.
   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

4) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment.
      When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

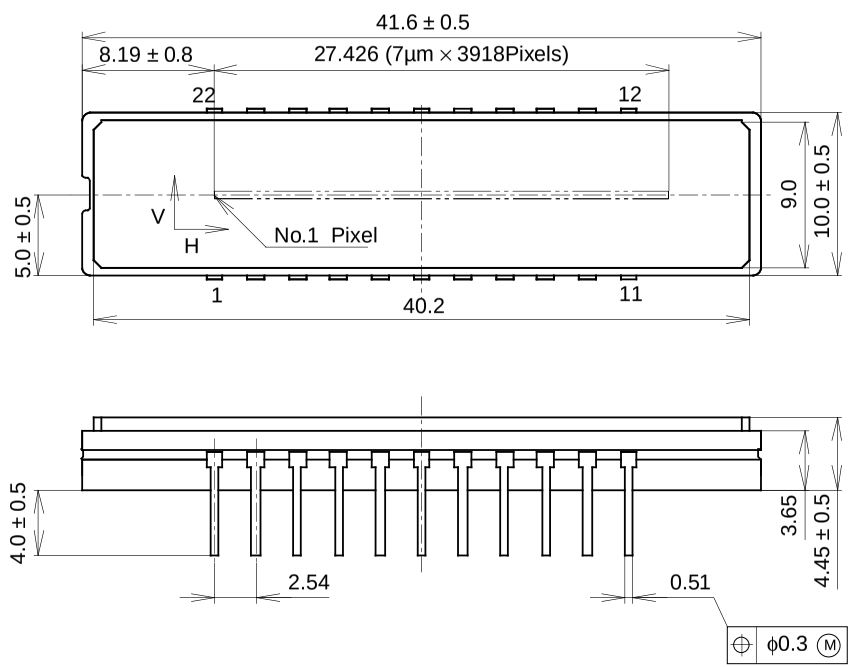
5) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained.
      Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

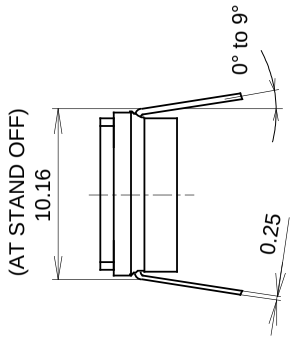
6) Exposure to high temperatures or humidity will affect the characteristics.
   Accordingly avoid storage or usage in such conditions.

7) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)





1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g