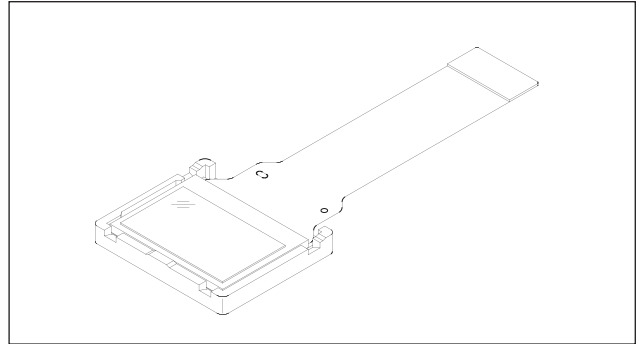


## 1.8cm (0.7-inch) NTSC/PAL/WID Color LCD Panel

### Description

The LCX018AK is a 1.8cm diagonal active matrix TFT-LCD panel addressed by the polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel provides full-color representation in NTSC/PAL/WID mode. RGB dots are arranged in a delta pattern featuring high picture quality of no fixed color patterns, which is inherent in vertical stripes and mosaic pattern arrangements.



### Features

- Number of active dots: 240,000 (0.7-inch; 1.8cm in diagonal)
- Horizontal resolution: 400 TV lines
- High optical transmittance: 4.4% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuit (built-in input level conversion circuit, TTL drive possible)
- High quality picture representation with RGB delta arranged color filters
- Full-color representation
- NTSC/PAL/WID compatible
- Up/down and/or right/left inverse display function
- Side-black function
- 16:9 and 4:3 aspect switching function

### Element Structure

- Dots

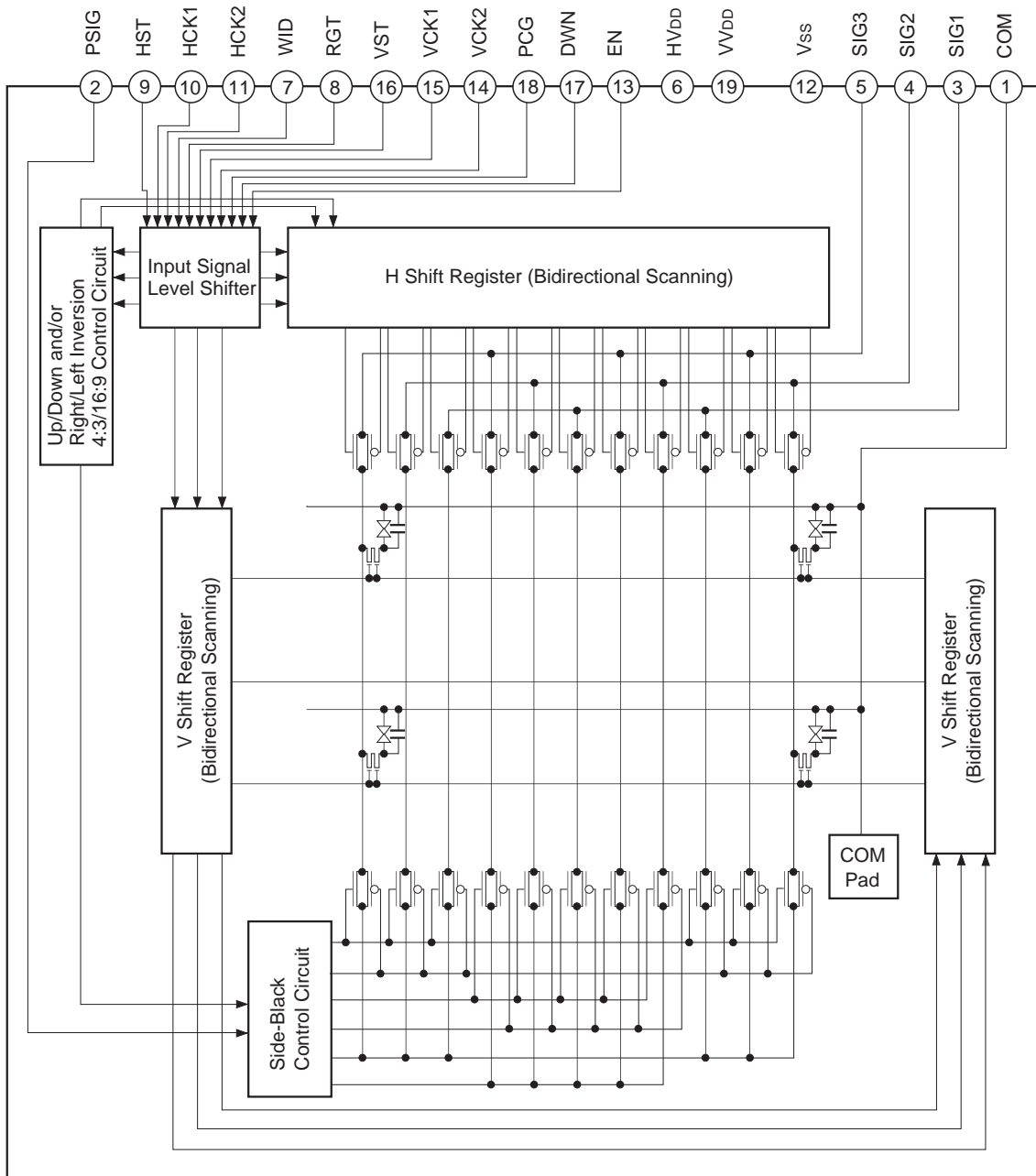
16:9 display: 1068.5 (H) × 225 (V) = 240,412

4:3 display: 803.5 (H) × 225 (V) = 180,787

- Built-in peripheral driving circuit using the polycrystalline silicon super thin film transistors.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



**Absolute Maximum Ratings** ( $V_{SS} = 0V$ )

• H driver supply voltage	HV <sub>DD</sub>	-1.0 to +17	V
• V driver supply voltage	VV <sub>DD</sub>	-1.0 to +17	V
• H driver input pin voltage	HST, HCK1, HCK2 RGT	-1.0 to +17	V
• V driver input pin voltage	VST, VCK1, VCK2 CLR, EN	-1.0 to +17	V
• Video signal input pin voltage	GREEN, RED, BLUE	-1.0 to +15	V
• Operating temperature	Topr	-10 to +70	°C
• Storage temperature	Tstg	-30 to +85	°C

**Operating Conditions** ( $V_{SS} = 0V$ )

- Supply voltage
 

HV <sub>DD</sub>	13.5 ± 0.5	V
VV <sub>DD</sub>	13.5 ± 0.5	V
- Input pulse voltage (V<sub>p-p</sub> of all input pins except video signal input pins)
 

V <sub>in</sub>	3.0V or more
-----------------	--------------

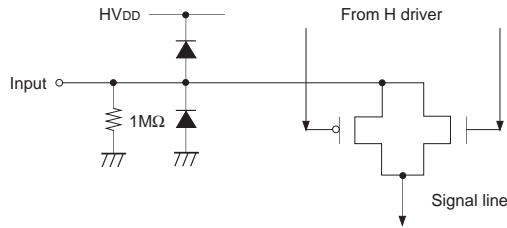
**Pin Description**

Pin No.	Symbol	Description
1	COM	Common voltage of panel
2	PSIG	Improvement signal for uniformity
3	SIG1	Video signal (Green) to panel
4	SIG2	Video signal (Red) to panel
5	SIG3	Video signal (Blue) to panel
6	HV <sub>DD</sub>	Power supply for H driver
7	WID	Aspect-ratio switching (H: 16:9, L: 4:3)
8	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)
9	HST	Start pulse for H shift register drive
10	HCK1	Clock pulse for H shift register drive
11	HCK2	Clock pulse for H shift register drive
12	V <sub>SS</sub>	GND (H, V drivers)
13	EN	Enable pulse for gate selection
14	VCK2	Clock pulse for V shift register drive
15	VCK1	Clock pulse for V shift register drive
16	VST	Start pulse for V shift register drive
17	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
18	PCG	Improvement pulse for uniformity
19	VV <sub>DD</sub>	Power supply for V driver
20	SOUT	H, V shift register drive confirmation

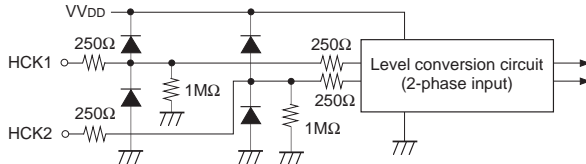
**Input Equivalent Circuit**

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. The equivalent circuit of each input pin is shown below. (The resistor value: typ.)

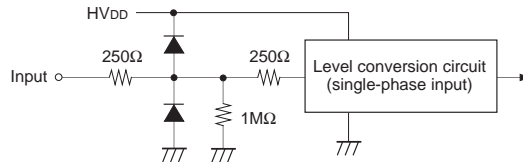
(1) SIG1, SIG2, SIG3, SID



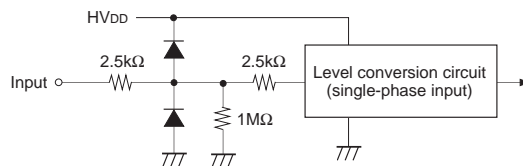
(2) HCK1, HCK2



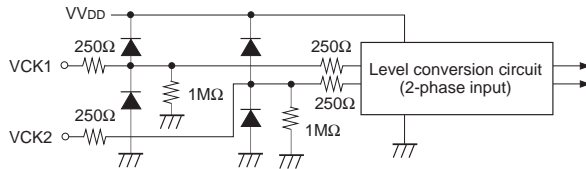
(3) HST



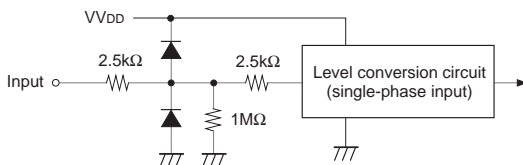
(4) RGT, WID



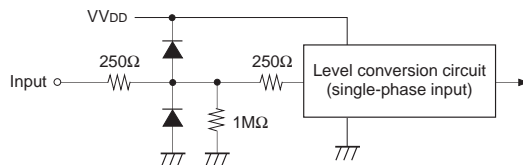
(5) VCK1, VCK2



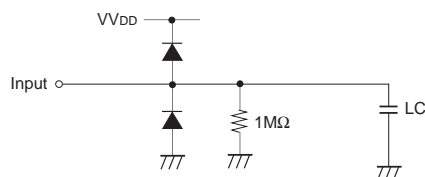
(6) VST, DWN, EN



(7) PCG



(8) COM



**Input Signals**

**1. Input signal voltage conditions (V<sub>SS</sub> = 0V)**

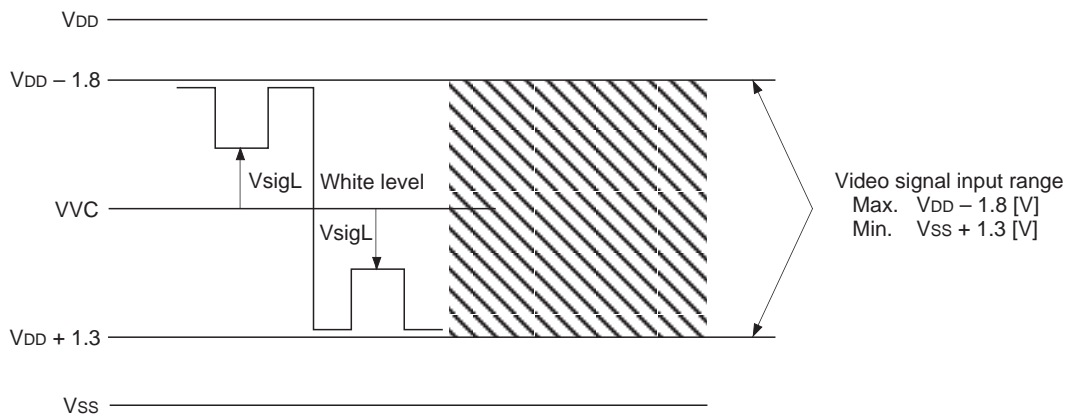
Item		Symbol	Min.	Typ.	Max.	Unit
H driver input voltage (HST, HCK1, HCK2, RGT, WID)	(Low)	VHIL	-0.30	0.0	0.30	V
	(High)	VHIH	2.7	3	5.5	V
V driver input voltage (VST, VCK1, VCK2, DWN, PCG, EN)	(Low)	VVIL	-0.30	0.0	0.3	V
	(High)	VVIH	2.7	3	5.5	V
Video signal center voltage		VVC	5.8	6.0	6.2	V
Common voltage of panel		V <sub>COM</sub>	VVC - 0.4	VVC - 0.25	VVC - 0.1	V

Item		Symbol	Min.	Typ.	Max.	Unit
Video signal input range*1	(V <sub>DD</sub> = 12.0V)	Vsig	VVC - 4.0		VVC + 4.0	V
Uniformity improvement signal PSIG input voltage		Vpsig	VVC - 4.0		VVC + 4.0	V
Video signal and uniformity improvement signal input white level		VsigL	0.5			V

\*1 Video input signal should be symmetrical to VVC.

**Supplement)** Video signal and uniformity improvement signal input range are set within the range shown below for V<sub>DD</sub> and V<sub>SS</sub>.

Also, video signal white level is defined for VVC as shown below.



## 2. Clock timing conditions (Ta = 25°C)

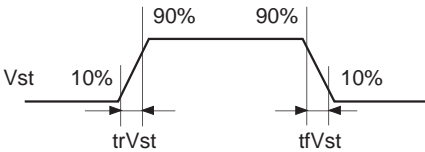
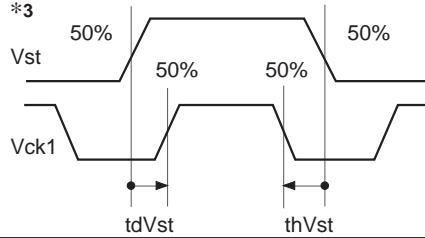
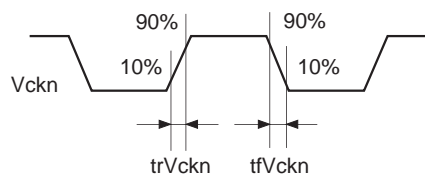
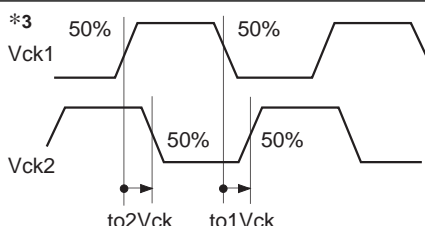
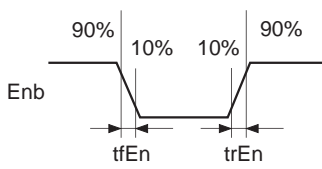
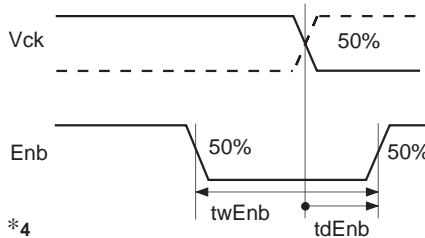
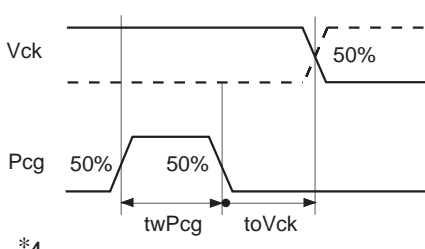
	Item	Symbol	Min.	Typ.	Max.	Unit	
HST	Hst rise time	trHst			30	ns	
	Hst fall time	tfHst			30		
	Hst data set-up time	tdHst	35	45	55		
	Hst data hold time	thHst	80	90	100		
HCK	Hckn*2 rise time	trHckn			30		
	Hckn*2 fall time	tfHckn			30		
	Hck1 fall to Hck2 rise time	to1Hck	-15	0	15		
	Hck1 rise to Hck2 fall time	to2Hck	-15	0	15		
VST	Vst rise time	trVst			100		μs
	Vst fall time	tfVst			100		
	Vst data set-up time	tdVst	-5.5	4.5	14.5		
	Vst data hold time	thVst	49	59	69		
VCK	Vckn*2 rise time	trVckn			100	ns	
	Vckn*2 fall time	tfVckn			100		
	Vck1 fall to Vck2 rise time	to1Vck	-20	0	20		
	Vck1 rise to Vck2 fall time	to2Vck	-20	0	20		
ENB	Enb rise time	trEnb	—	—	100		
	Enb fall time	tfEnb	—	—	100		
	Vck rise/fall to Enb rise time	tdEnb	2150	2200	2250		
	Enb pulse width	twEnb	5950	6000	6050		
PCG	Pcg rise time	trPcg	—	—	20		
	Pcg fall time	tfPcg	—	—	20		
	Pcg fall to Vck rise/fall time	toVck	-1050	-1000	-950		
	Pcg pulse width	twPcg	2450	2500	2550		

\*2 Hckn and Vckn mean Hck1, Hck2 and Vck1, Vck2. (fHckn = 3.72MHz, fVckn = 7.81kHz)

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		<ul style="list-style-type: none"> <li>• Hckn*2</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul>
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		<ul style="list-style-type: none"> <li>• Hckn*2</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul>
	Hst data hold time	thHst		
HCK	Hckn*2 rise time	trHckn		<ul style="list-style-type: none"> <li>• Hckn*2</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> <li>tdHst = 60ns</li> <li>thHst = -120ns</li> </ul>
	Hckn*2 fall time	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		<ul style="list-style-type: none"> <li>• tdHst = 60ns</li> <li>thHst = -120ns</li> </ul>
	Hck1 rise to Hck2 fall time	to2Hck		

<Vertical Shift Register Driving Waveform>

Item	Symbol	Waveform	Conditions	
VST	Vst rise time	trVst		<ul style="list-style-type: none"> <li>Vckn*2</li> <li>duty cycle 50%</li> <li>to1Vck = 0ns</li> <li>to2Vck = 0ns</li> </ul>
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		<ul style="list-style-type: none"> <li>Vckn*2</li> <li>duty cycle 50%</li> <li>to1Vck = 0ns</li> <li>to2Vck = 0ns</li> </ul>
	Vst data hold time	thVst		
VCK	Vckn*2 rise time	trVckn		<ul style="list-style-type: none"> <li>Vckn*2</li> <li>duty cycle 50%</li> <li>to1Vck = 0ns</li> <li>to2Vck = 0ns</li> <li>tdVst = 32μs</li> <li>thVst = -32μs</li> </ul>
	Vckn*2 fall time	tfVckn		
	Vck1 fall to Vck2 rise time	to1Vck		
	Vck1 rise to Vck2 fall time	to2Vck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Vck rise/fall to Enb rise time	tdEnb		
	Enb pulse width	twEnb		
PCG	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg fall to Vck rise/fall time	toVck		
	Pcg pulse width	twPcg		

\*3 Definitions: The right-pointing arrow (  $\bullet \rightarrow$  ) means +.

The left-pointing arrow (  $\leftarrow \bullet$  ) means -.

The black dot at an arrow (  $\bullet$  ) indicates the start of measurement.



**Electrical Characteristics** ( $T_a = 25^\circ\text{C}$ ,  $HV_{DD} = 13.5\text{V}$ ,  $V_{DD} = 13.5\text{V}$ )**1. Horizontal drivers**

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	Hckn		8	13	pF	
	Hst		8	13	pF	
Input pin current	Hck1	-450	-190		$\mu\text{A}$	Hck1 = GND
	Hck2	-900	-200		$\mu\text{A}$	Hck2 = GND
	Hst, Wid, Rgt	-130	-25		$\mu\text{A}$	Hst, Wid, Rgt = GND
Video signal input pin capacitance	Csig		150	200	pF	
Current consumption	IH		3.5	6	mA	Hckn: Hck1, Hck2 (3.72MHz)

**2. Vertical drivers**

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	Vckn		8	13	pF	
	Vst		8	13	pF	
Input pin current	Vck1	-450	-190		$\mu\text{A}$	Vck1 = GND
	Vck2	-900	-200		$\mu\text{A}$	Vck2 = GND
	Vst, En, Dwn, Pcg	-130	-25		$\mu\text{A}$	Vst, En, Dwn, Pcg = GND
Current consumption	IV		1.0	2.0	mA	Vckn: Vck1, Vck2 (7.87kHz)

**3. Total power consumption of the panel**

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	PWR		60	120	mW

**4. COM input resistance**

Item	Symbol	Min.	Typ.	Max.	Unit
COM – Vss input resistance	Rcom	0.5	1		$\text{M}\Omega$

**5. Improvement signal for uniformity**

Item	Symbol	Min.	Typ.	Max.	Unit
Improvement signal for uniformity	CPSIGon	—	7	10	nF

Electro-optical Characteristics

(Ta = 25°C, NTSC mode)

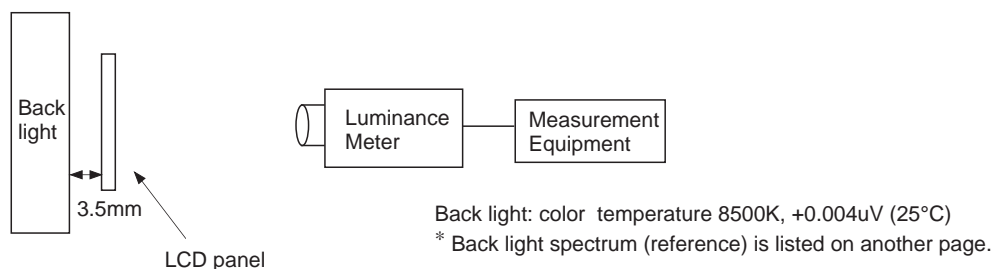
Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR <sub>25</sub>	1	80	200	—	—
		60°C	CR <sub>60</sub>		80	200	—	
Optical transmittance			T	2	3.8	4.4	—	%
Chromaticity	R	X	R <sub>x</sub>	3	0.580	0.620	0.660	CIE standards
		Y	R <sub>y</sub>		0.300	0.340	0.380	
	G	X	G <sub>x</sub>		0.250	0.290	0.330	
		Y	G <sub>y</sub>		0.550	0.590	0.630	
	B	X	B <sub>x</sub>		0.105	0.140	0.175	
		Y	B <sub>y</sub>		0.070	0.110	0.150	
V-T characteristics	V <sub>90</sub>	25°C	V <sub>90-25</sub>	4	1.1	1.5	2.2	V
		60°C	V <sub>90-60</sub>		1.0	1.3	2.1	
	V <sub>50</sub>	25°C	V <sub>50-25</sub>		1.5	2.0	2.5	
		60°C	V <sub>50-60</sub>		1.4	1.8	2.4	
	V <sub>10</sub>	25°C	V <sub>10-25</sub>		2.2	2.7	3.2	
		60°C	V <sub>10-60</sub>		2.1	2.5	3.1	
Half tone color reproduction range		R vs. G	V <sub>50RG</sub>	5	—	-0.10	-0.25	V
		B vs. G	V <sub>50BG</sub>		—	0.10	0.45	
Response time	ON time	0°C	ton0	6	—	25	100	ms
		25°C	ton25		—	8	40	
	OFF time	0°C	toff0		—	65	150	
		25°C	toff25		—	20	60	
Flicker		60°C	F	7	—	—	-40	dB
Image retention time		60min.	YT60	8	—	—	20	s
Optimum Vcom voltage			Vcomopt	9	5.60	5.75	5.90	V

<Electro-optical Characteristics Measurement>

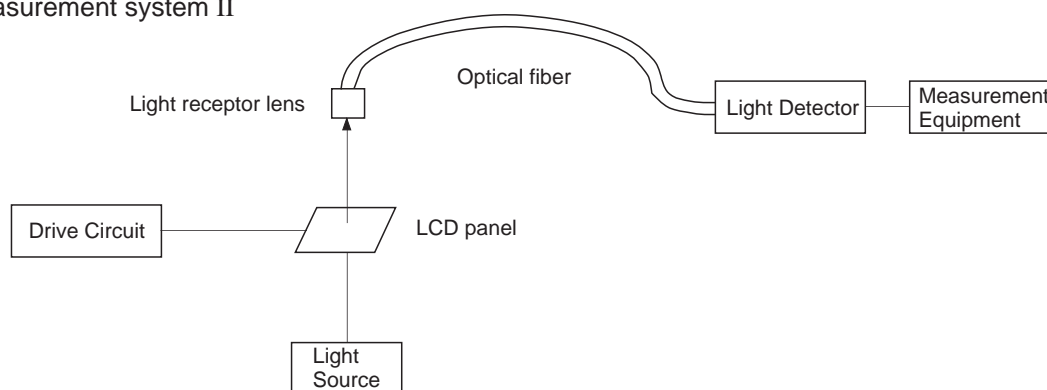
Basic measurement conditions

- (1) Driving voltage  
 $HV_{DD} = 13.5V$ ,  $VV_{DD} = 13.5V$   
 $VVC = 6.0V$ ,  $V_{com} = 5.75V$
- (2) Measurement temperature  
 25°C unless otherwise specified.
- (3) Measurement point  
 One point in the center of screen unless otherwise specified.
- (4) Measurement systems  
 Two types of measurement system are used as shown below.
- (5) RGB input signal voltage ( $V_{sig}$ )  
 $V_{sig} = 6 \pm V_{AC} [V]$  ( $V_{AC}$ : signal amplitude)

\* Measurement system I



\* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L \text{ (White)}}{L \text{ (Black)}} \dots (1)$$

L (White): Surface luminance of the TFT-LCD panel at the RGB signal amplitude  $V_{AC} = 0.5V$ .

L (Black): Surface luminance of the panel at  $V_{AC} = 4.5V$

Both luminosities are measured by System I.

**2. Optical Transmittance**

Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L \text{ (White)}}{\text{Luminance of Back Light}} \times 100 \text{ [\%]} \dots (2)$$

L (White) is the same expression as defined in the "Contrast Ratio" section.

**3. Chromaticity**

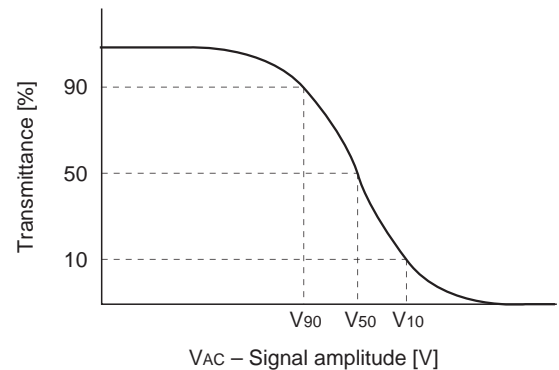
Chromaticity of the panels are measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses Chromaticity of x and y on the CIE standards here.

		Signal amplitudes (V <sub>AC</sub> ) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.5	4.5
	G	4.5	0.5	4.5
	B	4.5	4.5	0.5

(Unit: V)

**4. V-T Characteristics**

V-T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V<sub>90</sub>, V<sub>50</sub> and V<sub>10</sub> correspond to the each voltage which defines 90%, 50% and 10% of transmittance respectively.

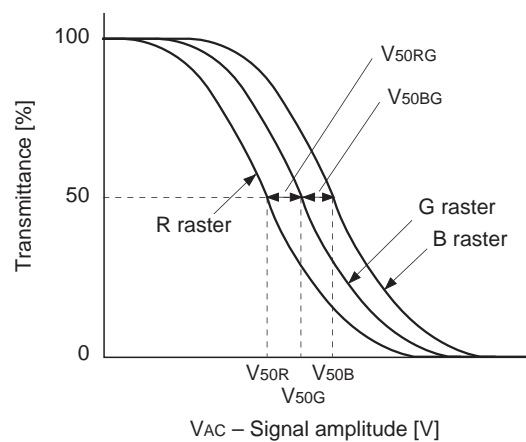


**5. Half Tone Color Reproduction Range**

Half tone color reproduction range of the LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G, B raster modes which correspond to 50% of transmittance, V<sub>50R</sub>, V<sub>50G</sub> and V<sub>50B</sub> respectively. V<sub>50RG</sub> and V<sub>50BG</sub>, the voltage differences between V<sub>50R</sub> and V<sub>50G</sub>, V<sub>50B</sub> and V<sub>50G</sub>, are simply given by the following formula (3) and (4) respectively.

$$V_{50RG} = V_{50R} - V_{50G} \dots (3)$$

$$V_{50BG} = V_{50B} - V_{50G} \dots (4)$$



**6. Response Time**

Response time  $t_{on}$  and  $t_{off}$  are defined by the formula (5) and (6) respectively.

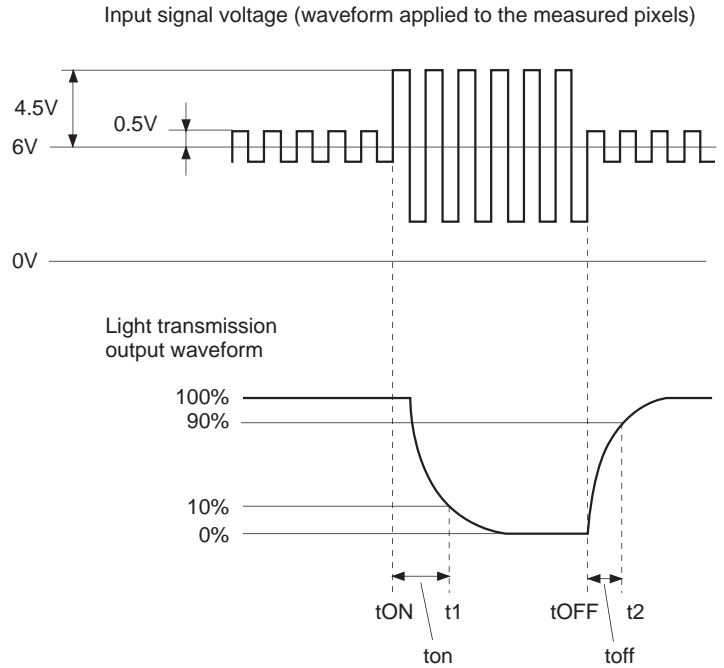
$$t_{on} = t_1 - t_{ON} \dots (5)$$

$$t_{off} = t_2 - t_{OFF} \dots (6)$$

$t_1$ : time which gives 10% transmittance of the panel.

$t_2$ : time which gives 90% transmittance of the panel.

The relationships between  $t_1$ ,  $t_2$ ,  $t_{ON}$  and  $t_{OFF}$  are shown in the right figure.



**7. Flicker**

Flicker (F) is given by the formula (7). DC and AC (NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster\* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

$$F [dB] = 20 \log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots (7)$$

\* R, G, B input signal condition for gray raster mode is given by  $V_{sig} = 6 \pm V_{50}$  [V]

where:  $V_{50}$  is the signal amplitude which gives 50% of transmittance in V-T curve.

**8. Image Retention Time**

Image retention time is given by the following procedures:

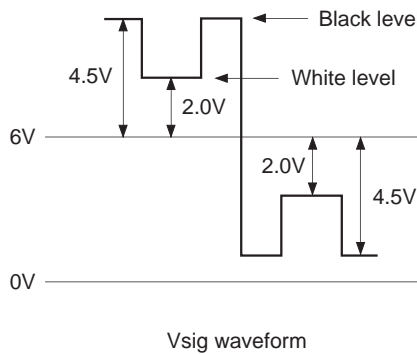
Apply monoscope signal to the LCD panel for 60 minutes and then change monoscope signal\* to gray scale signal ( $V_{sig} = 6 \pm V_{AC}$  (V);  $V_{AC} = 3$  to  $4$ V) so as to give the maximum image retention. Hold input signal  $V_{AC}$ . The time of the residual image to disappear gives the image retention time.

\* Monoscope signal conditions:

$$V_{sig} = 6 \pm 4.5 \text{ or } 6 \pm 2.0 \text{ [V]}$$

(shown in the right figure)

$$V_{com} = 5.6\text{V}$$



## 9. Method of Measuring the Optimum Vcom

There are two methods of measuring the optimum Vcom using the photoelectric element.

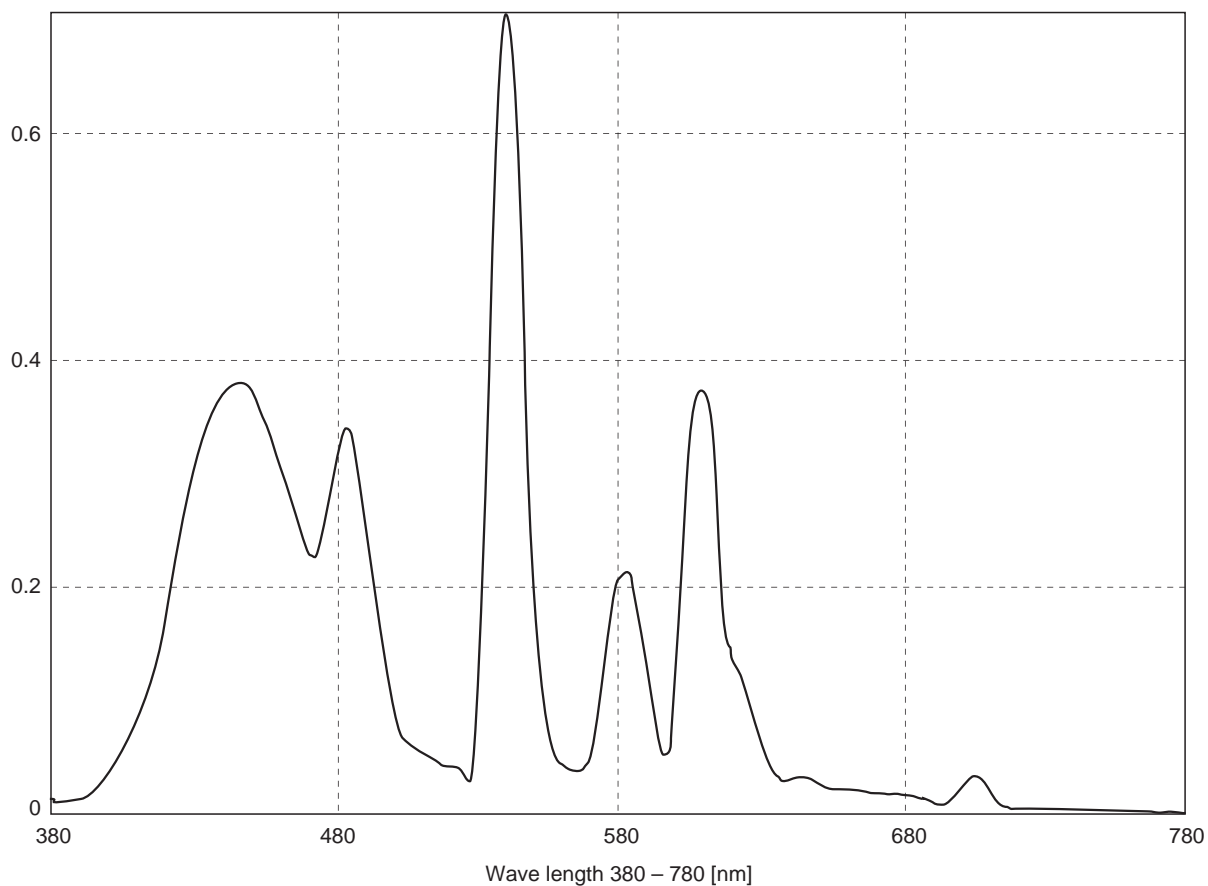
### 9-1. Method of Measuring Flicker

In the field invert drive mode, adjust the flicker level of the half tone ( $V_{sig} = 1.5$  to  $2.5V$ ) using the photoelectric element and oscilloscope so that its 30Hz component becomes minimum. The Vcom value at this time is taken to be the optimum Vcom.

### 9-2. Method of Measuring Contrast

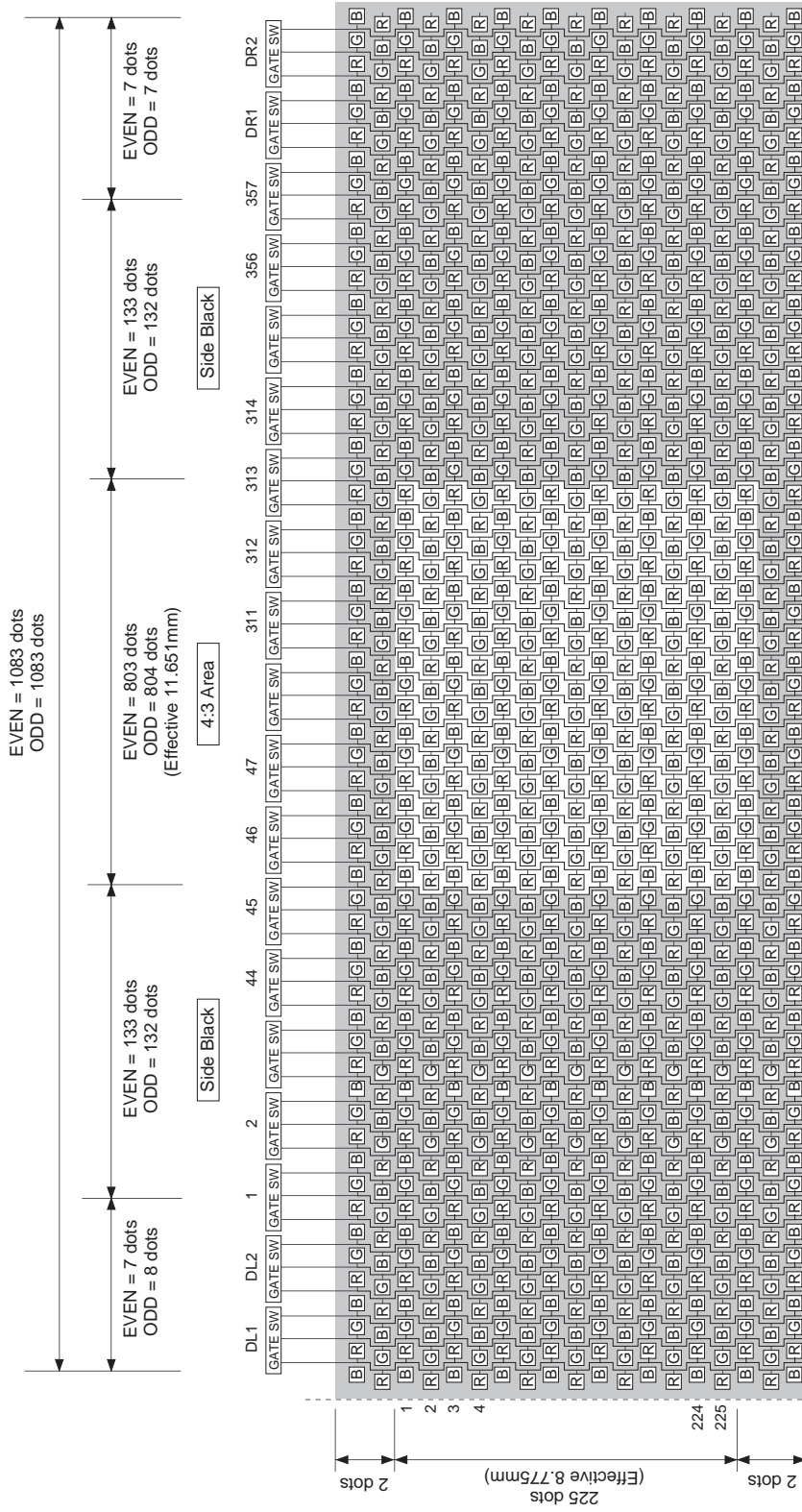
In the normal 1H invert drive mode, adjust the optical output voltage of the half tone ( $V_{sig} = 1.5$  to  $2.5V$ ) so that it becomes minimum. The Vcom value at this time is taken to be the optimum Vcom.

## Example of Back Light Spectrum (Reference)





LCX018AK Dot Arrangement (4:3)





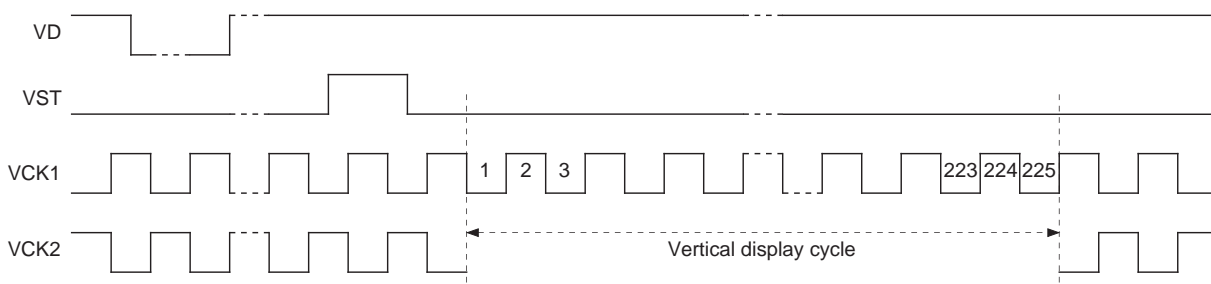
2. LCD Panel Operations

[Description of basic operations]

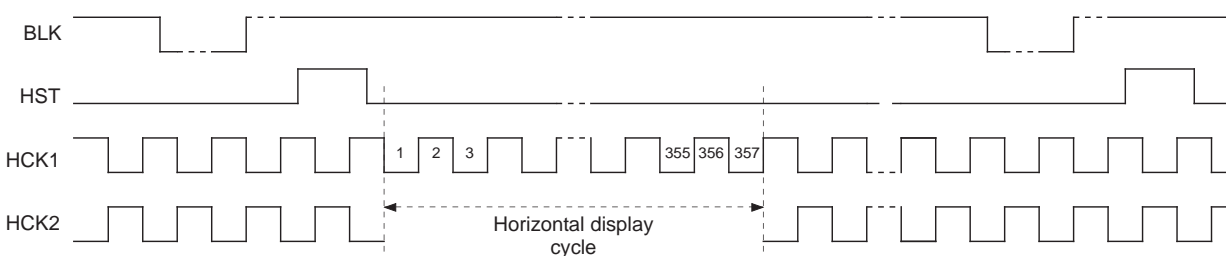
The basic operations of the LCD panel are shown below based on the wide-display mode.

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 225 gate lines sequentially in every single horizontal scanning period.
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuit, applies selected pulses to every 1068.5 signal electrodes sequentially in a single horizontal scanning period.
- Vertical and horizontal shift registers address one pixel, and then dot Thin Film Transistors (TFTs; two TFTs for one dot) turn on to apply a video signal to the dot. The same procedures lead to the entire 480 × 1068.5 dots to display a picture in a single vertical scanning period.
- The LCD pixel dots are arranged in a delta pattern, where the dots connected to the identical signal line are positioned with 1.5-dot offset against those of the adjacent horizontal line. Horizontal Start Pulse (HST) is generated with 1.5-bit offset between the horizontal lines to regulate the above offset. HCK and sample-and-hold (S/H) pulses follow the same 1.5-bit offset scheme.
- The video signal must be input with polarity-inverted system in every horizontal cycle.
- Timing diagrams of the vertical and the horizontal display cycle are shown below.

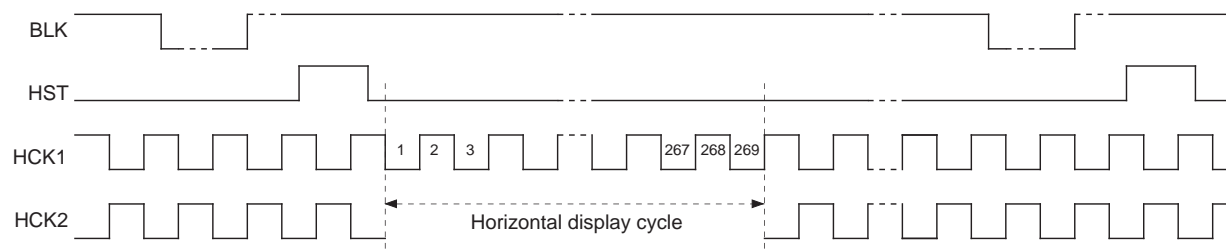
(1) Vertical display cycle (down-direction scanning)



(2) Horizontal display cycle (16:9)



(3) Horizontal display cycle (4:3)



**[Description of operating mode]**

The LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode
- 4:3 display mode with side-black display

These modes are controlled by three signals (RGT, DWN, and WID). The setting mode is shown below:

WID	RGT	Mode
H	H	16:9 right scan
H	L	16:9 left scan
L	H	4:3 right scan
L	L	4:3 left scan

DWN	Mode
H	Down scan
L	Up scan

The direction of the right/left and/or up/down mean when Pin 1 marking is located at right side with the pin block upside.

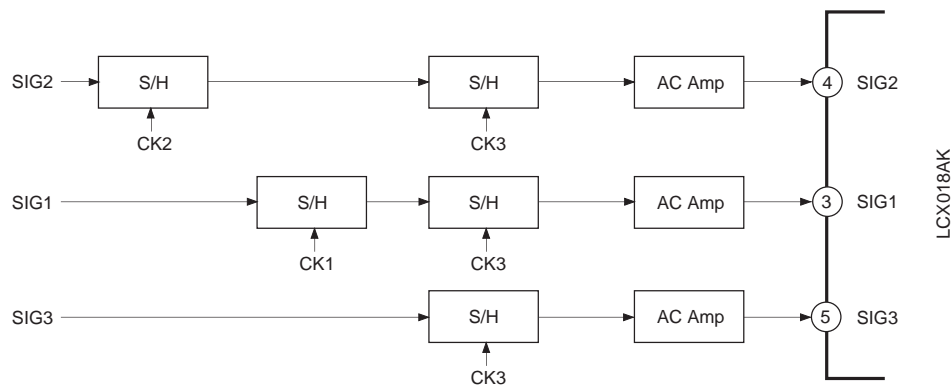
- The analog signal (PSIG) to display side-black shall be input by 1H inversion synchronized with the signal.

**3. 3-dot Simultaneous Sampling (RGB Simultaneous Sampling)**

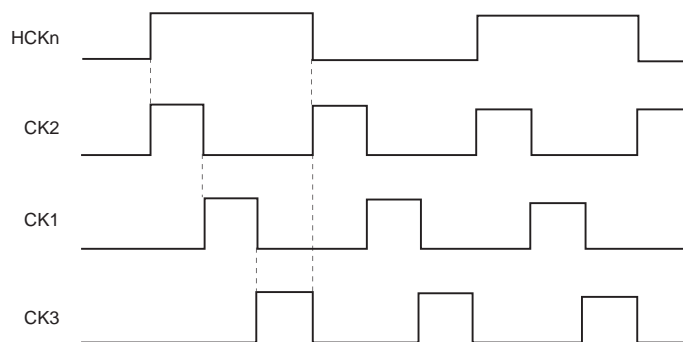
Horizontal driver samples SIG1, SIG2 and SIG3 signal simultaneously, which requires the phase matching between SIG1, SIG2, and SIG3 signals to prevent horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying video signal to the LCD panel.

The block diagram of the delaying procedure using sample-and-hold method is as follows.

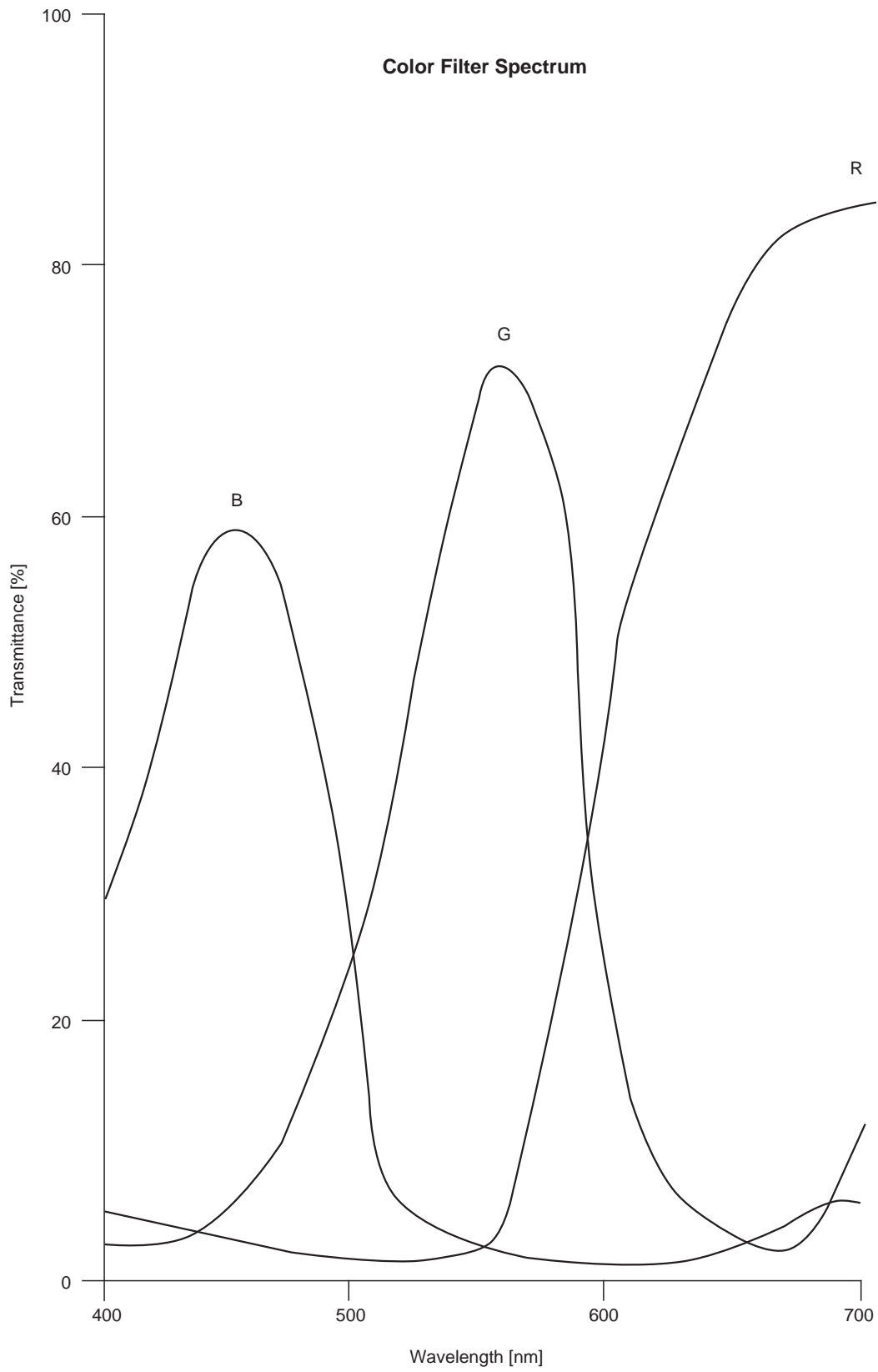
The LCX018 has the right/left inverse function. The following phase relationship diagram indicates the phase setting for the right scan (RGT = High level). For the left scan (RGT = Low level), the phase setting shall be inverted between SIG2 and SIG3 signals.



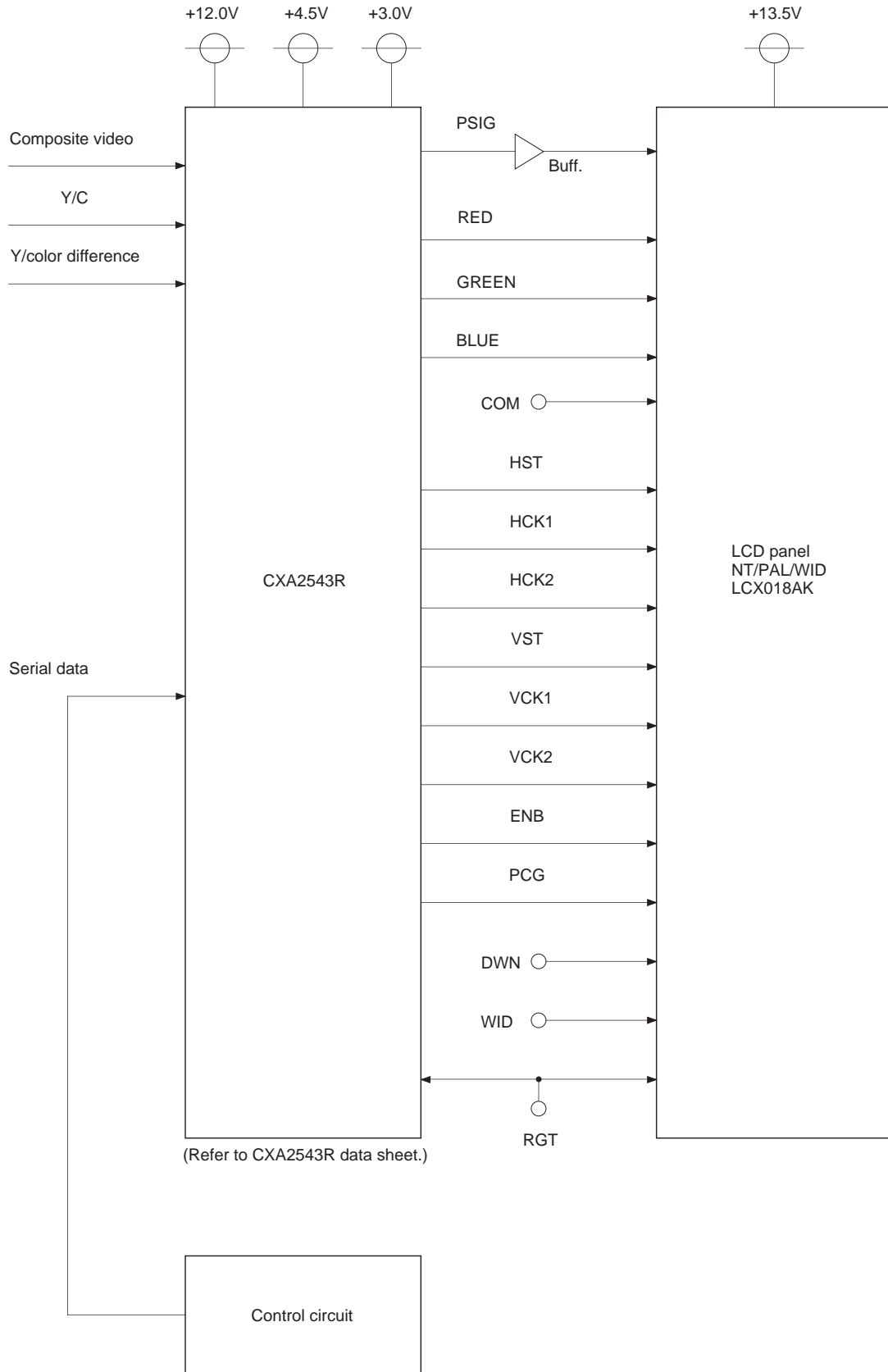
**<Phase relationship of delaying sample-and-hold pulses> (right scan)**



Example of Color Filter Spectrum (Reference)



Color Display System Block Diagram



**Notes on Handling**

- (1) Static charge prevention  
Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.
  - a) Use non-chargeable gloves, or simply use bare hands.
  - b) Use an earth-band when handling.
  - c) Do not touch any electrodes of a panel.
  - d) Wear non-chargeable clothes and conductive shoes.
  - e) Install conductive mat on the working floor and working table.
  - f) Keep panels away from any charged materials.
  - g) Use ionized air to discharge the panels.
  
- (2) Protection from dust and dirt
  - a) Operate in clean environment.
  - b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully not to damage the panel.
  - c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
  - d) Use ionized air to blow off dust at a panel.
  
- (3) Other handling precautions
  - a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
  - b) Do not drop a panel.
  - c) Do not twist or bend a panel or a panel frame.
  - d) Keep a panel away from heat source.
  - e) Do not dampen a panel with water or other solvents.
  - f) Avoid to store or to use a panel in high temperature or in high humidity, which results in panel damages.

