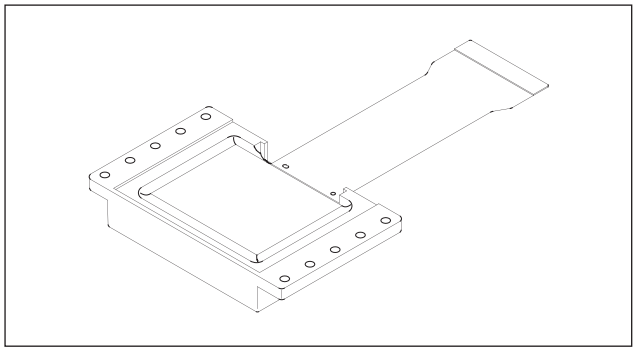
SONY

LCX021AM

4.1cm (1.6-inch) LCD Panel (with microlens)

For the availability of this product, please contact the sales office.

Description



The LCX021AM is a 4.1cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel allows full-color representation without color filters through the use of a microlens. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes high picture quality by incorporating a high luminance screen, cross-talk free and ghost free circuits.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports SVGA 4:3/PC98*1 8:5 data signals by changing the active area according to the type of input signal.

*1 "PC98" is a trademark of NEC Corporation.

Features

- The number of active dots: 1,456,000 (1.6-inch; 4.1cm in diagonal)
- Supports SVGA (804 × 3 × 604) and PC98*1 (804 × 3 × 500)
- Effective aperture ratio: 70% (reference value)
- Built-in cross talk free and ghost free circuits
- High contrast ratio with normally white mode: 150 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function

Element Structure

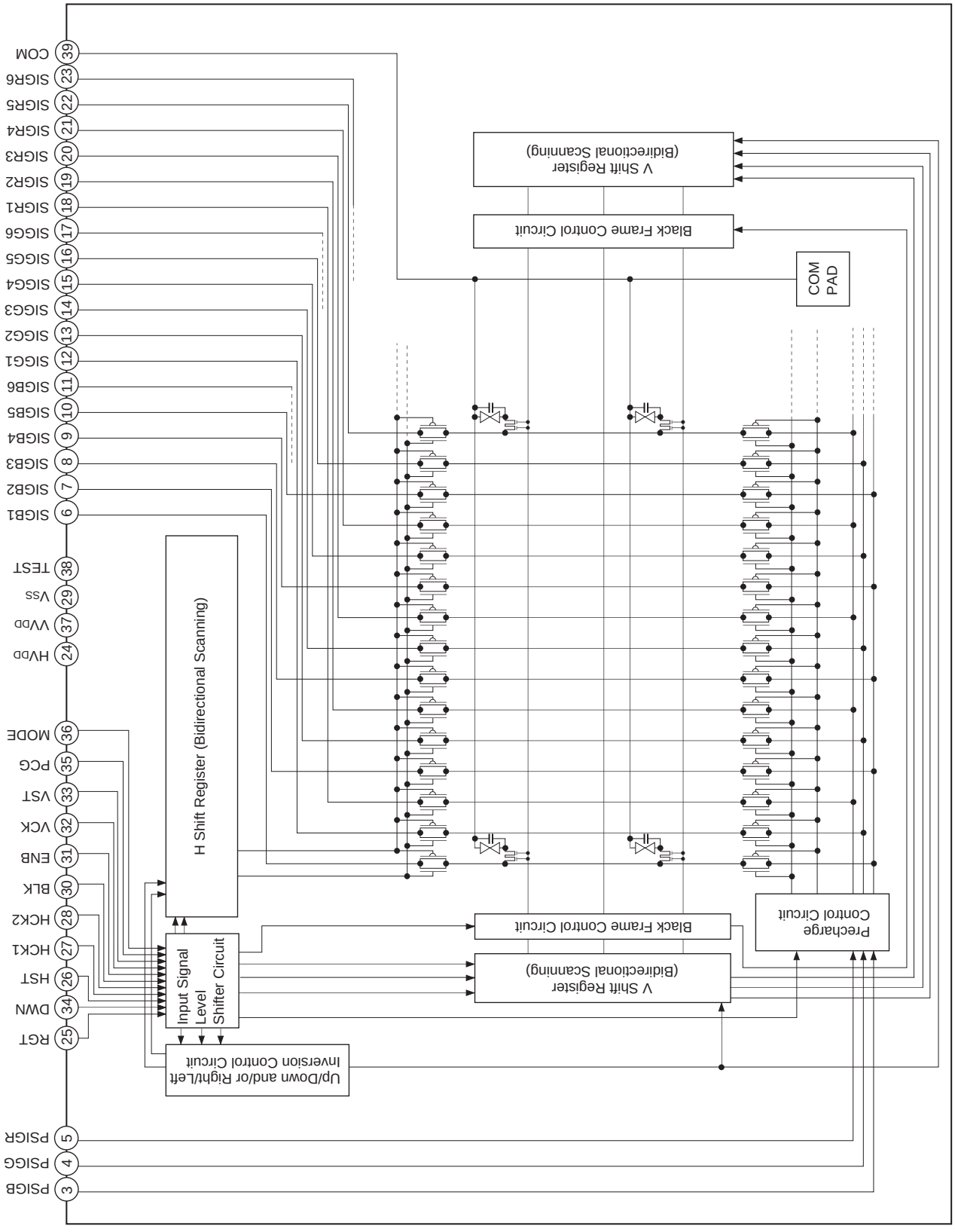
- Dots: 804 × 3 (H) × 604 (V) = 1,456,848
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

Applications

- Liquid crystal data projectors
- Liquid crystal projectors
- Liquid crystal rear projection TV, etc.

E98501A94-PS

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, BLK, ENB, DWN, MODE	–1.0 to +17	V
• Video signal input pin voltage	SIGB1, SIGB2, SIGB3, SIGB4, SIGB5, SIGB6, SIGG1, SIGG2, SIGG3, SIGG4, SIGG5, SIGG6, SIGR1, SIGR2, SIGR3, SIGR4, SIGR5, SIGR6, PSIGB, PSIGG, PSIGR	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD}	15.5 ± 0.5V
VV_{DD}	15.5 ± 0.5V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin	5.0 ± 0.5V

Pin Description

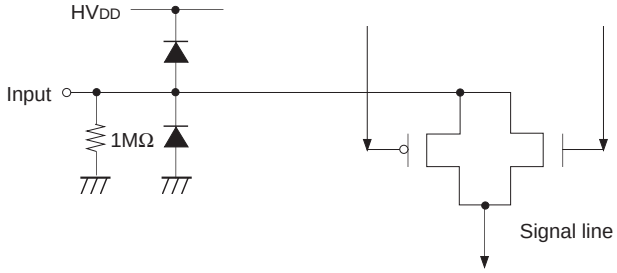
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	Leave this pin open.	21	SIGR4	Video signal R4 to panel
2	NC	Leave this pin open.	22	SIGR5	Video signal R5 to panel
3	PSIGB	Blue uniformity improvement signal	23	SIGR6	Video signal R6 to panel
4	PSIGG	Green uniformity improvement signal	24	HV_{DD}	Power supply for H driver
5	PSIGR	Red uniformity improvement signal	25	RGT	Drive direction pulse for V shift register (H: normal, L: reverse)
6	SIGB1	Video signal B1 to panel	26	HST	Start pulse for H shift register drive
7	SIGB2	Video signal B2 to panel	27	HCK1	Clock pulse 1 for H shift register drive
8	SIGB3	Video signal B3 to panel	28	HCK2	Clock pulse 2 for H shift register drive
9	SIGB4	Video signal B4 to panel	29	V_{SS}	GND (H, V drivers)
10	SIGB5	Video signal B5 to panel	30	BLK	Black frame display pulse
11	SIGB6	Video signal B6 to panel	31	ENB	Enable pulse for gate selection
12	SIGG1	Video signal G1 to panel	32	VCK	Clock pulse for V shift register drive
13	SIGG2	Video signal G2 to panel	33	VST	Start pulse for V shift register drive
14	SIGG3	Video signal G3 to panel	34	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
15	SIGG4	Video signal G4 to panel	35	PCG	Improvement pulse for uniformity
16	SIGG5	Video signal G5 to panel	36	MODE	Display area switching (H: SVGA, L: PC98)
17	SIGG6	Video signal G6 to panel	37	VV_{DD}	Power supply for V driver
18	SIGR1	Video signal R1 to panel	38	TEST	Test; Open
19	SIGR2	Video signal R2 to panel	39	COM	Common voltage of panel
20	SIGR3	Video signal R3 to panel	40	NC	Leave this pin open.

Note) RGB video signals of Pins 6 to 23 is an example. The order of RGB can be changed.

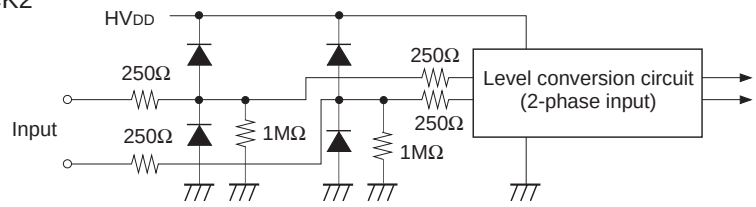
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except video signal inputs. All pins are connected to V_{SS} with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

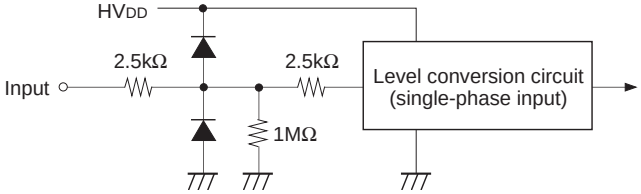
(1) SIGB1, SIGB2, SIGB3, SIGB4, SIGB5, SIGB6, SIGG1, SIGG2, SIGG3, SIGG4, SIGG5, SIGG6, SIGR1, SIGR2, SIGR3, SIGR4, SIGR5, SIGR6, PSIGB, PSIGG, PSIGR



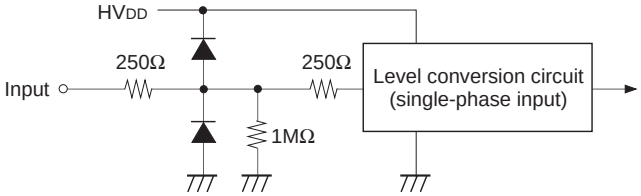
(2) HCK1, HCK2



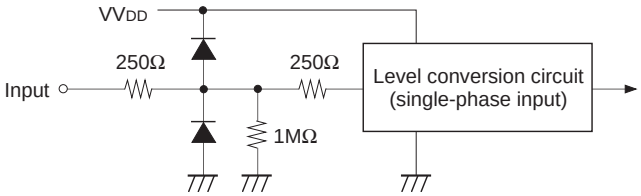
(3) RGT



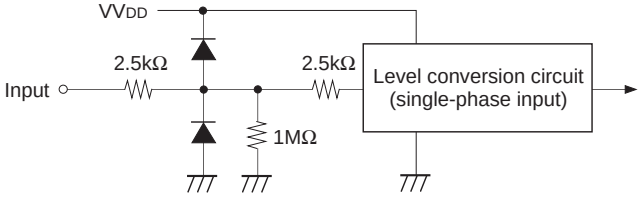
(4) HST



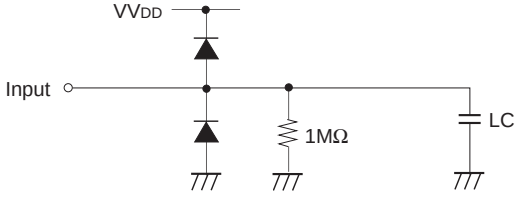
(5) PCG, VCK



(6) VST, BLK, ENB, DWN, MODE



(7) COM



Input Signals

1. Input signal voltage conditions (Vss = 0V)

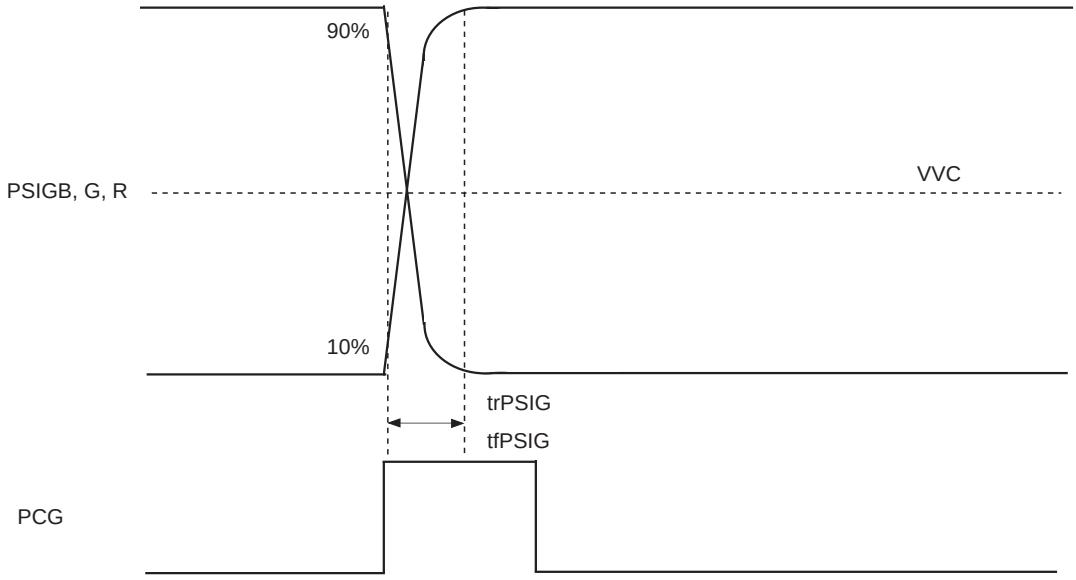
Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage MODE, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.8	7.0	7.2	V
Video signal input range*1		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.5	VVC – 0.4	VVC – 0.3	V
Uniformity improvement signal input voltage (PSIGB, PSIGG, PSIGR)*3		Vpsig	VVC ± 4.3	VVC ± 4.5	VVC ± 4.7	V

*1 Video input signal shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signals PSIGB, PSIGG and PSIGR in the same polarity with video signals SIGB1 to 6, SIGG1 to 6 and SIGR1 to 6 and which is symmetrical to VVC. Also, the rising and falling of PSIGB, PSIGG and PSIGR are synchronized with the rising of PCG pulse, and the rise time trPSIG and fall time tfPSIG are suppressed within 800ns (as shown in a diagram below).
PSIGB, PSIGG and PSIGR may change its suitable input voltage according to the drive conditions.

Uniformity Improvement Signals PSIGB, PSIGG and PSIGR Input Waveform



Level Conversion Circuit

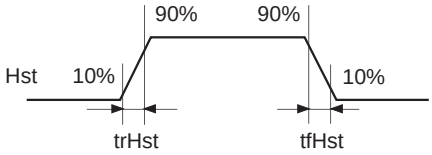
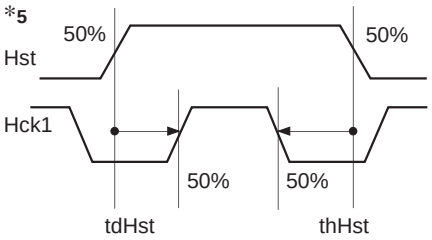
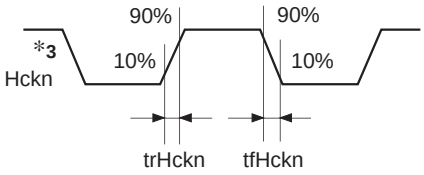
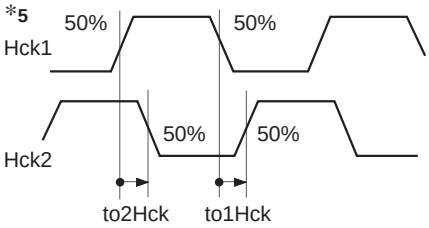
The LCX021AM has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (Ta = 25°C) (SVGA mode: fHCKn = 4.0MHz, fVCK = 24.0kHz)

	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	50	60	70	
	Hst data hold time	thHst	50	60	70	
HCK	Hckn rise time*4	trHckn	—	—	30	
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	5	10	15	µs
	Vst data hold time	thVst	5	10	15	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	toEnb	400	500	—	
	Horizontal video period completed to Enb fall time	tdEnb	900	1000	—	
	Enb fall to Pcg rise time	toPcg	630	700	—	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg rise to Vck rise/fall time	toVck	0	1000	1100	
	Pcg pulse width	twPcg	1100	1200	1300	
BLK	Blk rise time	trBlk	—	—	100	
	Blk fall time	tfBlk	—	—	100	
	Blk fall to Vst rise time	toVst	1	—	2	line
	Blk pulse width	twBlk	1	—	—	

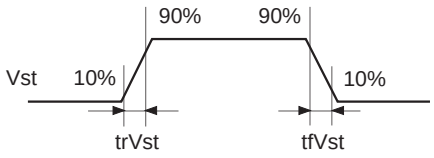
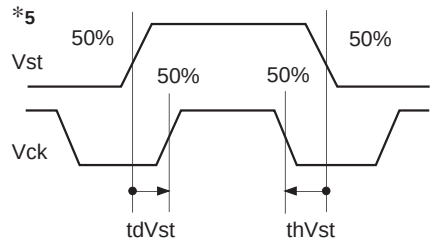
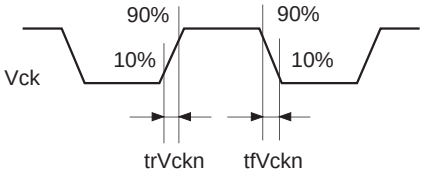
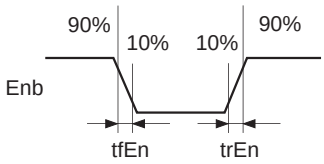
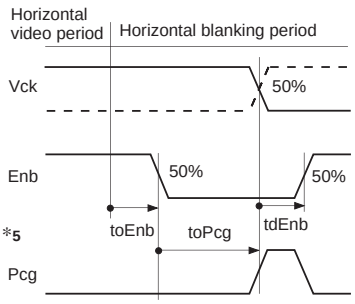
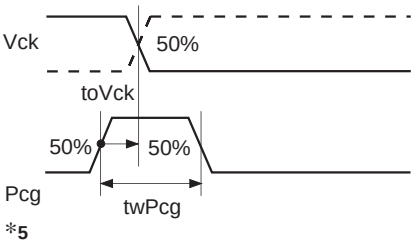
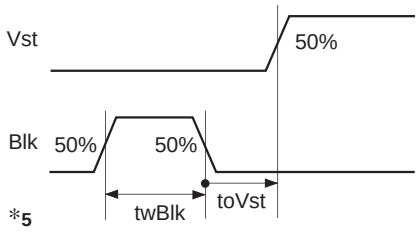
*4 Hckn means Hck1 and Hck2.

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn rise time*3	trHckn		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn fall time*3	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

*5 Definitions: The right-pointing arrow (•►) means +.
The left-pointing arrow (◄•) means –.
The black dot at an arrow (•) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Vck rise/fall to Enb rise time	toEnb		
	Enb pulse width	twEnb		
PCG*6	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg rise to Vck rise/fall time	toVck		
	Pcg pulse width	trPcg		
BLK	Blk rise time	twBlk		
	Blk fall time	tfBlk		
	Blk fall to Vst rise time	toVst		
	Blk pulse width	twBlk		

*6 Input the pulse obtained by taking the OR of the above pulse (PCG) and BLK to the PCG input pin.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, VV_{DD} = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance	HCKn	CHckn	—	12	17	pF	
	HST	CHst	—	12	17	pF	
Input pin current	HCK1		–500	–250	—	µA	HCK1 = GND
	HCK2		–1000	–300	—	µA	HCK2 = GND
	HST		–500	–150	—	µA	HST = GND
	RGT		–150	–30	—	µA	RGT = GND
Video signal input pin capacitance		Csig	—	120	170	pF	
Current consumption		IH	—	15.0	20.0	mA	HCKn: HCK1, HCK2 (4.0MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance	VCK	CVck	—	12	17	pF	
	VST	CVst	—	12	17	pF	
Input pin current	VCK		–1000	–150	—	µA	VCK = GND
PCG, VST, ENB, DWN, BLK, MODE			–150	–30	—	µA	PCG, VST, ENB, DWN, BLK, MODE = GND
Current consumption		IV	—	3.0	6.0	mA	VCK: (24.0kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (SVGA)	PWR	—	250	400	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIGo	—	10	15	nF

Electro-optical Characteristics (SVGA mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR	1	100	150	—	—
Effective apeature ratio		25°C	Teff	2	—	70	—	%
V-T characteristics	V_{90}	25°C	RV_{90-25}	3	1.3	1.6	2.0	V
			GV_{90-25}		1.4	1.8	2.2	
			BV_{90-25}		1.5	1.9	2.3	
		60°C	RV_{90-60}		1.3	1.6	1.9	
			GV_{90-60}		1.3	1.7	2.0	
			BV_{90-60}		1.4	1.8	2.2	
	V_{50}	25°C	RV_{50-25}		1.7	2.0	2.3	
			GV_{50-25}		1.8	2.1	2.4	
			BV_{50-25}		1.9	2.2	2.5	
		60°C	RV_{50-60}		1.7	1.9	2.2	
			GV_{50-60}		1.7	2.0	2.3	
			BV_{50-60}		1.8	2.1	2.4	
	V_{10}	25°C	RV_{10-25}		2.3	2.6	2.9	
			GV_{10-25}		2.4	2.7	3.0	
			BV_{10-25}		2.5	2.8	3.1	
		60°C	RV_{10-60}		2.3	2.5	2.8	
			GV_{10-60}		2.3	2.6	2.9	
			BV_{10-60}		2.3	2.7	3.0	
Response time	ON time	0°C	ton0	4	—	30	80	ms
		25°C	ton25		—	12	40	
	OFF time	0°C	toff0		—	100	200	
		25°C	toff25		—	30	70	
Flicker		60°C	F	5	—	–65	–40	dB
Image retention time		25°C	YT60	6	—	—	—	s
Cross talk		25°C	CTK	7	—	—	5	%

Reflection Preventive Processing

When a phase substrate which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a phase substrate with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 15.5V, VV_{DD} = 15.5V,

VVC = 7.0V, Vcom = 6.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

(4) Measurement systems

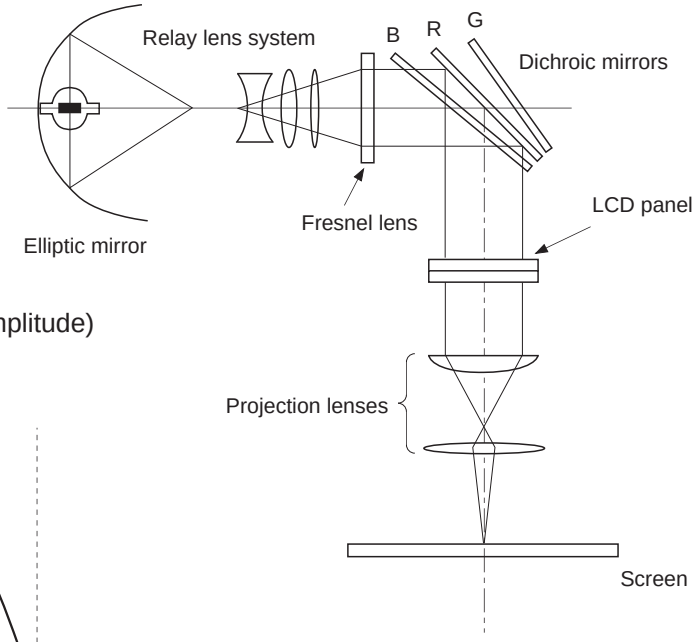
Two types of measurement systems are used as shown below.

(5) Video input signal voltage (Vsig)

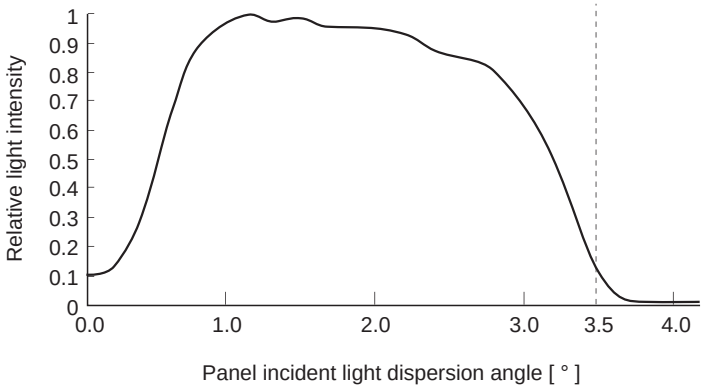
Vsig = 7.0 ± V_{AC} [V] (V_{AC}: signal amplitude)

(6) Optical measurement systems

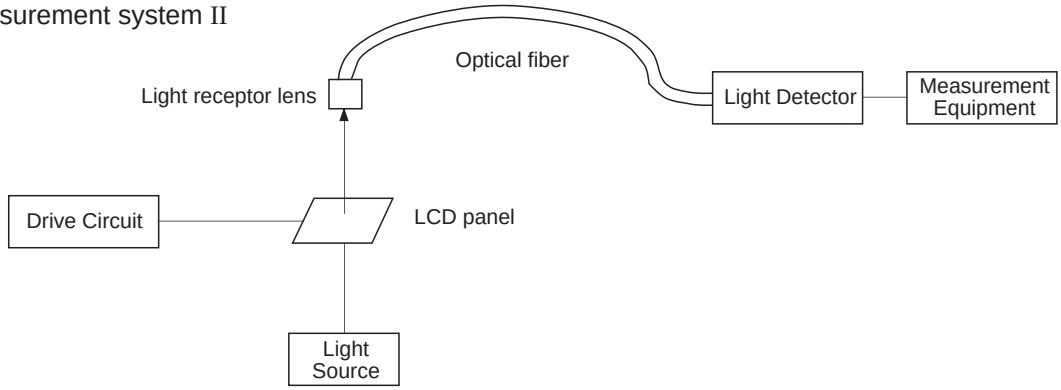
• Measurement system I



100W lamp angle distribution



• Measurement system II



1. Contrast ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad \ldots (1)$$

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude V_{AC} = 0.5V

L (Black): Surface luminance of the panel at V_{AC} = 4.5V

Both luminosities are measured by System I.

2. Effective aperture ratio

Measure the luminances below on the screen in System I, and calculate the effective aperture ratio using the following formula (2).

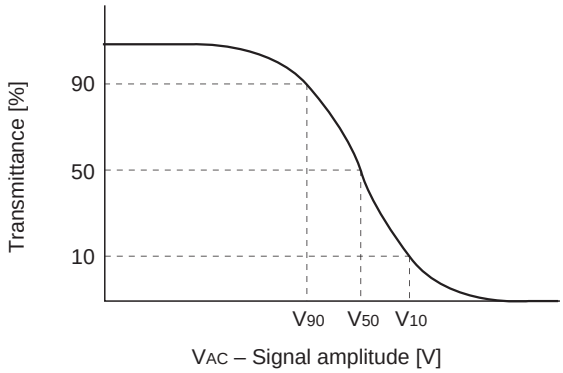
$$\frac{\text{Luminance for panel with microlens}}{\text{Luminance for panel without microlens}} \times (\text{TFT aperture ratio}) \times 100\ [\%] \quad \text{... (2)}$$

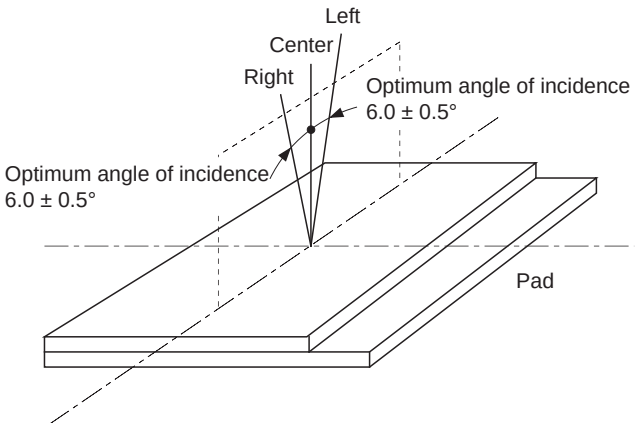
3. V-T characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.

The angles of incidence for R, G and B are as shown in the diagram below.

Red: Center: Vertical
Green: Left: 6.0 ± 0.5°
Blue: Right: 6.0 ± 0.5°





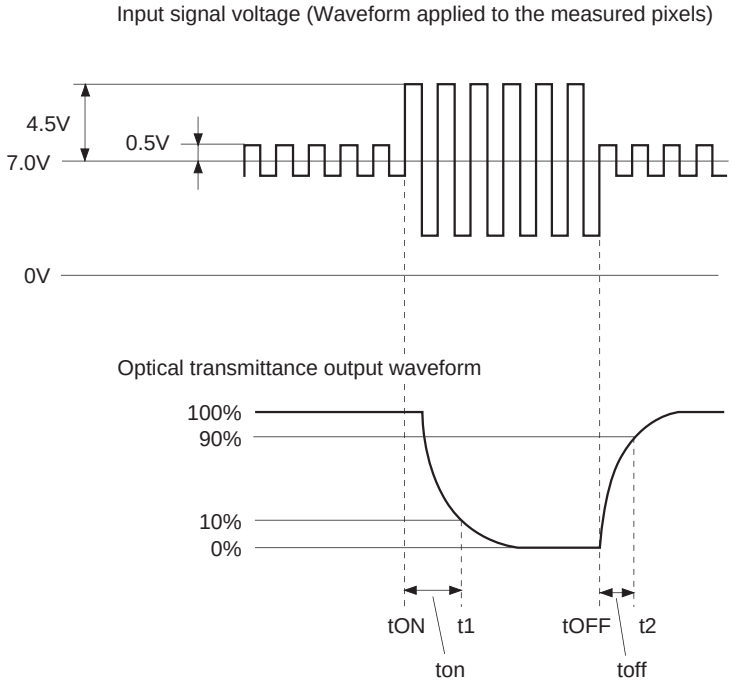
4. Response time

Response time ton and toff are defined by formulas (3) and (4) respectively.

ton = t1 – tON ...(3)
toff = t2 – tOFF ...(4)

t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



5. Flicker

Flicker (F) is given by the formula (5). DC and AC (SVGA:30Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in system II.

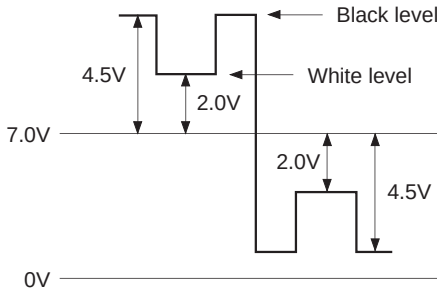
$$F\ [dB] = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \quad ...(5)$$

* Each input signal voltage for gray raster mode is given by Vsig = 7.0 ± V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image retention time

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.0 ± V_{AC} (V_{AC}: 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time till the residual image becomes indistinct.

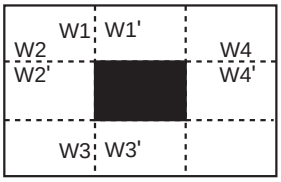
* Monoscope signal conditions:
Vsig = 7.0 ± 4.5 or ± 2.0 [V]
(shown in the right figure)
Vcom = 6.6V



Vsig waveform

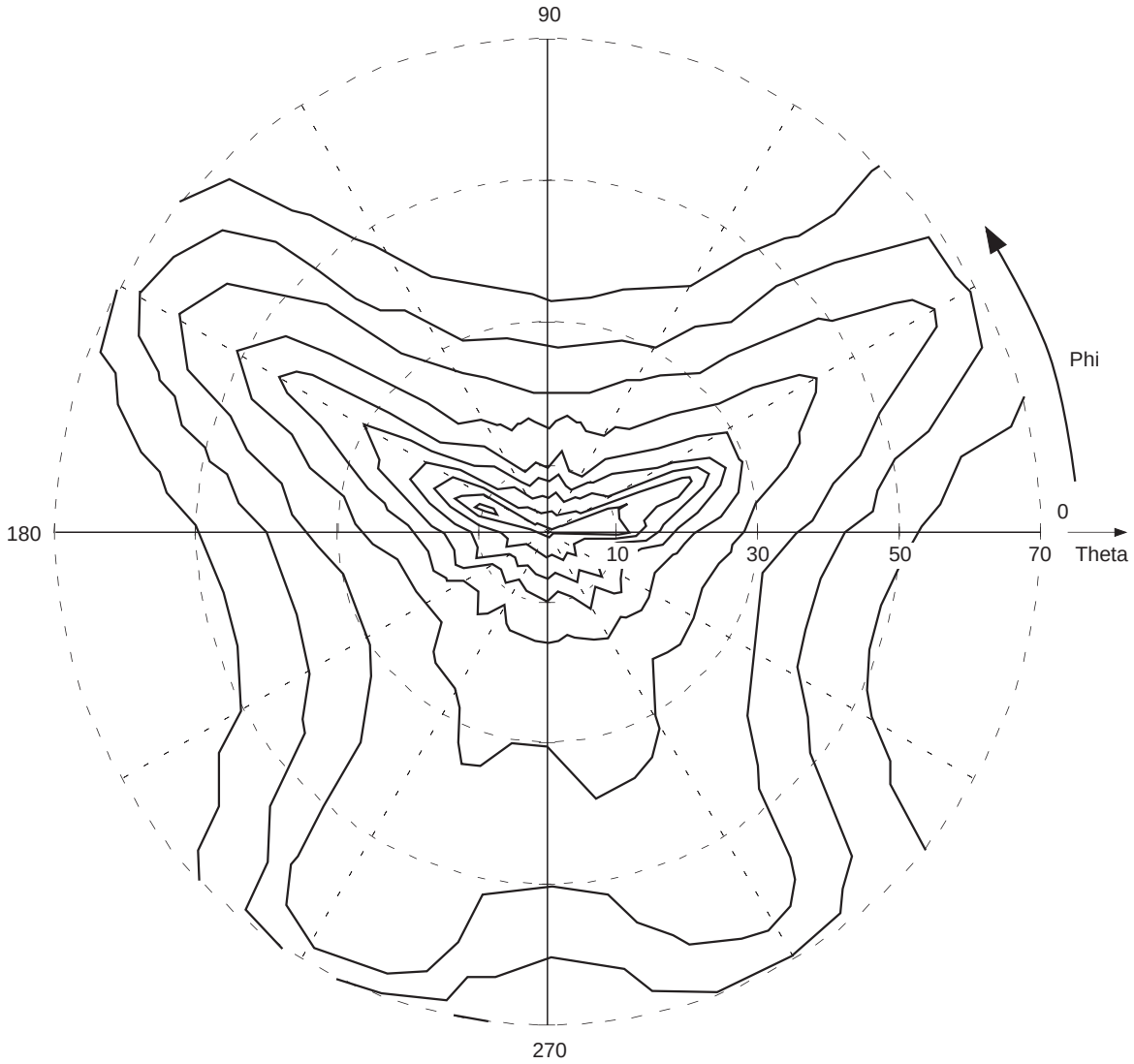
7. Cross talk

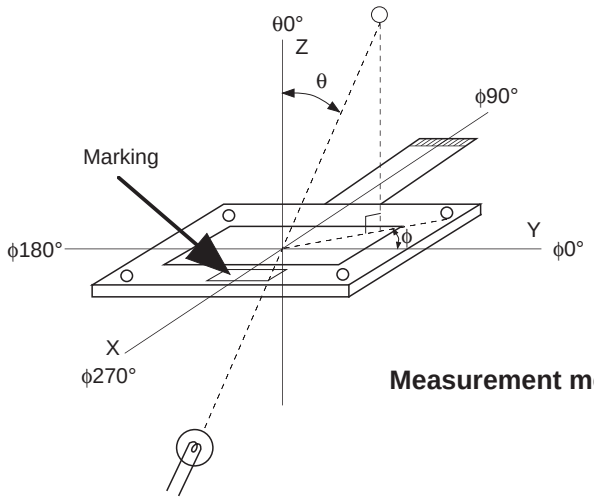
Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around a black window (Vsig = 4.5V/1V).



$$\text{Cross talk value CTK} = \left|\frac{Wi' - Wi}{Wi}\right| \times 100\ [\%]$$

Viewing Angle Characteristics (Typical Value)

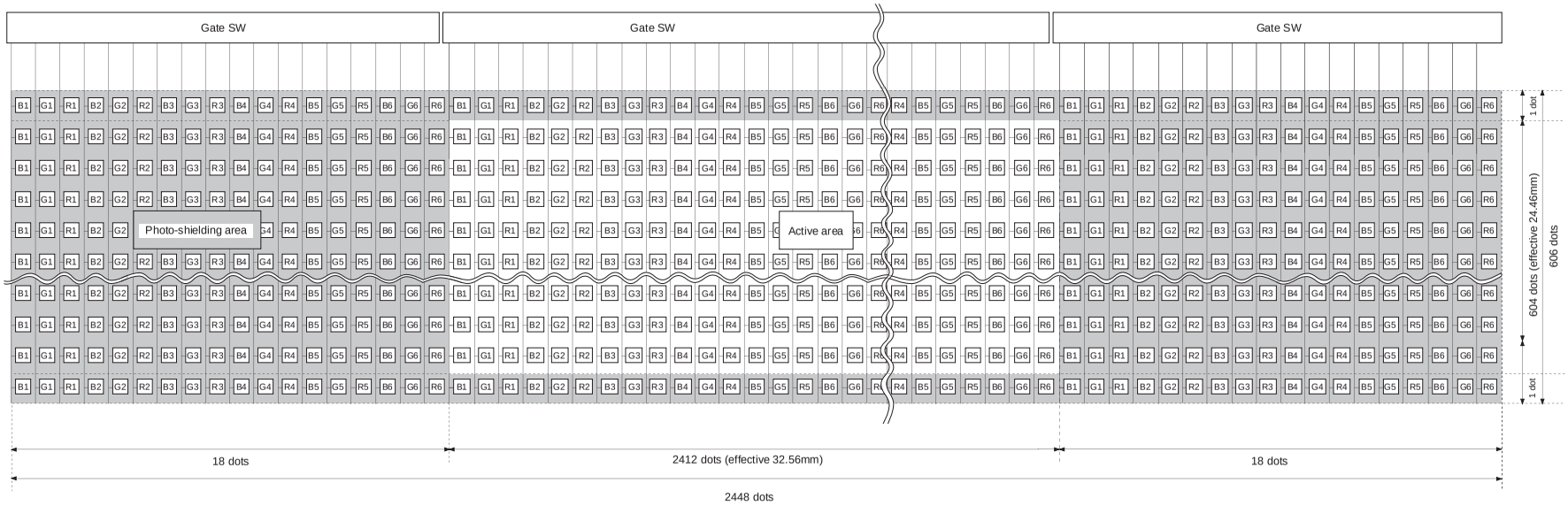




Measurement method

1. Dot arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.



Note) This RGB pixel arrangement agree with the items mentioned in the Pin Description. This RGB arrangement can be changed according to input signals.

2. LCD panel operations

[Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 604 gate lines sequentially in a single horizontal scanning period (in SVGA mode).

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 804 × 3 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- Vertical and horizontal shift registers address one pixel, and then turn on Thin Film Transistors (TFTs; two TFTs) to apply a video signal to the dot. The same procedures lead to the entire 604 × 804 × 3 dots to display a picture in a single vertical scanning period.

- The data and video signals shall be input with the 1H-inverted system.

[Description of operating mode]

This LCD panel can change the active area by displaying a black frame to support various computer or video signals. The active area is switched by MODE. However, the center of the screen is not changed. The active area setting modes are shown below.

MODE	Display mode
H	SVGA 804 × 3 × 604
L	PC98 804 × 3 × 500

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below:

RGT	Mode
H	Right scan
L	Left scan

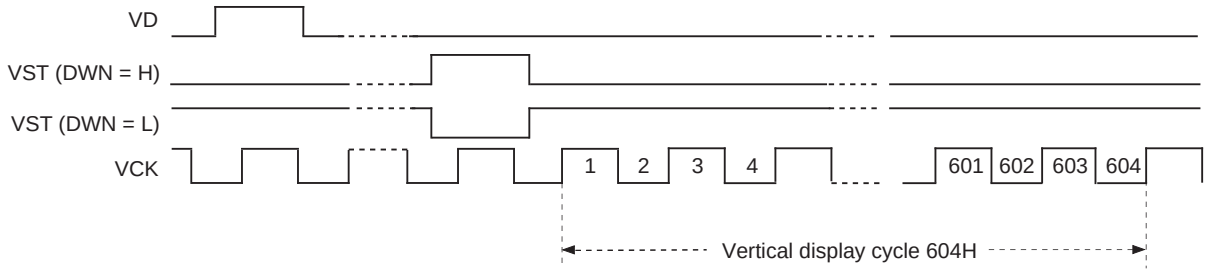
DWN	Mode
H	Down scan
L	Up scan

Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

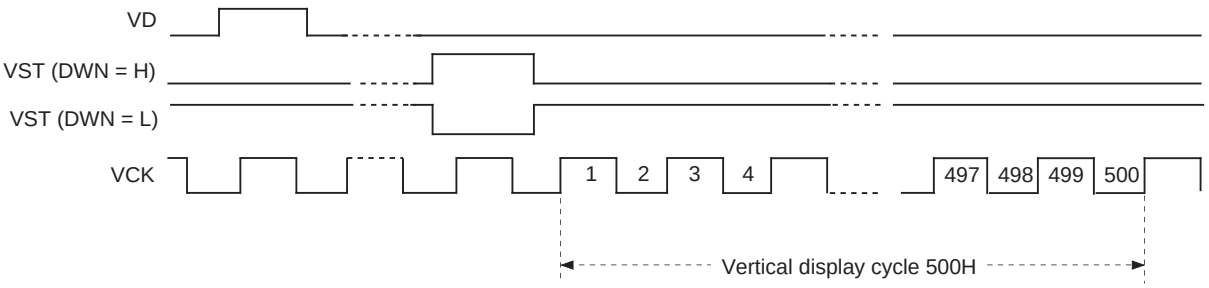
To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown on the following pages.

(1) Vertical direction display cycle

(1.1) SVGA

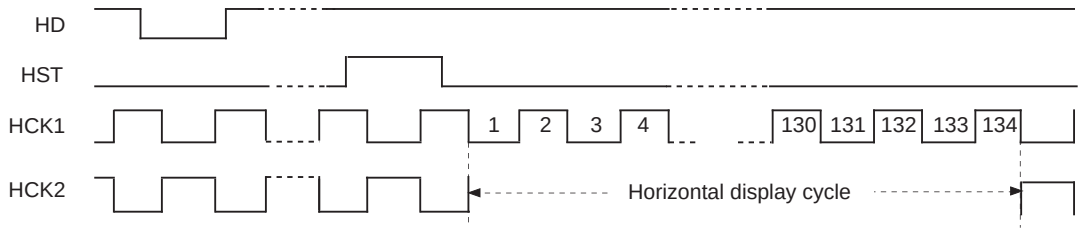


(1.2) PC98

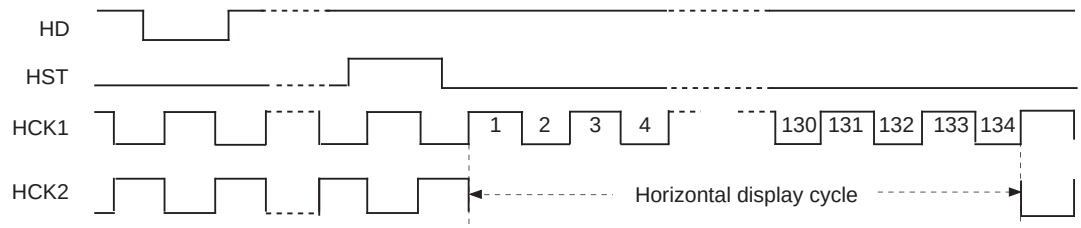


(2) Horizontal direction display cycle

(2.1) SVGA/PC98, RGT = H



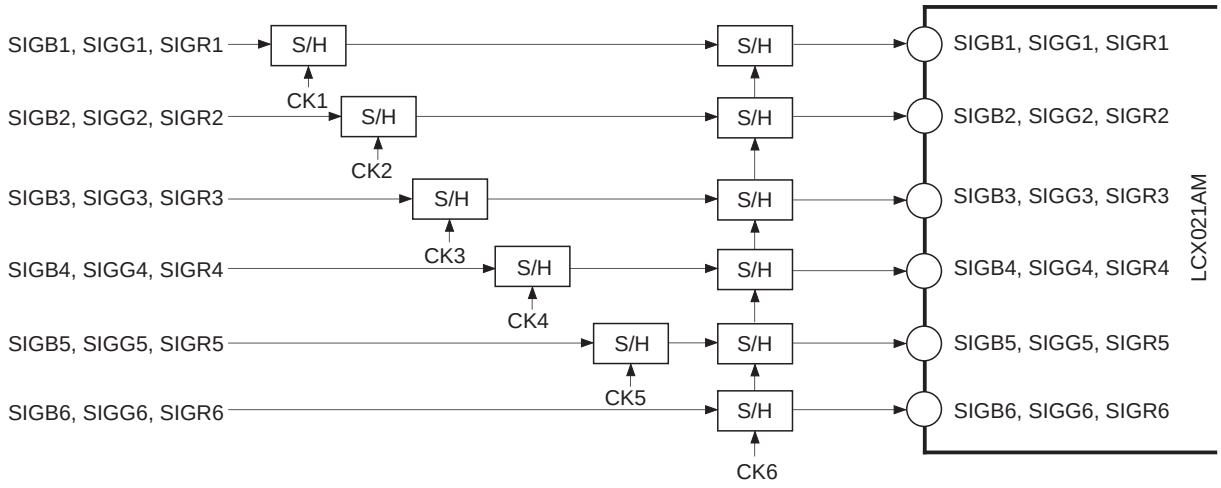
(2.2) SVGA/PC98, RGT = L



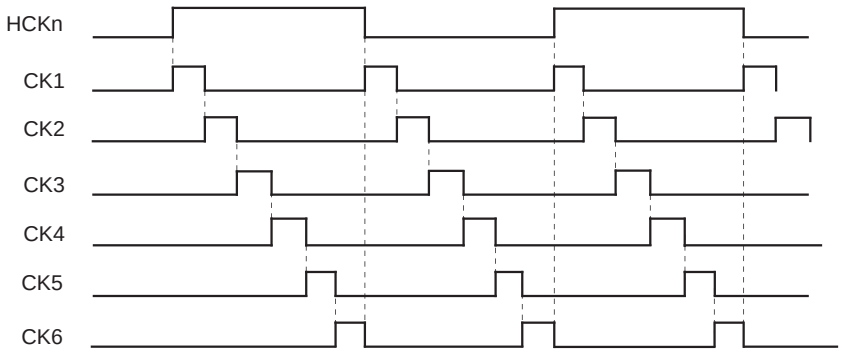
3. 18-dot simultaneous sampling

The horizontal shift register samples SIGB1 to SIGB6, SUGG1 to SIGG6 and SIGR1 to SIGR6 signals simultaneously. This requires phase matching between signals SIGB1 to SIGB6, SIGG1 to SIGG6 and SIGR1 to SIGR6 to prevent the horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using simple-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals SIGB1 to SIGB6, SIGG1 to SIGG6 and SIGR1 to SIGR6 are exactly reversed.

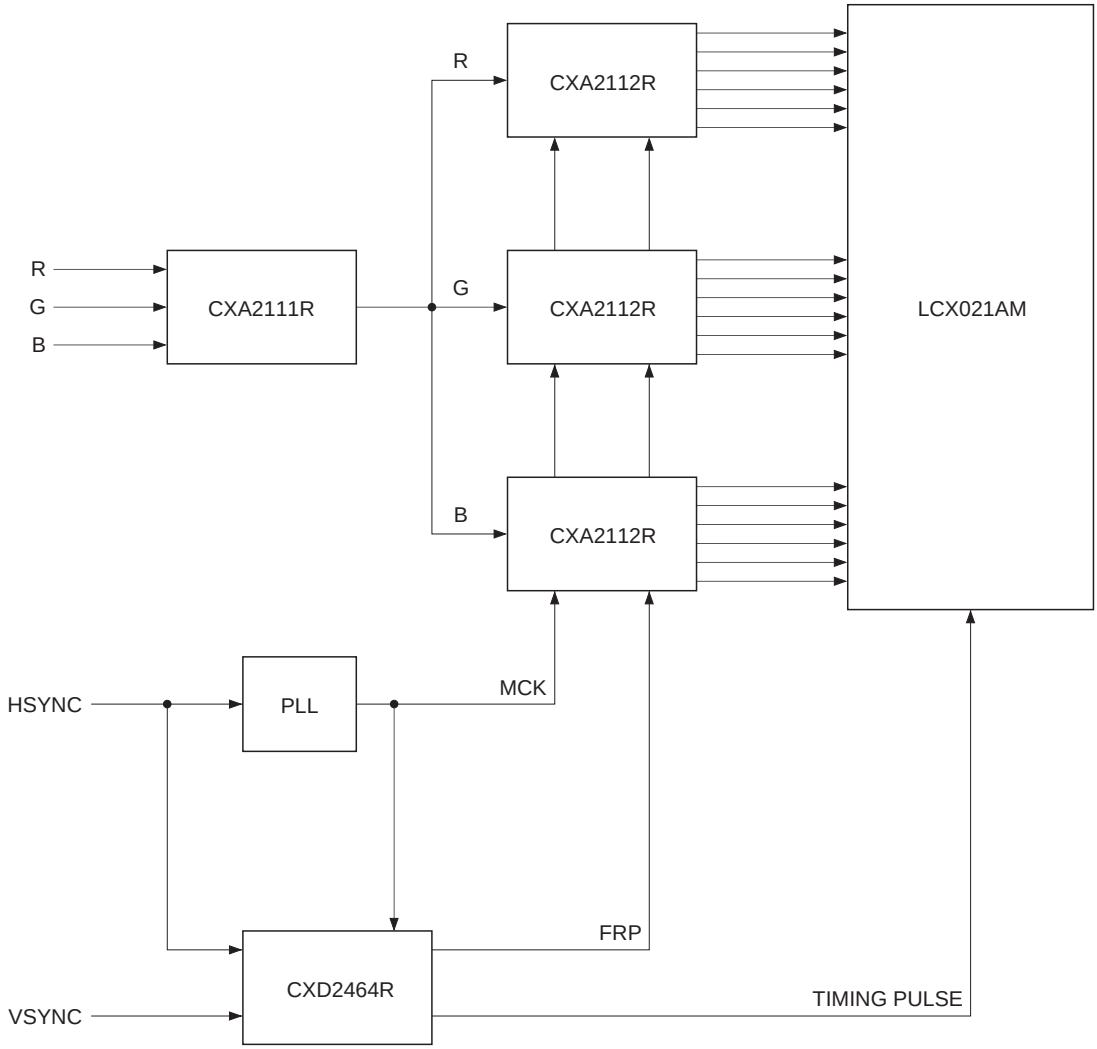


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



Optical Characteristics

1. Microlens outline

The LCX021AM has a single built-in microlens on the substrate side facing the TFT for the three TFT panel picture elements. This microlens serves the following purposes.

(1) The microlens converges the incident light striking the LCD panel to the dot aperture in order to improve the effective aperture ratio and increase the display brightness.

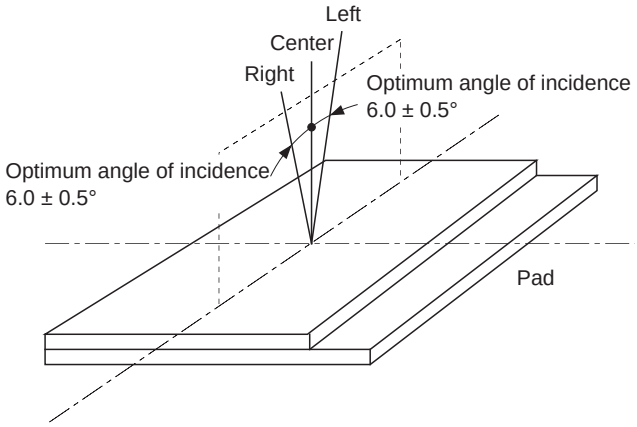
(2) The microlens provides a color representation by distributing the light flux for each of the three primary colors R, G and B which strike the panel at different angles to the dot apertures corresponding to each color.

This allows the light utilization efficiency to be improved by eliminating the light absorption by the color filter, which had been unavoidable with conventional single panel projectors.

2. Recommended lighting conditions

In order to bring out the full light converging effects of the microlens and provide a color representation with high color purity, the following lighting is recommended.

(1) The incident light angle of the three primary colors should be as shown in the figure below. The center light should strike the panel from the panel normal direction, and the left and right light from angles inclined to the right and left of the panel normal direction. The design optimal angle of incidence is the range of 6.0 ± 0.5°. However, the optimal angle of incidence may be altered slightly depending on the panel. Be sure to allow adjustment of the mutual angles of the dichroic mirrors so that the angle of incidence can be varied within the range of 6.0 ± 0.5°.



(2) Effective light: The normal direction (center light), left light and right light noted above should strike the panel at an angle of ±3.5° or less. Light with a dispersion angle greater than this value will strike adjoining dot apertures and cause the color purity to worsen. (See the incident angle distribution for System I.)

3. Recommended projection optical system

The maximum egress light angle for light passing through the LCD is approximately ±17°. Therefore, setting the F stop of the projection lens to about 1.7 is recommended in order to maximize the light converging effects of the microlens and provide a representation with excellent color balance. If the projection lens F stop is larger than this value, the right and left light are kicked accordingly by the projection lens, thereby reducing the egress light flux to the screen and the same time shifting the white balance.

Notes on Operation

(1) Lighting spectrum and intensity

Use only visible light with a wavelength λ = 415 to 780nm as a light source. Light with a wavelength λ > 780nm (infrared light) will produce unwanted temperature rises. Light with a wavelength λ < 415nm (ultraviolet light) will produce irreversible changes in the display characteristics. To prevent this, be sure to mount UV/IR cut filters between the LCX021AM and the light source as necessary depending on the light source.

The lighting intensity should be 1 million lx or less, and the panel surface temperature should not exceed 55°C.

(2) Lighting optical system

Care should be taken for the following points concerning the optical system mounted on the LCX021AM.

1) Light reflected from the optical system to the panel should be 20,000 lx or less.
2) Particular care should be taken for the panel incident angle distribution when designing optical systems for use with the LCX021AM.
3) The panel surface temperature distribution should not exceed 10°C.
4) Light should shine only on the effective display area within the LCD panel and not on other unnecessary locations. Leakage light may produce unwanted temperature rises.

Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

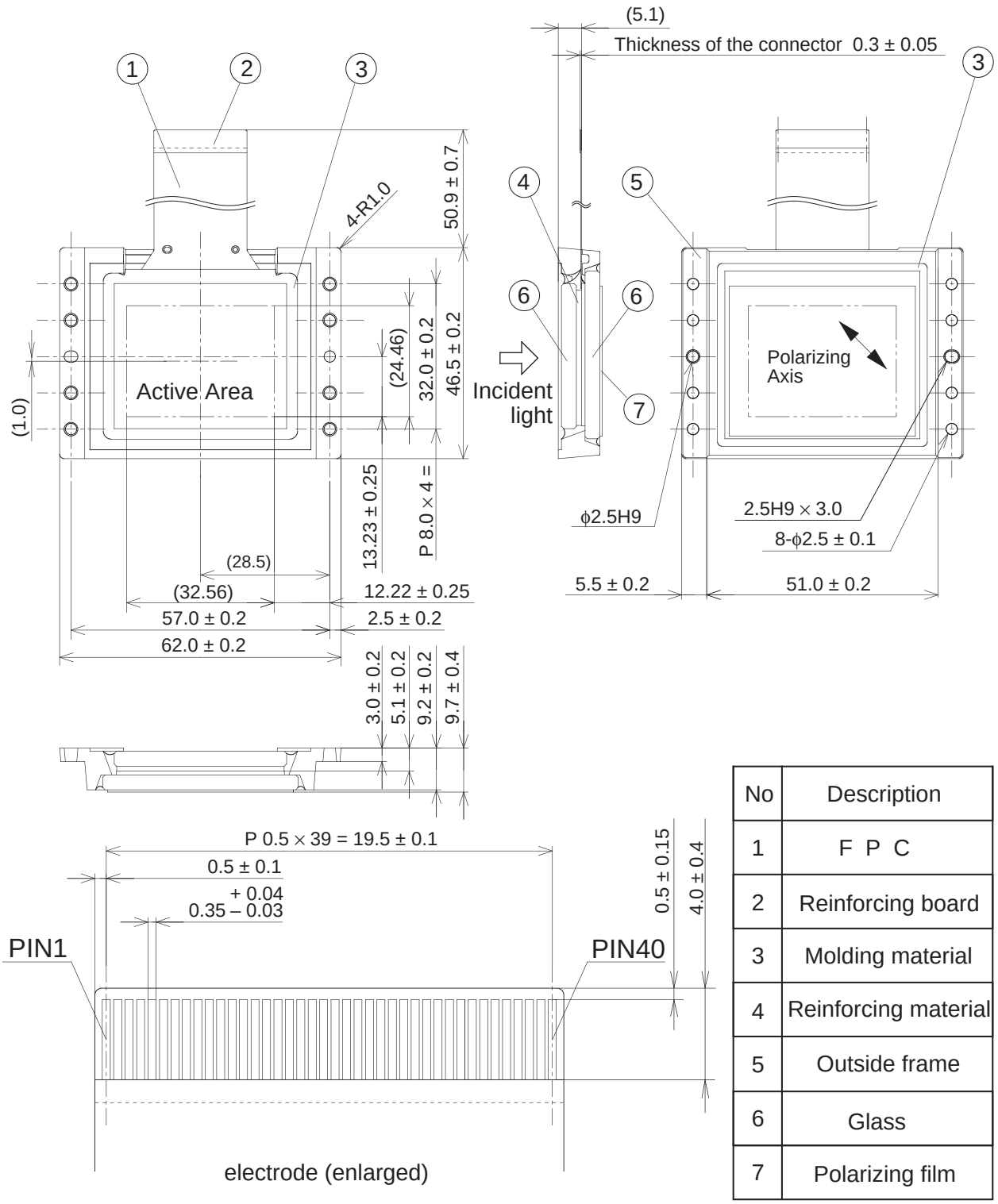
(2) Protection from dust and dirt

a) Operate in a clean environment.
b) When delivered, a surface of a panel (glass panel) is covered by a protective sheet.
Peel off the protective sheet carefully not to damage the glass panel.
c) Do not touch the surface of the glass panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow off dust at the glass panel.

(3) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop a panel.
c) Do not twist or bend a panel or panel frame.
d) Keep a panel away from heat source.
e) Do not dampen a panel with water or other solvents.
f) Avoid to store or to use a panel in a high temperature or in a high humidity, which may result in panel damages.
g) Minimum radius of bending curvature for a flexible substrate must be 1mm.
h) Torque required to tighten screws on a panel must be 3kg · cm or less.
i) Use appropriate filter to protect a panel.
j) Do not pressure the portion other than mounting hole (cover).

Package Outline Unit: mm



No	Description
1	F P C
2	Reinforcing board
3	Molding material
4	Reinforcing material
5	Outside frame
6	Glass
7	Polarizing film

The rotation angle of the active area relative to H and V is ± 1°.

weight 48g