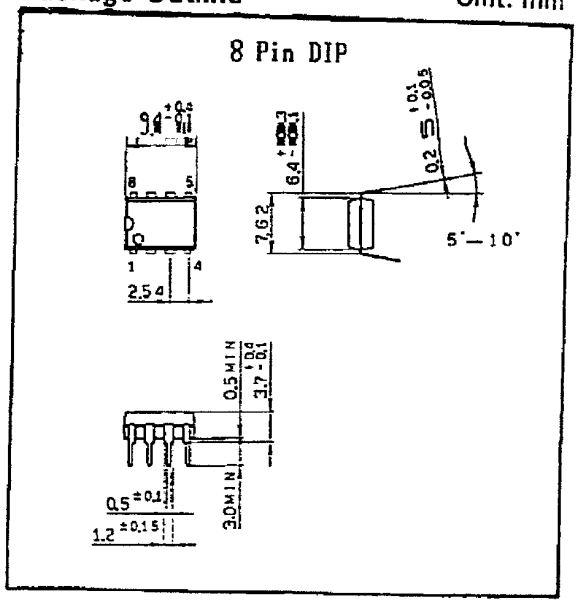
SONY **CXK1012P**

# 1024-bit (128word x 8bit) Non-volatile Memory

## Description

The CXK1012P is an electrically erasable and programmable E²PROM of 128word× 8 bit structure. It employs non-volatile memory transistors of the MNOS type. For the Input/Output, serial transmission of the data is executed. The built-in charge pump circuit permits all operations with a mere 5V power supply. With the built-in timer external parts are not required anymore, while Erasure and Write are conducted automatically. It is most suitable for the non-volatile channel memory of electronic tuners, for use instead of DIP switching as well as with the setting of various fixed numbers, or for the read only memory system necessary to rewrite immediately on the field.

**Package Outline** Unit: mm





## Features

- Single 5V power supply
- 128 word × 8 bit of full decoding structure
- Serial data transmission
- Rewritable in 1-word unit and in one chip
- Memory retention time of more than 10years with no power supply
- Number of erasures and writings: more than $10^5$ times
- TTL IC direct drive is possible
- low power consumption (35 mW Typ.)

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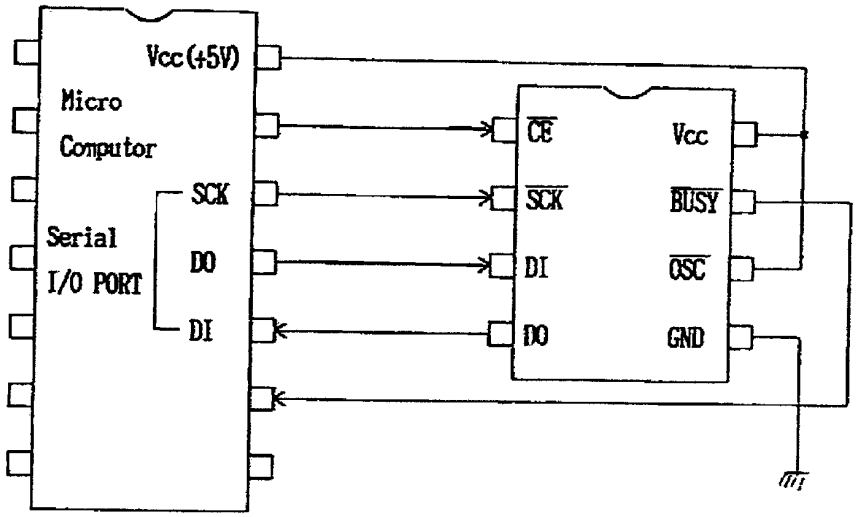
## Structure

P-channel MNOS IC

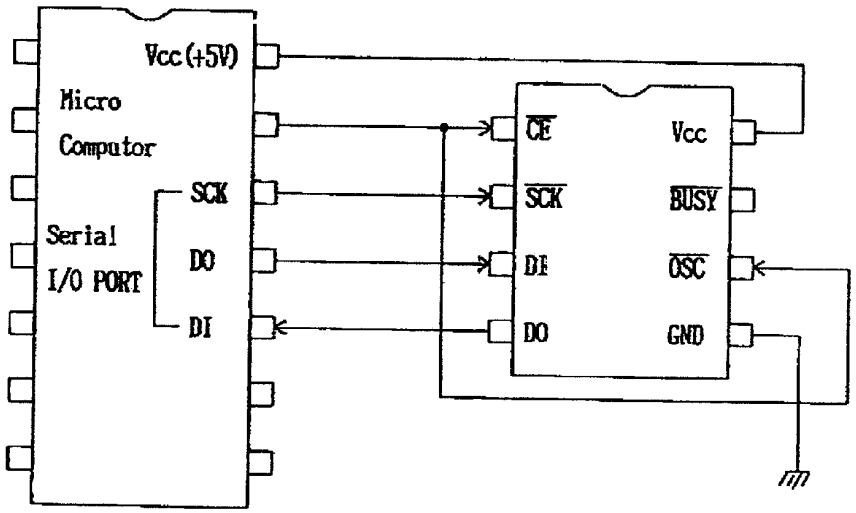
## Application Circuit

1) Using internal timer circuit

(In the example a serial port is used. A general port may also be used. It is also possible to refrain from using $\overline{BUSY}$ pin.)

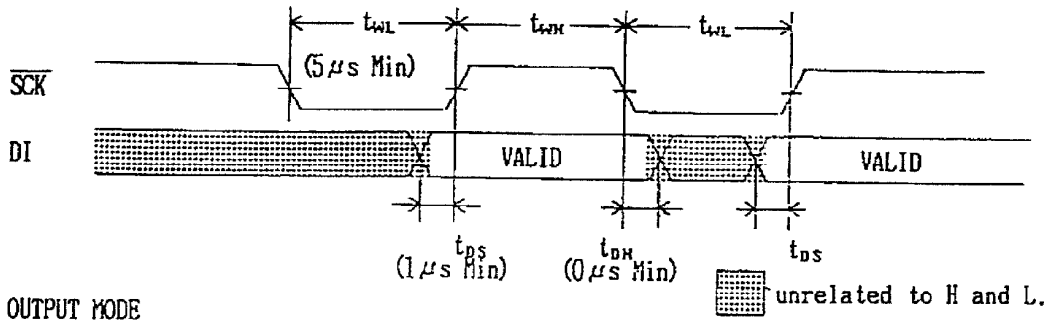



2) Using external control

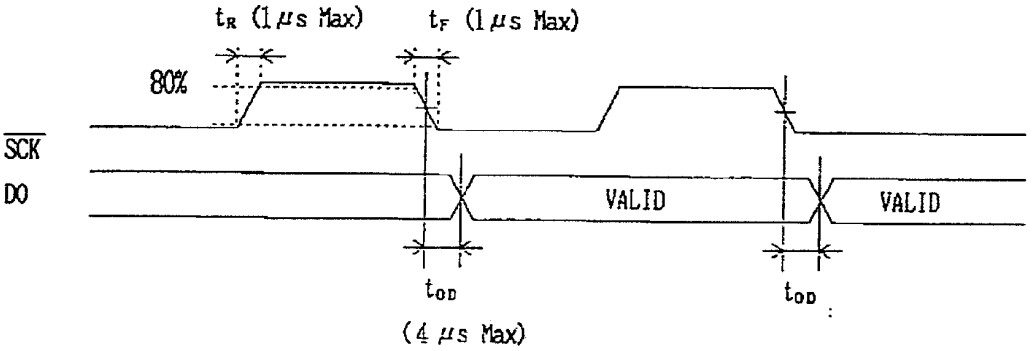


## Input/Output Timing Chart

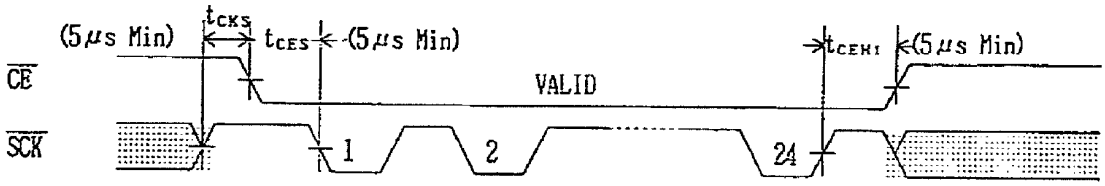
INPUT MODE



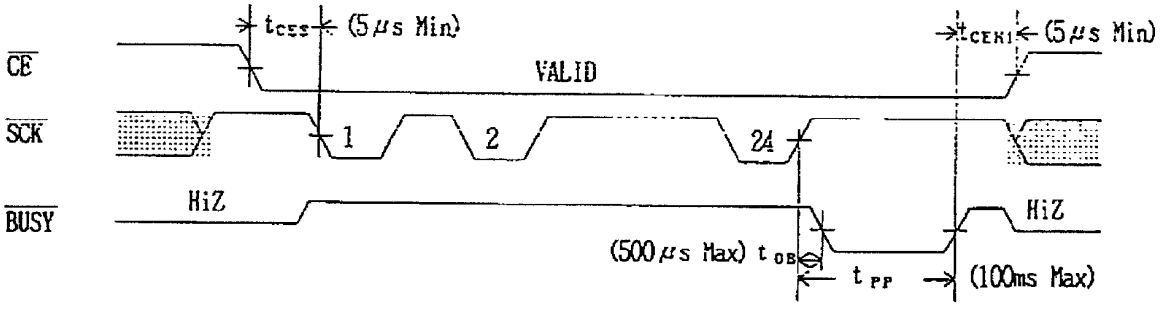

OUTPUT MODE



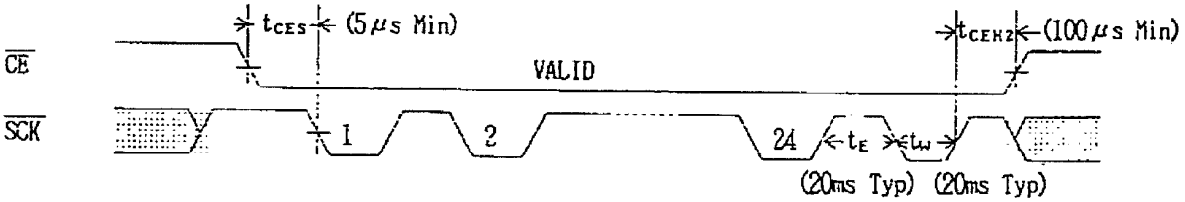

$\overline{CE}$ TIMING 1 (DR MODE)

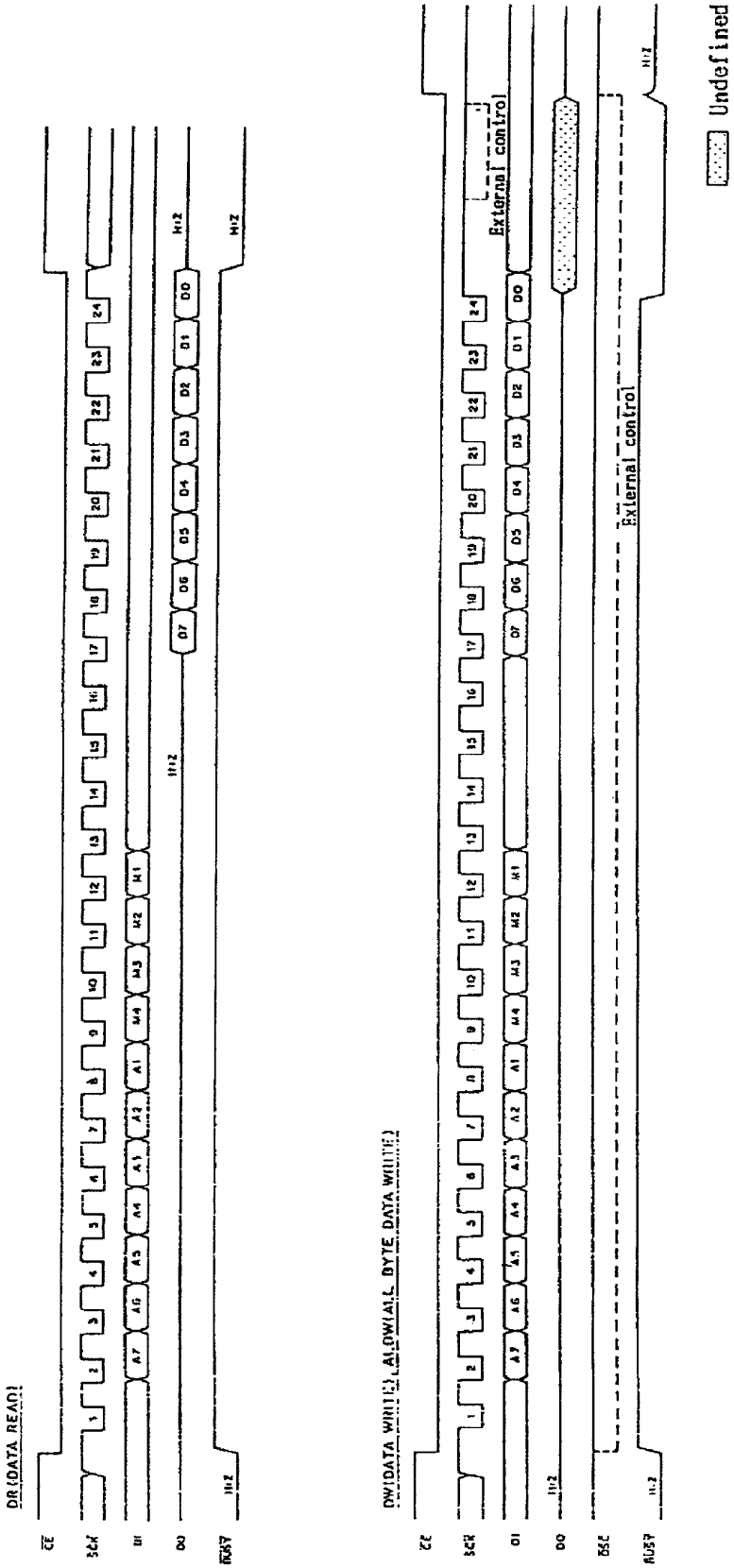



$\overline{CE}$ TIMING 2 (DW, ALDW MODE, INTERNAL TIMER)




$\overline{CE}$ TIMING 3 (DW, ALDW MODE, EXTERNAL CONTROL)




DR (DATA READ)
DW (DATA WRITE) ALLOWABLE BYTE DATA WRITE)
External control
External control
Undefined

## Pin Description

| No. | Type | Symbol | Description |
|---|---|---|---|
| 1 | IN | $\overline{CE}$ | Chip enable input pin |
| 2 | IN | $\overline{SCK}$ | Sync clock input pin |
| 3 | IN | DI | Data input pin |
| 4 | OUT | DO | Data output pin |
| 5 | Power | GND | Power supply pin (Normally 0V ) |
| 6 | IN | $\overline{OSC}$ | Oscillation pin (When using internal circuit, Open or fixed to $V_{CC}$) |
| 7 | OUT | $\overline{BUSY}$ | BUSY signal output pin |
| 8 | Power | $V_{CC}$ | Power supply pin (Normally +5V ) |

## Electrical Characteristics 1.

($Ta$=-40 to +85°C, $V_{CC}$=5V ±10%, GND=0V)

| Item | Symbol | Name | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply current | $I_{CC}$ | | *1 | | 6.5 | 12 | mA |
| Input pull-up current | $I_{IU}$ | $\overline{CE}$, $\overline{SCK}$, DI, $\overline{OSC}$ | $V_{IN}$=0V | -30 | -60 | -180 | μA |
| Output leakage current | $I_{OLK}$ | DO, $\overline{BUSY}$ | | | | ±10 | μA |
| Output voltage"High"level 1 | $V_{OH1}$ | DO | $I_{OH}$= -400μA | 2.4 | | | V |
| Output voltage"Low"level 1 | $V_{OL1}$ | DO | $I_{OL}$= 1.6mA | | | 0.4 | V |
| Output voltage"High"level 2 | $V_{OH2}$ | $\overline{BUSY}$ | $I_{OH}$= -400μA | 2.4 | | | V |
| Output voltage"Low"level 2 | $V_{OL2}$ | $\overline{BUSY}$ | $I_{OL}$= 400μA *2 | | | 0.4 | V |

*1. Including during Erase and Write.

*2. See Fig.2.

$t_{pp}$ Temperature Characteristics

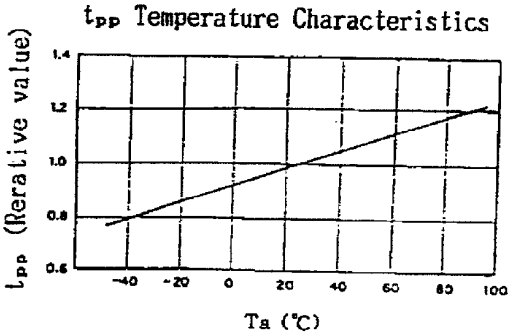



Fig.1

BUSY Pin Output Delay Characteristics

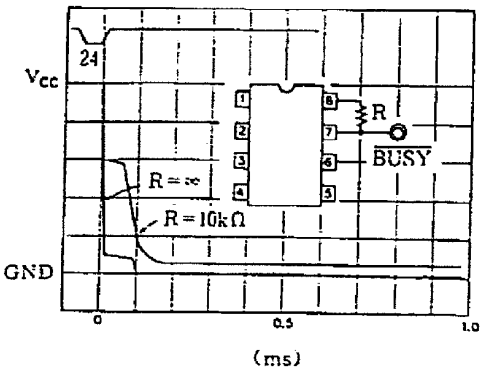



Fig.2

DO Pin Output Characteristics(Typ.)

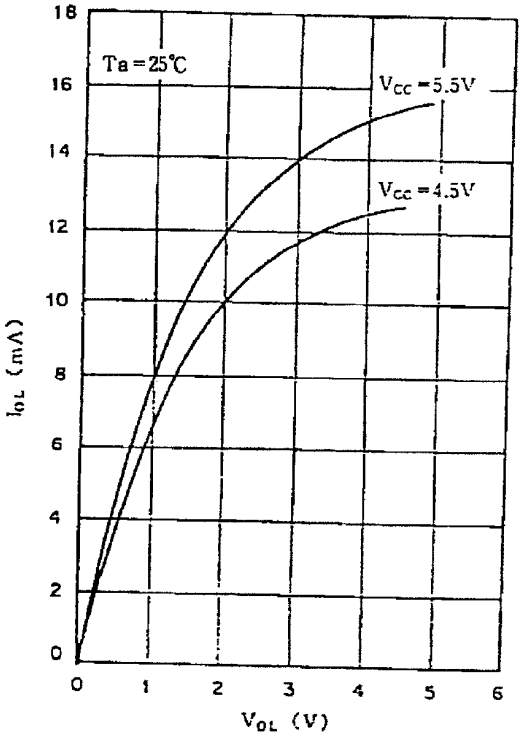
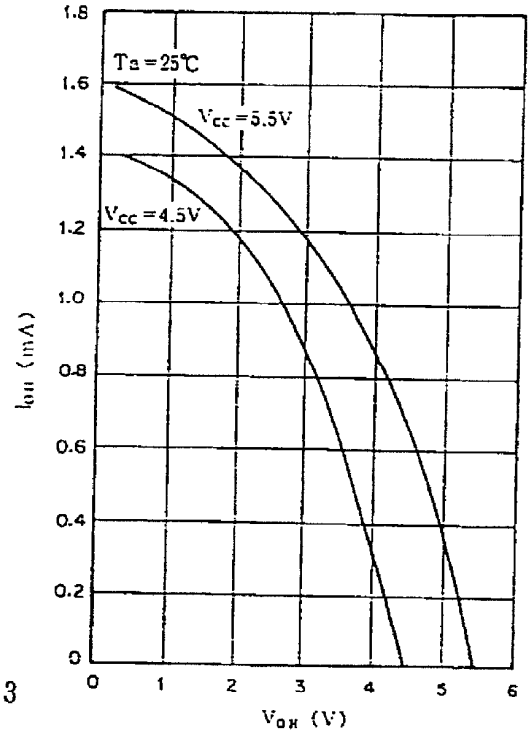



Fig.3




Supply Current Temperature Characteristics

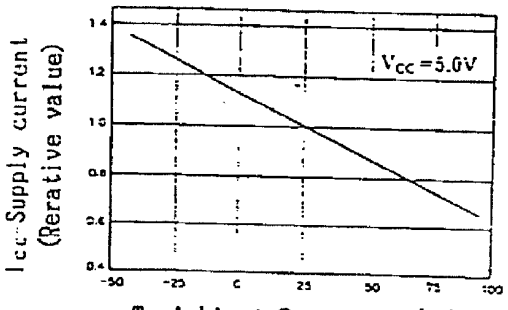



Fig.4

## Electrical Characteristics 2

(Ta=-40 to +85℃, $V_{CC}$=5V ±10%, GND=0V)

| Item | symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse width | $t_{WH}$ | | 5 | | | μs |
| Colck pulse width | $t_{WL}$ | | 5 | | | μs |
| Data input setup time | $t_{DS}$ | | 1 | | | μs |
| Data input hold time | $t_{DH}$ | | 0 | | | μs |
| Rise /Fall time | $t_{r,tf}$ | | | | 1 | μs |
| Chip enable setup time | $t_{CES}$ | | 5 | | | μs |
| Chip enable hold time 1 | $t_{CEH1}$ | | 5 | | | μs |
| Chip enable hold time 2 | $t_{CEH2}$ | | 100 | | | μs |
| Clock set up time | $t_{CKS}$ | | 5 | | | μs |
| Data delay time | $t_{OD}$ | DO, $C_L$ =100pF | | | 4 | μs |
| $\overline{BUSY}$ output delay time*3 | $t_{BD}$ | $\overline{BUSY}$, R=10kΩ | | | 500 | μs |
| Number of Read | $N_R$ | Refresh period | $10^7$ | $10^9$ | | time |
| Program time | $t_{PF}$ | During internal timer usage *1 | | 40 | 100 | mS |
| Erasure time | $t_E$ | During external control *2 | 16 | 20 | 100 | mS |
| Write time | $t_W$ | During external control *2 | 16 | 20 | 100 | mS |
| Memory retention time 1 | $t_{MH1}$ | After rewriting $10^4$ times, store at Ta=85℃ | 10 | | | year |
| Memory retention time 2 | $t_{MH2}$ | After rewriting $10^5$ times, store at Ta=85℃ | 1 | | | year |

*1. Including the value when Ta= 25℃ (See fig.1)

*2. Usage of ranges $t_E$ to $t_W$ (16 to 100ms) presents no problem for Erasure and Write in functions

*3. See Fig.2.

## Command Table

| M4 | M3 | M2 | M1 | Operational Command |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No operation |
| 0 | 0 | 1 | 0 | DW: Memory Write |
| 0 | 1 | 0 | 0 | ALDW:All byte write |
| 0 | 1 | 1 | 0 | Test Mode ,Usage forbidden |
| 1 | 0 | 0 | 0 | No operation |
| 1 | 0 | 1 | 0 | DR: Memory Read |
| 1 | 1 | 0 | 0 | Test mode,Usage forbidden |
| 1 | 1 | 1 | 0 | Test mode,Usage forbidden |
| X | X | X | 1 | Test mode,Usage forbidden |

## Description of Circuit Operations

1) Timing

At the rise time of Sync clock ($\overline{SCK}$), data is taken in from DI and with the fall time, data is output from DO. Input data should be stabilized, from $\overline{SCK}$ rise time and before 1 μs.

2) DR: Data Read (Memory Read)

$\overline{CE}$ is set to L and then the first clock is input after 5μs. By entering address data (A7 to A1) and mode data (M4 M3 M2 M1=1010), from the 17th clock and in synchronization with the fall time, D7 D6 through DO are output in the respective order. When the rise time of the 24th clock has taken place, set $\overline{CE}$ to H after 5μs.

3) DW: Data Write (Memory Write)

$\overline{CE}$ is set to L and then the first clock is input after 5μs. By entering Address data (A7 to A1), mode data (M4 M3 M2 M1=0010) and Data (D7 to DO), from the rise time of the 24th clock, Erasure and Write are performed automatically. As $\overline{BUSY}$ pin outputs L during Erasure and Write and H at the completion of Write, set $\overline{CE}$ to H following H output and after 5μs.

When $\overline{BUSY}$ pin is not in use, set $\overline{CE}$ to H after 100ms ( $t_{pp}$ Max.)

4) ALDW: All Byte Data Write

By entering Mode Data (M4 M3 M2 M1=0100), Write operation of the same data (D7 to DO) is carried out simultaneously to all addresses. CE timing and $\overline{BUSY}$ output are the same as in above article 3).

5) Electrical control of Erasure and Write

Erasure and Write pulses are generated by the built-in C and R. However, external control is also possible. By setting $\overline{OSC}$ pin to L in DW or ALDW modes, Erasure and Write control are possible through the usage of $\overline{SCK}$ pin. Erasure is carried out during $t_E$ (20ms Typ.) and write during $t_W$ (20ms Typ.).

By setting $\overline{SCK}$ pin to H after the lapse of $t_W$, write complete pulse is generated. However the actual completion takes place about 50 μs after the pulse generation, (50μs Typ, 100μs Max.) At that time $\overline{BUSY}$ pin changes from L to H. Over 5μs after it has turned to H, set $\overline{CE}$ pin to H. When $\overline{BUSY}$ pin is not in use, after $\overline{SCK}$ pin has turned from L to H ($t_W$) by over 100μs, set $\overline{CE}$ to H.

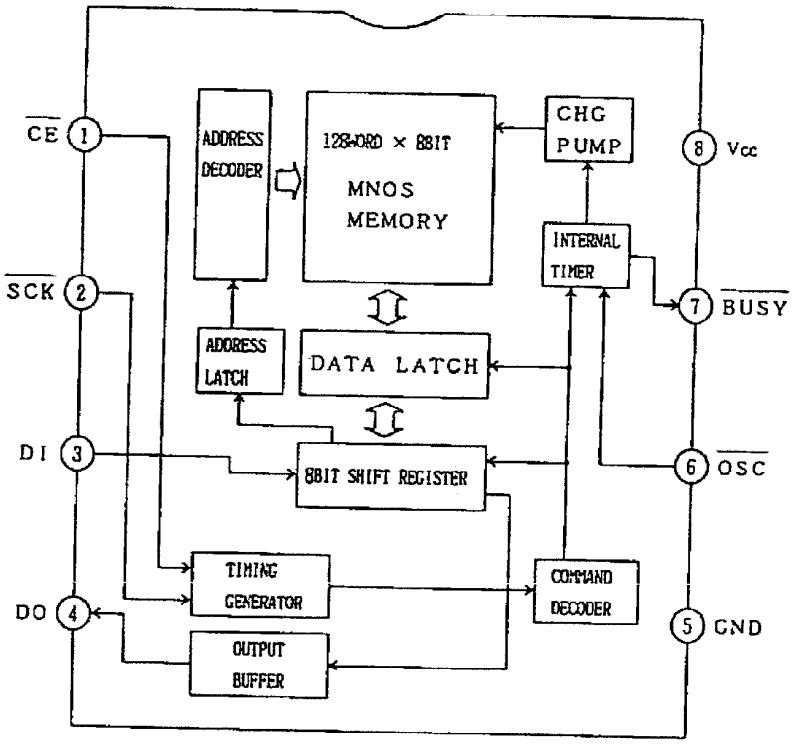
## Absolute Maximum Ratings (GND = 0V)

| | | | | | | |
|---|---|---|---|---|---|---|
| · Supply voltage | $V_{CC}$ | −0.3 | to | | +7.0 | V |
| · Input voltage | $V_{IN}$ | −0.3 | to | $V_{CC}$ | +0.3 | V |
| · Operating temperature | $T_{opr}$ | −40 | to | | +85 | ℃ |
| Storage temperature | $T_{stg}$ | −55 | to | | +150 | ℃ |

## Recommended Operating Conditions (Ta=-40 to+85℃, GND=0V)

| | | | | | |
|---|---|---|---|---|---|
| · Supply voltage | $V_{CC}$ | 4.5 | to | 5.5 | V |
| · Clock frequency | $f_{CLK}$ | DC | to | 100 | kHz |
| · High level input voltage | $V_{INH}$ | 0.7 $V_{CC}$ | to | $V_{CC}$ | V |
| · Low level input voltage | $V_{INL}$ | 0 | to | 0.3$V_{CC}$ | V |

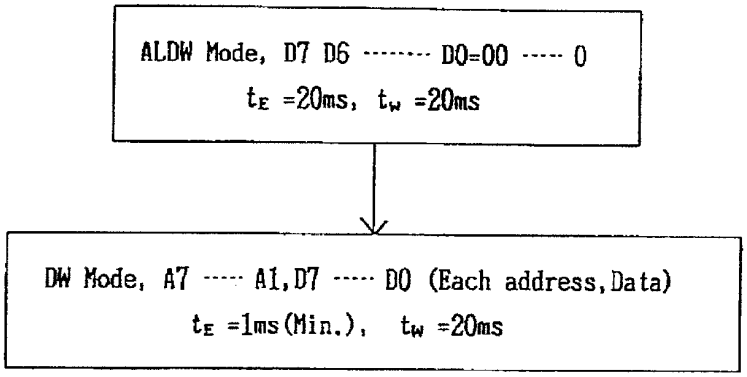
## Block Diagram and Pin Configuration



6) Usage of ALDW mode H.

Write is carried out to the Memory elements according to the 「Erase 」⟶「Write 」 cycle. During normal write procedures (DW mode), as write is executed for all the 128 address, 128 × $t_{PP}$ (or $t_E$ + $t_W$ )=5.12sec (Typ.)
amount of time is necessary.

With the CXK1012P, 「Erasure state 」and 「Data"0" 」are made to correspond. Once "0" has been written into all addresses (Erasure state), by writing data into each address, the program time can be shortened.




In this case, the program time becomes.

(20ms+20ms) +128 × (1ms +20ms) = 2.73sec